Eberhard Karls Universität Tübingen
Kepler Center for Astro and Particle Physics
and
GSI Helmholtzzentrum für Schwerionenforschung
Compressed Baryonic Matter Experiment
Darmstadt, Germany

Master's Thesis

Master of Science Astro and Particle Physics

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The Assembly and Integration of a Half-unit of the Silicon Tracking System(STS) Detector

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Submission Date:	October 29, 2025

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Abstract

The Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) aims to explore how strongly the matter interacts and behaves under extreme baryon-density conditions. The Silicon Tracking System (STS) is an important part of the experiment. It provides high-precision tracking of charged particles produced in heavy-ion collisions. The STS, with its high tracking and vertex reconstruction efficiency, helps in studying rare probes such as open charm and di-leptons. Its performance is directly connected to the core physics goals of CBM. Henceforth, a careful assembly and integration of its units is essential for the success of the experiment.

The aim of the thesis on the STS half-unit is to develop, implement, and verify a reliable assembly and integration protocol. The protocol ensures the precise placement of all components, including cooling components, ladders, and peripheral electronic components. Prototype components were used to replicate the assembly for safety before working with actual ladders and electronics. A key phase of the study involved configuring data and power connections between the Front-End Boards (FEBs) and the readout chain. This phase was critical because inaccurate placement or routing of the cables could effect signal performance and interfere with the integration of the half-unit. To prevent such issues, special attention was given to the mechanical constraints of the half-unit to ensure proper integration.

Functional tests were performed on the modules by configuring the front-end Application-Specific Integrated Circuits (ASICs) mounted on the FEBs. These tests confirmed stable Equivalent Noise Charge (ENC) values within the expected range, thermal stability under operation, and accurate transmission and reception of readout signals. In addition, signal noise was evaluated because the cables needed to be pre-bent and properly routed.

The cable routing protocol confirmed that the current routing setup did not compromise electronic performance. This work represents the first verification of a half-unit assembly protocol, including successful functional testing of the FEB boxes.

Thermal tests were also performed to assess the stability of the ASICs under operating conditions. It was verified that the heat dissipation remained within safe limits and did not affect performance. This evaluation is essential for identifying possible operational challenges and avoiding damage during long data-taking periods.

In addition to assembly and functional verification, this work provides a foundation for further optimizing the integration protocol. While the preliminary results indicate that the assembly and routing procedures are effective, additional studies are planned to evaluate the system under extended operational conditions and to confirm long-term reliability. The overall aim of the work is to prepare for integrating the STS half-units into the CBM experiment and to validate that the modules perform reliably and meet the required stability standards.

By establishing and testing a detailed protocol using prototype components, this study provides an essential step towards making the assembly and integration of STS half-units more effective. The risk of errors during future assembly is reduced and the CBM detector's operational procedures are validated. The methods and the results described here can guide future integration with complete detector modules and support ongoing efforts to optimize the STS within the CBM experiment.

Kurzfassung

Das Experiment Compressed Baryonic Matter (CBM) am Facility for Antiproton and Ion Research (FAIR) zielt darauf ab, die Wechselwirkungen und das Verhalten stark wechselwirkender Materie unter extremen baryonischen Dichtebedingungen zu untersuchen. Das Silicon Tracking System (STS) ist ein wesentlicher Bestandteil des Experiments. Es ermöglicht die hochpräzise Spurrekonstruktion geladener Teilchen, die in Schwerionenkollisionen erzeugt werden. Durch seine hohe Effizienz bei der Teilchenverfolgung und der Vertex-Rekonstruktion trägt das STS wesentlich zur Untersuchung seltener Sonden wie offener Charm-Teilchen und Di-Leptonen bei. Seine Leistungsfähigkeit ist direkt mit den zentralen physikalischen Zielen des CBM-Experiments verknüpft. Daher ist eine sorgfältige Montage und Integration seiner Einheiten entscheidend für den Erfolg des Experiments.

Ziel dieser Arbeit über die STS-Halbeinheit ist es, ein zuverlässiges Montage- und Integrationsprotokoll zu entwickeln, zu implementieren und zu verifizieren. Dieses Protokoll gewährleistet die präzise Platzierung aller Komponenten, einschließlich der Kühlkomponenten, der Ladders und der peripheren elektronischen Bauteile. Zu Sicherheitszwecken wurden Prototypkomponenten verwendet, um die Montage vorab zu reproduzieren, bevor mit den echten Ladders und Elektronikkomponenten gearbeitet wurde. Eine zentrale Phase der Studie bestand darin, die Daten- und Stromverbindungen zwischen den Front-End-Boards (FEBs) und der Auslesekette zu konfigurieren. Diese Phase war kritisch, da eine ungenaue Platzierung oder Führung der Kabel die Signalqualität beeinträchtigen und die Integration der Halbeinheit stören könnte. Um solche Probleme zu vermeiden, wurde besonderes Augenmerk auf die mechanischen Randbedingungen der Halbeinheit gelegt, um eine korrekte Integration sicherzustellen.

Funktionsprüfungen wurden an den Modulen durchgeführt, indem die auf den FEBs montierten Application-Specific Integrated Circuits (ASICs) konfiguriert wurden. Diese Tests bestätigten stabile Equivalent Noise Charge (ENC)-Werte innerhalb des erwarteten Bereichs, thermische Stabilität im Betrieb sowie eine korrekte Übertragung und den Empfang der Auslesesignale. Darüber hinaus wurde das Signalrauschen untersucht, da die Kabel vorgebogen und korrekt verlegt werden mussten. Das Kabelverlegeprotokoll bestätigte, dass die aktuelle Kabelführung die elektronische Leistung nicht beeinträchtigt. Diese Arbeit stellt die erste Verifizierung eines Montageprotokolls für eine Halbeinheit dar, einschließlich der erfolgreichen Funktionsprüfung der FEB-Boxen.

Zusätzlich wurden thermische Tests durchgeführt, um die Stabilität der ASICs unter Betriebsbedingungen zu bewerten. Es wurde bestätigt, dass die Wärmeabfuhr innerhalb sicherer Grenzen bleibt und die Leistung nicht beeinträchtigt. Diese Untersuchung ist entscheidend, um mögliche betriebliche Herausforderungen zu identifizieren und Schäden während längerer Datennahmephasen zu vermeiden.

Neben der Montage- und Funktionsüberprüfung bildet diese Arbeit die Grundlage für die weitere Optimierung des Integrationsprotokolls. Während die vorläufigen Ergebnisse zeigen, dass die Montage- und Verlegeverfahren effektiv sind, sind zusätzliche Untersuchungen geplant, um das System unter erweiterten Betriebsbedingungen zu testen und die langfristige Zuverlässigkeit zu bestätigen. Das übergeordnete Ziel der Arbeit besteht darin, die Integration der STS-Halbeinheiten in das CBM-Experiment vorzubereiten und zu validieren, dass die Module zuverlässig arbeiten und die geforderten Stabilitätsstandards erfüllen.

Durch die Erstellung und Erprobung eines detaillierten Protokolls mit Prototypkomponenten leistet diese Studie einen wesentlichen Beitrag zur effizienteren Montage und Integration der STS-Halbeinheiten. Das Risiko von Fehlern während zukünftiger Montagen wird reduziert, und die Betriebsverfahren des CBM-Detektors werden validiert. Die beschriebenen Methoden und Ergebnisse können zukünftige Integrationen mit vollständigen Detektormodulen leiten und die laufenden Bemühungen zur Optimierung des STS im Rahmen des CBM-Experiments unterstützen.

Acknowledgements

This thesis has been a journey of learning, patience, and determination, and I owe my gratitude to many people who have guided, supported, and encouraged me along the way.

First and foremost, I would like to express my sincere thanks to Prof. Dr. Hans Rudolf Schmidt for his constant guidance and support throughout this work. I am equally grateful to Dr. Maksym Teklishyn, whose insights and encouragement helped me grow not only as a researcher but also in the way I approach problems with curiosity and discipline. I would also like to thank Prof. Dr. Alberica Toia, Dr. Jörg Lehnert, Dr. Adrian Rodríguez Rodríguez, Lady Maryann Collazo Sanchez, Anju Sharma, Patryk Semeniuk, and Dairon Rodríguez Garces for their explanations and technical advice, which were invaluable at every stage of this work. Their patience and willingness to discuss even the smallest details helped me understand things more deeply. Thank you all for adding warmth and laughter to everyday work life. The coffee breaks, random conversations, and moral support during stressful days made everything lighter.

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To my family, I express my deepest gratitude and love. To my parents, thank you for believing in me even when I doubted myself, for your sacrifices, and for the constant love that has carried me through every phase of life. To my grandparents, whose blessings and gentle wisdom I still feel, I owe much of who I am to you.

I am truly grateful to everyone who has been part of this journey. Your guidance, support, and encouragement have made this thesis possible and this experience unforgettable, and have made it truly worthwhile.

A quote that has stayed with me from one of my favorite books, What You Are Looking for is in the Library by Michiko Aoyama, reflects my experience throughout this thesis: *"Life is one revelation after another. Things don't always go to plan, no matter what your circumstances. But the flip side is all the unexpected, wonderful things that you could never have imagined happening."* Each challenge during this work brought unexpected insights and personal growth.

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1 Introduction

Some of the unanswered questions that lie at the core of particle physics are: What is matter made up of at its sub-atomic level? Is it possible to recreate the initial conditions of the universe here on Earth? Particle physics is a field dedicated to exploring the smallest building blocks of nature. At its core, it answers what matter is made of and how it behaves at the microscopic scale. The elementary particles described by a strong theoretical framework known as the Standard Model are based on years of experimental testing. However, the Standard Model is incomplete, and new particles are expected to exist beyond its current scope. The early universe provides a special natural laboratory beyond the capabilities of particle accelerators, where extreme temperatures and densities enable interactions and phenomena far beyond the reach of current experiments. After the Big Bang, the universe was at an incredibly high temperature and density, which allowed particles to combine and forces to behave in ways we cannot observe today. In this early phase, the universe was filled with a hot, dense plasma of fundamental particles such as quarks, gluons, electrons, positrons, photons, neutrinos, and their antiparticles, all interacting frequently and existing in thermal equilibrium. As the universe expanded, it cooled, and the intensity of these interactions reduced. As the universe cooled, several key transitions took place, ie, quarks bound into hadrons, protons and neutrons combined to form light nuclei, and eventually neutral atoms began to form as electrons bound with nuclei. These events changed the universe from a chaotic soup of elementary particles into a suitable environment to form matter as we know it. Modern-day experiments in heavy-ion collisions aim to recreate similar energy densities in the laboratory, which are trying to explore phases of matter such as the quark-gluon plasma and test theoretical models of high-energy interactions.

1.1 Elementary Particles and the Forces they Mediate

The most widely accepted theoretical model that characterizes elementary particles and their interactions in the absence of gravity is the Standard Model (SM). Figure 1.1.1 provides an overview of the 17 particles in the SM, with 12 fermions and five bosons. Greek and Latin symbols are used to represent these particles [1].

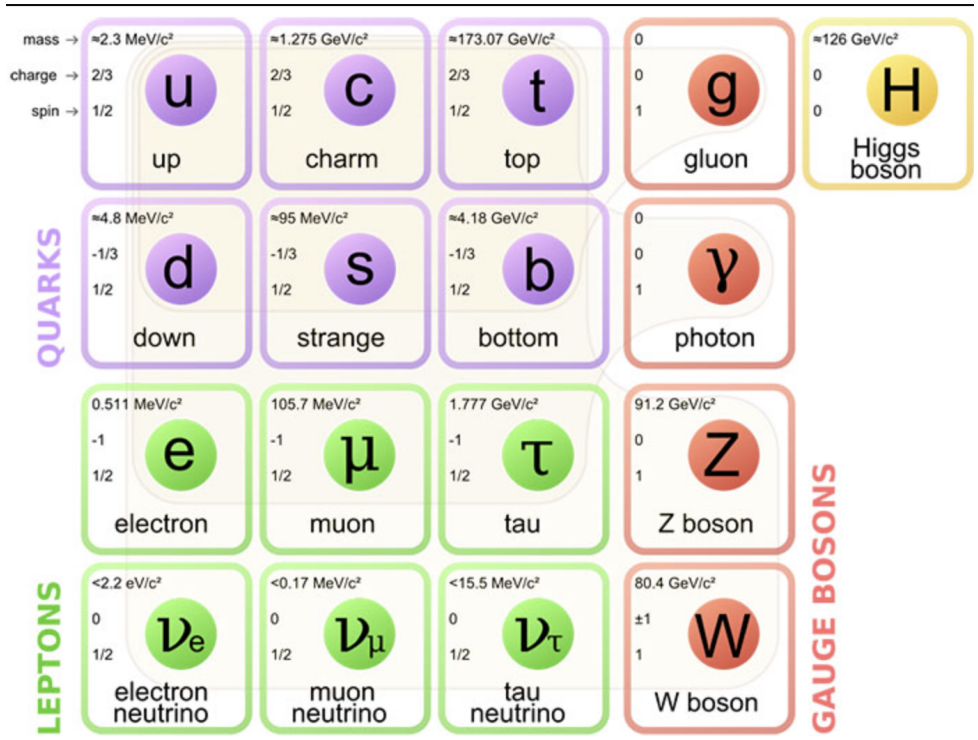

Figure 1.1.1: Overview of the Standard Model of particle physics. (Courtesy of [1])

The elementary particles are classified into two main categories: fermions that make up matter, and bosons that mediate the fundamental forces. Fermions are the primary building blocks of ordinary matter, which follow Fermi-Dirac statistics and obey the Pauli exclusion principle. They are organized into quarks and leptons, each appearing in three generations (Table 1).

Generation	Quarks	Leptons
1st	up (u), down (d)	electron (e^-), electron neutrino (ν_e)
2nd	charm (c), strange (s)	muon (μ^-), muon neutrino (ν_μ)
3rd	top (t), bottom (b)	tau (τ^-), tau neutrino (ν_τ)

Table 1: The three generations of quarks and leptons (Courtesy of [1])

Unlike fermions, bosons are force-carrying particles that follow Bose-Einstein statistics. Photons mediate through the electromagnetic force, gluons mediate through the strong force, and W and Z bosons mediate through the weak force. Bosons can interact with each other and with matter particles, transferring discrete amounts of energy and momentum.

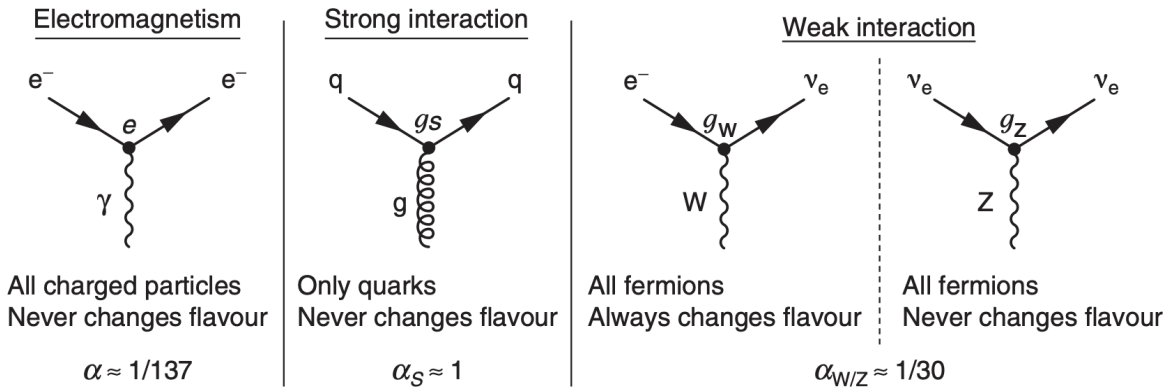

Figure 1.1.2: Feynman diagrams representing fundamental particle interactions via gauge boson exchange. (Courtesy of [2])

Feynman diagrams represent particle interactions through a three-point vertex. As seen in figure 1.1.2, each diagram includes a gauge boson and incoming and outgoing fermions [2].

1.2 QCD Matter under Extreme Conditions

The mathematical framework known as Quantum Field Theory describes the strong interaction, one of the four fundamental forces of nature, that binds together quarks and

gluons into protons, neutrons, and other hadrons. Quarks are characterized by a quantum number known as color charge, which comes in red, green, and blue. Gluons are responsible for the strong force and carry color charge in the form of color–anticolor combinations [3].

Unlike the photon in electrodynamics, gluons interact not only with quarks but also with each other. This special feature is due to the nonlinear structure of Quantum Chromodynamics (QCD) [4]. Two distinguishing features of QCD are confinement and asymptotic freedom. Quarks and gluons interact more weakly and this allows them to move freely at high energies [5]. Shortly after the Big Bang, QCD predicts a transition to a deconfinement phase known as the quark-gluon plasma (QGP). A similar transition occurs at very high temperatures and densities in the cores of neutron stars or in heavy-ion collisions [6]. At low energies, the coupling becomes strong, resulting in quarks and gluons confined within hadrons and cannot be isolated under usual conditions [7]. An equation of state is introduced to describe the properties of deconfined matter [8].

Equation of State (EoS)

The Equation of State (EoS) describes how pressure, density, energy density, and temperature are related to one another [9]. At the extreme densities found inside neutron stars, pressure becomes almost independent of temperature and is determined mainly by the mass density and the composition of matter. The EoS is expressed as

$$P = P(\rho) \tag{1}$$

The EoS (Eq. 1) plays an important role in compact objects, particularly neutron stars, that helps in modeling their internal structure, mass, and radius [10]. The EoS is essential for investigating exotic states of matter, including the quark-gluon plasma (QGP) [11].

Neutron Stars

Neutron stars (NS) are the compact remnants left behind when massive stars run out of nuclear fuel and undergo a core-collapse supernova. With typical masses of about 1.4 $M_\odot$ compressed into a radius of only 10–12 km, they are among the densest forms of matter in the universe [12]. The density at the core of a NS is extremely high, potentially leading to the formation of exotic matter phases like hyperons, or deconfined quarks [13]. To study and analyze the internal structure, it is necessary to employ the Tolman-Oppenheimer-Volkoff (TOV) equations (Eqs. 2 and 3), which describe the balance between gravitational collapse and internal pressure in relativistic conditions:

$$\frac{dP(r)}{dr} = -\frac{G\left[\varepsilon(r) + P(r)\right]\left[M(r) + 4\pi r^3 P(r)\right]}{r\left[r - 2GM(r)\right]} \tag{2}$$

$$\frac{dM(r)}{dr} = 4\pi r^2 \varepsilon(r) \tag{3}$$

Here, $P(r)$ is the pressure, $\varepsilon(r)$ is the energy density, $M(r)$ is the enclosed mass at radius r, and G is the gravitational constant [14]. The relationship between energy density and pressure $P(\varepsilon)$ - the EOS, is needed to solve these equations and predict the mass-radius relationship of neutron stars [15]. Further to help constrain the EoS, Pulsar timing, X-ray measurements, and gravitational-wave detections from binary neutron star mergers are studied to improve our understanding of the composition and behavior of matter at extreme densities [16]. These insights are consistent with results from heavy-ion collision experiments on Earth, helping to advance our knowledge of QCD under extreme conditions [17].

1.3 Phase Diagram of the Quark-Gluon Plasma(QGP)

Protons and neutrons are not indivisible, but are made up of quarks bound together by gluons. These quarks and gluons are fundamental constituents of the SM, each carrying a distinct property called color charge [18]. This force is much stronger than the other fundamental forces at the subatomic scale.

Quarks and gluons are generally not isolated; instead, they remain confined within composite particles such as protons, neutrons, and other hadrons [18]. However, at extremely high temperatures and densities, quarks are able to move more freely as they overcome the confinement. When nucleons melt in the dense and hot environment, their components become free to move, producing a new state of matter known as the quark-gluon plasma (QGP). These conditions existed naturally just a few microseconds after the Big Bang, when the universe was sufficiently hot and dense for quarks and gluons to move freely [19] [20].

At low temperatures and baryon chemical potential (μ_B), matter exists as a hadron gas, as seen in figure 1.3.1. And at high temperature, it transitions into a deconfined quark–gluon plasma [21]. Lattice QCD studies indicate that at low μ_B, this transition is a gradual change near $T = 155$ MeV. As μ_B increases, the models indicate a possible first-order phase change accompanied by a critical point. Until now, these predictions have not yet been experimentally verified. Different heavy-ion facilities are exploring corresponding regions of the phase diagram, such as the LHC and RHIC, which focus on high temperature and low μ_B, whereas FAIR and NICA target the high-density regime [21].

To investigate these questions, relativistic heavy-ion collision experiments aim to recreate conditions similar to those in heavy-ion collisions on Earth. High-energy laboratories - like the Relativistic Heavy Ion Collider (RHIC) at Brookhaven [22] and the A Large Ion Collider Experiment (ALICE) at CERN [23] probe matter at very high temperatures and low baryon density, ideal for studying crossover behavior and QGP properties.

In contrast, recently constructed facilities such as NICA in Dubna [24] and the CBM experiment at FAIR in Darmstadt [25] are designed to probe regions of higher baryon density, providing fresh insights into the QCD phase diagram at high μ_B [25].

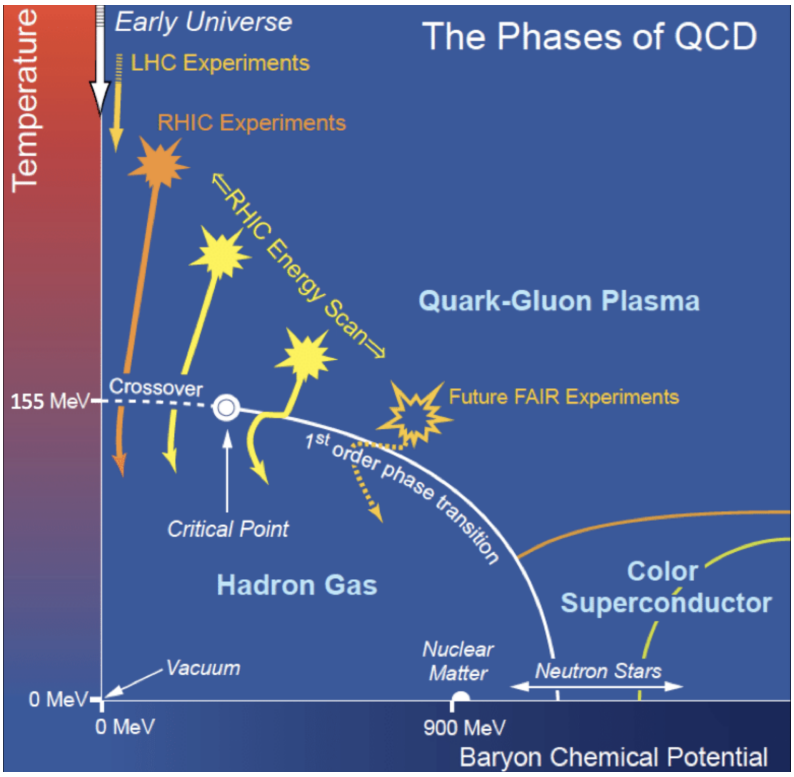

Figure 1.3.1: Shows the phases of strongly interacting matter as a function of temperature T and baryon chemical potential (μ_B). (Courtesy of [21])

Experiment	Beam Energy / $\sqrt{s_{NN}}$	Mode	Transition Region
CBM (FAIR, Darmstadt)	2–11 AGeV (Au ions, SIS100 fixed-target)	Fixed-target	1st-order transition, critical point, high μ_B
RHIC (Brookhaven)	$\sqrt{s_{NN}} = 7.7$–200 GeV	Collider	Crossover at low μ_B, search for critical point
ALICE (CERN, Pb–Pb)	$\sqrt{s_{NN}} = 5.02$ TeV per nucleon pair	Collider	High T, low μ_B; crossover
NICA (Dubna, MPD)	$\sqrt{s_{NN}} \approx 3$–9 GeV	Collider / hybrid	High μ_B; 1st-order transition; critical point

Table 2: Heavy-Ion Facilities and QGP Studies (Courtesy [26] [27])

Table 2 summarizes some of the heavy-ion experiments, their beam energies, and the QCD transition regions they explore. Each of these facilities investigates different parts of the QCD phase diagram through detailed studies of QGP formation, characterized by the center-of-mass energy per nucleon–nucleon pair ($\sqrt{s_{NN}}$) in heavy-ion collisions.

1.4 Physics Goals of the CBM Experiment

To achieve its objectives, the CBM experiment utilizes heavy-ion collisions, such as Au+Au at beam energies between 2 and 11 AGeV, provided by the SIS-100 at FAIR. This energy range is well suited for producing dense baryonic matter at moderate temperatures, allowing us to investigate both collective behaviour in the medium and the properties of individual particles emerging from the collision zone. To study rare probes that carry information about the early and dense stages of the collision, the high interaction rates are made achievable in CBM [28]. To explore these extreme conditions in detail, the experiment focuses on rare particles, which reveal different aspects of the dense matter created during the collisions.

Study of Di-Leptons

One of the primary probes of interest is the study of di-leptons, including electron-positron and muon–antimuon pairs. Di-leptons interact only electromagnetically and thus pass through the medium largely unaffected, providing a clean signal of the high-density conditions The CBM experiment investigates how vector mesons (ρ, ω, ϕ) change their properties in dense nuclear matter, providing insight into how hadrons behave under such extreme conditions [28] [29]. At the same time, di-lepton measurements give a glimpse into the thermal radiation emitted by the medium, helping to understand its temperature and evolution, as shown in figure 1.4.1 [29].

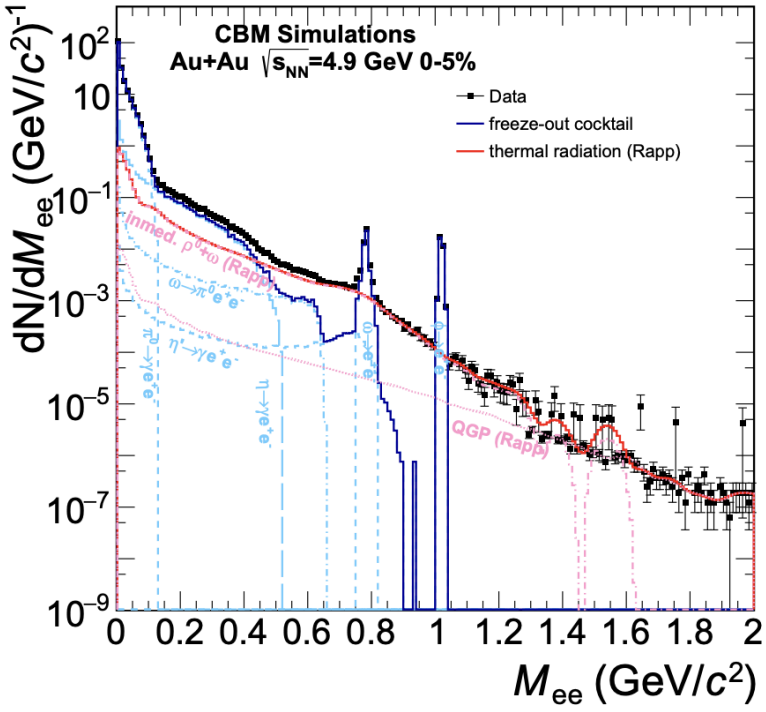

Figure 1.4.1: Highlighting the contributions from individual meson decays (blue) and thermal radiation components (red), the dielectron spectrum for central Au+Au collisions at $\sqrt{s_{NN}} = 4.9$ GeV is predicted. (Courtesy of [31])

Study of open and hidden charm

The next primary focus of the CBM experiment is the production of both open charm (D mesons) and hidden charm (charmonium states such as J/ψ). Charm hadrons are rarely created in heavy-ion collisions, but their behavior is highly sensitive to the medium. By studying production rates, the distribution of their momenta, and their suppression, CBM can probe the dense nuclear matter properties and search for signatures of deconfinement or QCD phase transitions in the high-density regime [28] [30].

Study of Strangeness and Hypernuclei

Another important aspect of the CBM experiment is the study of strangeness and hypernuclei. Strange quarks are not present in ordinary matter but are produced in heavy-ion collisions in the form of strange and multi-strange baryons (Λ, Ξ, Ω). The production of these particles would provide valuable insight into the dynamics of dense matter and the processes that lead to chemical equilibration. Hypernuclei, particularly those containing double Λ hyperons, allow the study of hyperon-nucleon and hyperon-hyperon interactions, which are essential for understanding the structure of neutron stars and the so called hyperon puzzle [31]. By measuring decay patterns, and interactions as shown in figure 1.4.2, CBM investigates exotic degrees of freedom and the role of strangeness in high-density QCD matter.

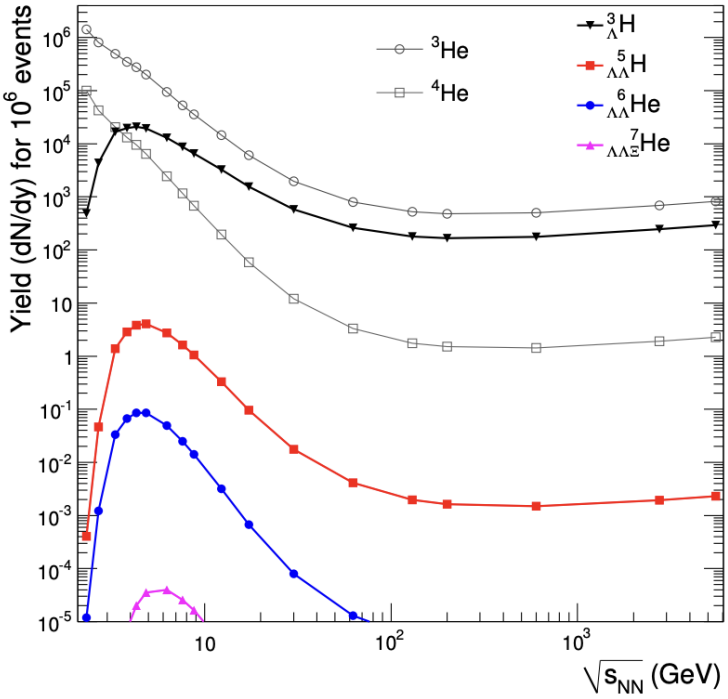

Figure 1.4.2: The thermal model predicting strange particle production in Au+Au collisions. (Courtesy of [28])

2 Overview of the Facility for Antiproton and Ion Research (FAIR)

The Facility for Antiproton and Ion Research (FAIR) is one of the most advanced accelerator facilities, located in Darmstadt, Germany, designed to explore the fundamental properties of matter under extreme conditions [32, 33]. Constructed as an extension of the existing GSI Helmholtz Centre for Heavy Ion Research, FAIR integrates a new high-performance accelerator complex with the extensively developed GSI infrastructure [32]. At the heart of FAIR's accelerator lies the SIS100 synchrotron, a superconducting accelerator ring with a circumference of approximately 1,100 m [32, 34].

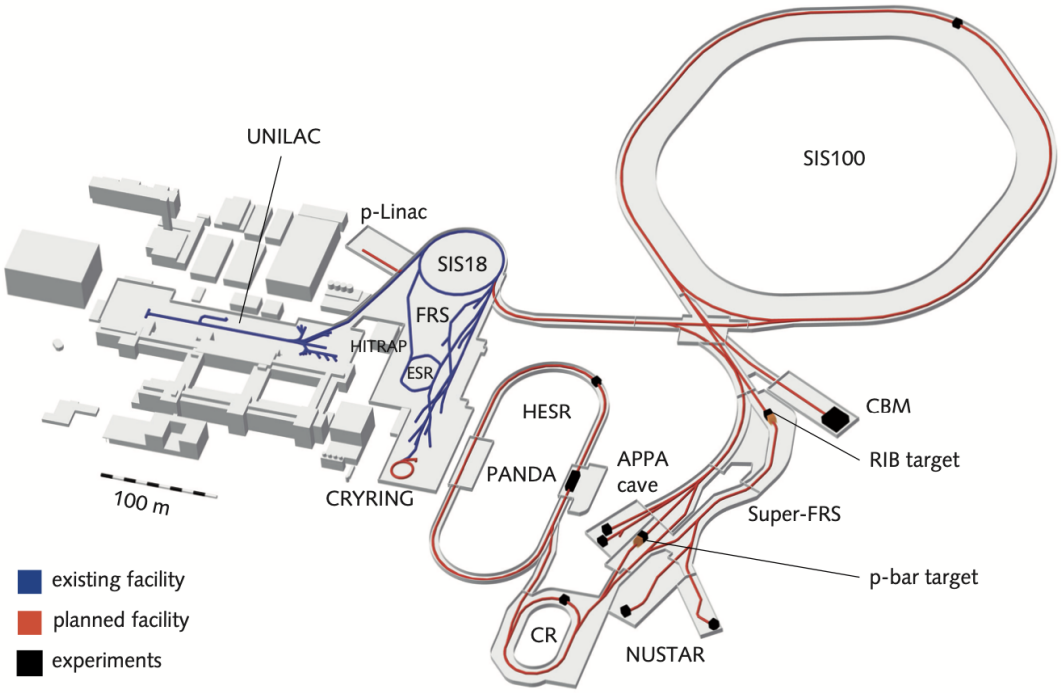

Figure 2.0.1: Overview highlighting the SIS100 synchrotron, which provides high intensity beams from the existing GSI campus (blue) to the CBM experiment in the planned FAIR facility (red). (Courtesy of GSI/FAIR Darmstadt)

It receives beams from the SIS18 synchrotron, which serves as its injector, and is capable of accelerating heavy ions to energies of up to 11 GeV per nucleon and protons up to 30 GeV [33] [35]. FAIR will use beams from the SIS100 synchrotron, including protons up to 29 GeV, gold ions up to 11 AGeV, and nuclei with Z/A = 0.5 up to 14 AGeV. In the future, the facility might be extended with the SIS300 synchrotron, which will accelerate protons up to 90 GeV, gold ions up to 35 AGeV, and nuclei with Z/A = 0.5 up to 45 AGeV [25]. Figure 2.0.1 shows the schematic layout of the FAIR accelerator, including the SIS18 injector, the SIS100 synchrotron, experimental halls, and beamlines.

The scientific program at FAIR is organized into four major collaborations, each addressing a distinct domain of modern physics [32] :

- **APPA – Atomic physics, Plasma Physics, and Applications.**
- **CBM – Compressed Baryonic Matter experiment, focusing on nuclear matter at high baryon densities.**
- **NuSTAR – NUclear STructure, Astrophysics, and Reactions.**
- **PANDA – AntiProton ANnihilation at DArmstadt, dedicated to hadron physics with antiprotons.**

Once operational, FAIR will deliver high-intensity beams, enabling experiments on heavy elements to investigate dense nuclear matter similar to that found in neutron stars [25].

2.1 The Compressed Baryonic Matter Experiment(CBM)

The Compressed Baryonic Matter (CBM) experiment at FAIR is designed to investigate nuclear matter at extreme densities and aims to explore the part of the QCD phase diagram where a first-order phase transition and the critical endpoint are expected, providing insight into how matter behaves under conditions of very high μ_B and moderate temperature [25].

CBM is designed to handle extremely high interaction rates,which is essential for studying rare probes such as charm particles, hypernuclei, and multi-strange hadrons, which provide sensitive signals of dense nuclear matter. The experiment features a fixed-target setup, allowing continuous collection of collision events and enabling precision measurements of observables such as particle production, flow patterns, and fluctuations [25].

The detector concept is based on fast, radiation hard subsystems arranged in a compact geometry around the target [25]. CBM's electronics are designed for free streaming readout, meaning data are continuously acquired and time stamped without relying on a conventional hardware trigger [36]. This approach allows the system to handle 10^7 events per second, with real-time event reconstruction and selection performed by a high-performance computing system [36]. Such a framework ensures that rare signals are captured efficiently while maintaining precise tracking, vertexing, and particle identification [37].

2.2 Overview of Sub-detectors in the CBM setup

This section provides a detailed description of the various detectors of the CBM experimental setup, highlighting the specific roles each detector plays within the overall system. Figure 2.2.1 illustrates a schematic representation of the major detectors comprising the system [25, 38]:

- Beam Monitor detector (BMON): Provides precise reference timing for collisions and continuously monitors the beam profile and stability to ensure accurate and safe measurements.
- Superconducting Magnet: Generates a stable magnetic field to bend he path of a charged particle, for accurate measurement of the momentum.
- Micro Vertex Detector (MVD): Provides high resolution vertex reconstruction close to the interaction point, enabling identification of short lived particles such as D mesons and hyperons.

- Silicon Tracking System (STS): Precisely tracks charged particle trajectories within the magnetic field and reconstructs their momentum. Positioned inside the dipole magnet, the STS is designed to handle high track densities and contributes to vertex reconstruction for heavy ion collisions.

- Ring Imaging Cherenkov (RICH): Identifies electrons by detecting Cherenkov light rings. Electron identification is essential for studying di-lepton production, which probes the early stages of heavy-ion collisions.

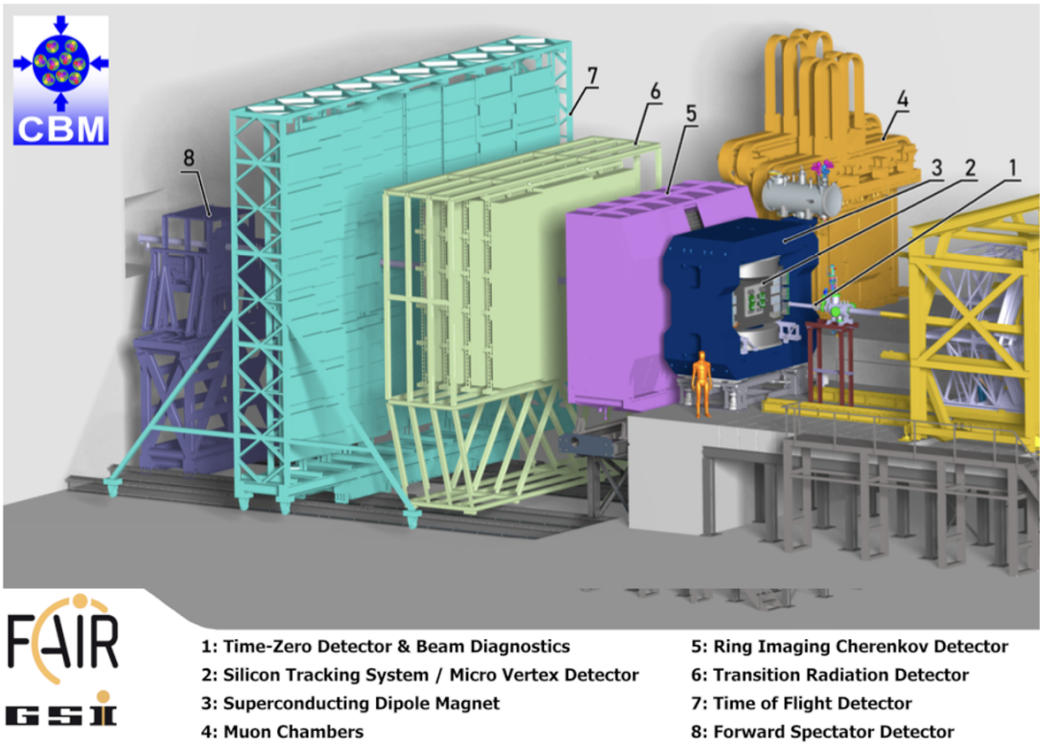

Figure 2.2.1: Overview of the CBM experimental setup illustrating the arrangement of its sub-detectors. (Courtesy of [39])

- Muon Chambers (MUCH): Detects and tracks muons by filtering out other particles using absorber layers. It measures muon pairs from vector meson decays, providing insight into modifications of hadrons.

- Transition Radiation Detector (TRD): Distinguishes electrons from heavier charged particles by detecting transition radiation photons. The TRD complements the RICH in electron identification and improves overall particle identification.

- Time of Flight (ToF): Measures particle flight times to determine velocity, aiding particle identification by separating hadrons such as pions, kaons, and protons.
- Forward Spectator Detector (FSD): Measures the energy of spectator fragments to provide information about the collision geometry and the orientation of the event plane. These measurements allow an evaluation of the nuclear interactions and serve as necessary input for the analysis of collision dynamics.

Beam Monitor (BMON)

The BMON system provides the start time (T_0) for time-of-flight measurements and continuously monitors the beam upstream of the target. It consists of a T_0 station positioned along the beam axis and a halo station positioned slightly to the side of the central beam path, allowing it to monitor the beam halo as shown in figure 2.2.2. Both stations use polycrystalline CVD diamond sensors that are about 1 × 1 cm^2 in size and 70–100 µm thick, with double-sided strip metallization (16 × 16 strips); this allows accurate measurements of both the timing and the position of the beam [40].

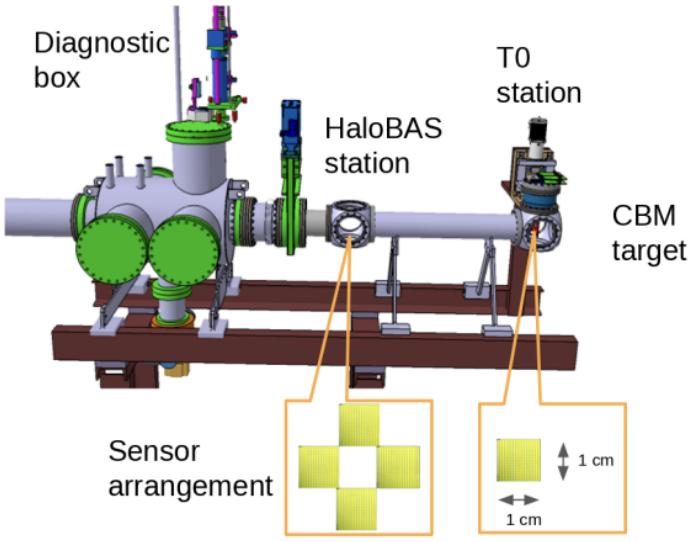

Figure 2.2.2: Schematic of the CBM BMON system with T timing and beam halo monitoring stations. (Courtesy of [40])

The sensors are mounted on motorized supports and can be safely moved away from the beam when required. The signals are amplified by front-end preamplifiers and processed through PreAmplifier Discriminator (PADI) ASICs, which convert the analog signals into digital pulses. These are further digitized by GSI Event-driven Time to Digital Converters (GET4 TDCs) to record precise arrival times. The signals are sent to the main Data Acquisition System (DAQ) for physics measurements and simultaneously to a safety system that monitors the beam [40].

Superconducting dipole magnet

The CBM experiment employs a superconducting dipole magnet with a magnetic power of 1 T · m and an H-type design as shown in figure 2.2.3. It is positioned directly downstream of the target, and the magnet houses the STS and MVD detectors. This configuration allows the detectors to track particle trajectories accurately, identify primary and secondary vertices, and measure particle momenta. The magnet provides a ±25° vertical and ±30° horizontal acceptance, ensuring that particles emitted within these angles are detected [41].

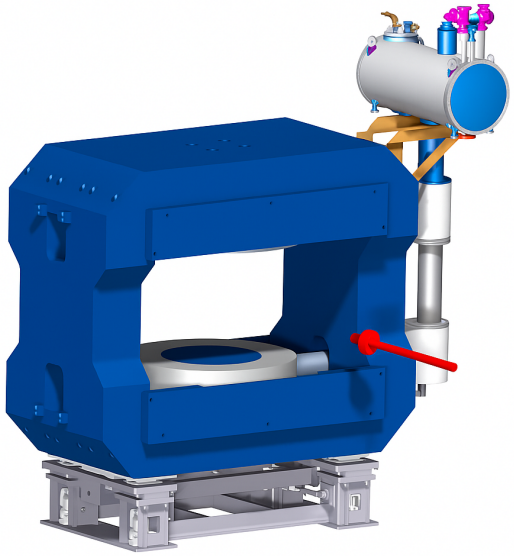

Figure 2.2.3: The Superconducting dipole magnet. (Courtesy of [42])

Micro Vertex Detector (MVD)

MVD, as illustrated in figure 2.2.4, is located inside the superconducting dipole magnet, 5 to 20 cm downstream of the target. Its main purpose is to measure the primary and secondary vertices of particles produced in heavy-ion collisions, particularly short-lived particles such as open charm mesons and hyperons [44].

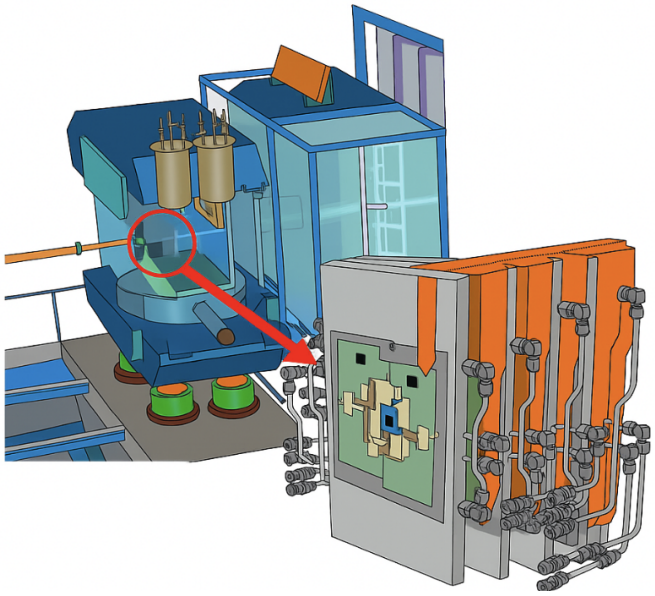

Figure 2.2.4: The MVD inside the superconducting dipole magnet. (Courtesy of [43])

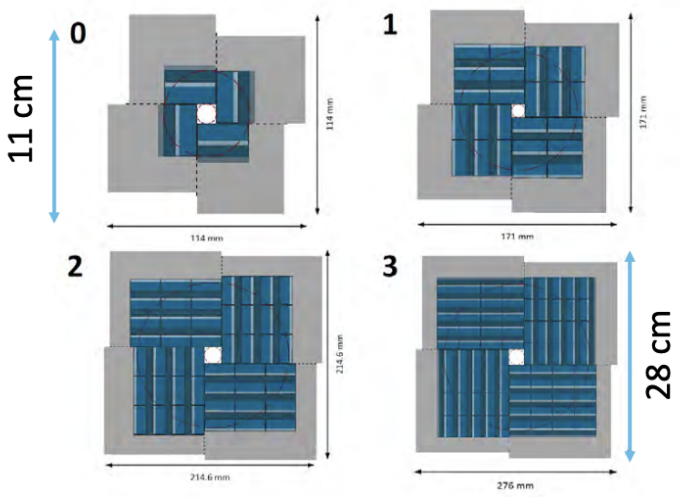

Figure 2.2.5: The four MVD detector stations, and arrangement of MAPS sensors in each station. (Courtesy of [43])

The MVD consists of four stations, as shown in figure 2.2.5. Stations 1 through 4 contain 8, 40, 84, and 160 Monolithic Active Pixel Sensors (MAPS), respectively, arranged around the beamline [43]. These sensors are crucial for detecting decay vertices of short-lived particles. MAPS provide high spatial resolution, can withstand the high radiation environment, and have a low material budget. These features enable the detector to reconstruct particle trajectories with high precision [43, 44]

Silicon Tracking System (STS)

The Silicon Tracking System (STS), as the central tracking detector in the CBM setup, is placed inside the dipole magnet, where the magnetic field enables precise momentum measurement and plays a key role in reconstructing charged particle trajectories. Further technical details are discussed in Section 3.

Ring Imaging Cherenkov Detector (RICH)

RICH detector, as shown in figure 2.2.6, identifies electrons by detecting Cherenkov radiation, which is emitted at a characteristic angle, forming a ring pattern. Located about 1.6 m downstream of the target, the RICH uses a gaseous radiator, primarily CO_2, and a segmented mirror system coated with aluminum and a thin MgF_2 layer to reflect Cherenkov light onto a plane of Multi-Anode Photomultiplier Tubes (MAPMTs). The MAPMTs multiple anodes record light at different positions simultaneously, and by analyzing these signals, the detector reconstructs the Cherenkov rings, measures their angles, determines particle velocity, and efficiently separates electrons and positrons from pions and other charged particles [45, 46].

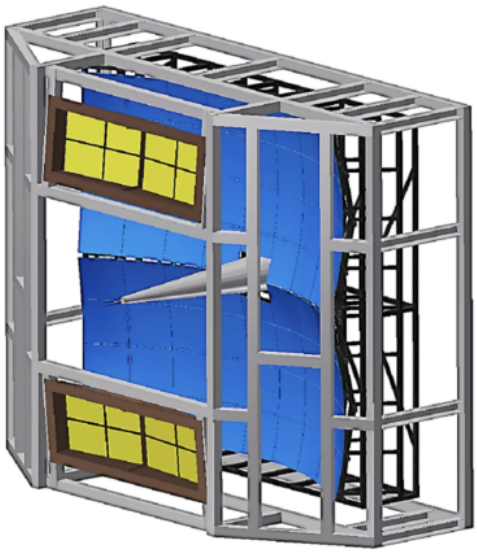

Figure 2.2.6: The RICH detector used for electron identification. (Courtesy of [46])

Muon Chambers System (MUCH)

The MUCH detector as seen in figure 2.2.7, is designed to detect di-muons ($\mu^+\mu^-$) produced in heavy-ion collisions, which are observed when rare probes such as low mass vector mesons (ρ, ω, φ, etc.) decay. The MuCh system consists of five hadron absorber layers, including a 60 cm carbon plate followed by iron plates of 20 cm, 30 cm, 35 cm, and 100 cm thickness, designed to stop most hadrons while allowing muons to pass. The muons are tracked and identified by a combination of absorber layers, Gas Electron Multipliers (GEMs), and multi-gap Resistive Plate Chambers (mRPCs). The system comprises four detector stations. Stations 1 and 2 are equipped with GEMs for precise tracking, while Stations 3 and 4 utilize Resistive Plate Chambers (RPCs) and mRPCs for high-precision timing [47].

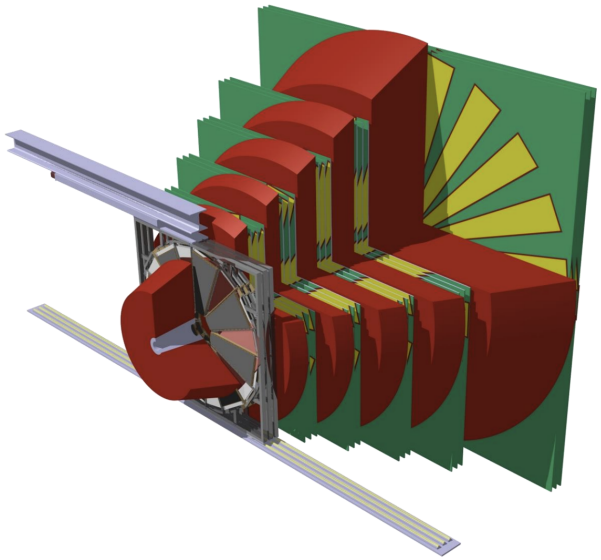

Figure 2.2.7: The MUCH detector designed for di-muon detection. (Courtesy of [47])

Transition Radiation Detector (TRD)

The TRD detector, as seen in figure 2.2.8a, identifies electrons with momenta above 1.5 GeV/c, similar to the capabilities of the RICH detector. It works on the principle of transition radiation, which occurs when a charged particle traverses from one material to another with different dielectric properties. The effect is much stronger for electrons than for heavier particles, so that the detector can separate electrons from pions. The TRD uses Multi-Wire Proportional Chambers (MWPCs) in combination with pad planes to measure particle tracks accurately. It is positioned approximately 4–5 m downstream of the target, after the RICH detector, which increases the chances of identifying higher-momentum electrons [48].

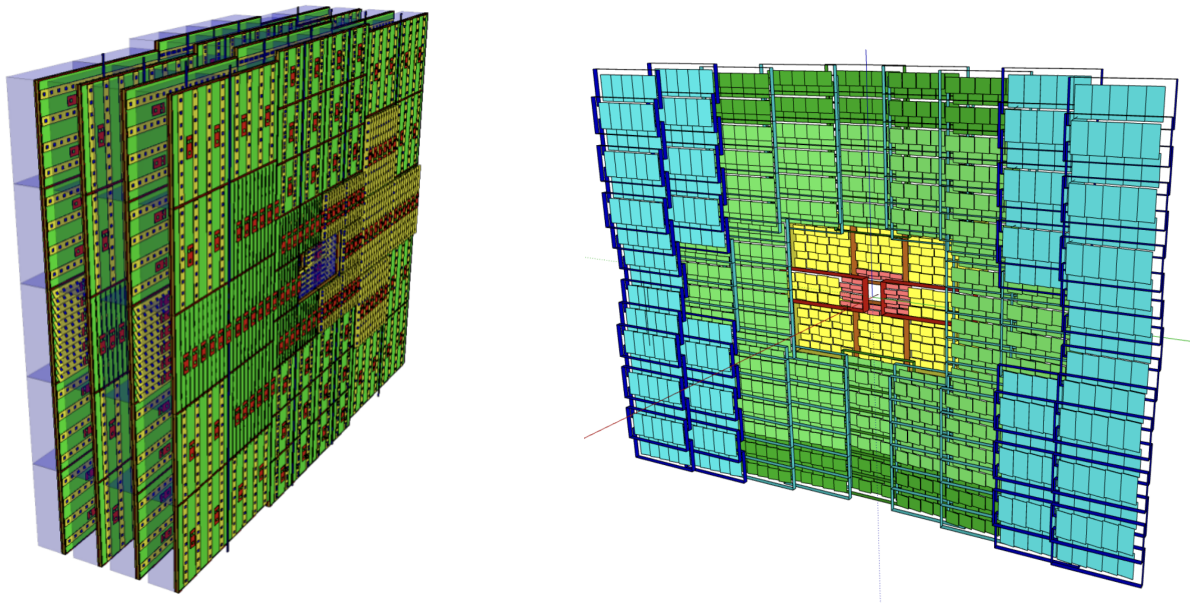

Figure 2.2.8: (a)The TRD detector design (Courtesy of [48] (Left side)); (b)The TOF detector design (Courtesy of [49] (right side))

Time of flight (TOF)

The TOF detector, as seen in figure 2.2.8b, is positioned approximately 10 m downstream from the target and occupies an active area of nearly 120 m^2. It is used to identify charged particles, mainly hadrons such as pions, kaons, and protons, by measuring their time of flight along with their momentum and track length to determine their mass. The detector is composed of Multi-Gap Resistive Plate Chambers (MRPCs), which provide excellent timing resolution and high detection efficiency, which helps in precisely identifying the particles. Particles with the same momentum can have different masses. As a result, their times of flight differ, enabling the detector to distinguish between them [49].

Forward Spectator Detector (FSD)

The FSD, as seen in figure 2.2.9a, measures spectator fragments from heavy-ion collisions to provide information on the collision geometry and the event plane orientation. It is placed downstream of the target along the beam axis, where most spectator fragments travel, and consists of a lead-scintillator calorimeter made up of 44 modules, each measuring 20 × 20 cm^2, as seen in figure 2.2.9b, arranged in a horizontal, elongated layout around the beam. A small central hole in the four central modules allows the main beam of particles to pass through without hitting the detector. The scintillator light in each module is read out by micropixel avalanche photodiodes (MAPDs), and the signals are processed by dedicated front-end electronics integrated with the CBM data acquisition system. Using these measurements, the FSD can estimate the number of participating nucleons, characterize the collision geometry, and determine the orientation of the event plane, providing critical input for the CBM physics [50].

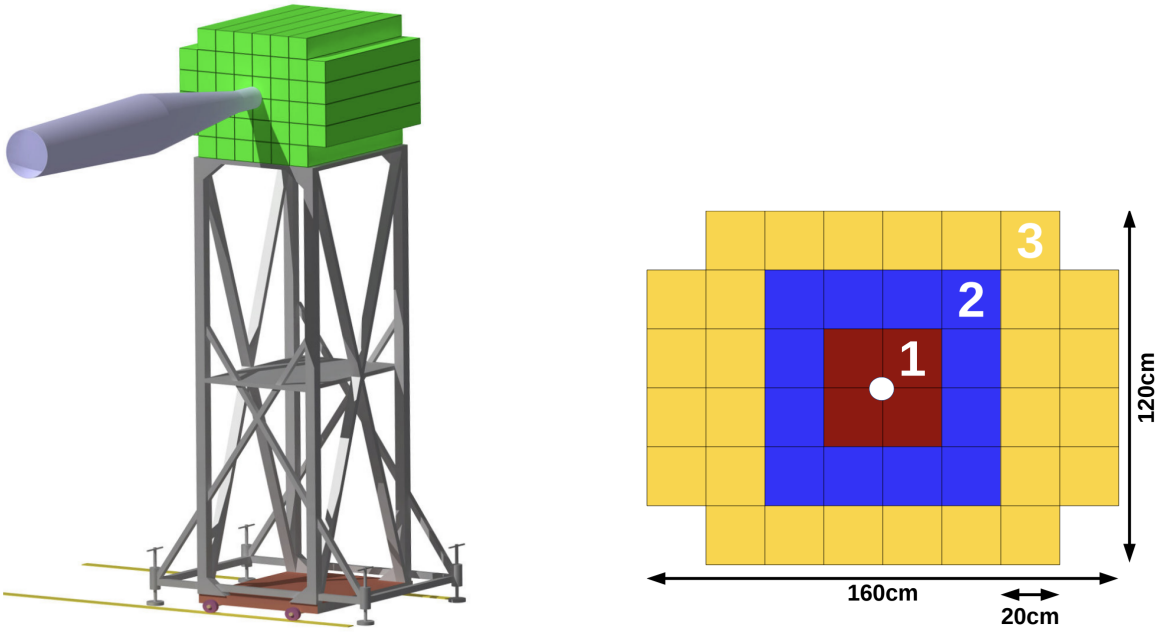

Figure 2.2.9: (a) The PSD detector design (Courtesy of [50]); (b) The modules (Courtesy of [50])

3 Silicon Tracking System (STS)

The Silicon Tracking System (STS) is positioned 30 cm to 100 cm downstream of the fixed target inside the dipole magnet, covering polar angles from approximately 2.5° to 25° as seen in figure 3.0.1, and it serves as the central detector for charged particle tracking. The STS precisely measures the trajectories of the particles in the magnetic field, and it achieves a tracking efficiency higher than 95% and a momentum resolution of nearly 1.5% for particles with momenta above 1 GeV/c [51]. This high accuracy is essential for studying short-lived particles, which provide insight into QCD matter at high μ_B [52, 53].

The STS comprises eight tracking stations, as seen in figure 3.0.2, containing 106 ladders that support 896 modules mounted on carbon-fiber (CF) framework. This framework provides mechanical support, while keeping the material budget low, matches the properties of thermal expansion of silicon sensors, and minimizes the stress from temperature variations [55]. This arrangement ensures precise alignment of the modules and optimal placement of the Front-End Boards (FEBs) and cooling systems [53, 54]]. The STS uses double-sided silicon microstrip sensors (DSMS) (more details in Section 4.1.1), which convert particle interactions into measurable electrical signals [55, 57]. Each module is connected to the FEBs through ultra-thin aluminum-polyimide micro-cables [57]. The FEBs house custom STS-XYTER (STS X and Y coordinate, Time and Energy Readout chip) ASICs (Application Specific Integrated Circuits), which amplify, shape, and digitize signals from the micro-strip sensors [58, 59]. Each ASIC handles 128 input channels with low noise and low power consumption. The system measures momentum with high precision and also records timing information. The ASICs generate timestamps with nanosecond accuracy. This allows the detector to distinguish overlapping events in CBM's continuous, free-streaming data acquisition [53, 54, 59].

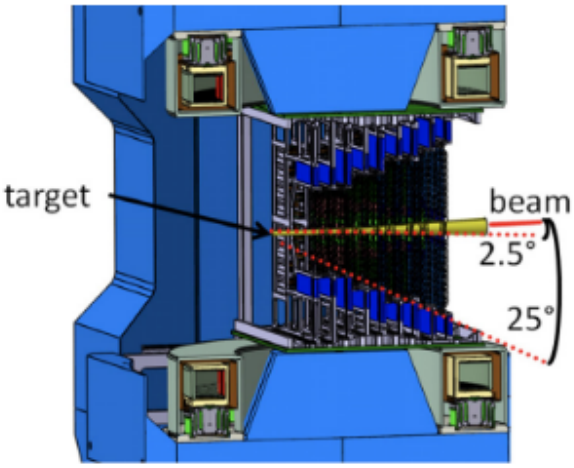

Figure 3.0.1: The STS detector placed inside the dipole magnet. (Courtesy of [52])

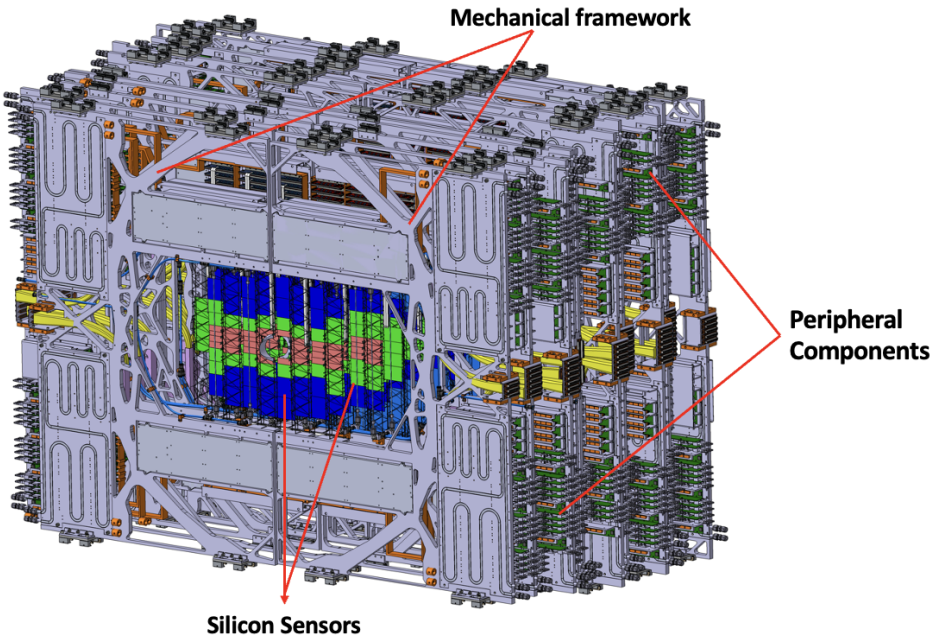

Figure 3.0.2: 8 Tracking stations of STS detector with modules arrangement. (Courtesy of O. Vasylyev (GSI, Darmstadt))

Supporting self triggered, continuous readout at interaction rates of up to 10 MHz, the FEBs generate high data volumes (several gigabytes per second), which are processed by the first-level event selection (FLES) computing system, demonstrating the close integration between the detector and computing infrastructure [53, 54, 57].

The design of the detector follows several key requirements, which are summarized below in Table 3 [52, 53]:

Design Requirement	**Description**
High tracking accuracy	Ensure particle trajectories are reconstructed with high precision, aiming for momentum resolution of about 2% or better.
Minimal material interference	Limit the material in each tracking station to $\leq 1\%$ of a radiation length to reduce scattering and preserve measurement accuracy.
Radiation Hardness	Maintains reliable detector operation under high particle fluxes, and ionizing doses near 1 Mrad without loss of performance [60].
Continuous high-rate readout	Supports continuous self-triggered data at high interaction rates, and is capable of tracking hundreds of particles simultaneously.
Front-end reliability	Guarantee stable performance of electronics under long-term exposure to radiation.
Thermal management	Efficiently removes heat from sensors and electronics to maintain stable operating temperatures and prevent performance degradation [61].

Table 3: Key Design Requirements of the Silicon Tracking System (STS)

The STS units are enclosed in a thermal box that maintains a stable environment by controlling temperature and humidity, preventing condensation that could damage the sensors. Each FEB dissipates a few watts of heat and is mounted on cooling blocks to ensure optimal operating conditions [61]. Overall, the detector dissipates roughly 50 kW of thermal power, mainly from the front-end and readout electronics, with smaller contributions from the sensors and low-voltage data and power cables [57, 61], which is effectively removed by a cooling system [61].

This section gives an overview of the STS's function. The following chapters focus on the modules and ladders, their testing, and the integration of the STS half-unit. They also describe mechanical assembly and performance assessments carried out during prototyping and full-scale mock-up phases.

4 Modules and Ladders as a Functional Unit

Building upon the general design of the STS, this section provides a detailed examination of its fundamental structural units: The modules and ladders.

4.1 STS Detector Module

The module, as seen in figure 4.1.1, is the fundamental building block of the STS detector, comprising two FEBs connected via ultra-thin microcables. Each FEB hosts eight ASICs that are connected to the strip sensors [62].

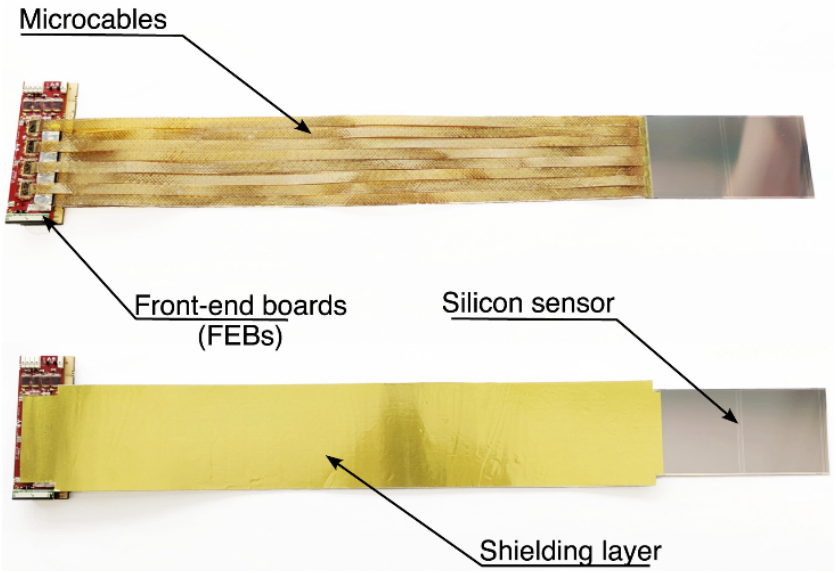

Figure 4.1.1: Module of sts detector(Courtesy of [56]).

4.1.1 Microstrip Sensors

Silicon is one of the most widely used detector materials, primarily because of its bandgap of 1.12 eV, which provides an optimal balance between signal strength and low thermal noise. In contrast, germanium, with its smaller bandgap (0.66 eV), produces higher leakage current and noise, while diamond, with a much larger bandgap (5.5 eV), requires significantly more energy to generate electron–hole pairs, resulting in weaker signals. In silicon, approximately 3.6 eV is needed to produce a single electron–hole pair [63].

Silicon detectors are made by doping silicon with p-type and n-type impurities to form p–n junctions, which create an internal electric field [64]. This field separates the electron–hole pairs produced by passing particles, directing electrons to the n-side and holes to the p-side. The p-type region is doped with acceptors like boron, while the n-type region uses donors such as phosphorus or arsenic [64]. When these regions meet, electrons from the n-side diffuse into the p-side and recombine with holes, while holes from the p-side diffuse into the n-side. This creates a depletion region at the junction, almost entirely free of mobile charge carriers. A reverse-bias voltage pushes electrons and holes away from this region, widening it and strengthening the internal electric field [64]. This field is essential for quickly collecting the charges generated when a particle passes through the sensor. In the STS, the sensors are made from n-type silicon. n^+ strips are created by doping one side, and p^+ strips are doped on the other side, forming multiple p–n junctions across the sensor [68]. This is the active region, where charged particles passing through generate electron–hole pairs. The p^+ and n^+ regions are doped with optimized concentrations to achieve maximum detection efficiency [68].

As a charged particle moves through a silicon sensor, it loses energy by ionizing silicon atoms, which creates electron-hole (e-h) pairs. The electrons move toward the n-side and holes toward the p-side as seen in figure 4.1.2. This produces a small current pulse that reflects the particle's energy loss [65].

The charge collected by the sensor depends on the amount of energy the particle loses while moving through the silicon. This energy loss can be described using the Bethe-Bloch formula (Eq. 4) [66]:

$$-\frac{dE}{dx} = K\frac{z^2 Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_e c^2\beta^2\gamma^2 T_{\max}}{I^2} - \beta^2 - \frac{\delta}{2}\right] \tag{4}$$

where:

- $K \approx 0.307$ MeV $\cdot$ cm^2/g is a constant,
- z is the charge of the incoming particle,
- Z and A are the atomic number and mass of the medium,
- $\beta = v/c$ is the particle velocity relative to the speed of light,
- $\gamma = 1/\sqrt{1-\beta^2}$ is the Lorentz factor,
- $T_{\max}$ is the maximum kinetic energy transferred to an electron in a single collision,
- I is the mean excitation energy of the medium,
- δ is the density effect correction.

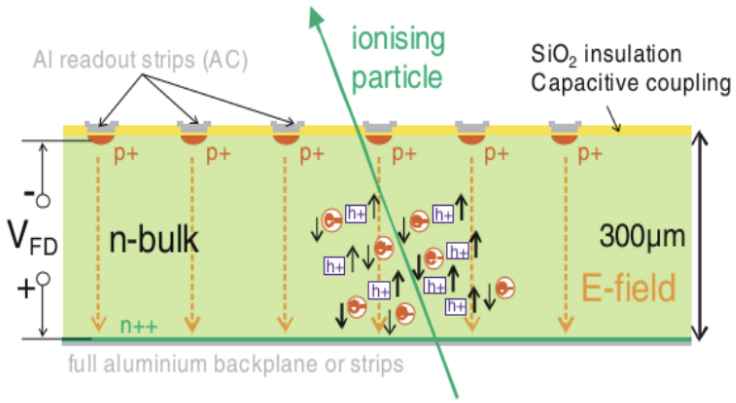

Figure 4.1.2: Schematic of a sensor under reverse bias, showing the generation of a primary electron–ion pair by a traversing ionizing particle(Courtesy of [67]).

The pulse passes through preamplifiers, which convert the collected charge into a measurable voltage while preserving timing and pulse shape. The amplified signal is then digitized for particle tracking [65].

Compared to other silicon detectors, such as pixel sensors, micro-strip sensors provide an excellent balance between high spatial resolution, large sensitive area coverage, and low power consumption. They comprise a thin, high-purity silicon wafer with narrow conductive strips fabricated on both sides [70, 71]. Single-sided strip sensors measure coordinates along a single axis. But, the DSMS sensors have n-side strips oriented vertically (along the y-axis), while the p-side strips are set at a slight stereo angle of 7.5°, as shown in Figure 4.1.3a. This arrangement is crucial for 3D track reconstruction and helps minimize ghost hits.

These sensors are manufactured by Hamamatsu K.K. Each side of the sensor contains 1024 strips with a pitch of 58 µm, allowing precise spatial measurements across the sensitive area. The sensors are produced in four sizes, as shown in figure 4.1.3b, with strip lengths of 22 mm, 42 mm, 62 mm, and 124 mm, and a fixed width of 62 mm.

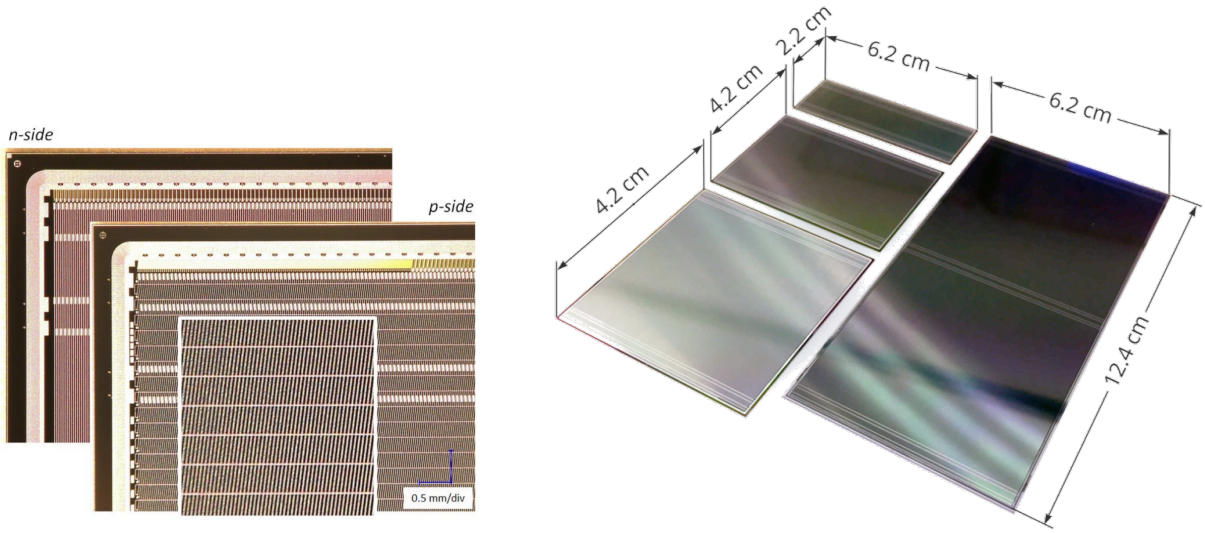

Figure 4.1.3: (a) The n-side and p-side of the silicon wafer (Courtesy of [72]) (b) STS silicon micro-strip sensors: same width of 6.2 cm, available in four strip lengths (2.2, 4.2, 6.2, and 12.4 cm) for different module requirements (Courtesy of [74]).

The strips collect the analog signals generated when charged particles pass through the silicon. These signals are transmitted through low-mass microcables to the front-end electronics (FEEs), which are amplified and prepared for digitization and further processing [70, 71, 56]. The sensors are optimized for radiation hardness, ensuring stable operation even under high particle fluxes over long periods [70, 71].

4.1.2 Ultra light Aluminium–Polyimide Microcables

The ultra-light aluminium–polyimide microcables connect the silicon strip sensors and the FEEs [72]. They carry the signals coming directly from the sensors without adding distortion. They achieve this by combining very thin polyimide insulation with fine aluminium traces. Because the materials are extremely light, the cables add almost nothing to the overall material budget [73].

Aluminium is chosen because it combines low mass, good electrical conductivity, and strong resistance to radiation, all of which are essential for the STS environment [72, 73]. The architecture of the microcables, consisting of a multilayer stack, is seen in figure 4.1.4. This also includes outer shielding layers that reduce crosstalk and provide protection against electromagnetic interference (EMI), ensuring the integrity of the analog signals transmitted between the sensors and FEEs by minimizing noise pickup in the challenging high-rate radiation environment [76]. Inside the stack, aluminium conductors only a few micrometers thick are deposited directly on the polyimide base. This design maintains a very low capacitive load, typically 0.4–0.6 pF/cm, due to the 2 µm Foamtac II spacer, which minimizes the capacitance. This is crucial for reducing electronic noise at the FEE input [56, 77].

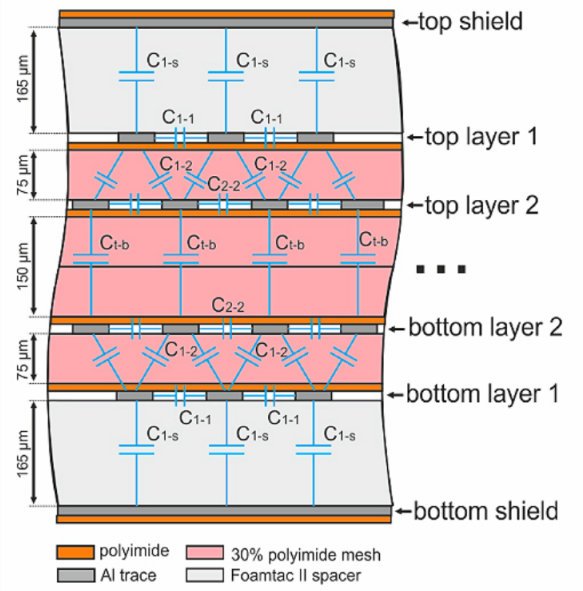

Figure 4.1.4: Ultra thin microcables. (Courtesy of [75])

Altogether, choosing the right materials, multilayer shielding, and low capacitance ensures that even the tiny signals from the sensors are transmitted reliably. This reliability helps the STS maintain its high precision [69].

4.1.3 Front End Boards(FEBs)

The FEBs are a vital part of the STS, acting as the immediate electronic interface between the silicon sensor modules and the downstream DAQ system [52, 73]. Each FEB is a highly integrated board hosting readout ASICs (8 per sensor side, each with 128 channels), designed to process all 2048 output channels from a single sensor [72]. Each FEB receives two voltage levels, 1.8 V and 1.2 V, delivered through four low-noise, low-dropout (LDO) regulators. This ensures clean and stable power for the ASICs and minimizes the noise that could affect the sensitive analog signals [72].

The FEB layout shown in figure 4.1.5 highlights the 16 ASICs mounted on the two boards. The hardware (HW) addresses are numbered on the ASICs. The mapping between ASIC numbers and their respective hardware addresses is summarized in Table 4, allowing for clear identification of the readout channels.

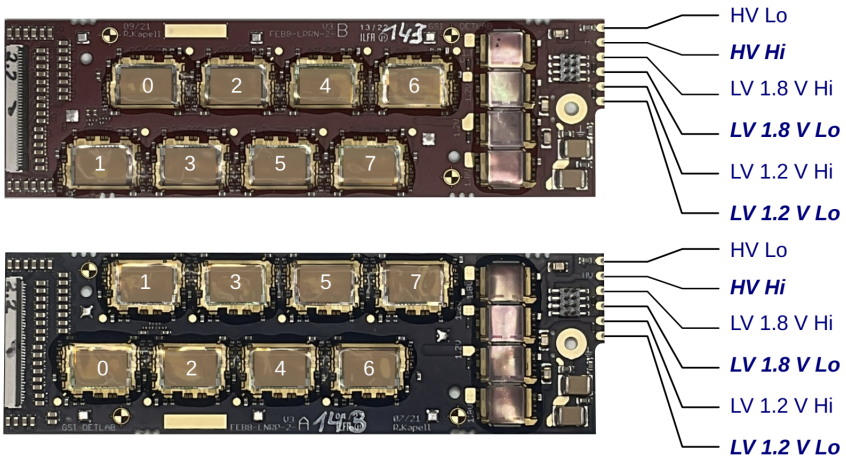

Figure 4.1.5: Front-End Board with SMX ASIC (Courtesy of [72])

ASIC Number	FEB-8A (HW Address)	FEB-8B (HW Address)
0	7	1
1	6	0
2	5	3
3	4	2
4	3	5
5	2	4
6	1	7
7	0	6

Table 4: Mapping of ASIC numbers (0–7) to their corresponding HW addresses for the two FEB types, FEB-8A and FEB-8B.

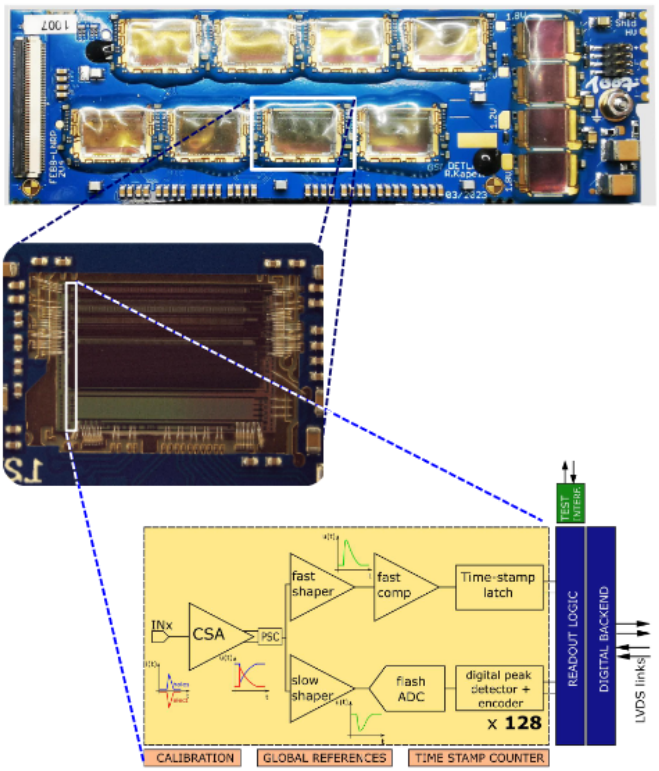

Figure 4.1.6: Front-End Board and Block diagram of the SMX ASIC (Courtesy of [72])

The STS-XYTER ASIC, as shown in figure 4.1.6, was developed at GSI. These ASICs integrate several critical functionalities [56, 75] such as

- **Charge Sensitive Amplifier (CSA):** Converts the small charge from the silicon sensor into a measurable voltage signal. It is optimized for low noise and fast response, ensuring the integrity of the signal is preserved for further processing [**?**].
- **Fast and Slow Shaping Amplifiers:** The two shaping amplifiers work in parallel to optimize both timing and amplitude measurements [75].
  - **Fast Shaper:** Produces a narrow, fast pulse to provide precise timing information. This allows the system to accurately time-stamp events, which is crucial in high rate environments with closely spaced hits.
  - **Slow Shaper:** Produces a broader pulse that takes longer to reach its maximum (longer peaking time), improving the signal-to-noise ratio and allowing more accurate measurement of the particle's deposited charge.

- **Fast Comparator:** Monitors the fast-shaped signal and triggers when it exceeds a set threshold. This initiates timing and data processing, ensuring relevant events are correctly captured [75].
- **Flash Analog-to-Digital Converter (Flash ADC):** Digitizes the shaped analog signals directly on the ASIC. This supports high speed readout while minimizing signal distortion, enabling reliable data acquisition [75].
- **Time Stamp Latch:** Records the precise time when a signal crosses the threshold. This digital register holds the timing information for each hit, which is essential for accurate event reconstruction [75].
- **Digital Peak Detector and Encoder:** Captures the peak amplitude of the slow-shaped pulse and encodes it for downstream transmission. This ensures that amplitude information is accurately formatted for further analysis [75].

A distinctive feature of the FEBs is their support for a triggerless, free-streaming readout mode, enabling continuous data acquisition without hardware triggers crucial for capturing rare or closely spaced events without loss [56, 75]. The ASICs on the FEBs monitor functions including temperature, voltage, and current, to ensure stable operation and early detection of potential issues [56]. Thermal management is provided by mounting the FEBs on a cooling block, ensuring reliable performance during sustained operation [61].

4.1.4 Module Testing

To ensure that each STS module functions accurately and meets quality standards, a comprehensive testing procedure is carried out. This process helps identify potential issues early on and determine appropriate solutions, ensuring that only fully functional modules proceed to the next stage of testing. Module testing is performed in three successive stages [56, 77]:

1. Electrical characterization of the silicon sensor via current-voltage.
2. Functional verification and calibration, including noise evaluation.
3. Assessment of thermal stress performance through repeated thermal cycling.

Current-Voltage (IV) Measurements: IV testing plays a crucial role in evaluating a silicon sensor, helping detect defects before modules are integrated into larger assemblies such as ladders or half-units. This test enables the identification of potential defects at an early stage [77]. Sensors are biased according to their assigned grade - Type A up to 500 V, Type B up to 350 V, Type C up to 250 V, and Type D up to 200 V. During an IV scan, a high voltage is gradually applied across the sensor, as seen in figure 4.1.7, and the resulting leakage current is measured. At a certain voltage, known as the breakdown voltage, the current rises sharply, marking the maximum safe operating voltage.

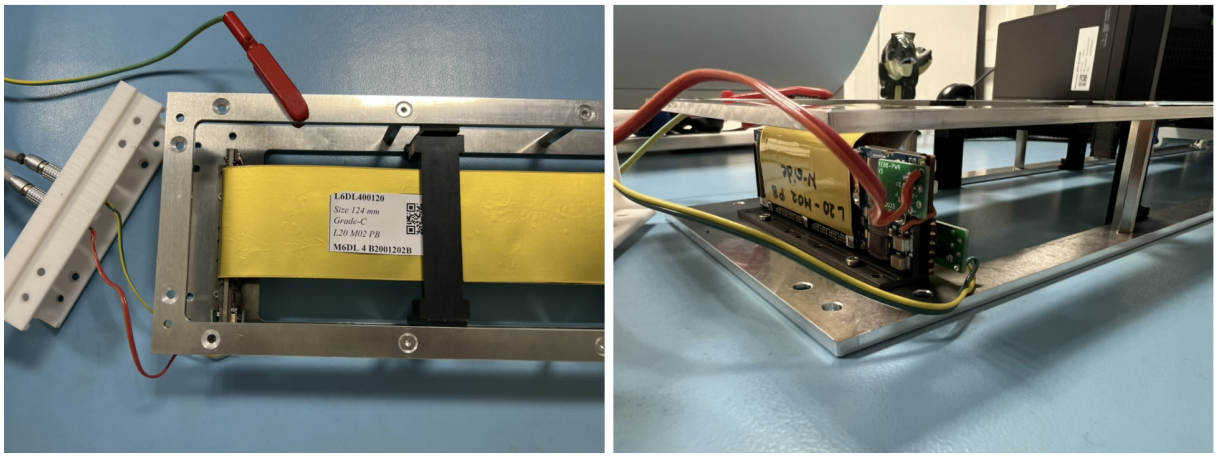

Figure 4.1.7: Ground connection clipped to the carrier, and High voltage is supplied through the FEBs: n-side(left FEB) and p-side(right FEB) connected to the sensors via microcables.

The shape of the IV curves provides a good indication of sensor quality. Only modules with stable electrical behavior and low leakage currents proceed to further functional testing. As shown in plot 4.1.8, the IV curve of module M3DL1T0001120A2 exhibits stable behavior and proceeds to the next stage of testing. Modules exhibiting unusual current

increases or early/slow breakdowns undergo additional treatments, such as cleaning the sensor edges and storing the modules in a controlled humidity environment, to restore functionality [71].

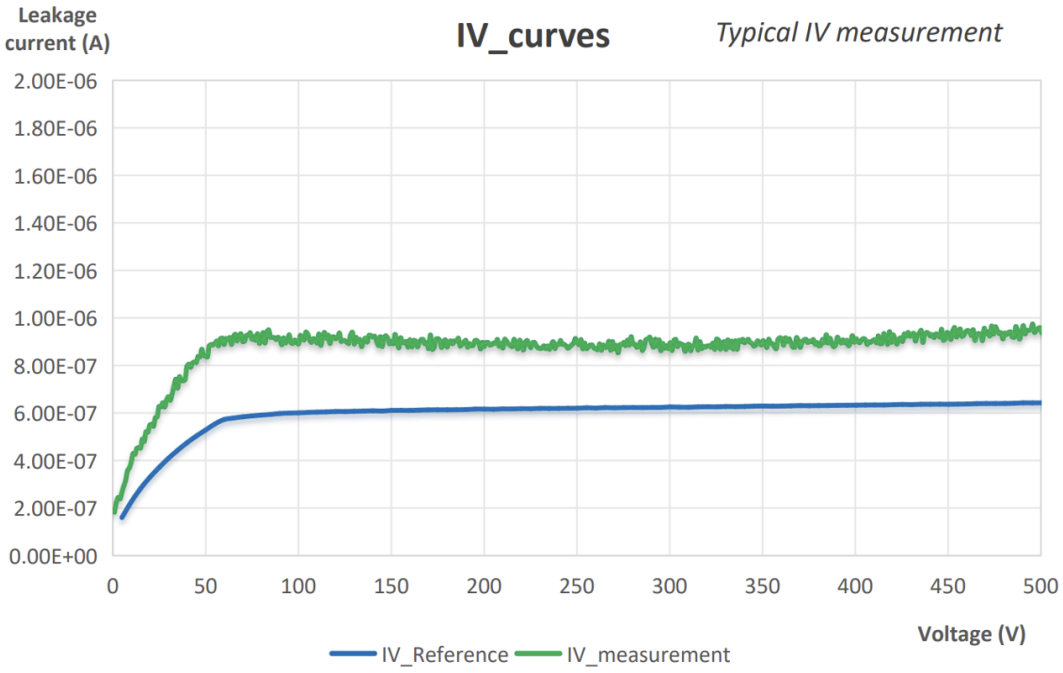

Figure 4.1.8: Current–Voltage (IV) curve of module M3DL1T0001120A2 (Grade A), showing stable behavior.

Functional characterization of the module: After electrical verification, the modules undergo functional testing. For this purpose, each module is connected to a GBTx-Emulator (EMU) board, which acts as the interface between the readout electronics (FEBs) and the DAQ system. The EMU handles configuration, communication, and data collection from all ASICs [56, 77]. The connection between the FEBs and the EMU is established through readout cables. The setup also includes a cooling block with circulating water to stabilize the module temperature, and a panel providing low-voltage (LV) and high-voltage (HV) supplies, as shown in figure 4.1.9. Once powered on, the LV supply is activated to monitor FEB power consumption, which typically ranges from 1.1 to 3.0 A. The HV is then gradually applied symmetrically to both sides of the FEB up to 75 V, corresponding to an operational voltage of 150 V across the module [56].

Figure 4.1.9: Three setups for module functional tests

The module is then run through calibration steps, beginning with data link initialization and synchronization to establish reliable uplink and downlink communication with each ASIC. Once communication is verified, register configuration parameters are set, and multiple write/readback actions are performed. Following the configuration, key parameters such as power consumption, temperature, and VDDM (a potential used to evaluate the analog response) are recorded and verified [56].

Next, channel-to-channel threshold corrections are determined by injecting fixed charge pulses using the ASIC's internal pulse generator. The resulting discriminator responses are analyzed to extract ADC thresholds and gain, which characterize the linearity and uniformity of the ADC response [56].

Trim DAC (Digital-to-Analog Converter) parameters are stored in calibration files for each ASIC. Fixed charge pulses are sent again to each channel, while recording the response of all discriminators through S-curve scans to confirm uniform response across channels [77]. The noise performance is an important part of module testing, which estimates the module's noise and compares it with analytical expectations. This step allows identification of noisy or non-functional channels, ensuring that only properly functioning modules proceed further [56, 77].

Noise performance of the modules

The Noise is measured using the Equivalent Noise Charge (ENC), derived from S-curve scans of each channel. During these tests, the discriminator response is recorded as a function of injected charge; the slope of the S-curve provides the noise level, while the mean corresponds to the channel threshold [77]. The total noise includes contributions from the ASIC's intrinsic noise, the sensor capacitance, and the microcable capacitance.

As seen in the plot 4.1.10, the green dashed line represents the noise contribution from the sensor and microcables, while the intrinsic ASICs noise is approximately 350e ENC, is indicated by the yellow dashed line [56, 72, 77]. The total ENC can be broken down according to its sources: L_{sensor} and L_{cable} denote the lengths of the sensor and microcable, respectively, and the factor 25 e/pF characterizes the dependence of ASIC noise on input

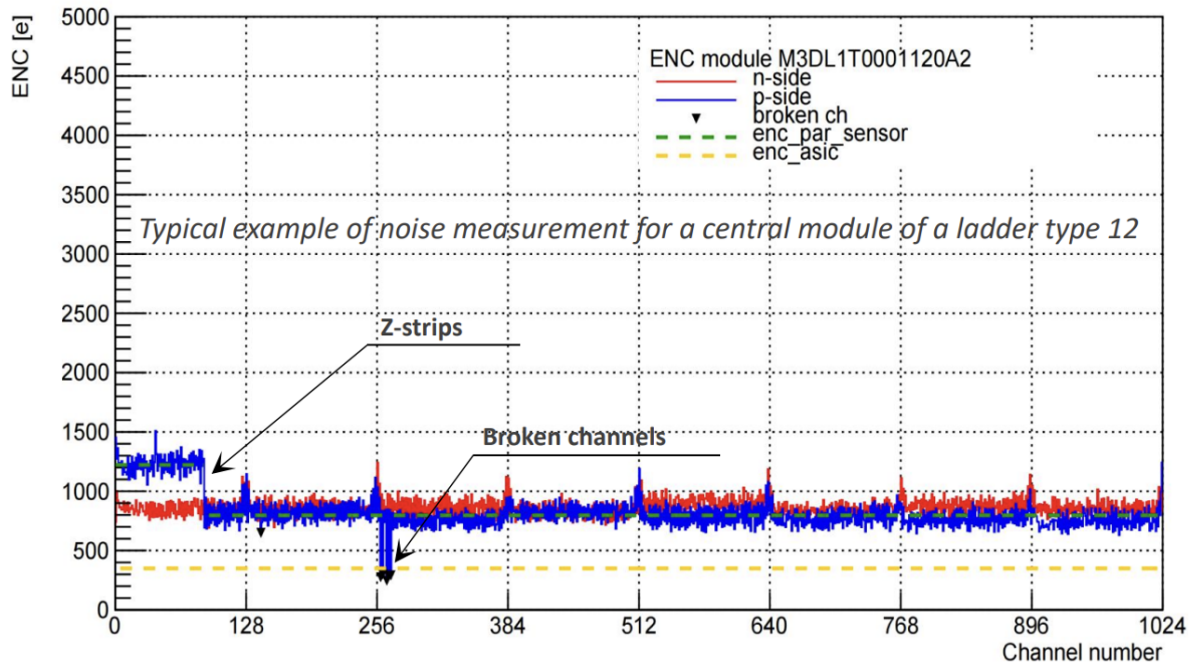

Figure 4.1.10: Noise performance (ENC) analysis across all channels of module M3DL1T0001120A2

capacitance. Each sensor strip has a capacitance of 1.02 pF/cm, and the effective capacitance per unit length of the microcable, including contributions from neighboring traces and coupling to the shielding layer, is 0.38 pF/cm [77]. The resulting ENC can be expressed as:

$$\text{ENC [e]} = \left[\underbrace{L_{\text{sensor}} \cdot 1.02 \text{ pF/cm}}_{\text{Sensor}} + \underbrace{L_{\text{cable}} \cdot 0.38 \text{ pF/cm}}_{\text{Microcable}} \right] \cdot 25 \text{ e/pF} + \underbrace{350 \text{ e}}_{\text{ASIC}} \tag{5}$$

By comparing the measured noise with analytical expectations, noisy modules and non-functional channels can be identified. This process ensures that only modules exhibiting stable, low-noise behavior advance to the next stage of testing. For each module, a detailed report is generated, summarizing noise patterns, signal response, threshold uniformity, which is critical for reliable performance in the final detector assembly [56, 72].

Thermal stress test

After functional verification, modules undergo a thermal burn-in test to ensure long-term stability and to identify early failures. The modules are exposed to repeated thermal cycles, typically down to −20 °C [72, 77]. This setup creates the expected operating conditions of the STS experiment. Additionally, it introduces a safety margin beyond the usual temperature, allowing potential weaknesses, such as increase in leakage currents, mechanical stress, or poor performance under temperature variations, to be revealed.

The burn-in test depends on the principle of thermal cycling that accelerates stress in semiconductor devices. Temperature changes affect leakage currents, charge carrier mobility, and bias stability in both sensors and ASICs. Cooling below zero also stresses mechanical interfaces and bonding connections due to differences in thermal expansion between materials. Modules are placed in a dedicated test chamber, as shown in figure 4.1.11, equipped with cooling plates connected to a chiller for precise temperature control. A constant flow of nitrogen gas maintains low humidity, preventing condensation on sensitive electronics [77]. Throughout each cycle, the sensors in the module are biased at their operational voltage, while the readout and FEBs remain connected to monitor

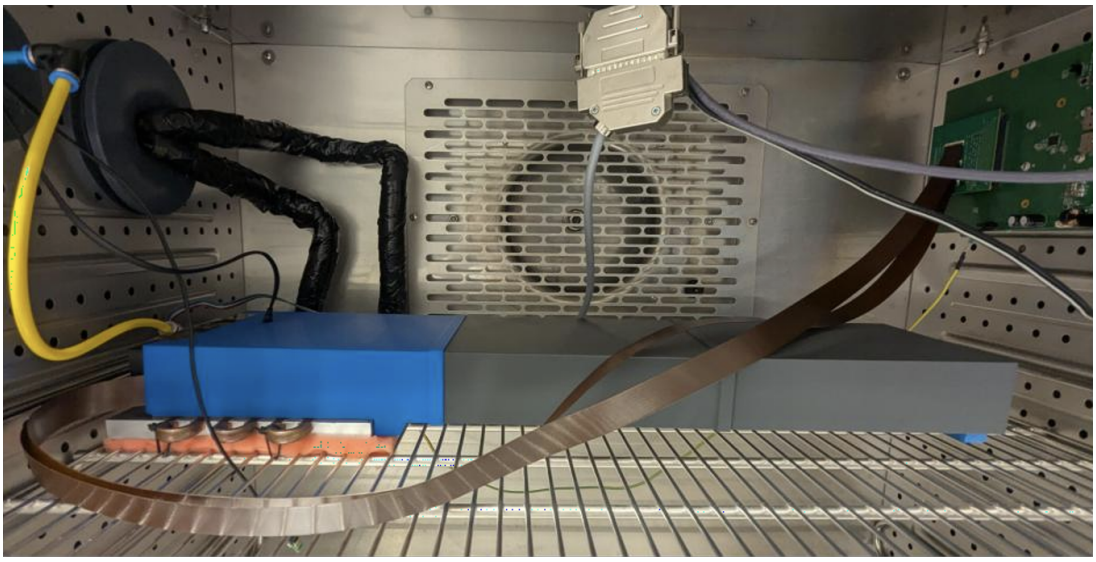

Figure 4.1.11: Thermal test setup for modules with integrated cooling plate and readout connections.

stability under thermal stress [72]. Temperature is increased in steps and is stabilized at each level to ensure equilibrium. Parameters such as communication with ASICs, sensor leakage current, and ENC are monitored throughout the cycles to detect any degradation. A burn-in test is considered successful if communication with all ASICs remains stable, no systematic degradation is observed, and all planned thermal cycles are completed. After this test, the modules are confirmed to be thermally stable and ready for integration into the STS ladders, representing the final step before complete ladder assembly [77].

4.2 STS Ladder Integration

The STS ladders form the primary mechanical support structure for the detector modules. Figure 4.2.1 shows a general view of a detector ladder. The concept of using CF structures was initially developed for the barrel geometry of the Inner Tracking System (ITS) in the ALICE experiment. To fit the experimental geometry and operational needs the STS uses similar design with minor variations to suit the experimental geometry and operational requirements [78]. The CF framework provides enough strength and rigidity while using little material, which helps achieve precise tracking and reduces multiple scattering [80].

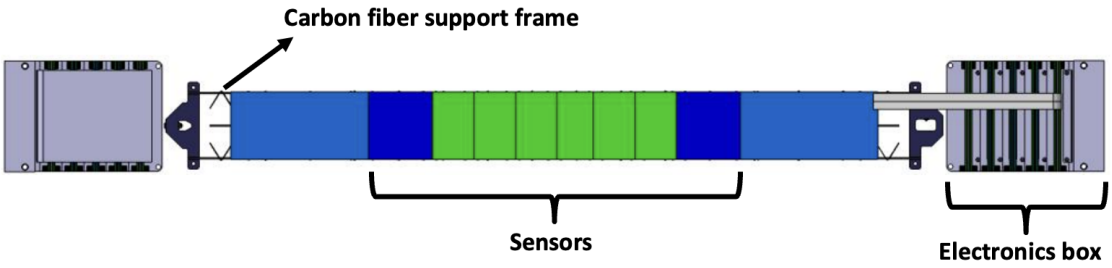

Figure 4.2.1: Computer-Aided Design (CAD) representation of a standard detector ladder with sensors and electronics box mounted at each end (Courtesy of [79]).

Each ladder supports multiple detector modules, that consists of silicon sensors, micro-cables, and shielding layers. The modules must be precisely aligned along the ladder to maintain the spatial resolution necessary for accurate reconstruction of charged particle trajectories [80]. A typical ladder can accommodate 2–10 modules; the weight and mechanical stresses require careful design to prevent bending [80, 81]. Excessive deformation could introduce mis-alignments that compromise tracking accuracy and introduce systematic errors. To eliminate this issue, ladders are fabricated with carefully controlled stiffness and mechanical tolerances, ensuring they maintain their shape under load and throughout the experiment's lifetime [81]. Special attention is given to central ladders positioned close to the beamline, as seen in figure 4.2.2. These ladders include cutouts and semi-rings that are stiff, allowing the beam to pass through without compromising rigidity. Structural integrity and stiffness of both standard and central ladders were validated through a series of prototype tests, which confirmed that the selected materials and design are adequate for stable operation under experimental conditions [78, 81]. A visual overview of the different ladder types and arrangements is shown in figure 4.2.3. This CAD representation highlights the variety of ladder configurations used within the STS, illustrating how modules are positioned along the frames while maintaining precise alignment, mechanical stability, and minimal material contribution [81].

Overall, STS ladders provide a lightweight, rigid, and precisely aligned backbone that integrates multiple detector modules while ensuring stable performance and minimal contribution to the overall material budget [78, 80].

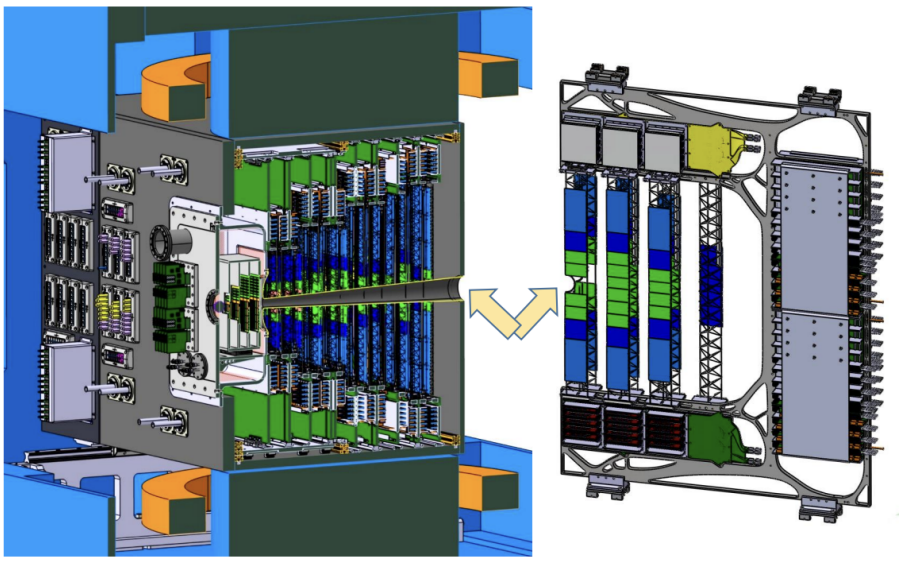

Figure 4.2.2: CAD representation of a central ladder frame.((Courtesy of O. Vasylyev (GSI, Darmstadt))

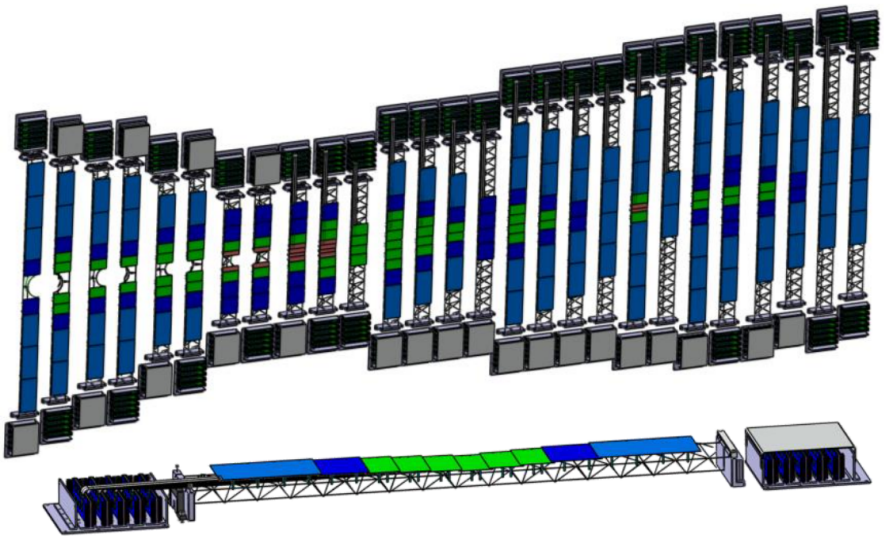

Figure 4.2.3: CAD representation of multiple ladder configurations. (Courtesy of O. Vasylyev (GSI, Darmstadt))

Electronics box (FEB Integration) The readout electronics of each module in the ladder are housed in dedicated electronics boxes (hereafter referred to as FEB box) located at the ends of the ladder [52]. These assemblies consist of FEBs associated with each module. A single half-ladder typically requires ten FEBs to ensure complete readout of all modules, as seen in figure 4.2.4. The FEBs are arranged to minimize electrical interference and enable efficient cooling, while the readout channels maintain stable operation and remain accessible for testing and maintenance [83, 84].

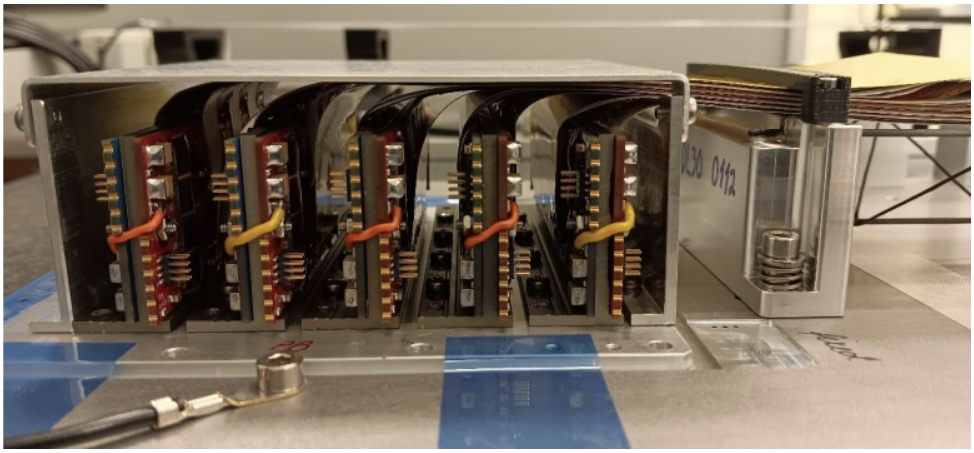

Figure 4.2.4: Arrangement of FEBs arranged together forming a complete FEB box for a half-ladder readout.

A CAD image of a fully assembled ladder, with FEB boxes positioned on both ends, forms a complete mechanical and electronic unit ready for integration into the STS (See figure 4.2.1). The design of the FEB box also accounts for thermal management [52]. FEBs generate heat during operation, and proper spacing, thermal conduction paths, and potential integration of cooling interfaces ensure that operating temperatures remain within safe limits [61]. This prevents performance degradation, maintains low-noise operation, and ensures long-term stability. By combining the mechanical ladder structure with the integrated FEB box, each ladder becomes a self-contained, stable subsystem. This integration guarantees precise alignment, stable readout, and efficient thermal management, forming the backbone of the STS and enabling reliable high-resolution particle tracking in the CBM experiment [80, 84].

4.2.1 Ladder testing

After individual modules have been verified, the next After individual modules have been verified, the next step is ladder testing. A ladder is a structure that holds multiple modules together, typically up to ten, and serves as a higher-level assembly in the STS detector [85, 86]. While module testing focuses on the performance of a single module, ladder testing, as seen in figure 4.2.5, evaluates the modules collectively to ensure that they not only function individually but also work reliably as a coherent unit [85, 87]. Ladder testing is essential because interactions between modules, such as shared readout electronics and signal cross-talk, can introduce issues that are not visible in single module tests. It verifies system level integration, confirming that multiple modules operate together as intended. In addition, ladder testing provides a more realistic assessment of the thermal and electrical behavior under conditions closer to actual detector operation [85]. By identifying potential issues early at the ladder level, the overall reliability and performance of the STS detector can be maintained [86].

The procedure at the ladder level follows the same principles as module testing, including electrical characterization (IV measurements), functional verification, calibration, and noise evaluation [87]. However, the scale and complexity of testing increase because multiple modules are monitored simultaneously, making cable management, readout, and power distribution more critical.

Electrical Characterization (IV Measurements): As with module testing, the first step in ladder testing is electrical characterization using IV measurements. However, at the ladder level, this is performed simultaneously for all modules. Each sensor is biased according to its assigned grade, and the resulting IV curves are analyzed for abnormal behavior such as early breakdown or unusually high leakage currents. Modules showing issues can be temporarily disconnected, treated individually, and then reintegrated. This ensures that the fully assembled ladder exhibits stable electrical behavior and low leakage currents, extending the verification from single-module performance to multi-module operation [85, 87].

Functional Verification and Calibration: Ladder functional testing builds on the procedures established during module testing, but evaluates multiple modules at once. The ladder is connected to the GBTx-EMU board via readout cables, and a cooling system maintains uniform temperatures across all modules. Low-voltage currents are monitored for each FEB, and high voltage is gradually applied to fully deplete all sensors. Calibration steps data link initialization, ASIC synchronization, registers configuration, and monitoring of key parameters such as power, temperature, and VDDM are performed for every module. Calibration pulses are sent to all channels of each ASIC to determine threshold corrections, ADC gains, and uniformity across the ladder. S-curve scans and equivalent noise charge (ENC) measurements are used to identify noisy or faulty channels [56]. Faulty modules may be treated individually and reintegrated, maintaining the overall integrity of the ladder [85].

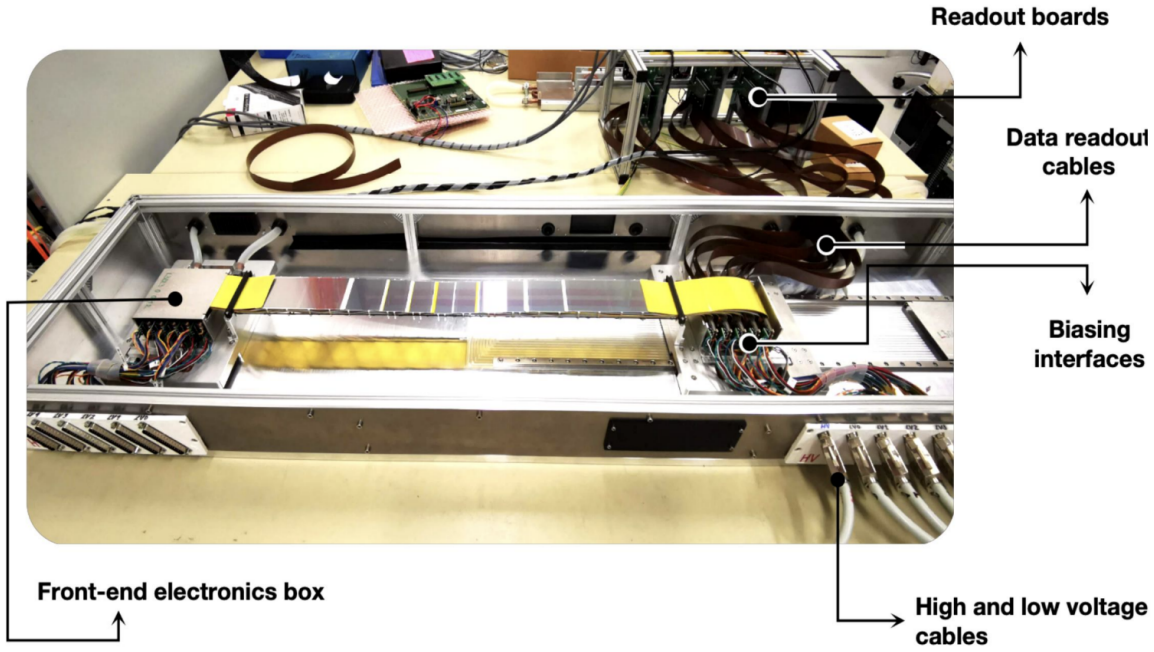

Figure 4.2.5: Ladder functional test setup showing connections for cooling and readout. (Courtesy of [87])

Finally, results from all modules are compiled into a comprehensive report summarizing noise performance, signal response, threshold uniformity, and other critical parameters [85]. While module testing ensures the functionality of individual modules, ladder testing confirms that multiple modules operate coherently as a single unit a key requirement for reliable performance in higher level detector assemblies [86].

5 Half-Unit(HU) Assembly and Integration

5.1 Structural Overview of the Half-Unit

In the STS, each unit provides the mechanical framework for arranging sensors on ladders together with readout electronics. A unit consists of two half-units, positioned symmetrically on the left and right of the vertical axis enclosing the beam pipe at the center. Each half-unit is equipped with dedicated low-voltage, sensor bias voltage (high voltage), optical fibers, and cooling, enabling independent installation and operation [52].

The HU is the primary structural unit of the STS, serving as both the mechanical backbone and the functional core where ladders and readout electronics are integrated. The aluminum C-frame is mechanically symmetrical [88]. The C-frame is designed to hold several ladders along with peripheral components such as the Readout Boards (ROBs), Power Boards (POBs), and cooling blocks [89]. These components are placed outside the detector acceptance region to keep the material budget low, while still providing efficient readout and good thermal control [88].

Altogether, the STS comprises 20 half-units distributed across eight tracking stations. The outermost upstream and downstream stations are covered by a single half-unit, while the remaining stations each consist of paired upstream (STSu) and downstream (STSd) half-units, forming continuous sensor surfaces without gaps [90]. The stations are generally spaced 105 mm apart, except between stations 3 and 4, where an additional 5 mm gap is present because station 3 is split into STSu and STSd [90]. Each half-unit is labeled according to its position as UL (Upper Left), UR (Upper Right), DL (Down Left), or DR (Down Right), which helps identify its location within a unit and along the beamline for assembly and cabling purposes. At the upstream end, an additional single half-unit completes the coverage. This configuration, with eight half-units upstream and 12 downstream, ensures full tracking coverage while accounting for the bending of the

particle trajectories in the dipole magnet as seen in figure 5.1.1a. Collectively, these 20 half-units constitute the eight stations forming continuous tracking surfaces [89, 90]. Figure 5.1.1b is the CAD image of Unit 3, Downleft (DL) half-unit.

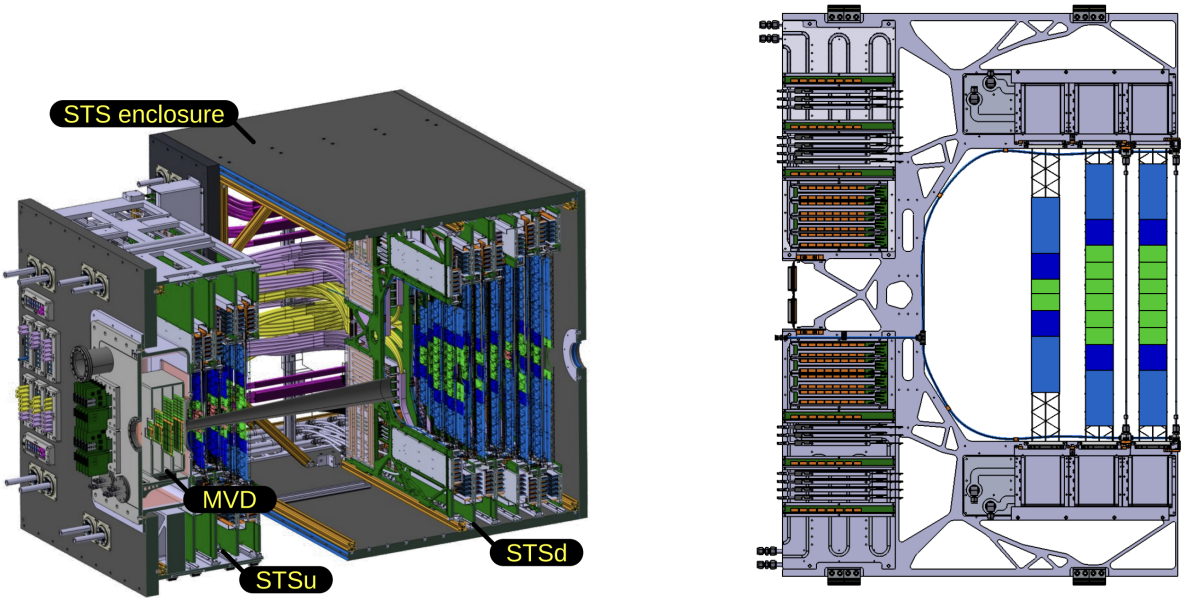

Figure 5.1.1: (a) CAD illustration of the STS enclosure, showing the relative positions of the MVD, STSu, and STSd subdetectors (Courtesy of [72, 79]). (b) CAD illustration of the Structural view of CBM STS Half-Unit 3 DL, displaying the ladders, FEB boxes, and peripheral components (Courtesy of O. Vasylyev (GSI, Darmstadt))

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To test the design, integration, and assembly procedures, mockup studies were carried out. Non-functional ladders and full-scale prototype models of the POBs, ROBs, and FEB boxes were made for this purpose. These mockups helped check the mechanical fit, alignment, accessibility of components, and the overall assembly workflow before constructing the final detector stations. The tests were performed on the Unit 3 DL half-unit C-frame. The following sections provide detailed descriptions of the assembly procedures, integration methods, and cabling sequence for the HU.

5.2 Building Blocks of HU

The Half-Unit (HU) integrates multiple mechanical, electronic, and thermal components to form a complete functional unit. The following subsections provide an overview of these building blocks and their respective roles within the HU.

5.2.1 C-Frame: Integration and Alignment Framework

The C-frame is a key structural component, providing a strong foundation for integrating ladders and associated electronics [89]. Its design emphasizes mechanical stability, precise alignment, and minimal material use to ensure optimal detector performance.

The C-frame made from a high-strength aluminum alloy offers a good balance between rigidity and low mass [89, 91]. Its C-shaped cross-section, as seen in figure 5.2.1, provides easy accessibility and minimal interference during assembly. Additionally, the C-frame provides space for cooling systems without interfering with the ladders. Its hardness ensures that mechanical vibrations or small temperature changes do not affect alignment, which is essential for accurate measurements and reliable detector performance over time [91, 92].

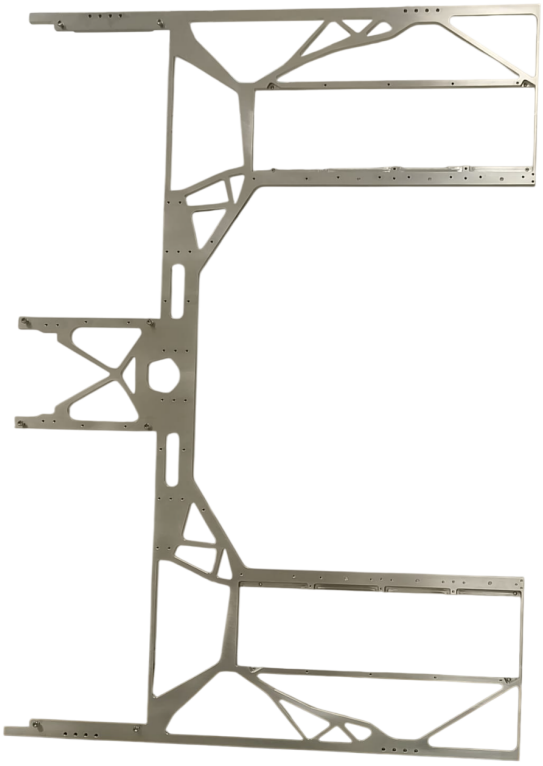

Figure 5.2.1: Photograph of the C-frame of Unit-03DL

Cooling Blocks for FEB Boxes and Peripheral Components

The cooling blocks are essential for thermal management, as they dissipate the significant heat generated by the readout and powering electronics. These are mounted on the C-frame and are cooled via a liquid cooling system using water-glycol as the coolant [84, 93, 94].

The FEB cooling blocks: includes an aluminum plate, as shown in figure 5.2.2. Its surface area is maximized to help dissipate heat efficiently [93, 94]. Coolant flows through the plate, taking away heat from the FEBs. Thanks to its low viscosity and high thermal stability at low temperatures, this coolant works well for the application [93, 94].

Thermal Interface Materials (TIMs) are placed between the FEBs and the cooling plate to improve thermal conductivity and ensure efficient heat transfer while remaining suitable with the detector's operating environment [94, 95]. The system is designed to maintain the FEBs at a stable operating temperature, preventing thermal runaway and ensuring that the electronics function consistently over time [93, 94]. By enhancing the thermal contact between the FEBs and the cooling plate, the TIMs help achieve uniform temperature distribution across the modules, which is essential for consistent performance and stable operation over time.

Figure 5.2.2: Photograph of the FEB cooling plate of the C-frame of Unit-03DL

Peripheral Cooling Blocks: Manages the thermal load of other components, including those responsible for power distribution and data transfer. As shown in figure 5.2.3, these blocks contain internal cooling channels through which the coolant flows, effectively removing heat from the components they are designed to cool [86,98]. Similar to the FEB cooling blocks, these peripheral cooling blocks are constructed from aluminum alloys, chosen for their thermal conductivity and lightweight properties. The cooling blocks are mounted outside the detector's acceptance region [84].

The combined cooling solutions for the FEBs and peripheral components are integrated into a comprehensive thermal management system, ensuring the CBM STS operates within its thermal specifications [84].

Figure 5.2.3: Photograph of the peripheral cooling plate of the C-frame of Unit-03DL

Peripheral Components

Peripheral components are essential for signal readout and power management, including ROBs, RPOBs, and FPOBs. They are mechanically mounted onto the C-frame and placed on dedicated cooling blocks to ensure stable and reliable operation. Each peripheral component is described in detail in the following sections, including its function:

- **The STS-ROB (Silicon Tracking System Read-Out Board):** as seen in figure 5.2.4, serves as the central communication hub between the FEE modules and the Field programmable gate array (FPGA)-based backend. Its primary functions include sending control commands via the downlink path to the front-end modules and distributing clock signals both to these modules and to the slave GigaBit transceiver (GBTx) chips on the board. Detector data flows in the opposite direction through the uplinks, where it is forwarded to the backend for further processing. The core of the STS-ROB is a GBTx chip operating in master configuration, supported by additional GBTx devices acting as slaves, as well as a Slow Control Adapter (GBT-SCA)chip that provides control and monitoring capabilities [96]. An essential component of the board is its optical modules: Versatile Transceiver (VTRx)

and Versatile Twin Transmitter (VTTx). The VTRx functions as a bidirectional transceiver, allowing the reception of commands and transmission of status data.

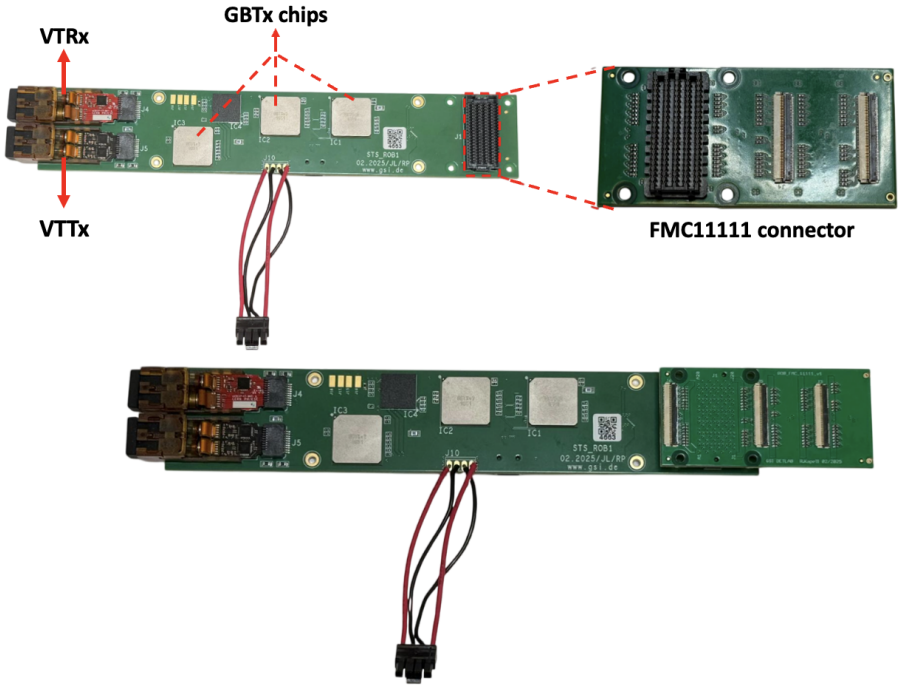

Figure 5.2.4: STS Readout Board (STS-ROB) with FMC11111 connector and FMC connector attached.

The VTTx modules are unidirectional transmitters that send data received from the slave GBTx devices via the uplink [97]. These modules convert electrical signals into optical ones, enabling fast and reliable data transfer to the backend. This allows the STS-ROB to maintain long distance communication with high signal integrity [91]. The ROB interfaces with the FEEs through an FMC connector, which serves as the interface between the FEEs and the STS readout system. Signals from the FEEs are routed via data cables to the FMC, following a defined mapping [97]. The FMC connector is plugged into the STS-ROB (fig 5.2.4), where the signals pass through three GBTx ASICs before reaching the optical modules. These modules convert the electrical signals into optical signals, which are transmitted via optical fibers to the backend electronics and finally processed by the FPGA. This ensures high-speed, reliable data transfer from the front-end modules to the backend system [97].

- **The RPoB (Readout-Powering Board):** is a specialized, radiation tolerant power supply module designed to provide the required operating voltages for the STS ROBs. Its primary function is to ensure stable and efficient power distribution in a high radiation environment. The RPoB is based on FEAST DC-DC converters, developed at CERN [98]. These converters have an input voltage in the range of 6 V to 12 V and generate two stable low voltage outputs: 1.5 V and 2.5 V as seen in the figure 5.2.5 [93]. The converters are designed for high efficiency, low noise, and radiation tolerance, which are essential for maintaining reliable operation. The 1.5 V output powers the GBTx ASICs, which are critical components of the high speed data read-out chain.

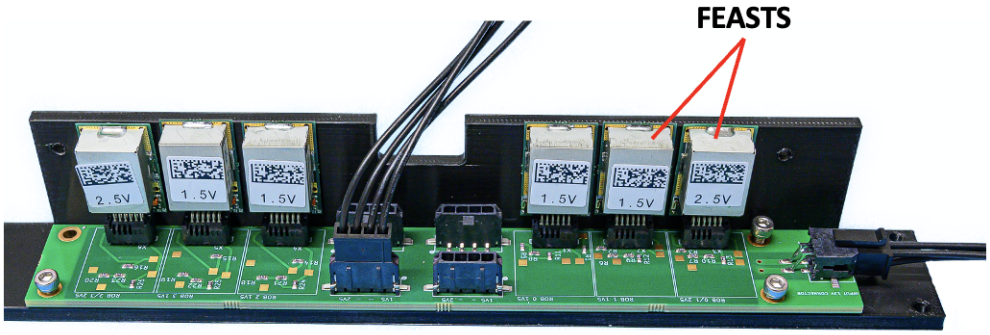

Figure 5.2.5: RPoB PCB with FEAST DC–DC converters (Courtesy of [99]).

The 2.5 V output powers the optical transceiver modules, ensuring stable optical data transfer between the STS and the DAQ system. A single RPoB can supply power to up to four STS-ROBs, making it a efficient solution. Within the C-frame, it functions as a radiation tolerant power interface, ensuring reliable and stable operating conditions for the readout system [99].

- **The FPoB (Front-end Powering Board):** The powering of the STS FEE relies on the FPoB, which is designed to provide regulated voltages to the FEBs. Each FPoB is capable of supplying four modules simultaneously. The FPoB is built on a 6 layer PCB with 210 , μm copper thickness [100].

Thick copper layers were chosen to minimize voltage drops, and the stack up is optimized for electromagnetic compatibility (EMC) [100]. The board layout, shown in figure 5.2.6, features the 8 input voltage channels of the PoB and is split between the FEASTMP DC–DC converters, arranged in two rows of eight, producing voltages of 2.4 V and 3.0 V [99]. These outputs are further stabilized by low-dropout regulators (LDOs) on the FEBs, producing the final ASIC operating voltages of 1.2 V and 1.8 V. Four output connectors on the right-hand side connect one detector module each (4 modules × 2 FEBs × 2 FEAST converters per FEB, totaling 16 FEAST outputs) [99]. This provides stable power delivery over long cables and minimizes voltage drops.

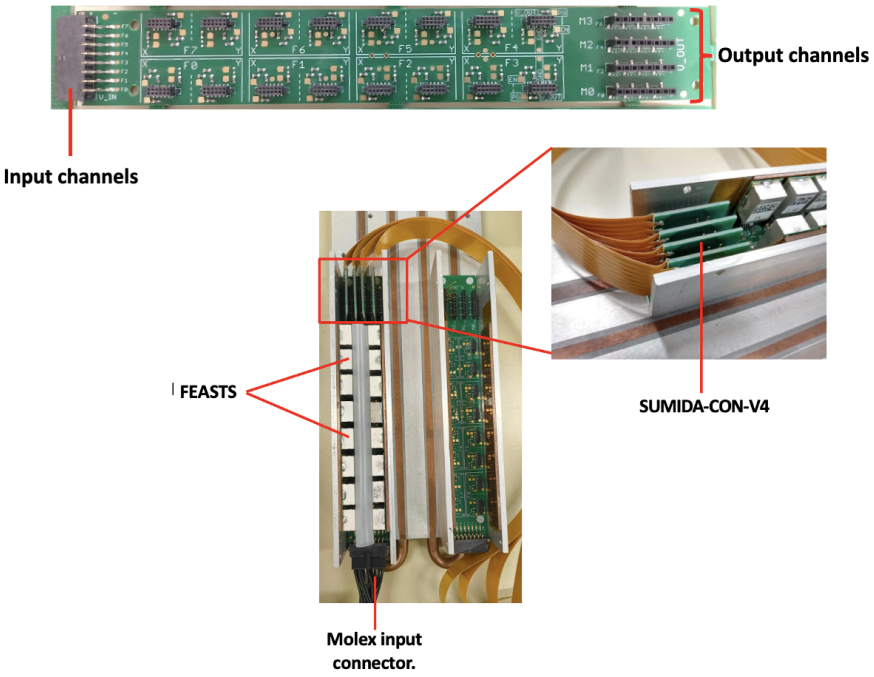

Figure 5.2.6: FPoB PCB with input/output connectors and FEAST DC–DC converters.

The typical current per input channel is approximately 1.5 A. The FEAST outputs are interfaced through SMD Samtec sockets, while the Sumida PANTA FIX power cables [101] from the modules are soldered at one end to the FEBs and the other end to the SUMIDA-CON-V4 connector, which are plugged into the sockets on the board.

This arrangement ensures a secure, low-resistance connection for reliable current delivery. A low voltage, slightly below 12 V, is supplied to the FPoB via a Molex MicroFit input connector.

This combination of FEAST converters, LDOs, cabling, and carefully designed PCB layers provides stable, low-noise, and radiation-tolerant power to the FEBs, ensuring reliable operation of the STS FEE.

- **Ladders:** The design and characteristics of the ladders have already been explained in detail in Section 4.2. Here, the ladders are mounted on the half-unit, and the power and data cables are connected, as described in the following section.

6 HU Integration and Assembly protocol

Integrating the HU is an essential step in building the detector, as it affects both the mechanical stability and the long-term performance of the system. The HU serves as the main structural unit, that holds the ladders, power distribution boards, readout electronics, and cooling plates. Each of these components has specific requirements for alignment, tolerances, and electrical connections. Failure to meet these conditions during assembly can lead to misalignment or excess mechanical stress, which may compromise the efficiency and reliability of the detector.

To address these risks, a standardized and clearly defined assembly protocol was developed within the scope of this work. This reduces the likelihood of errors in alignment, mounting, and cable routing. A well-defined sequence of mounting, positioning, and verification steps was followed. This approach helped maintain assembly quality and made it easier to repeat the process on a larger scale. Before assembling the real components, the sequence was tested and improved using full-scale 3D printed mockups of the HU components [102]. These mockups helped to examine mechanical interfaces, check clearances, and adjust handling procedures safely, without risking any damage to sensitive hardware. These tests confirmed that the assembly steps from installing ladders to positioning power and readout boards could be carried out efficiently under realistic conditions. The insights gained from these mockup trials were used to establish the final protocol, which serves as a guideline for the assembly with real components. The complete procedure with actual hardware is still to be carried out. The Integration and Assembly Protocol, detailing preparation, mounting, and verification, is outlined below.

6.1 Mounting and the integration protocol

The integration process begins with positioning the C-frame mounting frame (CFMF), which serves as the primary mechanical support. The frame is adjusted to match the

CAD-specified height for the respective C-frame variant. These adjustments are carried out manually with a measuring tape and verified at multiple points to minimize deviations. For secure mounting, sliding wagons and 3D-printed rail adapters are secured together as seen in figure 6.1.1, and then are mounted along the upper and lower edges of the frame and initially fastened loosely with screws.

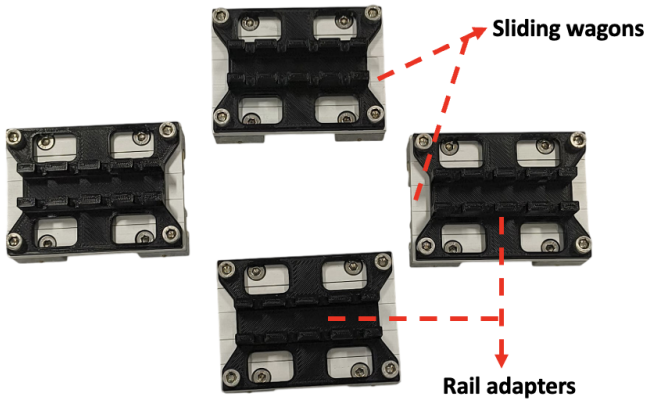

Figure 6.1.1: The sliding wagons with attached 3D-printed rail adapters.

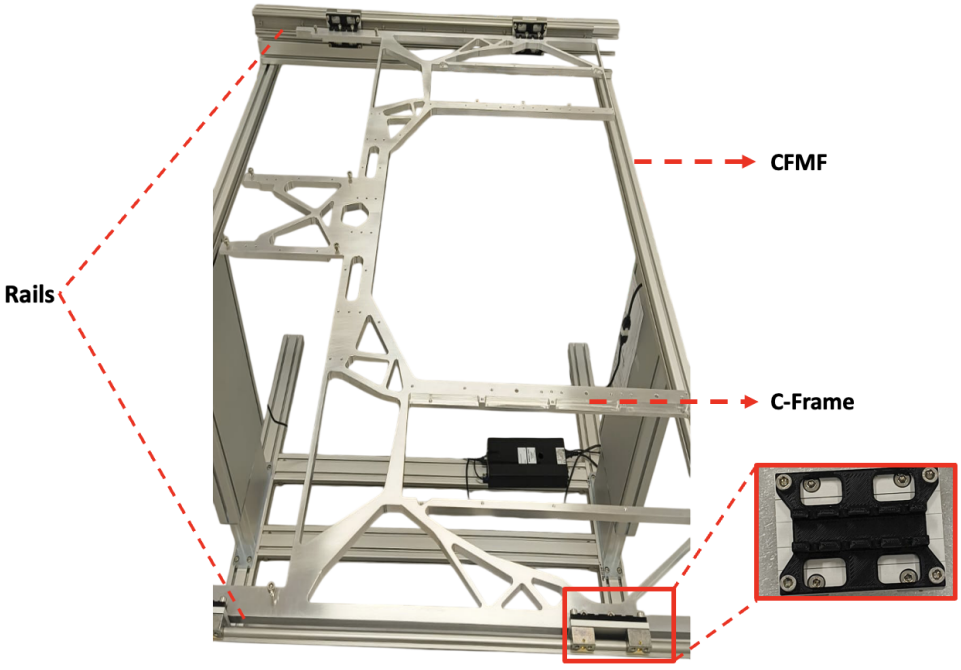

Figure 6.1.2: C-frame guided along rails on sliding wagons.

The C-frame is then carefully guided along the rails using the sliding wagons to ensure smooth insertion, as seen in figure 6.1.2. If necessary, minor adjustments are made to achieve precise alignment. This process may be repeated as needed to ensure that the C-frame is stable and properly aligned at all mounting points.

The mounting process is completed by performing a final verification of the frame's height, orientation, and alignment. By carefully following a stepwise procedure, this ensures precise and safe assembly, while facilitating the efficient installation of ladders and FEEs without introducing mechanical stress or misalignment. Once the C-frame is stable and the adapters are tightened, it is moved horizontally.

6.1.1 Installation of Thermal and Peripheral Components

After the mechanical setup, the thermal management and peripheral systems are mounted onto the HU. The detector electronics are very sensitive to temperature fluctuations, so dedicated measures will be implemented to dissipate heat during continuous operation and prevent failures caused by overheating.

The thermal cooling blocks are mounted first on the HU, followed by the peripheral components, which are represented using 3D-printed models [100]. These models allow verification, including checking that the cooling plates specified mounting holes align correctly, ensuring that components fit properly, and that no size or dimensional issues arise when mounting the real parts. This step is necessary to detect any misalignments at an early stage, to observe how the handling works in practice, and to evaluate how easily other parts can be mounted around them during assembly.

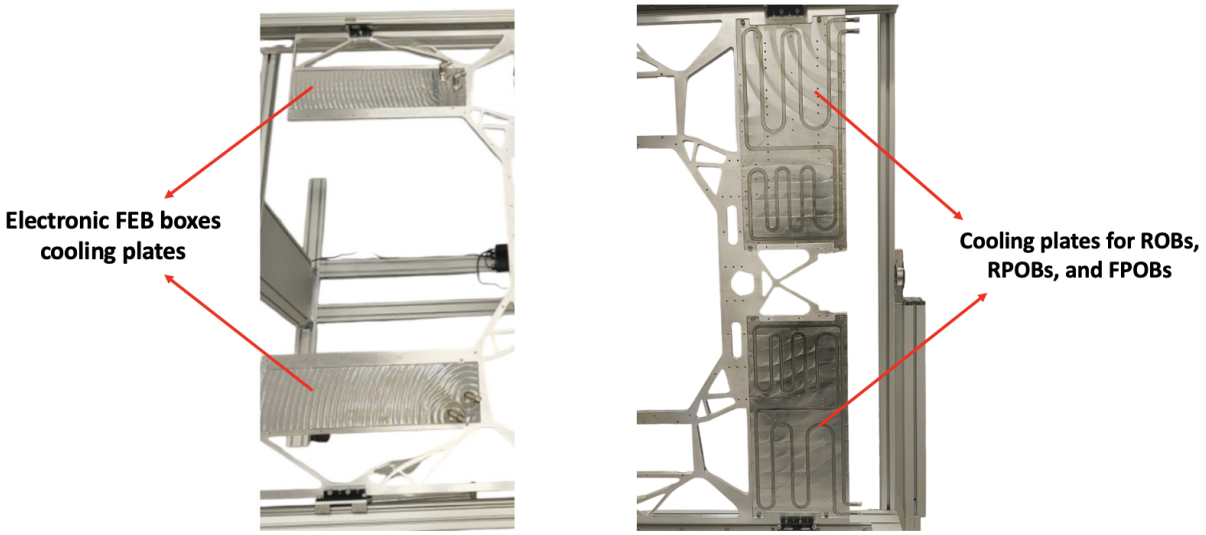

Figure 6.1.3: Four aluminum cooling plates mounted on the C-frame to provide thermal management for FEBs and peripheral components.

Four aluminum cooling plates are arranged within the structure, with one positioned above and one below for the FEBs, and one above and one below the peripheral components, as shown in figure 6.1.3. Aluminum is selected for its high thermal conductivity and mechanical strength, enabling efficient heat removal without adding significant weight. In the mockup, the cooling block primarily represents the actual thermal setup.

After mounting the cooling blocks and peripheral components as seen in figure 6.1.4, the thermal interfaces are installed in their respective positions. It ensures close thermal contact and reduces temperature gradients across the unit. Even with the mockup, proper contact is essential to replicate realistic assembly constraints and prepare the unit for integration with active electronics.

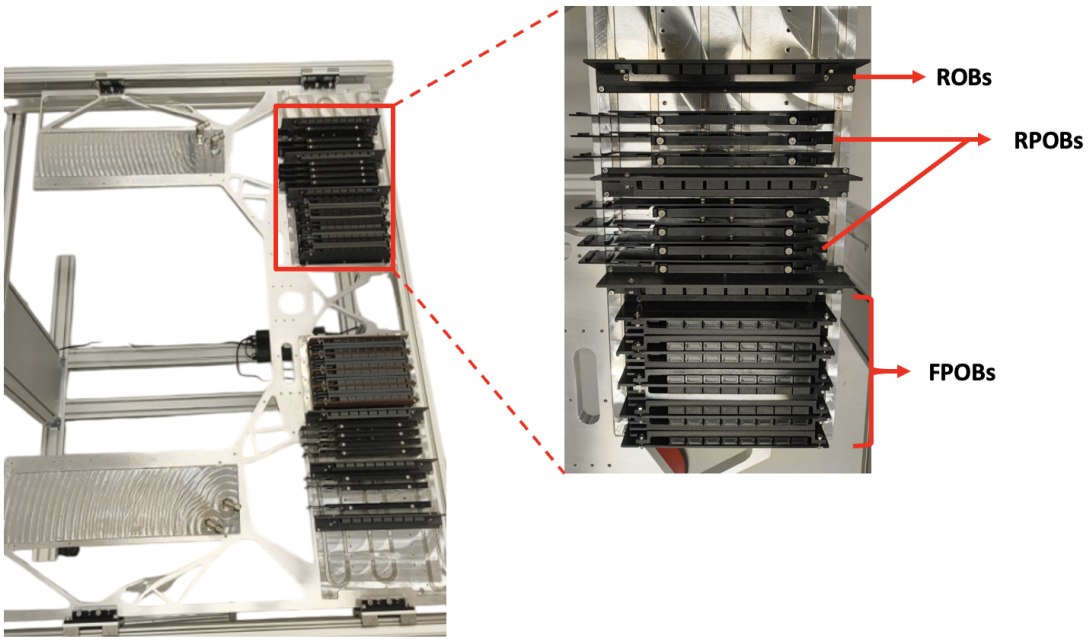

Figure 6.1.4: Arrangement of ROBs, RPOBs, and FPOBs on the C-frame.

6.1.2 Ladder Installation Procedure

The ladders are installed onto the C-frame one at a time, starting from the open side and moving toward the closed side (fig. 6.1.5a). Each ladder is handled with a specially designed pick-up tool to avoid mechanical damage during installation. The ladder is first secured at its bearing points and then fixed through the FEB boxes, as shown in figure 6.1.5b. It keeps the ladder firmly in place and prevents any deformation that could affect the alignment of the sensor modules. Careful positioning at this stage is crucial because even minor deviations can influence the overall performance of the sensors and ladder. Once the ladders are properly secured, the read-out cables are routed to the ROBs and RPOBs, while power cables are routed to their respective FPOBs (see fig 6.1.6).

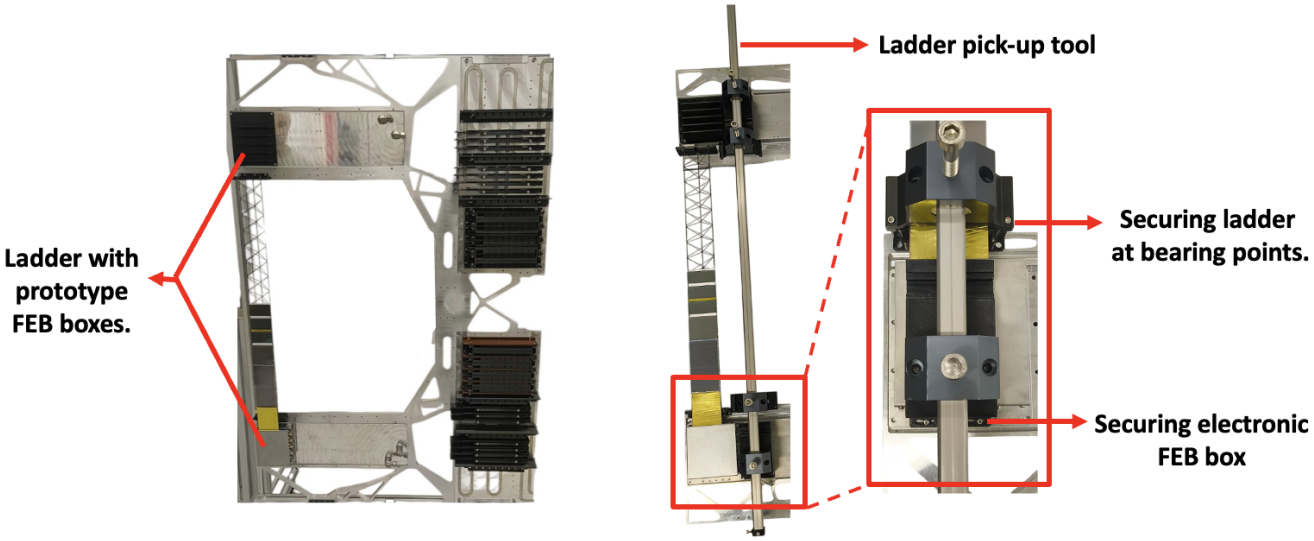

Figure 6.1.5: (a) Sequential placement of ladder and FEB box from the open side (left side). (b) Securing the ladder and FEB box using the pick-up tool (right side).

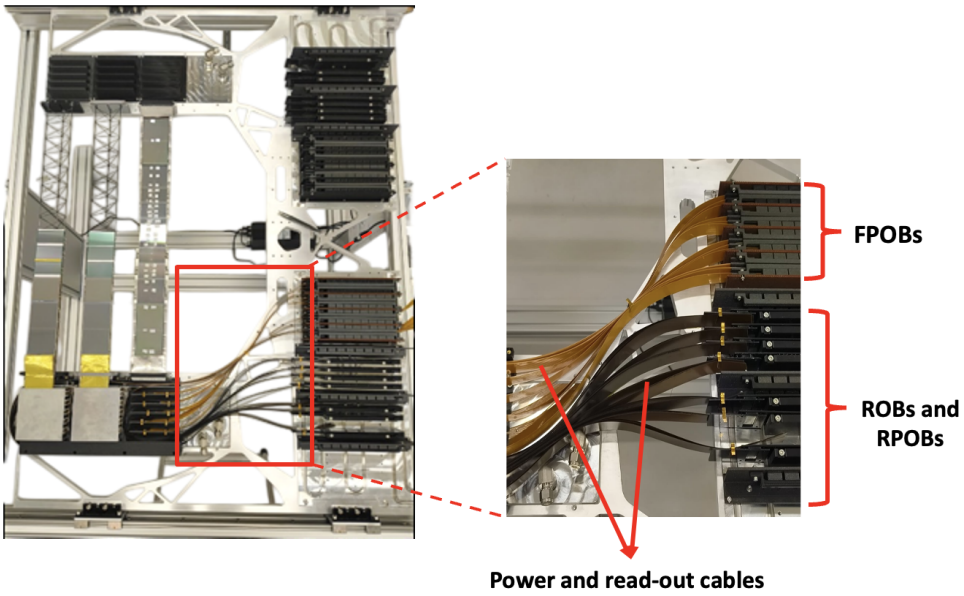

Figure 6.1.6: Routing of cables to the corresponding peripheral components.

Once all the electrical connections are completed, a cable duct is installed to keep the read-out cables organized and secure. During the process, care is taken to minimize cable tension and keep power and read-out cables separated. It helps reduce interference and ensures reliable signal transmission. The same procedure is repeated for each ladder along the C-frame. Following this method throughout the assembly ensures the ladders remain mechanically stable, properly aligned, and function correctly.

6.1.3 Cable Connection Sequence

The cable routing follows a structured and efficient flow to ensure stability and guide further connections. In this cabling exercise, only the FEBs were placed in the FEB

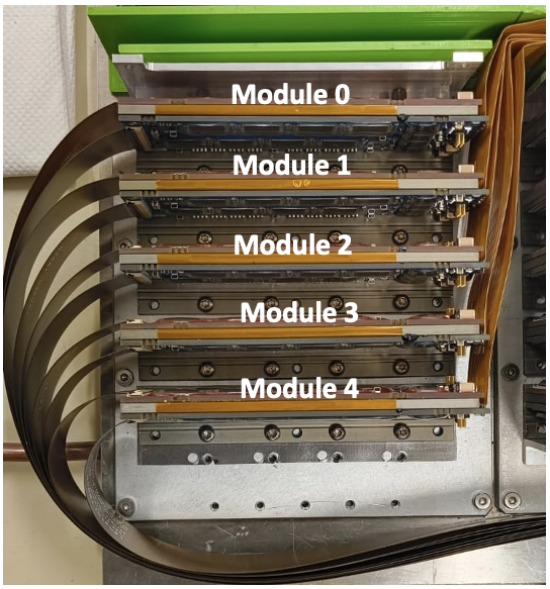

Figure 6.1.7: Sequential connection of data and power distribution cables across the modules of FEB box 1.

boxes, without the sensor modules and microcables; these FEBs are treated as representative modules, allowing the routing procedure to be practiced safely before full integration with assembled ladders and sensors. Data cable routing begins at the left side of module 4 (located at the bottom of the FEB box) and proceeds sequentially through modules 3, 2, 1, and 0, as seen in figure 6.1.7.

For each module, the readout cables are guided below the FEB box to the corresponding ROBs and RPOBs, and then followed by soldering the power distribution cables on the right side (fig 6.1.7) of the FEB box, starting from module 0 at the top of the FEB box and continuing sequentially through modules 1, 2, 3, and 4. For each module, the cables are guided above the FEB box to the respective FPOBs. A similar routing pattern is then used for all other FEB boxes, ensuring the connections follow a consistent path.

As shown in figure 6.1.8, the cabling sequence was practiced on the remaining FEB boxes. Connecting the data cables to the modules in the second FEB box was slightly more challenging because of the narrow openings. To address this, the cables were carefully pre-bent and guided through the modules to fit properly without adding mechanical stress. With careful handling, the process remained feasible.

In contrast, soldering the power cables to the modules was relatively simple, as the connectors were on the opposite side, providing easier access and less mechanical constraint before the next ladder was installed. During this exercise, a third FEB box was mounted on the C-frame to practice soldering of power cables, under realistic assembly conditions (fig. 6.1.9). This practice help improve the procedure safely before working with fully assembled ladders and sensor modules. In the real setup, connecting both data and power cables should be manageable thanks to the improved accessibility. Finally, cable ducts is installed to secure all data cables, maintaining uniform separation, minimizing overlap and mechanical stress, and improving reliability and ease of future maintenance.

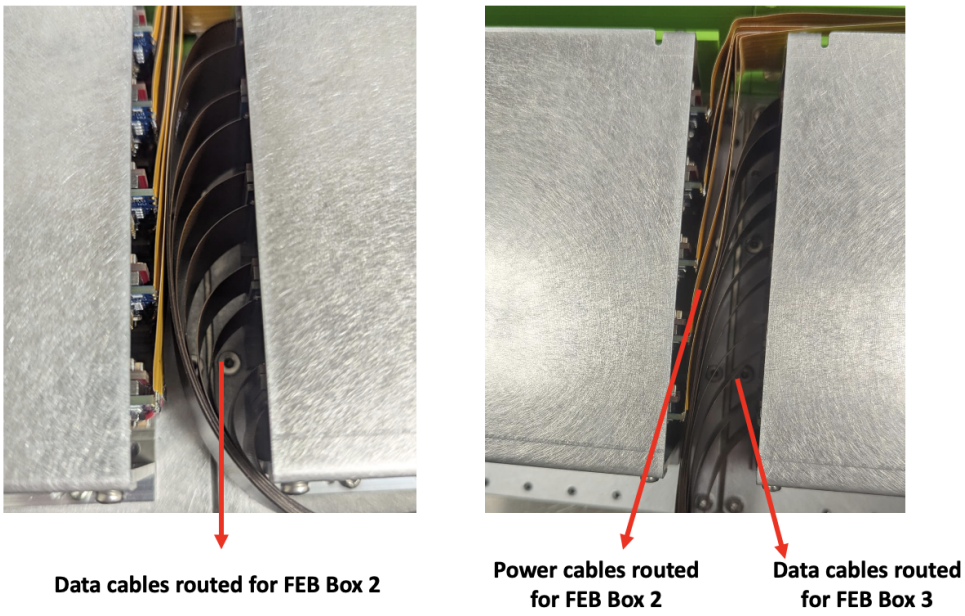

Figure 6.1.8: Sequential connection of data and power distribution cables across the modules of FEB boxes 2 and 3.

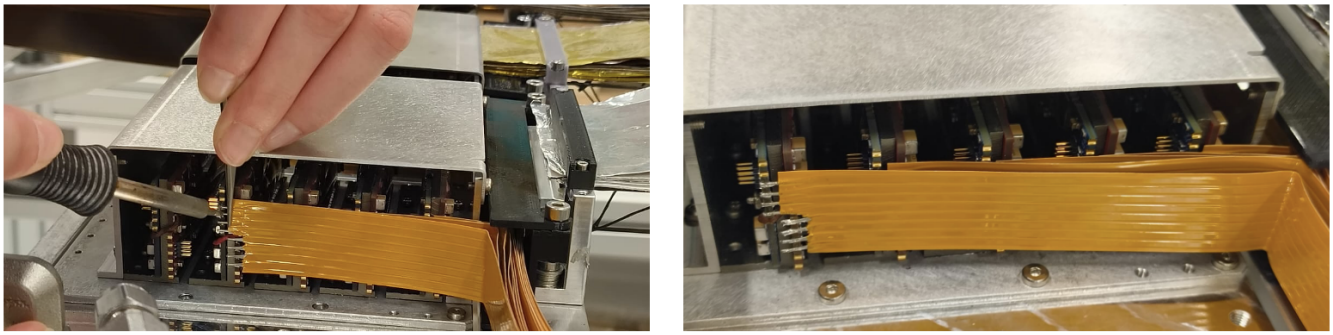

Figure 6.1.9: Soldering power cables on the third FEB box mounted on the C-frame.

After completing the routing, functional tests were performed on the modules to confirm correct cable connections, routing flow, and signal integrity, as discussed in the next section. This approach provides a structured and reliable framework for cable installation, verification, and maintenance across all modules, while accommodating minor routing challenges at the inner FEB boxes. This approach provides a structured and reliable framework for cable installation, verification, and maintenance across all modules, while accommodating minor routing challenges at the inner FEB boxes.

6.2 Functional Testing and Powering of FEB Boxes with FPOB

After completing the cable routing procedure, the modules went through functional testing not only to confirm that all cable connections were properly established and the overall signal integrity was maintained, but also to verify that the defined cabling sequence could be reliably implemented in the actual detector configuration without introducing additional noise or connectivity issues. To further validate this, two FEB boxes were tested to measure their equivalent noise charge (ENC), and the results confirmed that the adopted cabling protocol performs reliably under operating conditions. Additionally, the tests provided an opportunity to evaluate the routing of data and power cables, particularly in compact areas of the inner FEB boxes where cables had to be pre-bent. This exercise confirmed that the slight pre-bending of cables does not compromise the performance of the modules. Overall, these tests validated the cabling procedure and confirmed reliable practices for installation and verification.

Powering of the modules was achieved by soldering the power cables to Sumida connectors, which were then plugged into the FPoB. The FPoB distributes stable, regulated voltages to the modules via FEAST modules and LDO regulators. The FPoB is connected to a low-voltage supply delivering slightly below 12 V, ensuring safe operation. Data cables were connected to the EMU boards, while modules were powered individually through the FPoB, without the use of ladders or additional detector components. Both the FPoB and FEB boxes were mounted on their respective cooling plates, with active thermal

management provided by a LAUDA chiller, enabling complete powering of the modules while maintaining effective cooling of the cables, thereby ensuring robust thermal management throughout the system.

For the functional evaluation, the equivalent noise charge (ENC), VDDM voltage stability, and temperature of the ASICs were monitored. ENC measurements were taken across all operating ASICs. And in general, the results matched theoretical expectations. The corresponding ENC plots for all modules in FEB Boxes 1 and 2 are presented in figures 6.2.1 through 6.2.10. The prototype electronics FEB Boxes were used to study the equivalent noise charge (ENC) of all ASICs across ten modules, complementing the functional evaluation presented in Section 5.4. The ENC average values were calculated across all 1024 channels, with typical ASIC noise around ≈ 350 e. independent of the setup.

The average ASIC noise performance was first measured on FEB Box 1 across five modules. But, one p-side ASIC in Module 0 failed, with the affected channels indicated in the plot. Modules 1 and 2 performed as expected. In Module 3, two p-side and three n-side ASICs failed, with the affected channels indicated in the plot. In Module 4, five p-side ASICs failed, and the fifth ASIC exhibited high irregular behavior across channels. Next, the average noise performance was measured on FEB Box 2. Modules 0, 1, 2, and 4 performed as expected. In Module 3, three ASICs failed: two are indicated in the plot, and the third exhibited highly irregular behavior across channels.

All ASIC failures were cross-checked using their hardware addresses, which confirmed that the problems were caused by corrupted registers rather than mechanical damage due to the cables. Despite these few failures, the noise performance of all modules met the expected values, confirming that the FEB Box design and cable routing configuration are valid across both FEB boxes.

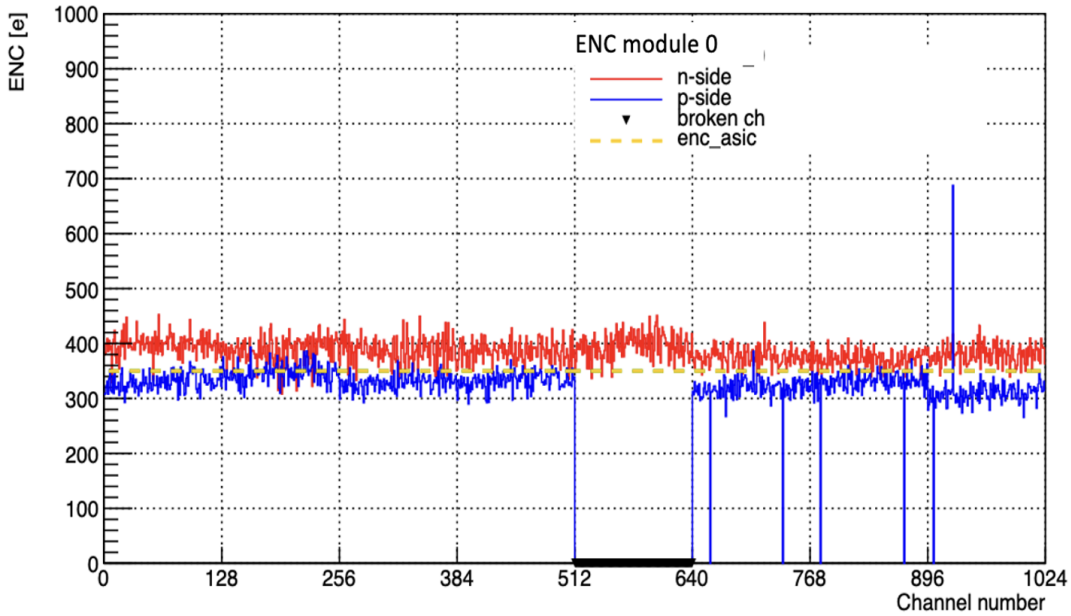

Figure 6.2.1: Average ASIC noise performance for Module 0 of FEB Box 1.

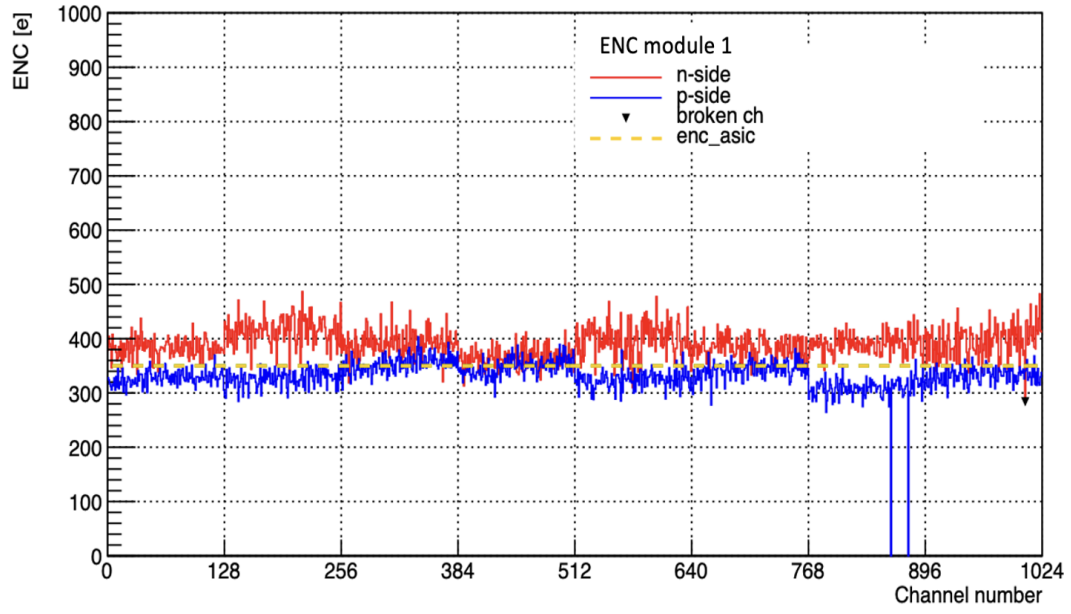

Figure 6.2.2: Average ASIC noise performance for Module 1 of FEB Box 1.

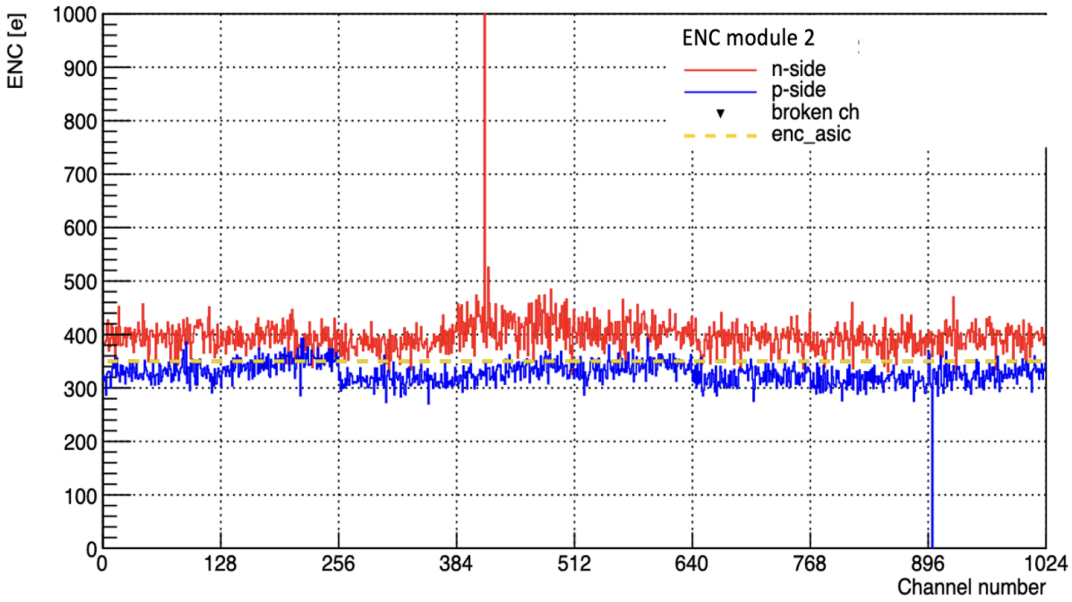

Figure 6.2.3: Average ASIC noise performance for Module 2 of FEB Box 1.

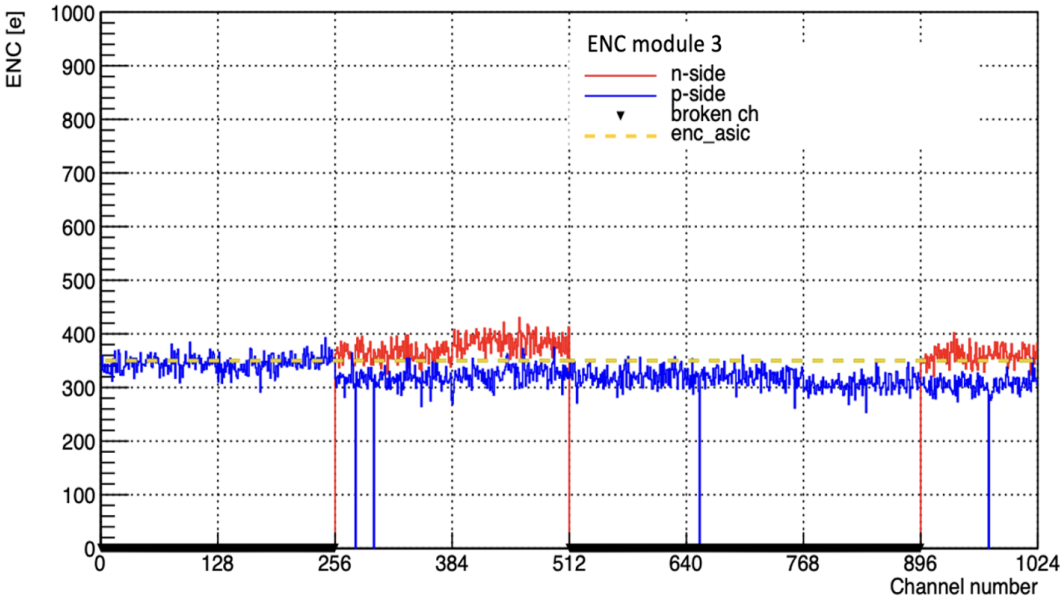

Figure 6.2.4: Average ASIC noise performance for Module 3 of FEB Box 1.

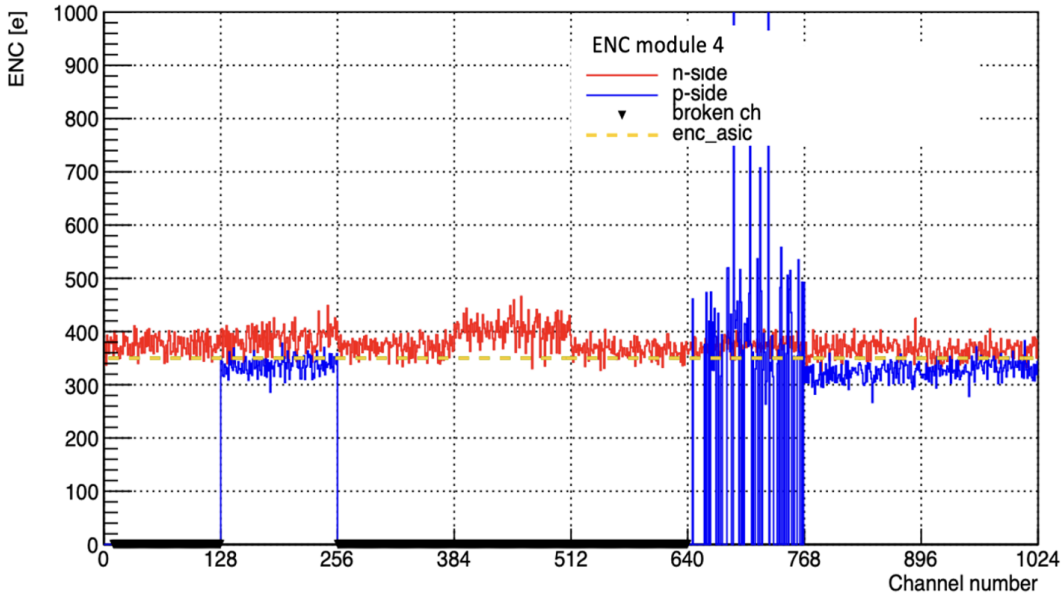

Figure 6.2.5: Average ASIC noise performance for Module 4 of FEB Box 1.

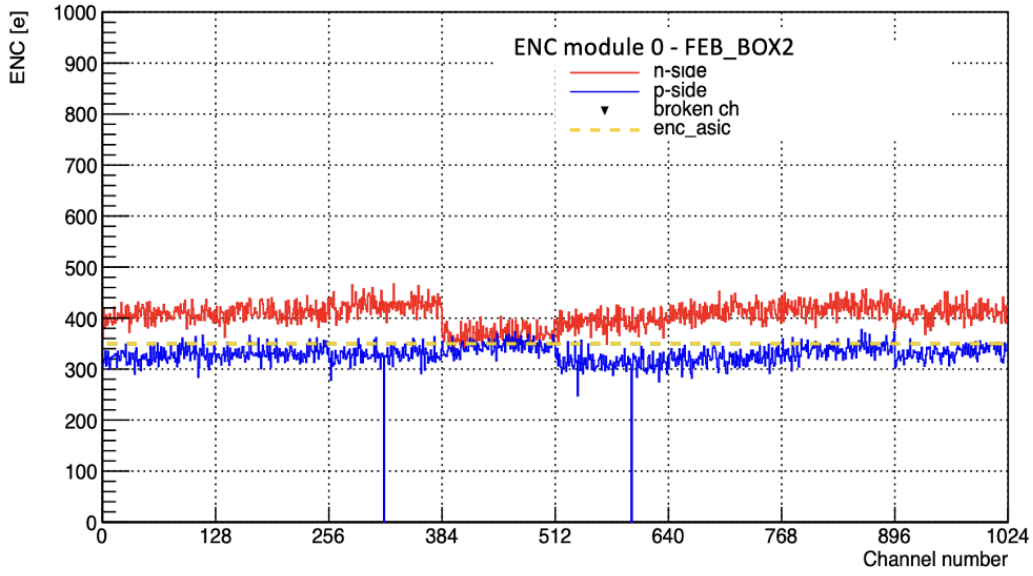

Figure 6.2.6: Average ASIC noise performance for Module 0 of FEB Box 2.

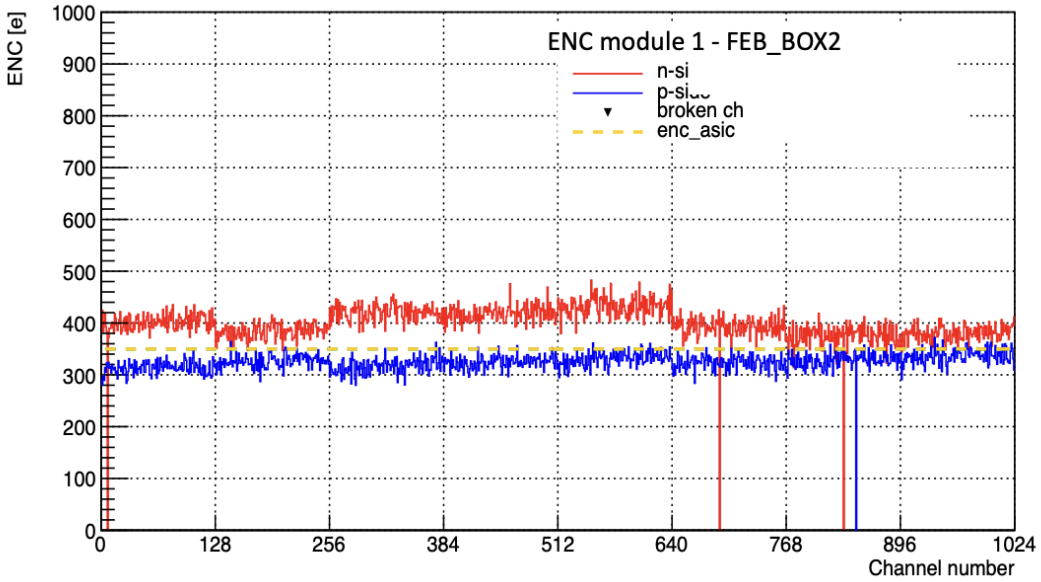

Figure 6.2.7: Average ASIC noise performance for Module 1 of FEB Box 2.

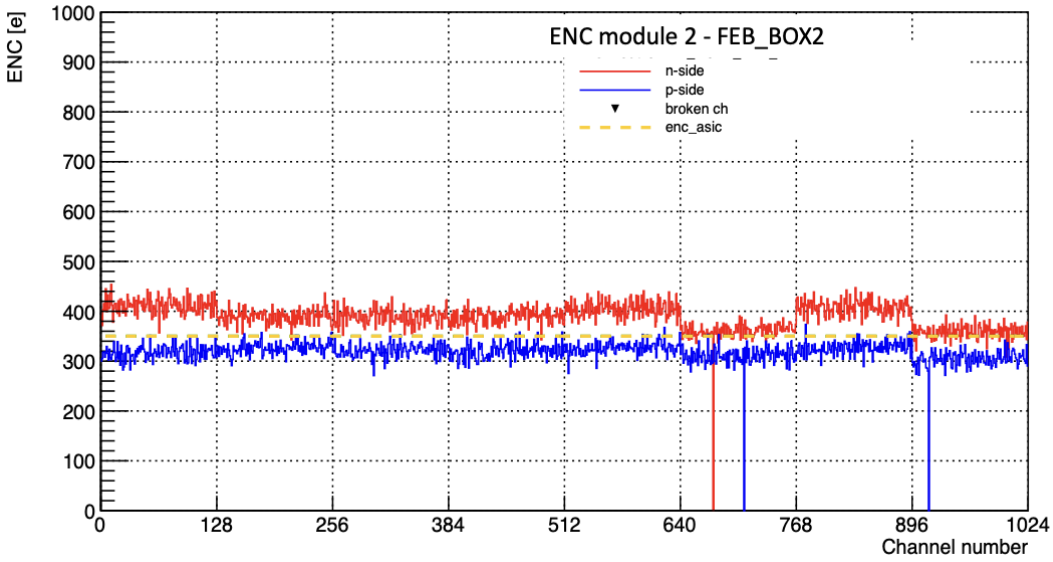

Figure 6.2.8: Average ASIC noise performance for Module 2 of FEB Box 2.

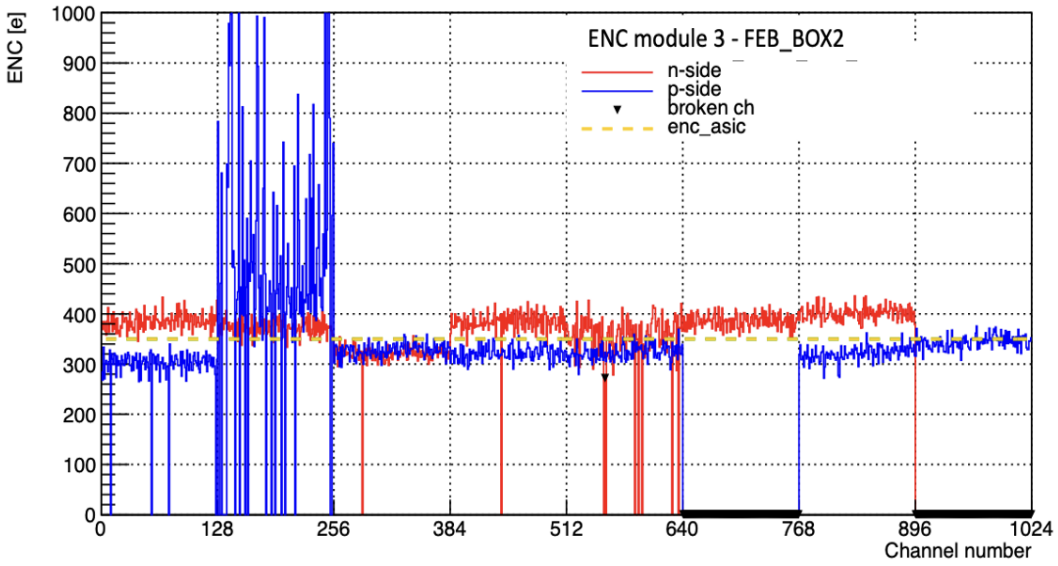

Figure 6.2.9: Average ASIC noise performance for Module 3 of FEB Box 2.

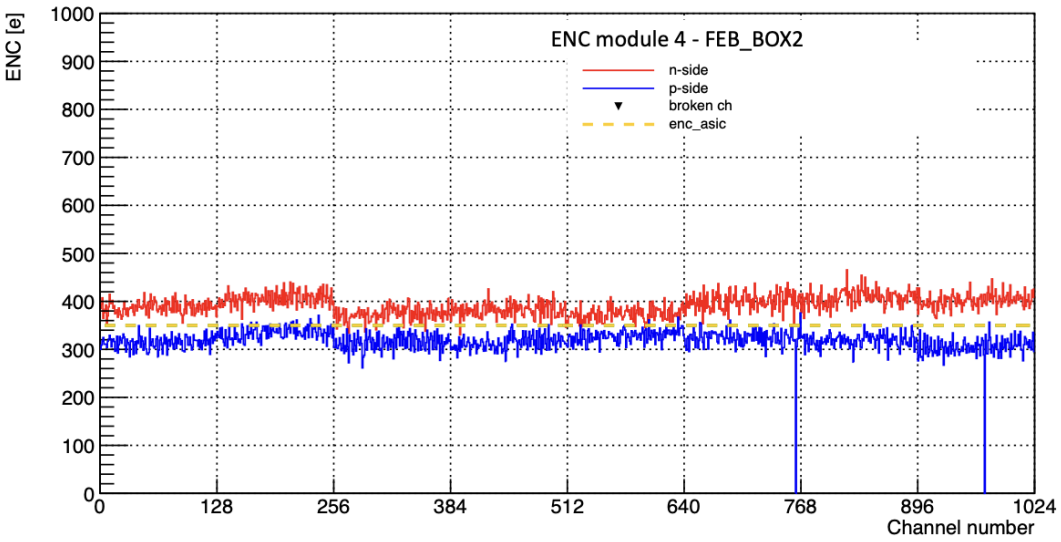

Figure 6.2.10: Average ASIC noise performance for Module 4 of FEB Box 2.

Thermal imaging was performed on all modules of FEB Box 1 as an additional precaution to verify the temperature distribution, identify potential hotspots, and confirm that all ASICs operated within safe limits throughout the tests.FEB Box 1 was selected as a representative module for the purpose of performing a detailed analysis before testing the other boxes. Appropriate emissivity settings were selected for the thermal camera to ensure measurement accuracy. The observed discrepancy of 15–20 °C is expected, as it arises partly from the selected emissivity and because the thermal camera measures the surface temperature of the ASICs. At the same time, the configured temperatures reflect their operational heating. All ASICs in the modules remained well below the target operating temperature of 60 °C. Quantitative thermal results for FEB Box 1, along with representative thermal images corresponding to the measurements captured using a thermal camera, are summarized in figures 6.2.11 - 6.2.15. These plots specifically show the thermal images of the n-side and p-side for Modules 0–4 of FEB Box 1, respectively.

The temperatures obtained from the thermal camera measurements are presented in Tables 5 - 9, alongside the temperatures recorded during the configuration of tests. Thermal images showed no significant hotspots across any of the modules. The system's cooling setup was effective, and all modules stayed within safe temperatures during testing. The differences between the thermal camera readings and the configured test temperatures, as reported in the tables, remained within acceptable limits.

The thermal measurements showed the relative temperatures across the modules and confirmed that all ASICs stayed within safe operating limits. The tests also gave practical lessons for integration. These results confirm that the cabling protocol worked well even in tight spaces, and pre-bending the data cables did not noticeably affect the noise performance. The FPoB delivered stable voltages throughout the tests, showing that it is suitable for operation in the actual detector setup. Although additional tests on more FEB boxes would increase statistical confidence, these preliminary findings support the methodology and provide a solid foundation for integrating FEBs with fully assembled detector modules in the future.

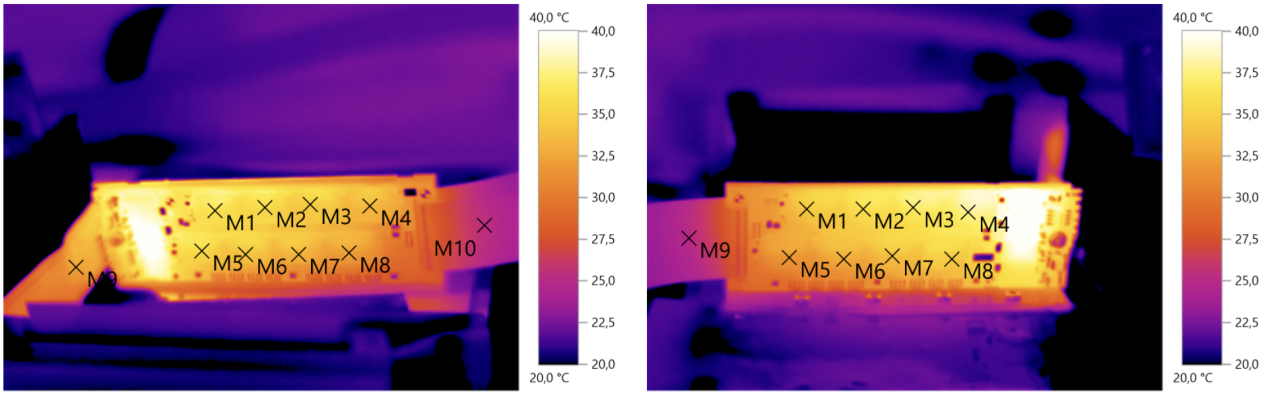

Figure 6.2.11: Thermal images of Module 0: n-side(left) and p-side (right).

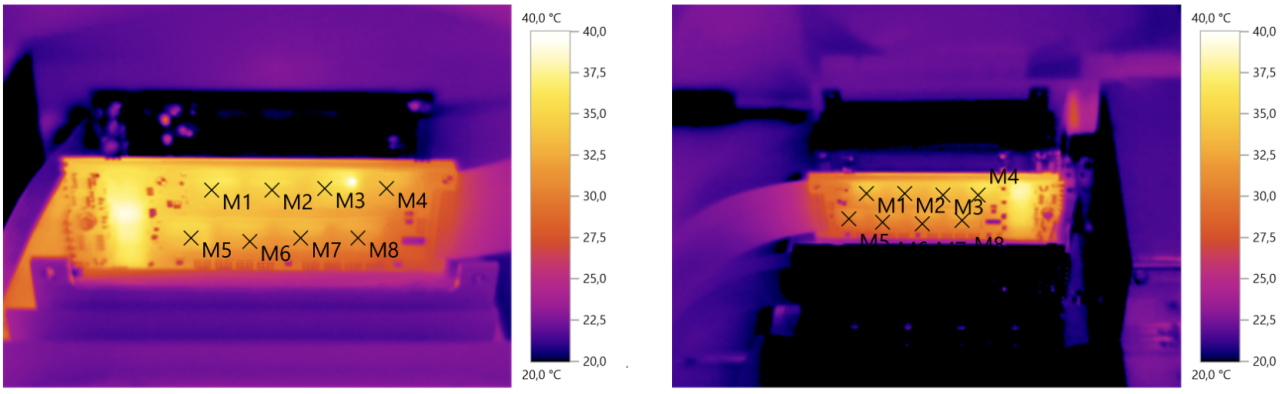

Figure 6.2.12: Thermal images of Module 1: n-side(left) and p-side (right).

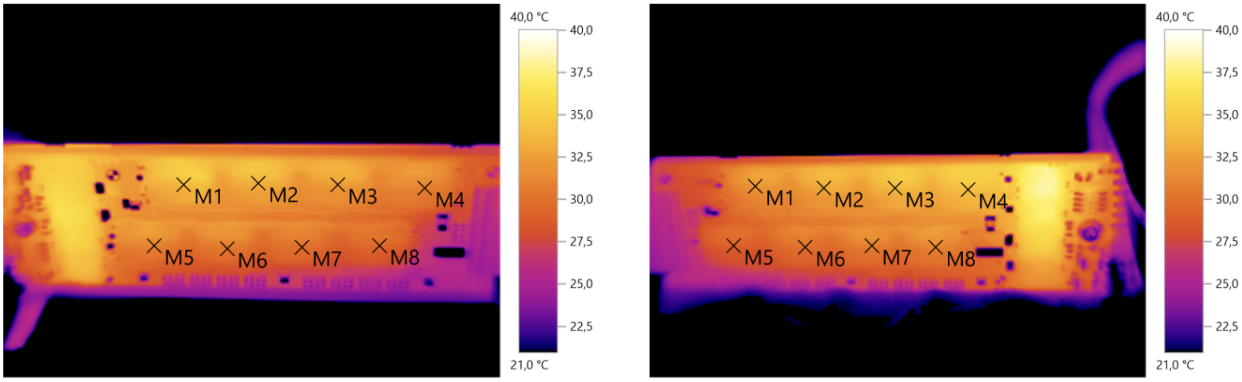

Figure 6.2.13: Thermal images of Module 2: n-side(left) and p-side (right).

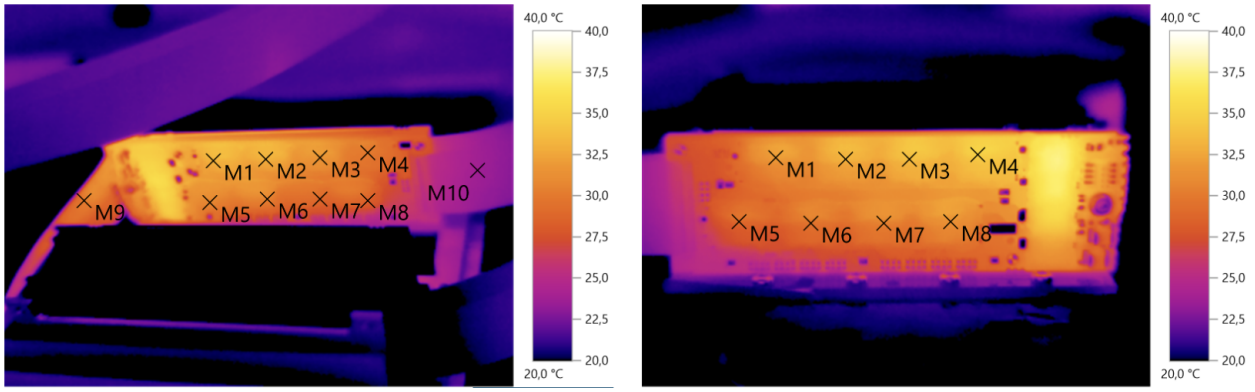

Figure 6.2.14: Thermal images of Module 3: n-side(left) and p-side (right).

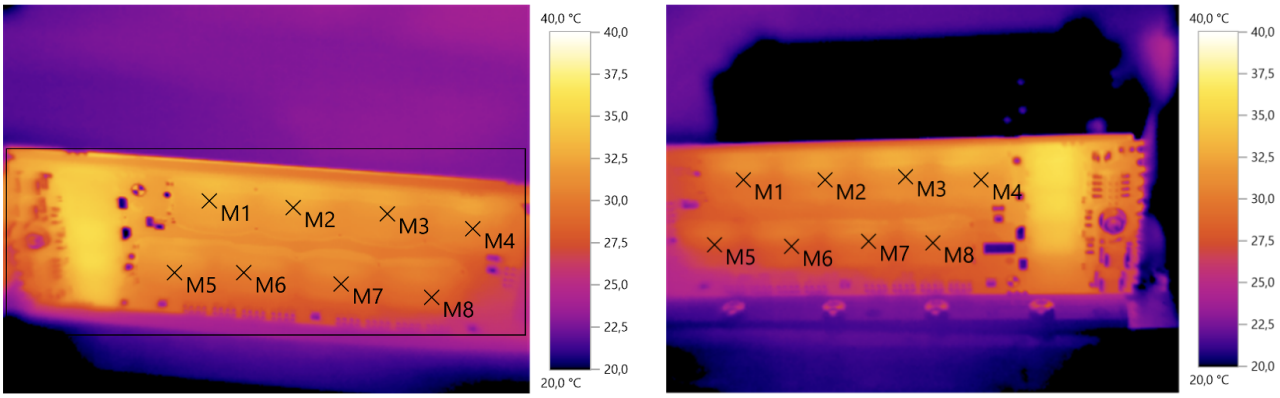

Figure 6.2.15: Thermal images of Module 4: n-side (left) and p-side (right).

POLARITY	HW ADDRESS	Configured Temperature (°C)	Temperature Recorded by Thermal Camera (°C)
P	0	44.4	34.5
P	1	44.4	36.1
P	2	53.9	37.1
P	3	47.5	37.8
P	4	47.5	31.8
P	5	-	32.7
P	6	50.7	34.0
P	7	44.4	34.5
N	0	47.5	36.2
N	1	44.4	35.7
N	2	47.5	34.8
N	3	34.9	33.6
N	4	50.7	35.5
N	5	50.7	34.1
N	6	44.4	33.3
N	7	47.5	32.2

Table 5: Thermal temperatures and configured test temperatures of Module 0 of FEB BOX 1 for P-side and N-side ASICs.

POLARITY	HW ADDRESS	Configured Temperature (°C)	Temperature Recorded by Thermal Camera (°C)
P	0	38.0	33.4
P	1	47.5	33.3
P	2	38.0	33.7
P	3	38.0	34.9
P	4	41.2	30.3
P	5	50.3	30.5
P	6	47.5	30.9
P	7	50.3	32.1
N	0	51.2	32.7
N	1	44.4	32.4
N	2	53.9	31.6
N	3	57.1	31.2
N	4	50.7	31.4
N	5	47.5	30.1
N	6	47.5	30.5
N	7	53.5	38.7

Table 6: Thermal temperatures and configured test temperatures of Module 1 of FEB BOX 1 for P-side and N-side ASICs.

POLARITY	HW ADDRESS	Configured Temperature (°C)	Temperature Recorded by Thermal Camera (°C)
P	0	50.7	31.5
P	1	44.4	33.0
P	2	53.9	33.5
P	3	43.5	34.2
P	4	47.5	38.6
P	5	57.1	49.6
P	6	53.9	30.5
P	7	57.1	32.5
N	0	44.4	32.7
N	1	44.4	32.4
N	2	48.0	31.6
N	3	44.4	41.2
N	4	47.5	44.2
N	5	55.1	30.5
N	6	50.7	45.7
N	7	47.5	48.0

Table 7: Thermal temperatures and configured test temperatures of Module 2 of FEB BOX 1 for P-side and N-side ASICs.

POLARITY	HW ADDRESS	Configured Temperature (°C)	Temperature Recorded by Thermal Camera (°C)
P	0	53.9	32.0
P	1	47.5	33.1
P	2	38.6	33.8
P	3	44.4	34.9
P	4	38.0	39.0
P	5	44.4	39.7
P	6	57.1	30.5
P	7	57.1	41.5
N	0	50.7	33.0
N	1	-	33.0
N	2	-	31.7
N	3	-	40.0
N	4	44.4	40.7
N	5	50.7	30.4
N	6	-	40.9
N	7	-	38.5

Table 8: Thermal temperatures and configured test temperatures of Module 3 of FEB BOX 1 for P-side and N-side ASICs.

POLARITY	HW ADDRESS	Configured Temperature (°C)	Temperature Recorded by Thermal Camera (°C)
P	0	38.0	31.2
P	1	34.9	31.6
P	2	42.0	32.3
P	3	-	33.2
P	4	-	38.1
P	5	-	39.2
P	6	34.9	30.5
P	7	-	44.4
N	0	43.0	32.7
N	1	41.7	32.2
N	2	44.4	31.4
N	3	41.2	41.0
N	4	41.2	42.3
N	5	48	30.4
N	6	46.6	45.0
N	7	42.5	45.1

Table 9: Thermal temperatures and configured test temperatures of Module 4 of FEB BOX 1 for P-side and N-side ASICs.

6.3 Challenges and Limitations

The assembly of the HU required careful planning to make sure all components were assembled properly and without issues. Early in the process, we encountered practical problems that required adjustments to some of the initial plans. The main challenges were the reliability of the 3D-printed mockup parts, the sequence of ladder mounting, and the proper approach to connecting and routing the cables to the FEB boxes. Addressing each of these issues was essential to demonstrate that the assembly procedure could be performed under realistic conditions without compromising either mechanical stability or electrical functionality.

A problem with the 3D printer delayed the production of the mockup components. These mockups included the peripheral electronics, a few FEB boxes, and cable ducts. They were essential for recreating realistic assembly conditions before performing the procedure with the actual components. Repeated printer failures occasionally produced parts that were deformed and unusable for reliable alignment, cable routing practice, or general testing. Several components had to be reprinted. While these problems did not prevent the continuation of tests, they introduced inefficiencies and highlighted the strong dependency of the workflow on accurate mockup parts.

The next challenge was determining the order in which the ladders should be mounted. In the initial assembly plan, the ladders were to be installed starting from the inner side of the C-frame and progressing outward. This approach initially appeared logical from a mechanical standpoint, as it provided a seemingly straightforward sequence for placing the ladders in order. However, when this sequence was tested with the mockup, it became clear that the arrangement made it difficult to access the power and data cables. Once the ladders on the inner side were installed, the available space for routing and soldering cables to the ladders became constrained, making it challenging to establish proper cable connections. As a result, the ladder mounting sequence was modified to give importance for enough access for cabling than the original order. The new method was then implemented, ensuring enough space for routing and connecting cables to all modules while keeping the ladders properly aligned and mechanically stable.

A third limitation was encountered during the functional testing phase when powering the FEB boxes with the FPoB. One of the Molex connectors responsible for supplying low voltage to the FPoBs was damaged. Although a single FPoB is capable of powering four modules simultaneously, the broken connector limited the testing to only three modules at a time. This incident resulted in additional time for the testing procedure and highlighted the importance of careful handling of the distribution of power. It also made clear that having spare connectors on hand during assembly and commissioning helps avoid delays and keeps the process running smoothly.

Overall, the HU assembly workflow worked well and was fairly realistic, despite the practical challenges faced during testing. Mockup tests proved valuable, especially in helping to plan and verify that the assembly steps could be carried out, cable routes were accessible, and powering through the FPoB remained reliable. These lessons provided key takeaways for the future integration with fully functional components, although minor adjustments may still be necessary. When assembling the actual HU with ladders, FEEs, and soldering the cables, the step-by-step protocol serves as a dependable guide, helping the following assembly stages proceed efficiently and showing that the workflow performs well under realistic conditions.

7 Summary

This work demonstrates that the assembly and integration of the STS half-unit (HU) is technically possible and operationally reliable. The step-by-step assembly protocol developed in this study, together with functional testing of the FEB boxes, enabled verification of both mechanical alignment and electrical performance. These hands-on exercises provided valuable practical findings and established a clear framework for future HU assemblies.

Mockups of the ladders and other components played an essential role in this study, as they allowed the arrangement of the components on the HU to be evaluated without exposing actual ladders or electronics to risk. The Functionality and cable routing were confirmed by utilizing FEB boxes. This approach contributed to identifying potential complications in advance, ensured accessibility to all connection points, and allowed for the accurate execution of assembly steps.

Functional tests with the FEB boxes confirmed that the assembly protocol performed reliably under representative operating conditions. The electrical and thermal performance of the HU was stable, with consistent power delivery to the ASICs, proper communication, and expected configuration throughout the system. Temperature and noise levels (ENC) were observed. They remained stable across all modules, indicating that neither the cable layout nor the power configuration introduced unwanted disturbances. The electronics performed as expected, well within the expected range. Thermal imaging confirmed that the cooling system maintained all the modules in good condition, with no significant hotspots. Overall, these results indicate that the protocol maintains both electrical and thermal integrity, providing a strong basis for the reliable operation of the HU.

Looking at the bigger picture, these exercises revealed several key lessons. They revealed the unexpected difficulties and provided opportunities to refine the assembly protocol without risk. Ensuring easy access for cable handling remained a central factor in the integration strategy. Careful management of cables is important, since clear routing and accessible cable connections enable the assembly to be carried out efficiently and precisely.

Even minor imperfections can impact test continuity and overall assembly performance, highlighting the need for careful attention to both mechanical and electrical aspects. The lessons learned from repeated attempts contributed to further improvements in assembly procedures and overall reliability. These experiences highlighted that successful assembly requires a balance between mechanical accuracy and flexible design.

Overall, this study demonstrates that the STS HU can be assembled accurately while maintaining both its structure and the electronics stable and working reliably. The cable routing procedure was tested as part of the assembly, and its efficiency was checked through functional tests. The tests also gave useful information on handling the components, checking connections, and ensuring quality and performance. This work provides a solid basis for future HU assemblies and helps define practical best practices for building and integrating detectors in the CBM STS.

The upcoming work focuses on integrating the half units onto multi-station sections and examining their impact on overall system performance. This includes mechanical stability, proper alignment, and overall detector operation. The project also involves refining procedures for assembling, aligning, and validating the HUs, along with quality assurance protocols that cover all necessary mechanical, alignment, and performance checks under realistic conditions. Using full-scale mockups and functional prototypes, integration steps such as mounting, cabling, and thermal connections will be performed and evaluated for their effect on overall system performance.

In this next phase, the goal is to build and qualify larger STS structures that bring the system closer to its final detector configuration. The focus is on assembling and installing the components, making sure power and cooling connections function well, and that the readout remains stable. The work will also make sure the assembled structures remain steady and reproducible during operation. Altogether, these activities will help finalize the integration procedure and prepare the STS for installation and commissioning in the CBM experiment.

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