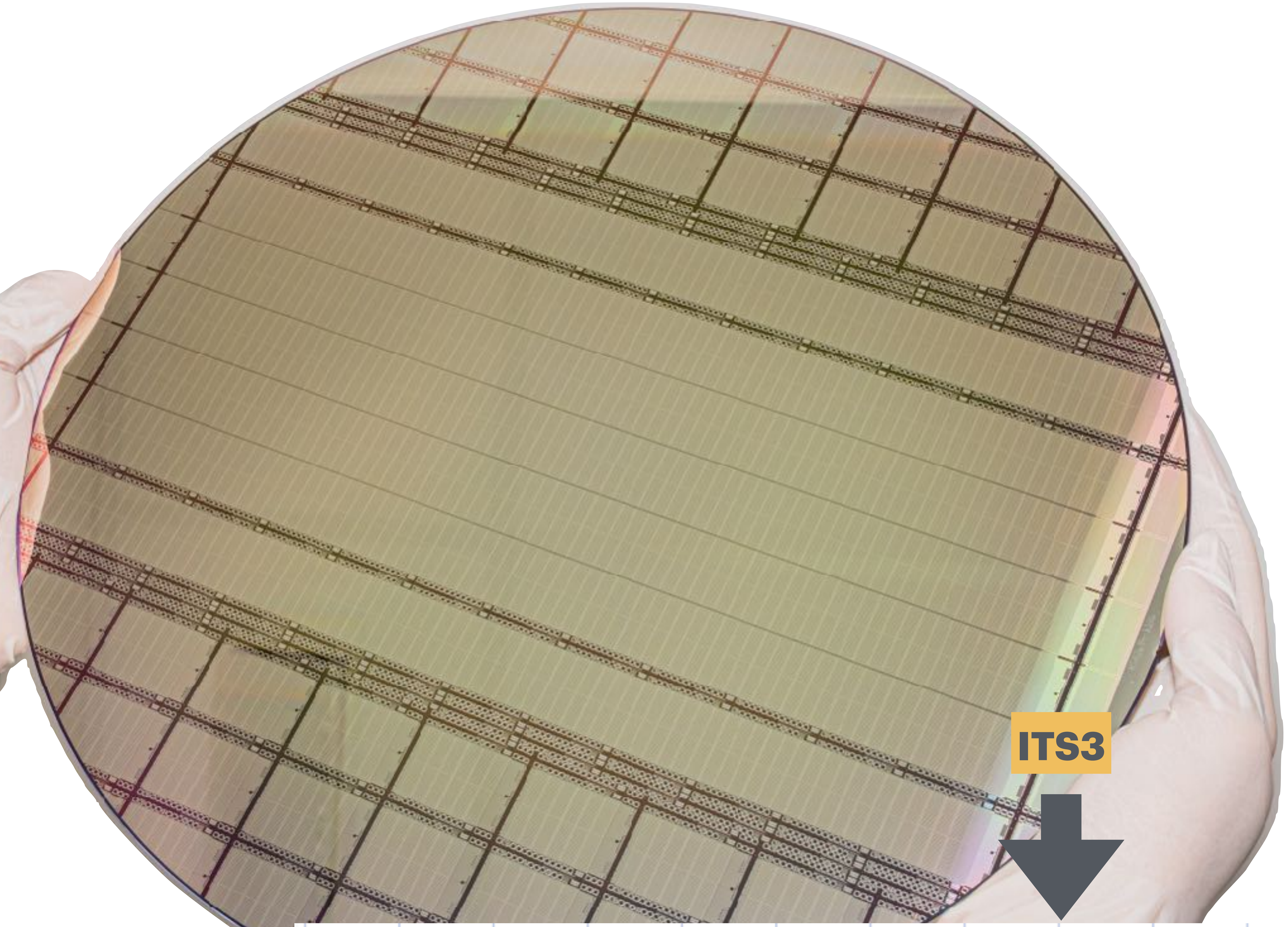
Recent and future developments in Monolithic Active Pixel Sensors
ALICE ITS3 and ALICE 3

Magnus Mager (CERN) on behalf of ALICE

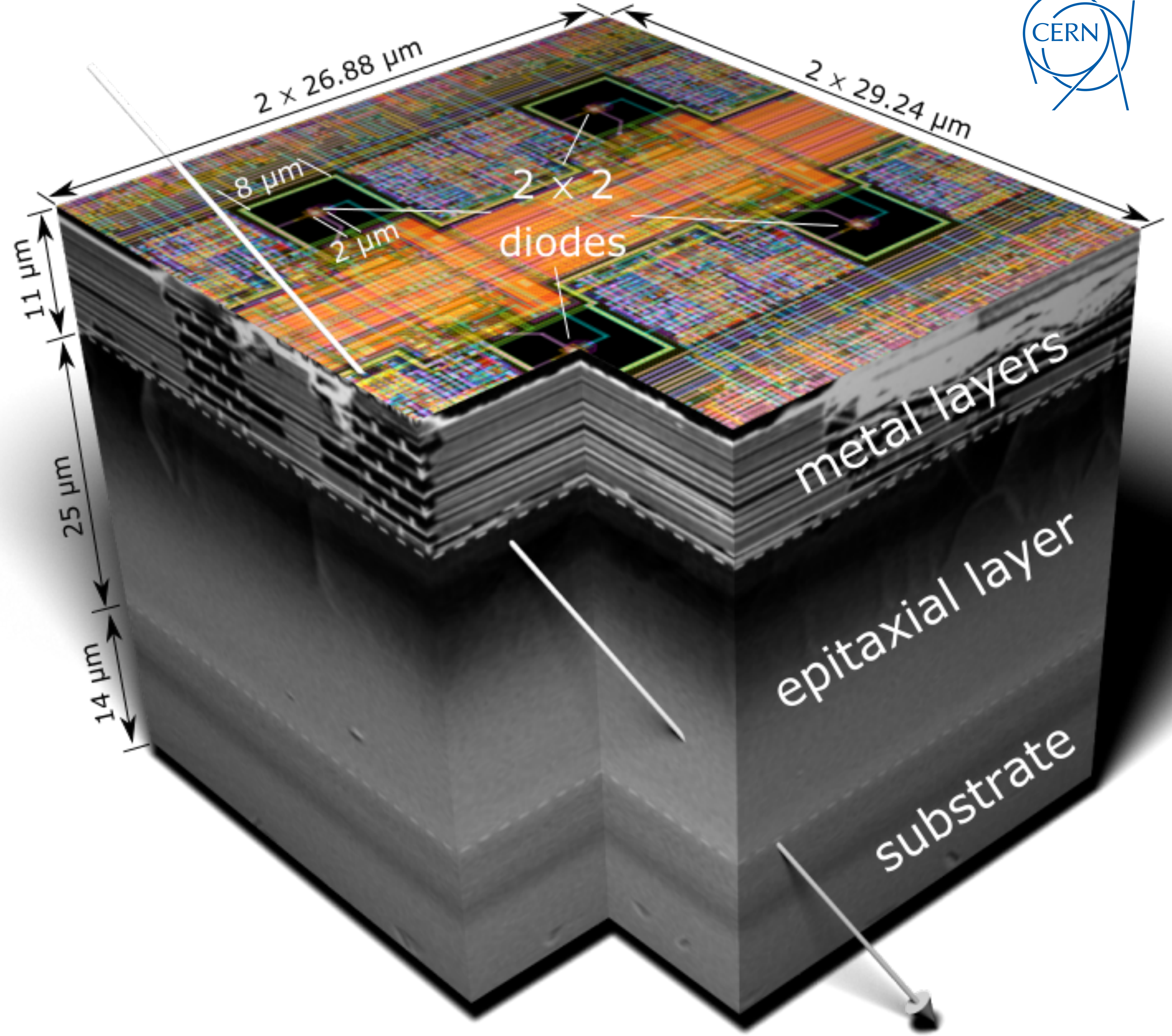
23.03.2026 GSI

Outline



- Monolithic Active Pixel Sensors (MAPS)
  - motivation / key specs
- Starting points
  - STAR Heavy flavor tracker (HFT)
  - ALICE Inner Tracking System 2 (ITS2, ALPIDE)
- **ALICE Inner Tracking System 3 (ITS3)**
  - 65 nm technology
  - wafer-scale
  - bent
- **ALICE 3**
  - high radiation loads
  - large area
- *More ideas*

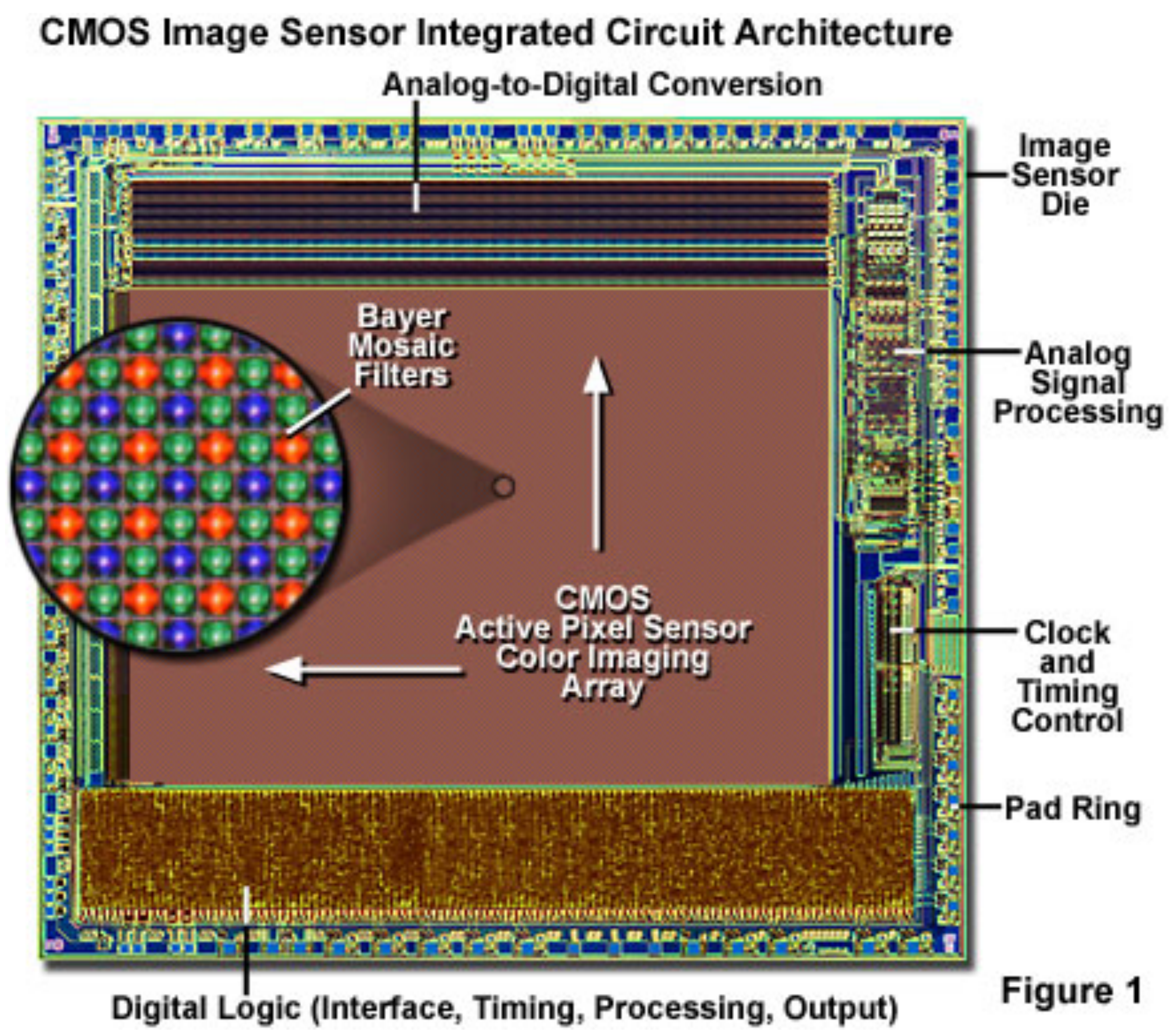
MAPS

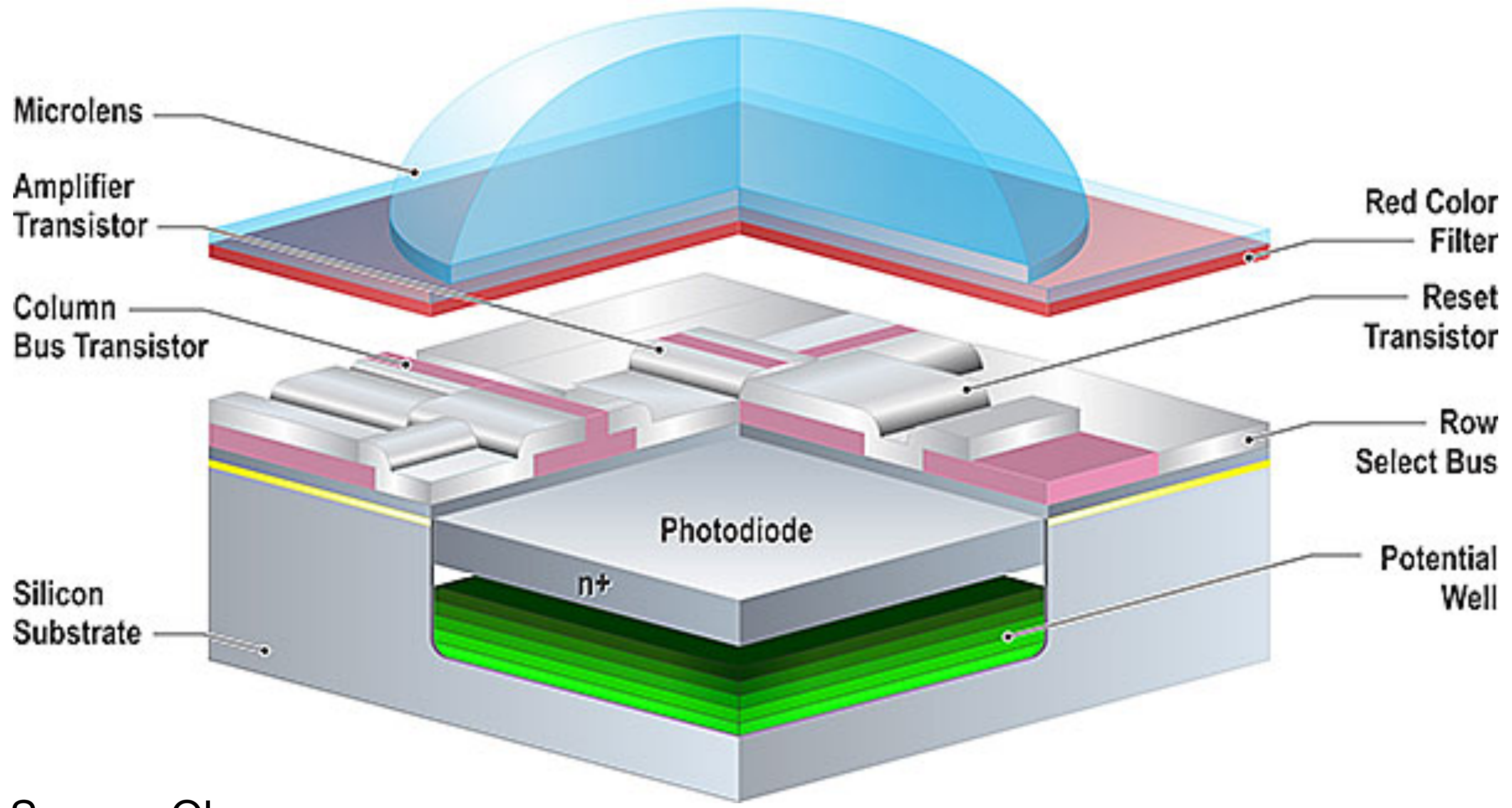


2 × 26.88 µm
2 × 29.24 µm
8 µm
2 µm
2 × 2
diodes
11 µm
25 µm
14 µm
metal layers
epitaxial layer
substrate

Monolithic CMOS pixel sensors

sensor and readout on same chip

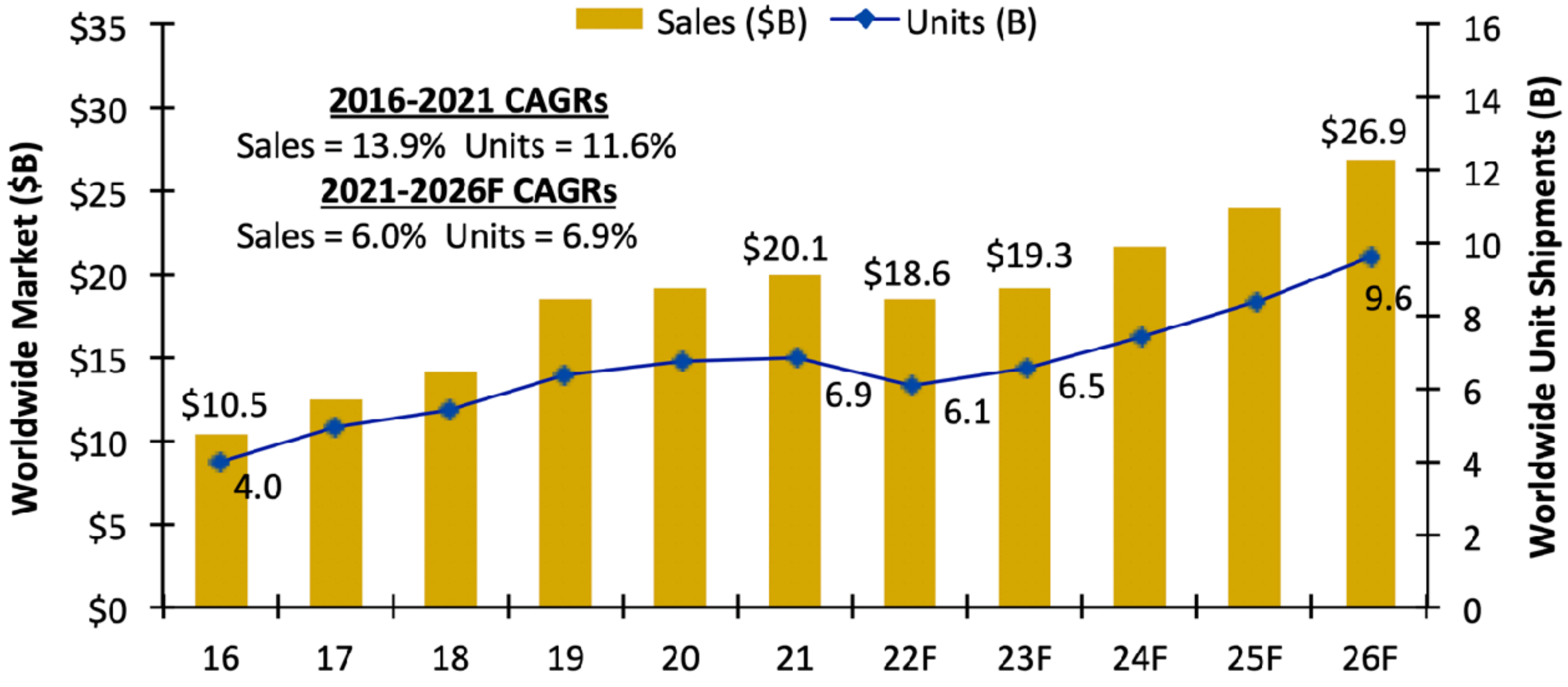




Source: Olympus

- Nowadays the most widespread implementation of image sensors
  - main advantage: price
- Light vs charged particles:
  - both generate electron/hole pairs
  - need to increase sensitive area to 100% (no focusing lenses for charged particles)

CMOS image sensor market

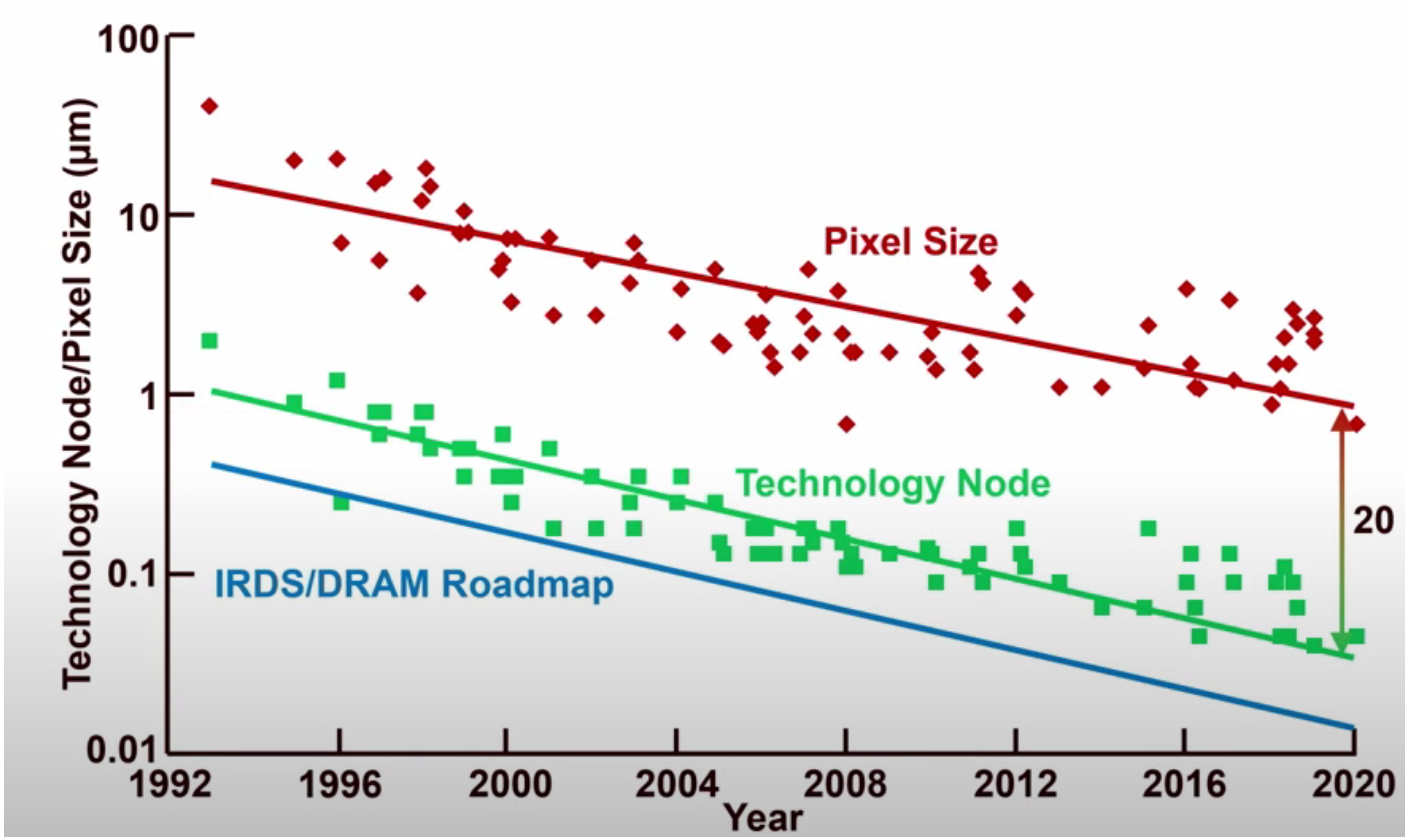


[IC Insights]

- Rapid increase of sales
- HEP *can* profit from a huge commercial interest
- Our job: make these light sensors particle sensors

Evolution of technology node / pixel size

for image sensors

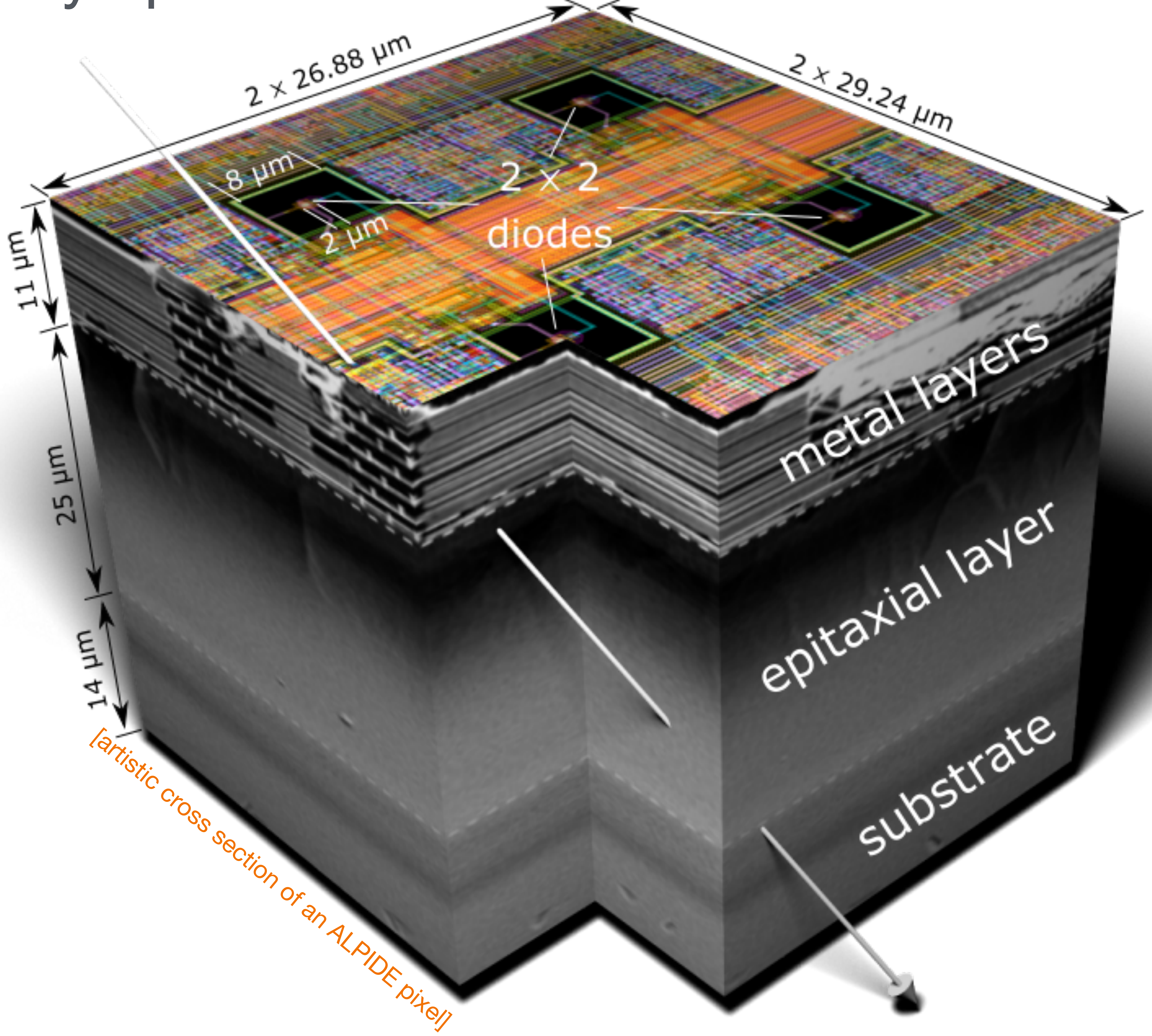


[A. Theuwissen, ISSCC 2021]

- **Pixel size:** 20x above technology feature size
- **Technology:** 10 years behind DRAM technology
- **Functionality:** typically only very few (1-4) transistors per pixel
- HEP applications have many more transistors per pixel (see later)

Monolithic Active Pixel Sensors (MAPS)

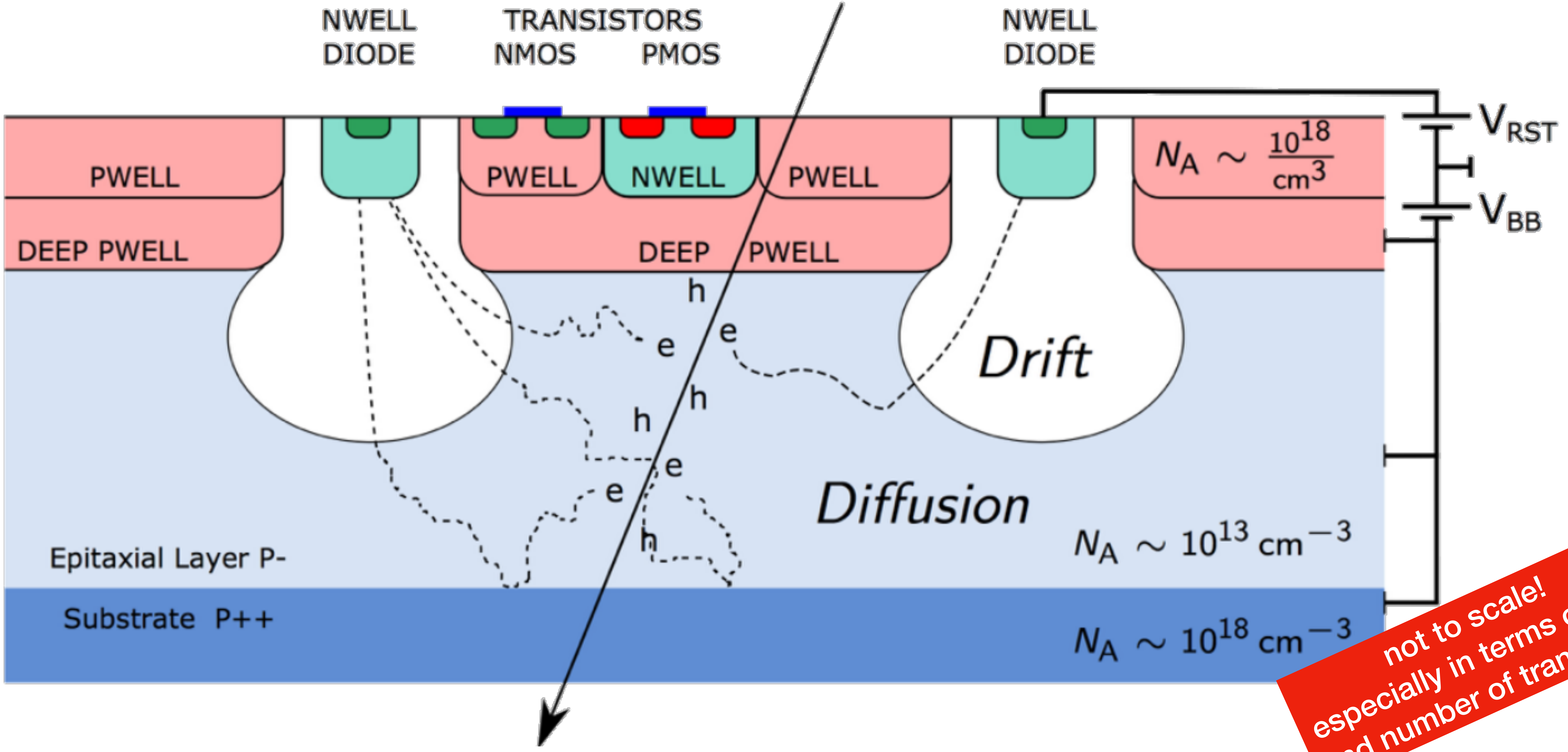
key specifications of state of the art sensors



- **Thin:** O(50 µm)
- **Very granular:** O(10-30 µm)
- **Small diodes:** capacitances of O(1-5 fF)
- **Highly integrated:** O(100) transistors/pixel

Monolithic Active Pixel Sensors (MAPS)

working principle



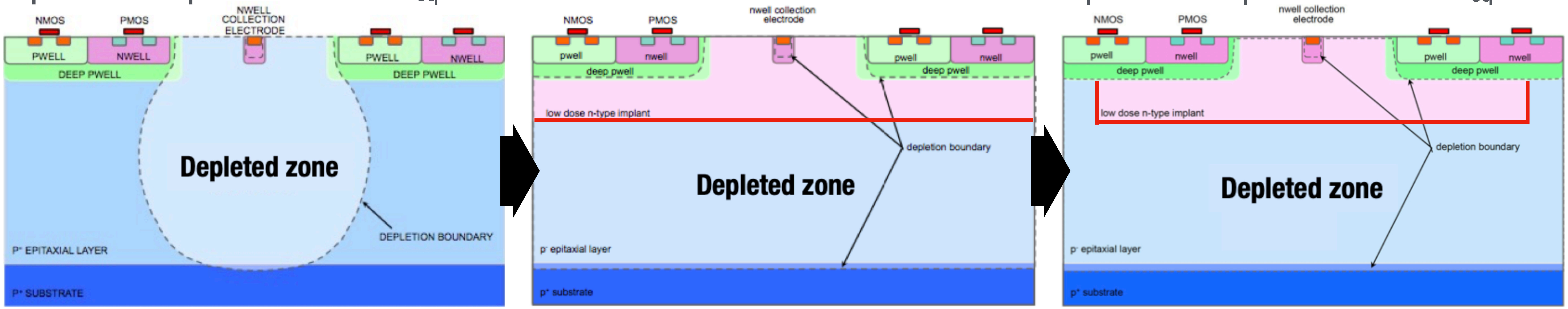
not to scale!
especially in terms of size
and number of transistors.

MAPS improvements

process optimizations

Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

Fully depleted epitaxial layer
Charge collection time < 1 ns
Operational up to 10^{15} 1 MeV n_{eq}/cm^2



[doi:10.1016/j.nima.2017.07.046]   [doi:10.1088/1748-0221/14/05/C05013]

- Charge collection in MAPS is a combination of:
  - diffusion (slow) in low field regions
  - drift (fast) in high field regions (i.e. in the “depleted zone”)
- Doping profiles of MAPS have been repeatedly improved to:
  - reach full depletion
  - direct the field lines towards the collection electrodes
- Resulted in significant improvements of:
  - radiation hardness
  - charge collection speed
- This optimization continues:
  - lower capacitance
  - even higher radiation hardnesses

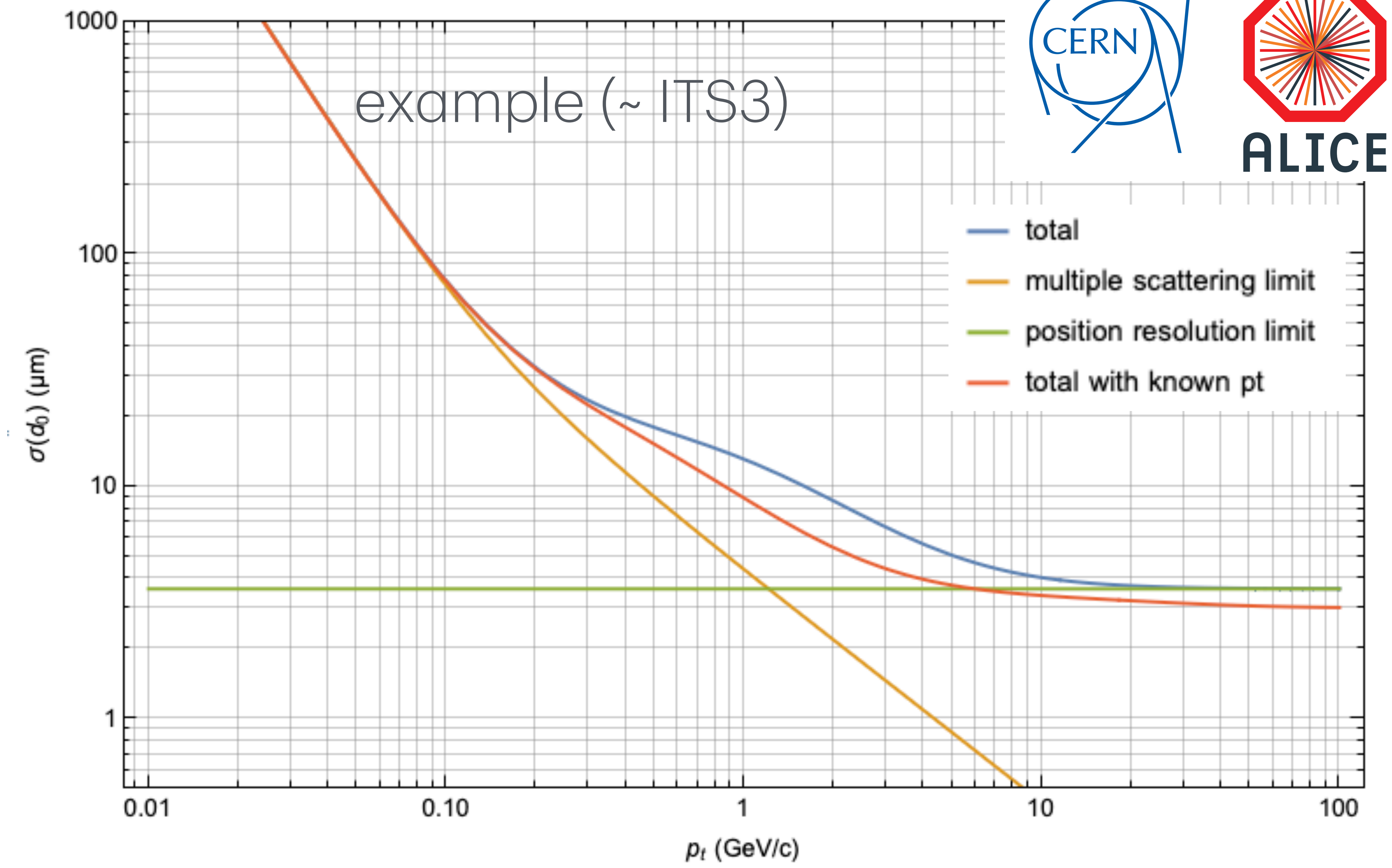
Key concepts

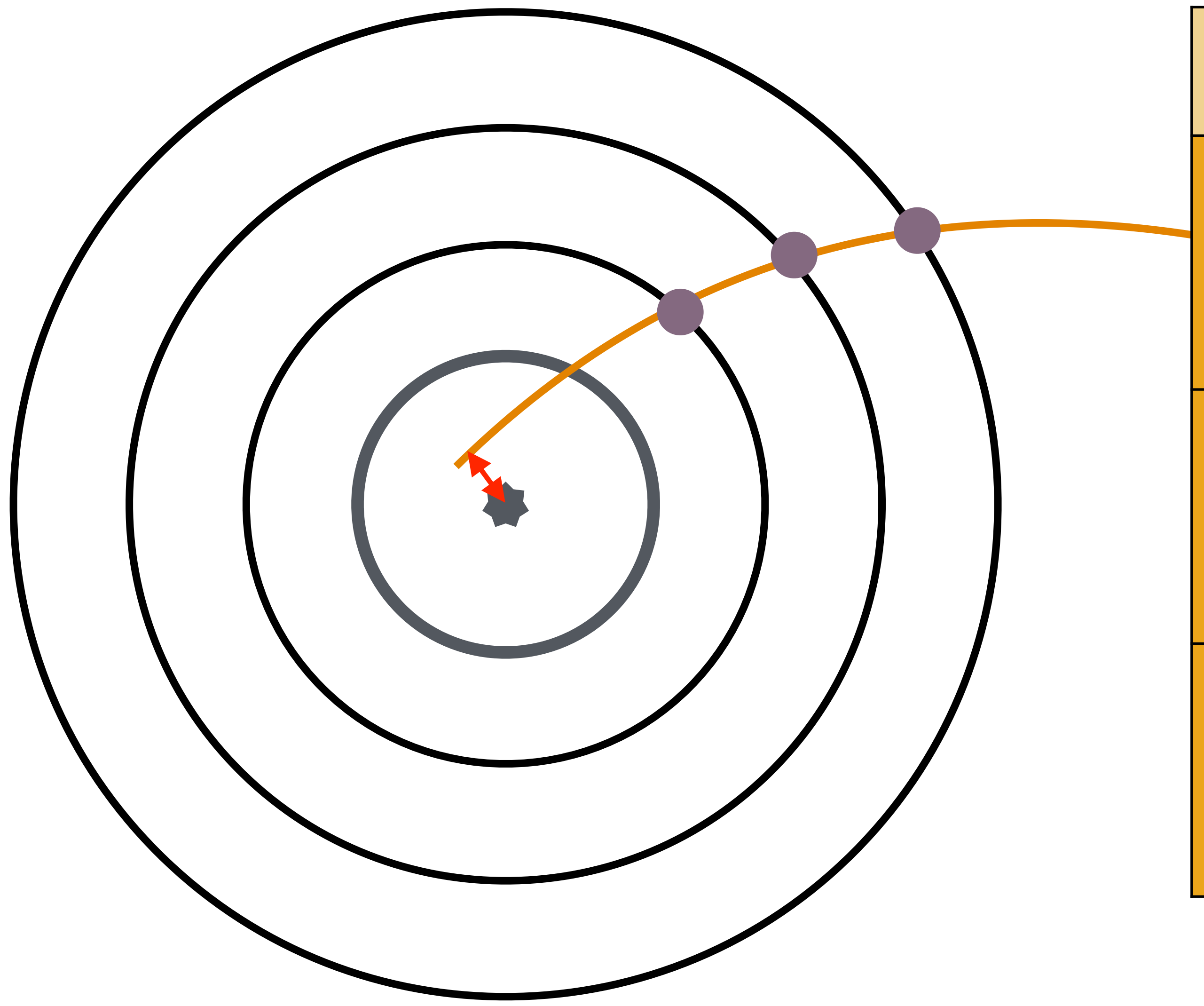
resolution, material budget

- Tracking and vertexing is based on finding *and* extrapolation of tracks

- **Performance figures**
  - impact parameter resolution
  - momentum resolution
  - readout rate ("time resolution")
  - tracking efficiency

- **Three key contributions**
  - material budget
  - distance to interaction point
  - intrinsic sensor position resolution
  - (intrinsic detector efficiency)





Limit	Momentum	Pointing
	$\frac{\Delta p_t}{p_t}$	$\Delta d_{0,xy}$
sensor resolution	$\propto \frac{\sigma p_t}{BL^2}$	$\propto r_0\sigma$
material budget	$\propto \frac{1}{\beta BL}\sqrt{x/X_0}$	$\propto \frac{r_0}{\beta p_t}\sqrt{x/X_0}$

more info: [doi:10.1016/j.nima.2018.08.078]

Starting points

STAR PXL [doi:10.1016/j.nima.2018.03.003]

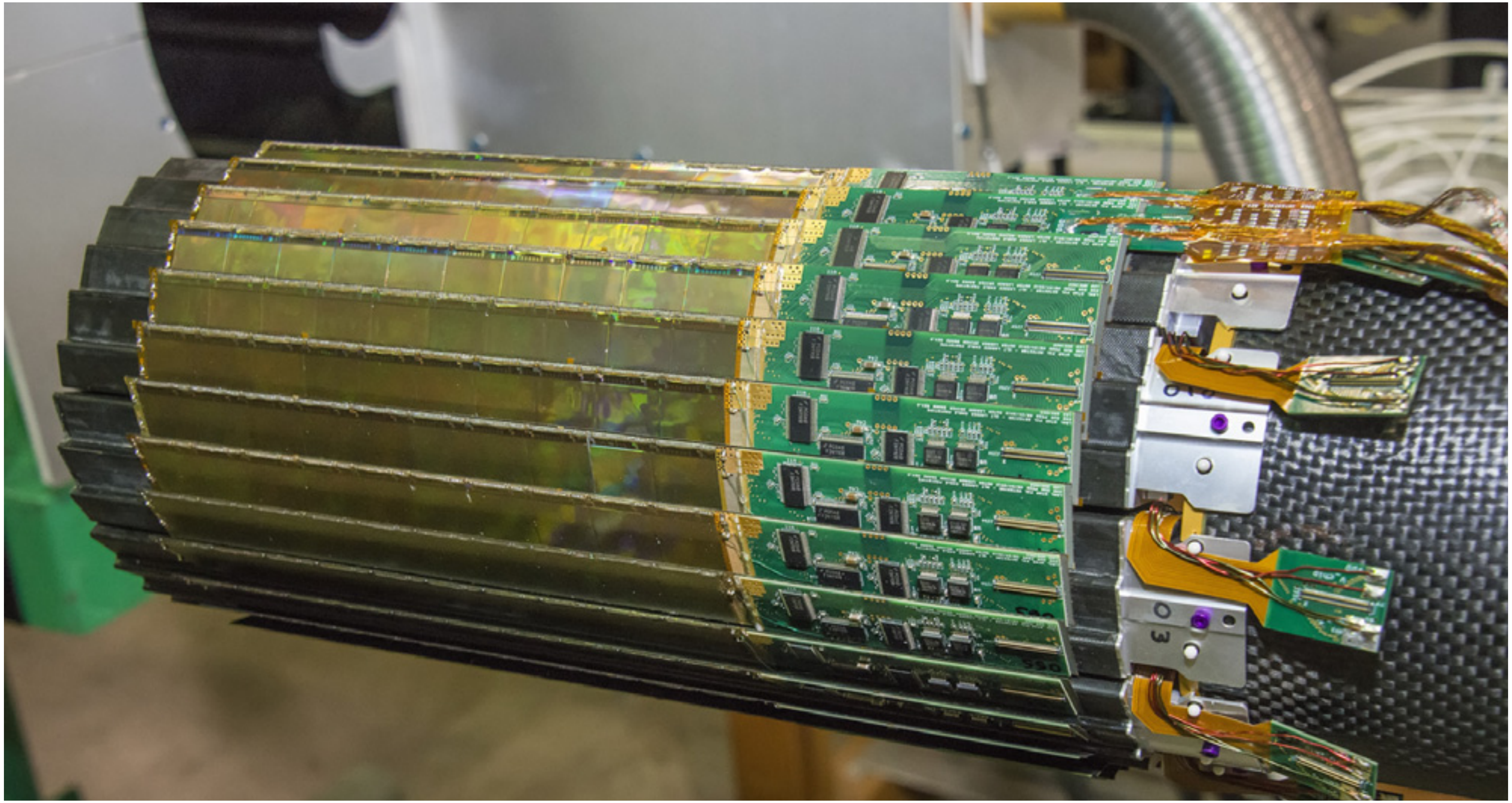
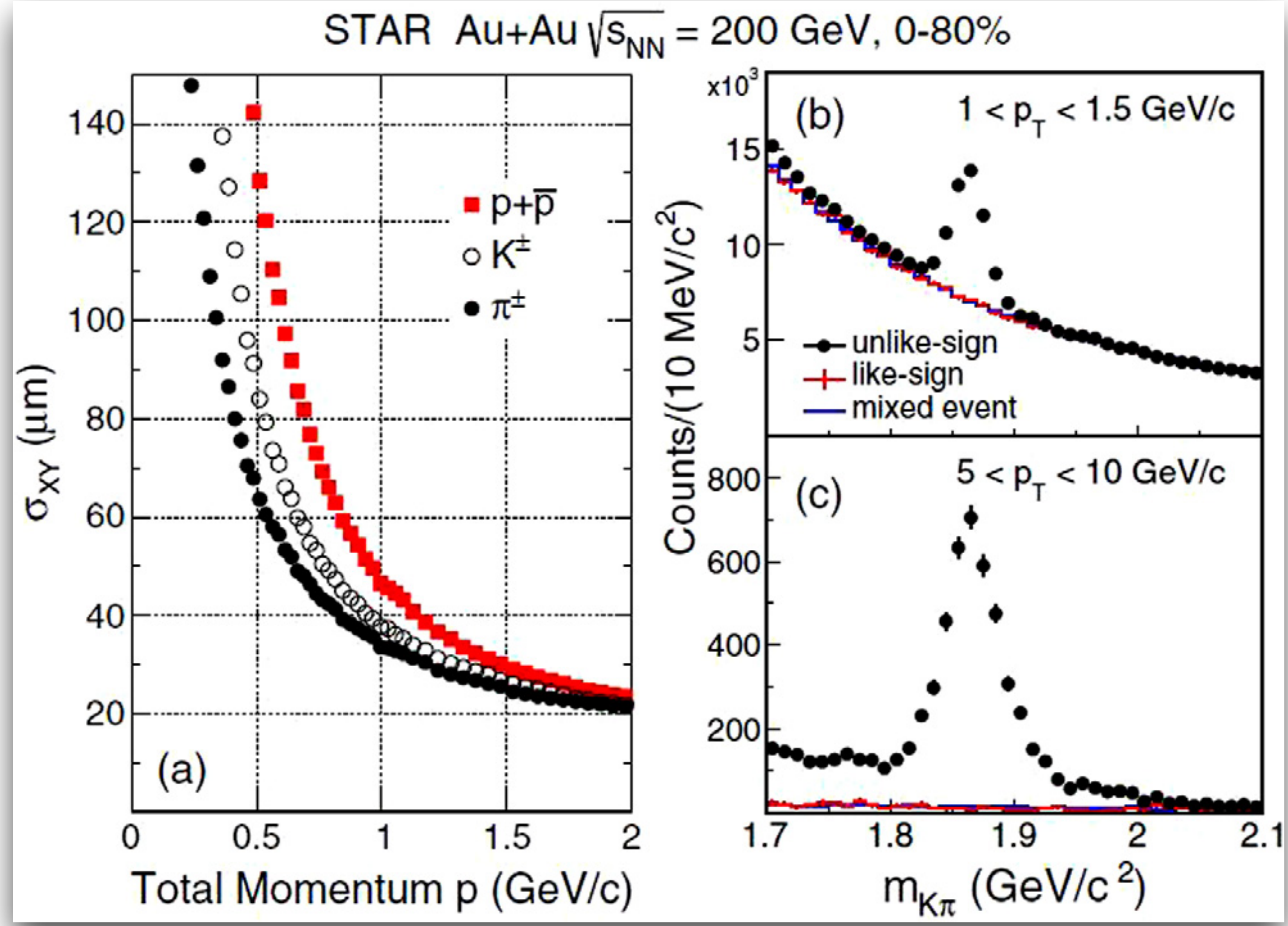
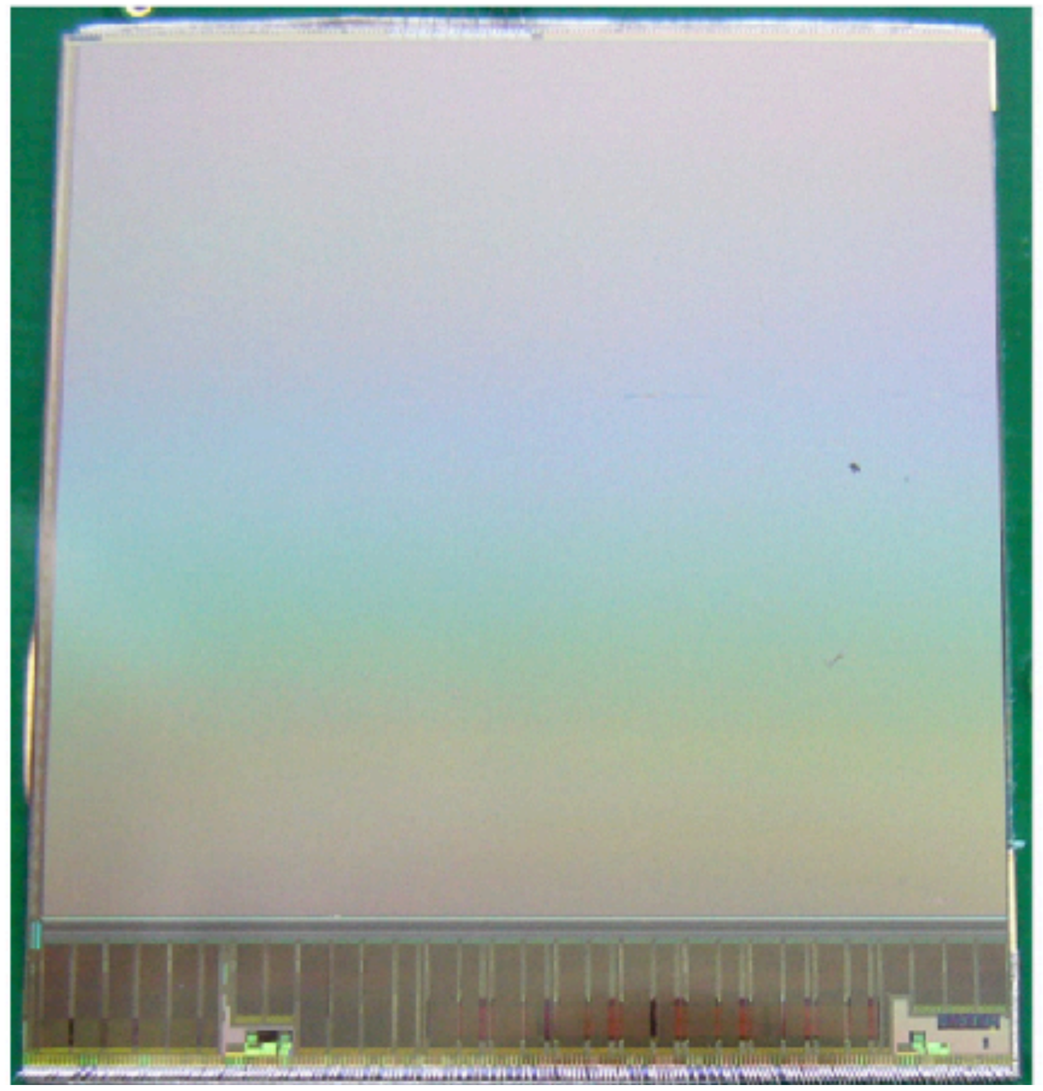


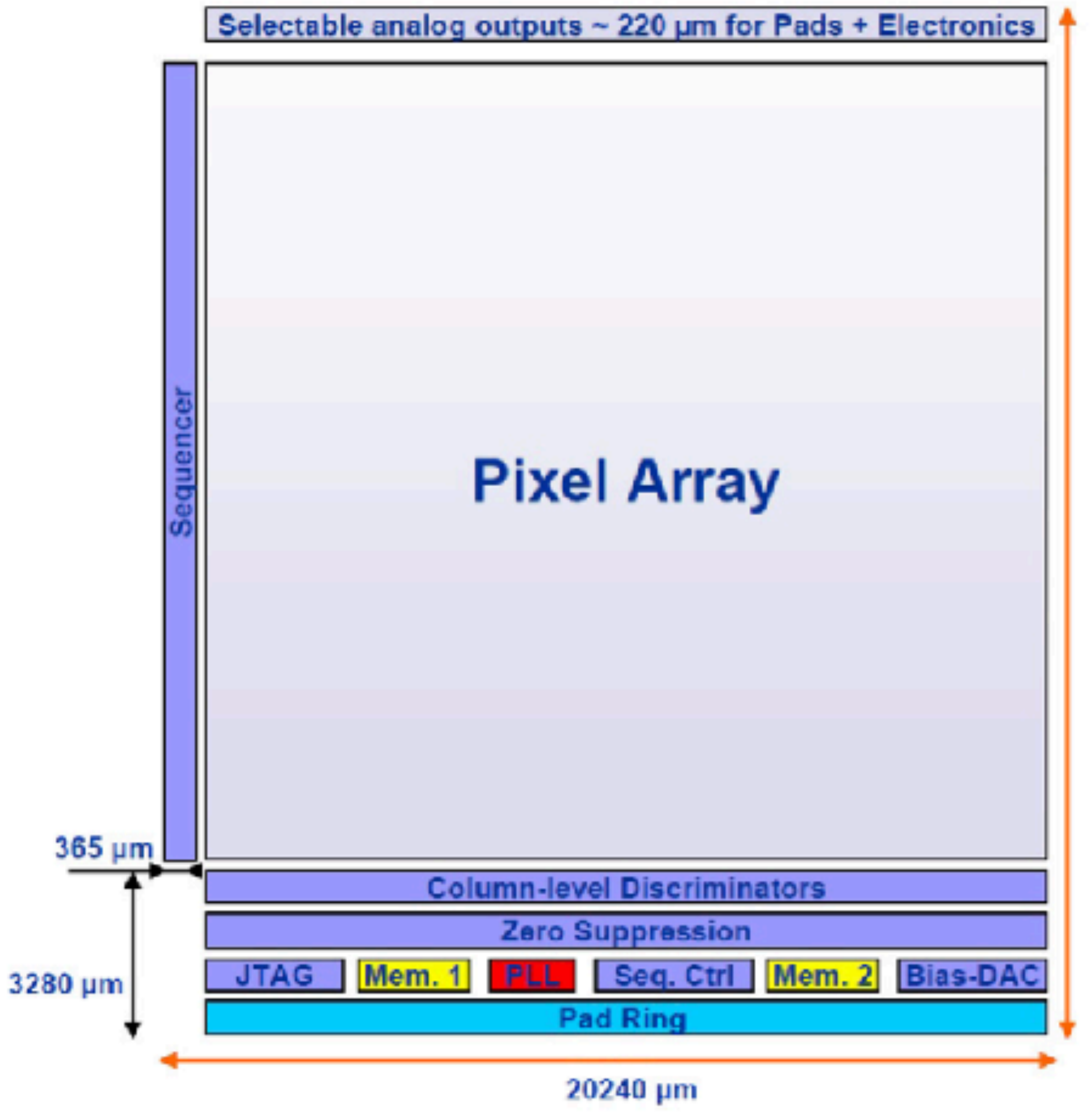
Fig. 1. The HFT PXL detector (*photography by Roy Kaltschmidt - Berkeley Lab*).

STAR HFT PXL
overview

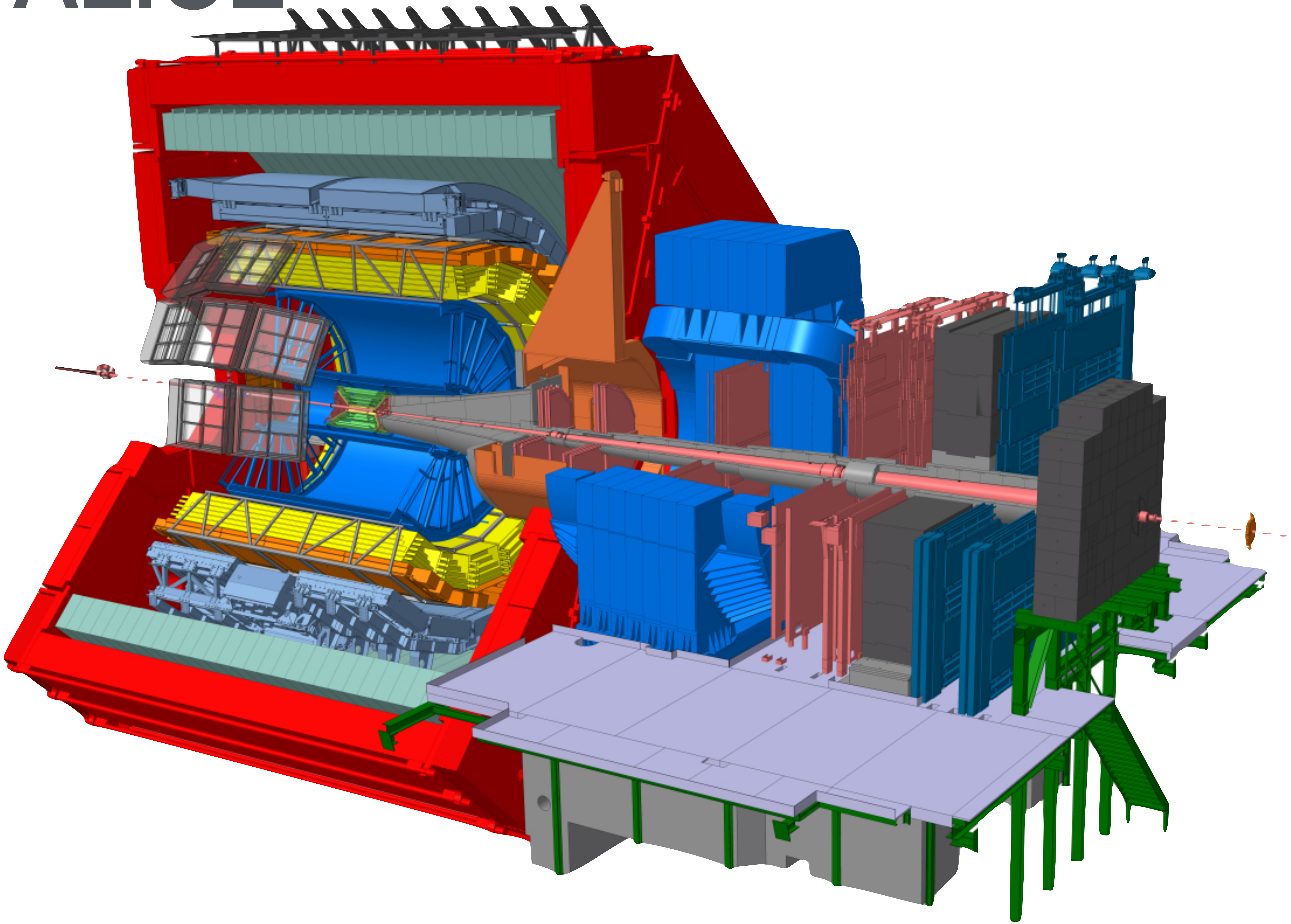
- **First application in HEP**
- Based the Ultimate 2 chip (aka Mimosa28)
  - 0.35 µm technology
  - twin-well process
  - 150 mW/cm²
- 400 sensors
- 2 layers
- 0.16 m²
- 356 MPixel





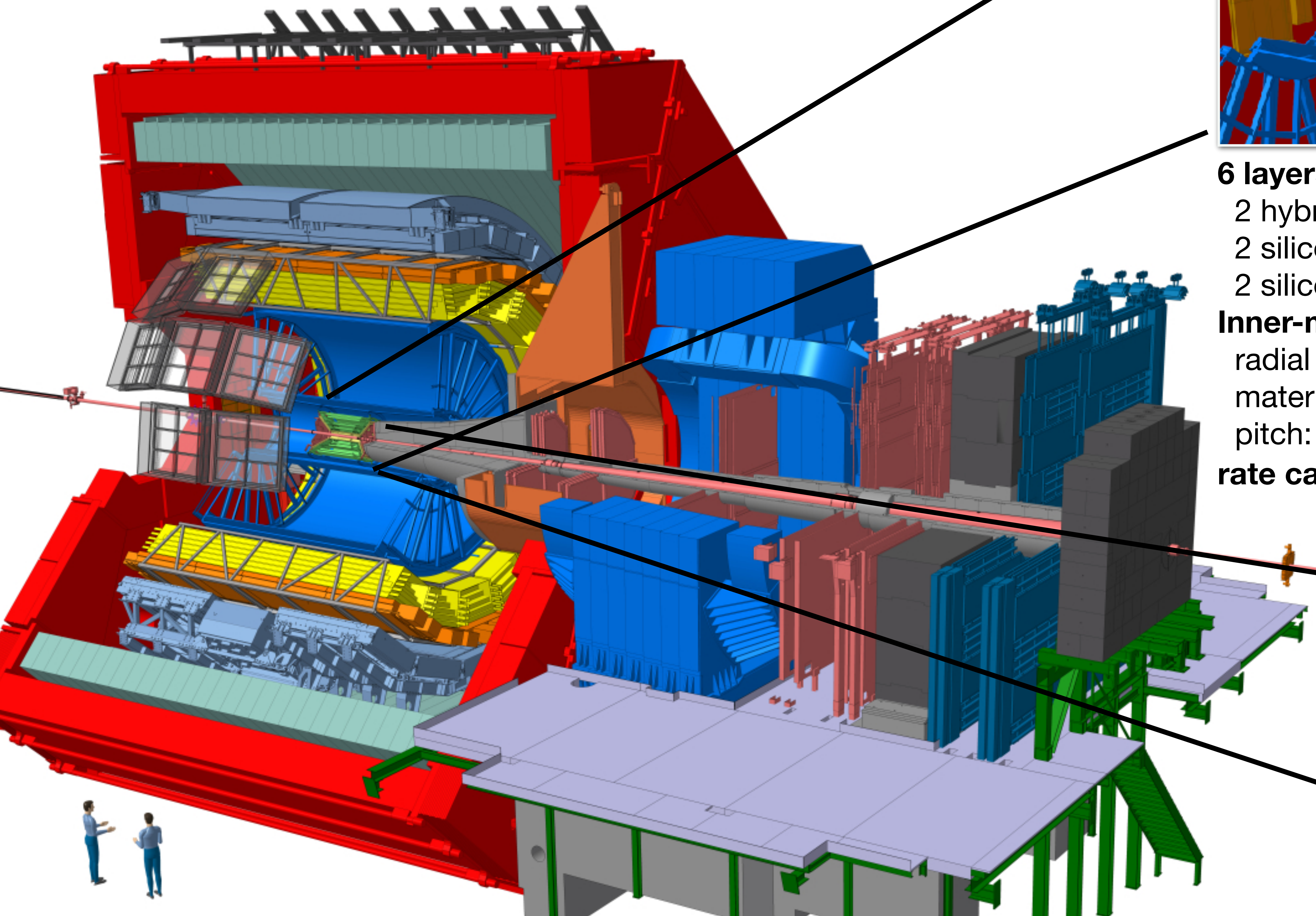


ALICE

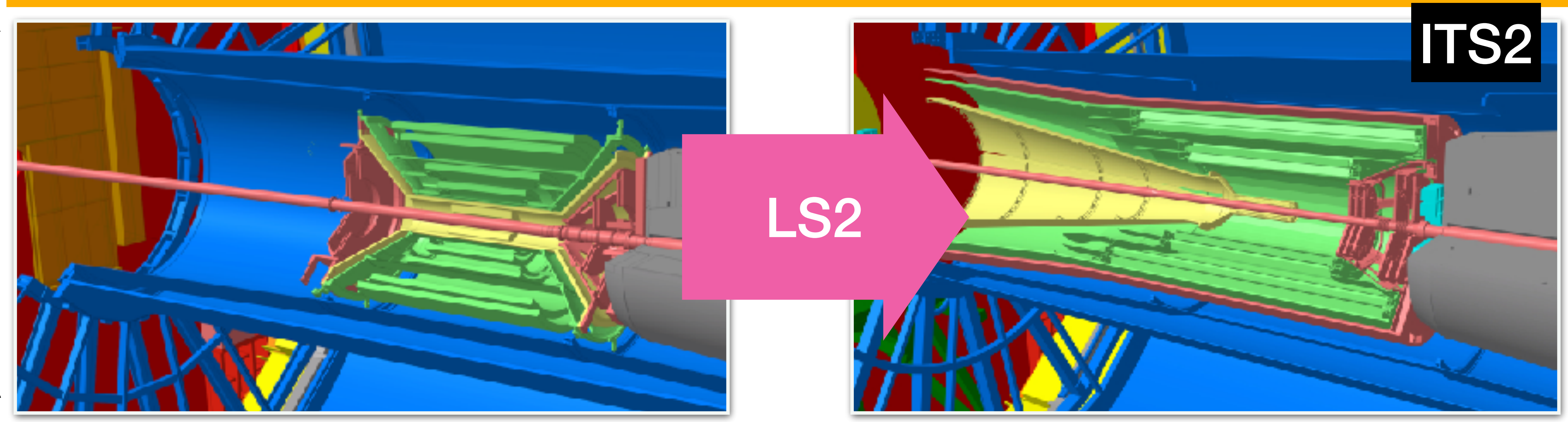


- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to *O*(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum (≲1 GeV/c) particle reconstruction

ALICE ITS2 upgrade (done)



Inner Tracking System

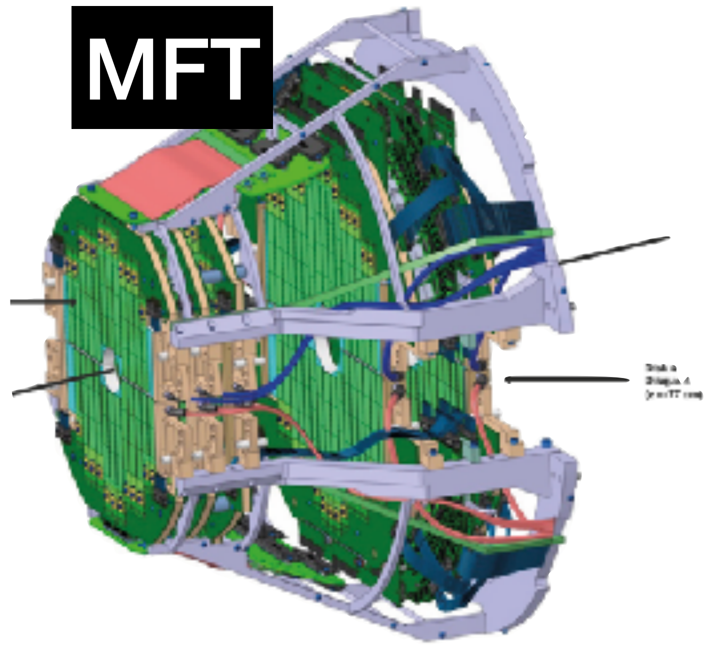


6 layers:
2 hybrid silicon pixel
2 silicon drift
2 silicon strip
Inner-most layer:
radial distance: 39 mm
material: $X/X_0 = 1.14\%$
pitch: $50 \times 425\ \mu m^2$
rate capability: 1 kHz

7 layers:
all MAPS
10 m², 24k chips, 12.5 Giga-Pixels

Inner-most layer:
radial distance: 23 mm
material: $X/X_0 = 0.36\%$
pitch: $29 \times 27\ \mu m^2$
rate capability: 100 kHz (Pb-Pb)

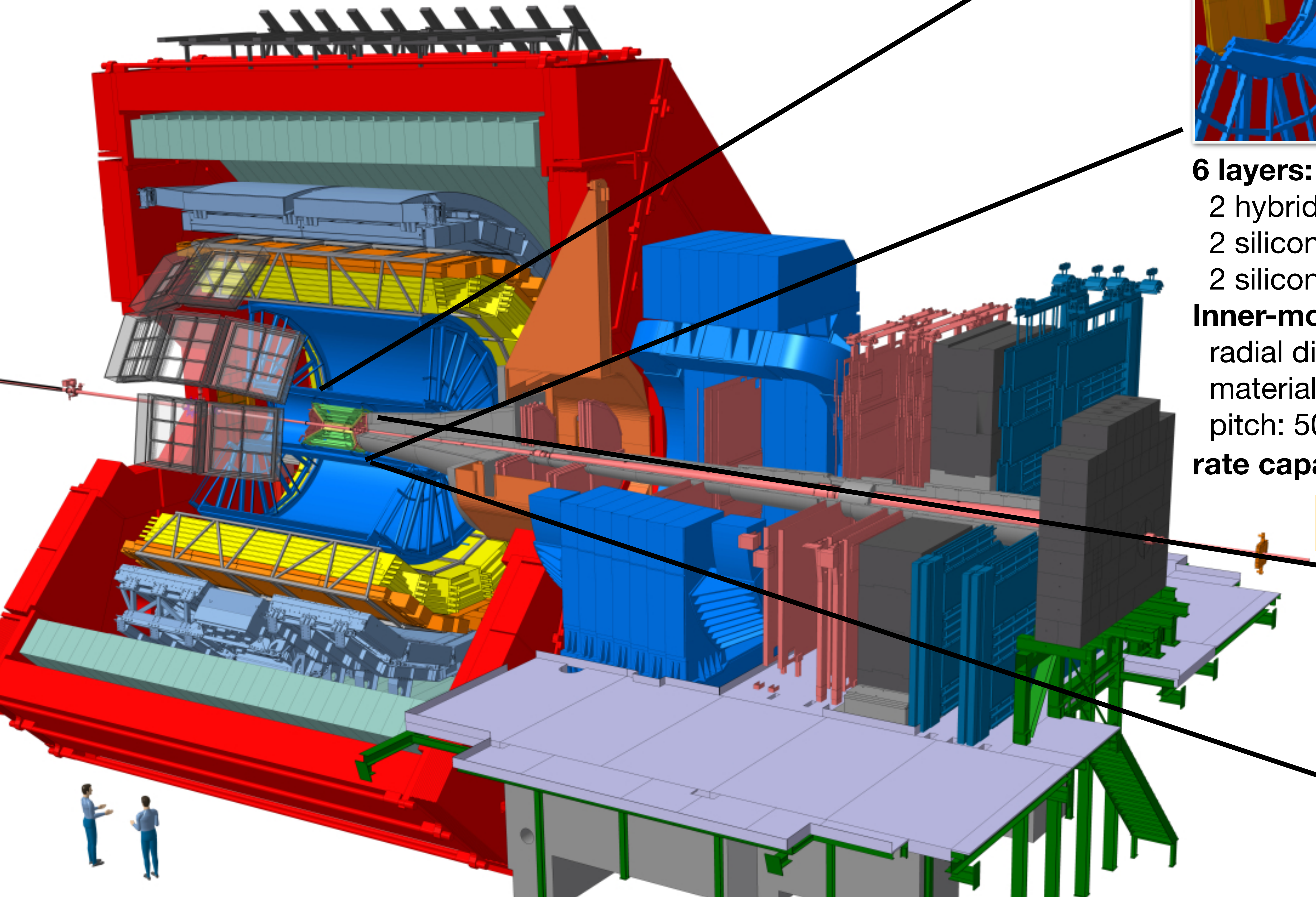
Muon Forward Tracker

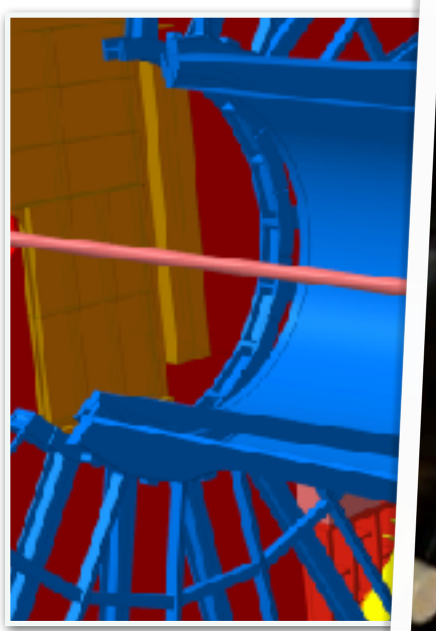


new detector

5 discs, double sided:
based on same technology as ITS2

ALICE ITS2 upgrade (do





6 layers:
2 hybrid sili
2 silicon dri
2 silicon str
Inner-most
radial dista
material: X/
pitch: 50 ×
rate capabi

TS2

ITS2 chip development roadmap

2012	Explorer	• study of technology • detection diode geometry • starting materials • radiation hardness
2013	pALPIDEss	• digital front-end • priority-encoder readout
May 2014	pALPIDE-1	• full-scale sensor • simplified interface
Apr 2015	pALPIDE-2	• chip-chip communication interface • module integration • *slow-speed serial link*
Oct 2015	pALPIDE-3	• multiple-hit memory, final interfaces • last optimisation of pixel • *high-speed serial link (jitters)*
Aug 2016	**ALPIDE**	• final chip

One needs a number of prototypes, especially of large scale (sensor+readout on same chip)

The ALPIDE chip

the state of the art Monolithic Active Pixel Sensor (180 nm)

> 70k chips produced and tested

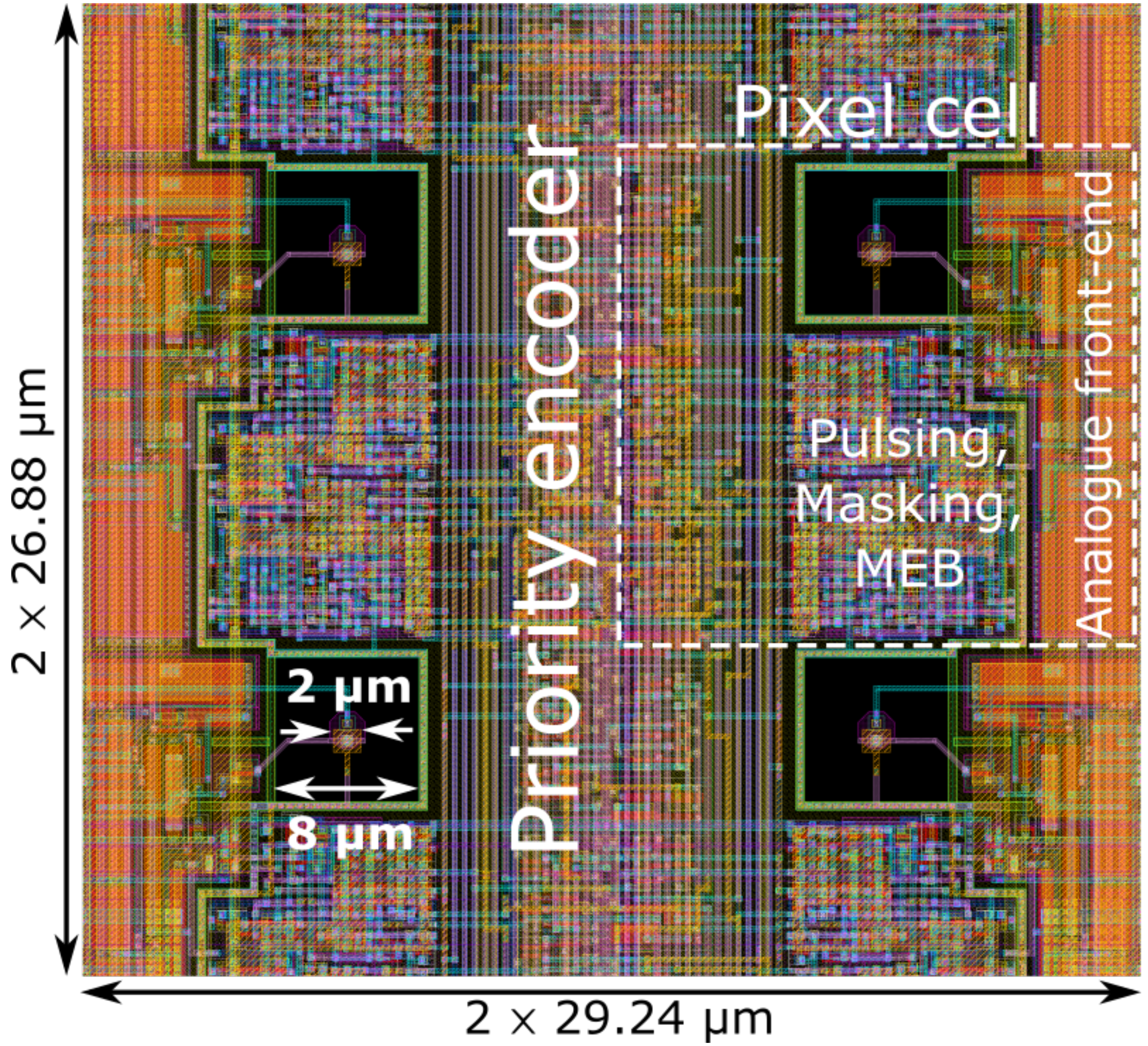
24k in continuous operation in ALICE

+ several other applications

Parameter	Req.	ALPIDE
Spatial resolution (µm)	≈ 5	≈ 5
Integration time (µs)	< 30	< 10
Fake-hit rate (/pixel/event)	< 10^{-6}	<< 10^{-6}
Detection efficiency	> 99%	>>99%
Power density (mW/cm²)	< 100	< 48
TID (krad)	> 270 (IB)	OK
NIEL (1 MeV n_{eq} / cm²)	> 1.7×10^{12}	OK

The ALPIDE chip

pixel matrix

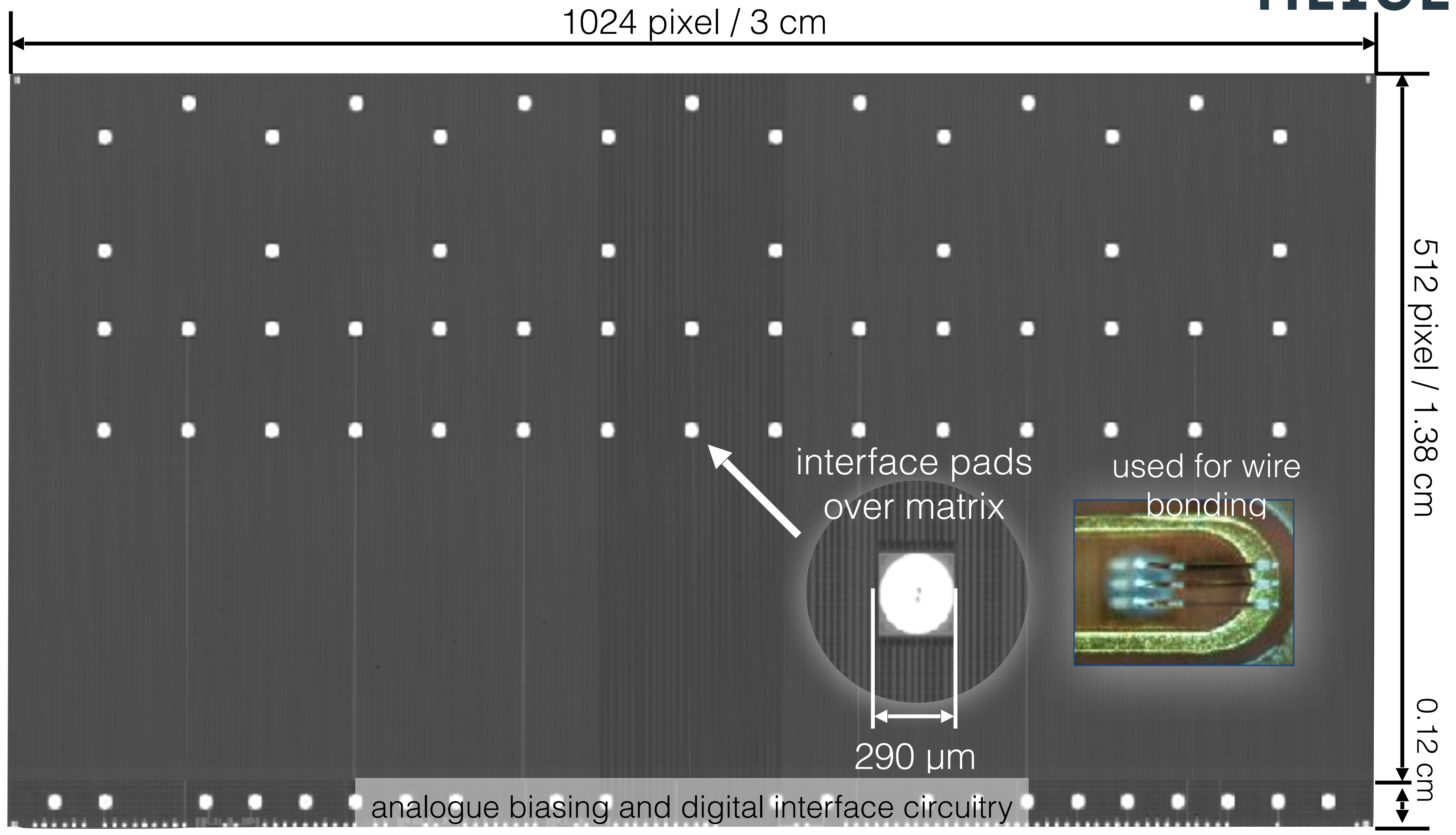


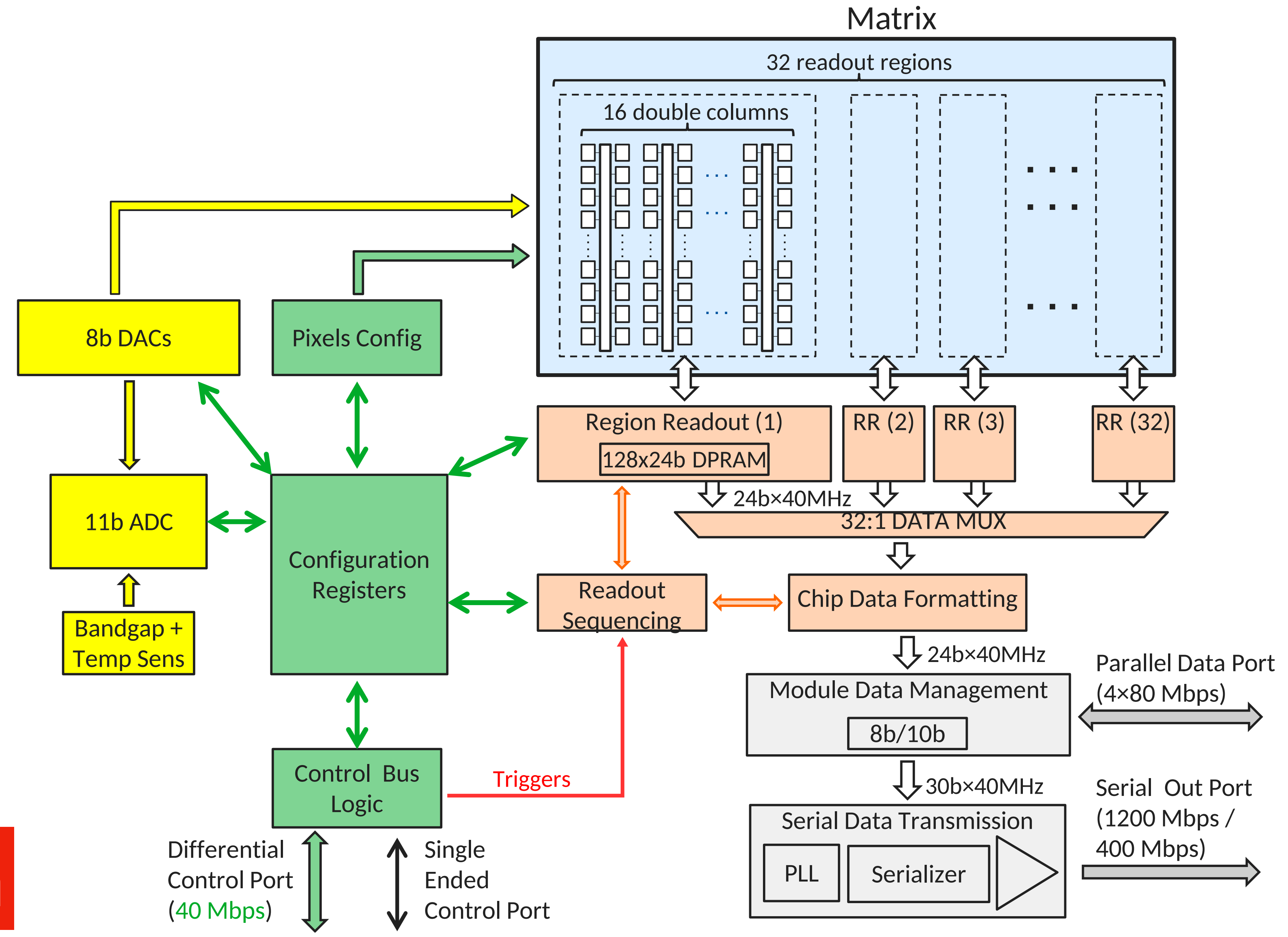
- Very dense integration inside pixel cell
  - amplifier, memories, testing
- Hit driven matrix readout
  - fast (zero skipping)
  - low power (digital information)
- *O*(200) transistors per pixel

The ALPIDE chip

system level aspects

- Takes full advantage of TowerJazz CIS process:
  - 6 metal layers
  - small (180 nm) feature size
  - deep p-well
- Continuously active, in-pixel front-end, asynchronous readout (>100 transistors/pixel)
- Peripheral circuitry for biasing (DAC) and monitoring (ADC)
- On-chip PLL and serialiser to send data directly via 8 m of copper off-detector

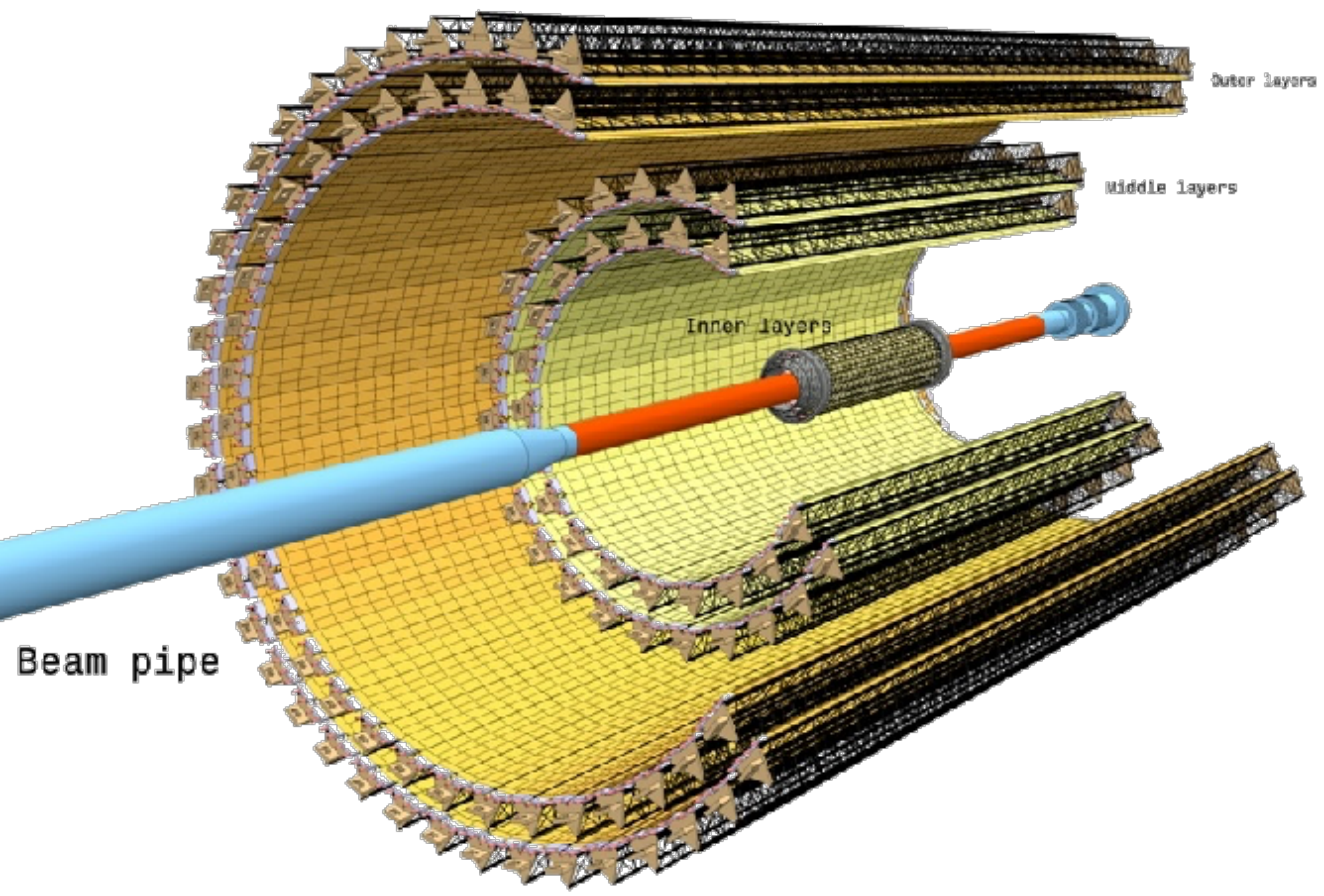




The final chip is much more than the pixel cell times half a million

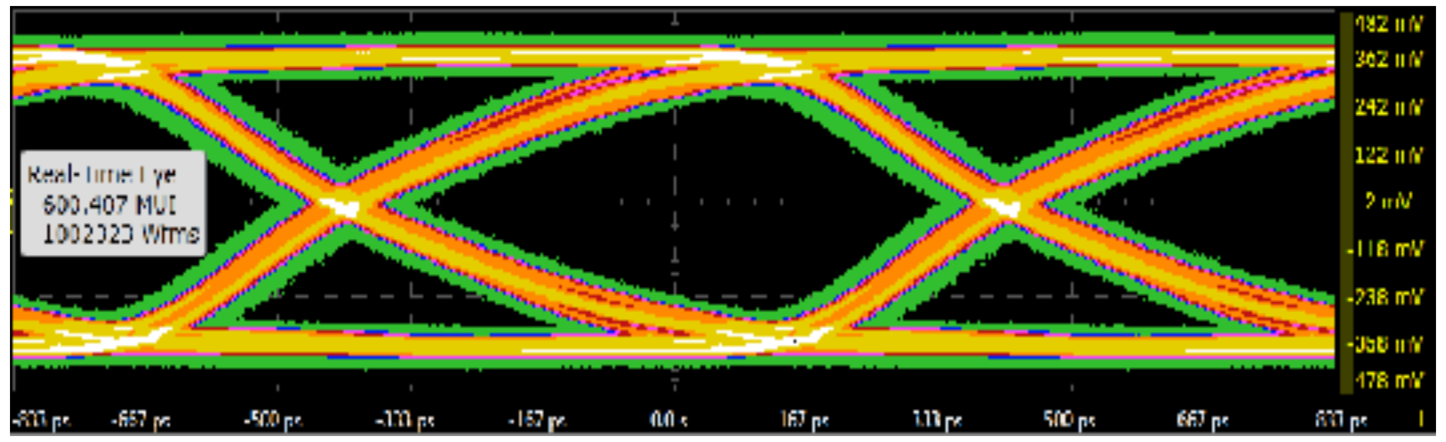
Readout electronics

Detector



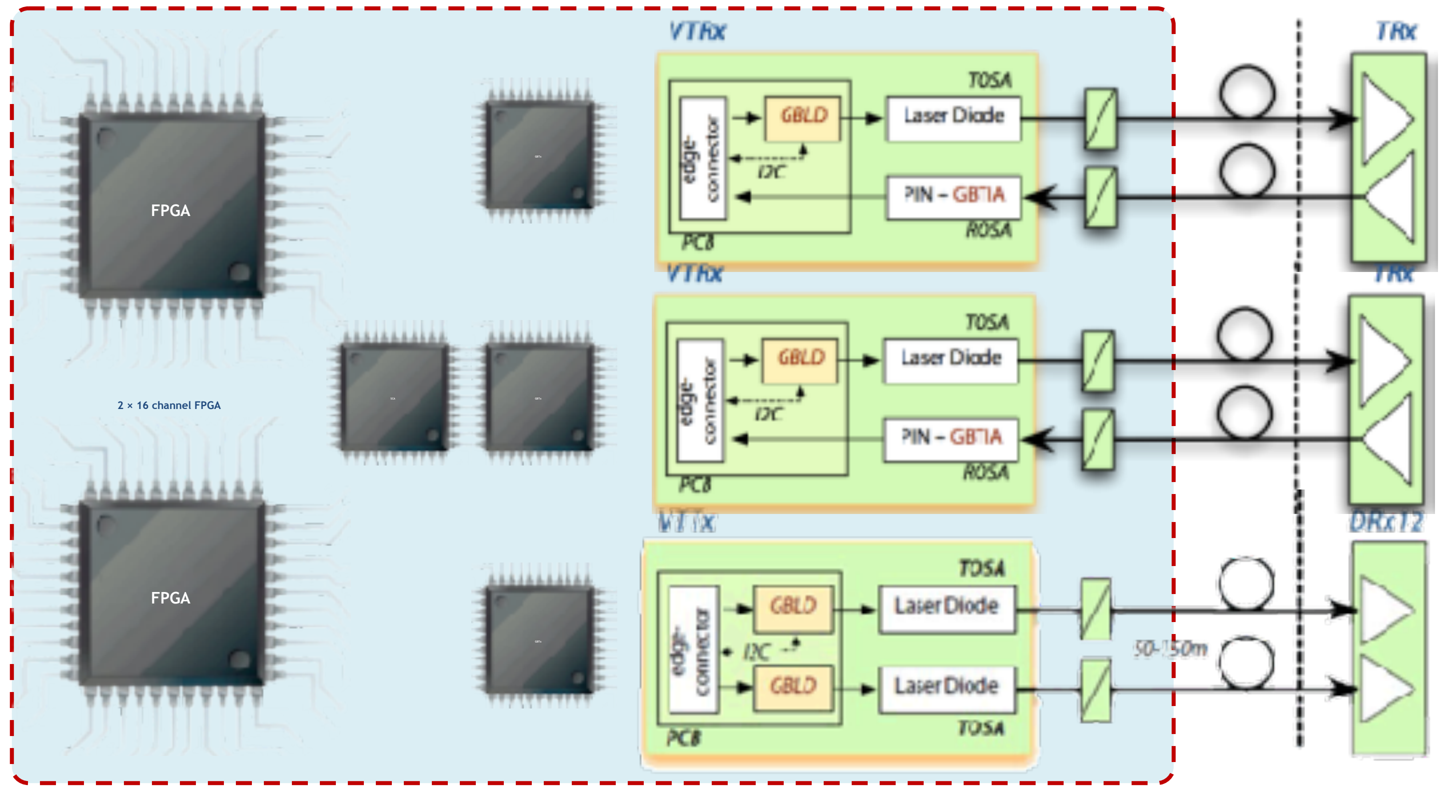
- Readout logic fully integrated into ALPIDE
- ALPIDE can directly drive 8 m cables using integrated high speed transmitters (up to1.2 Gb/s)
- No further electronics on detector

8 m cable



- 1.2 Gb/s (data IB)
- 400 Mb/s (data OB)
- 80 Mb/s (ctrl IB/OB)
- clock
- power

Readout Units

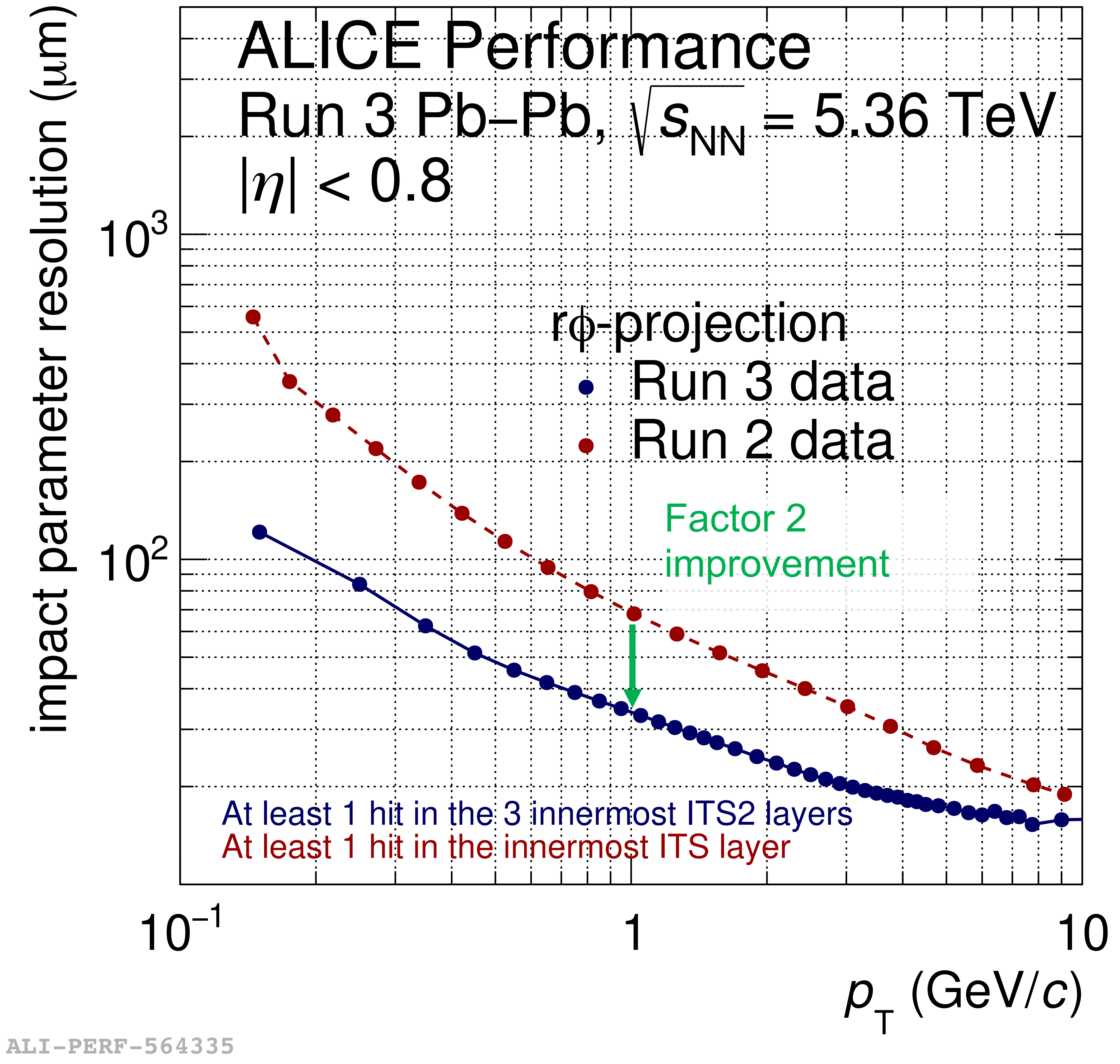


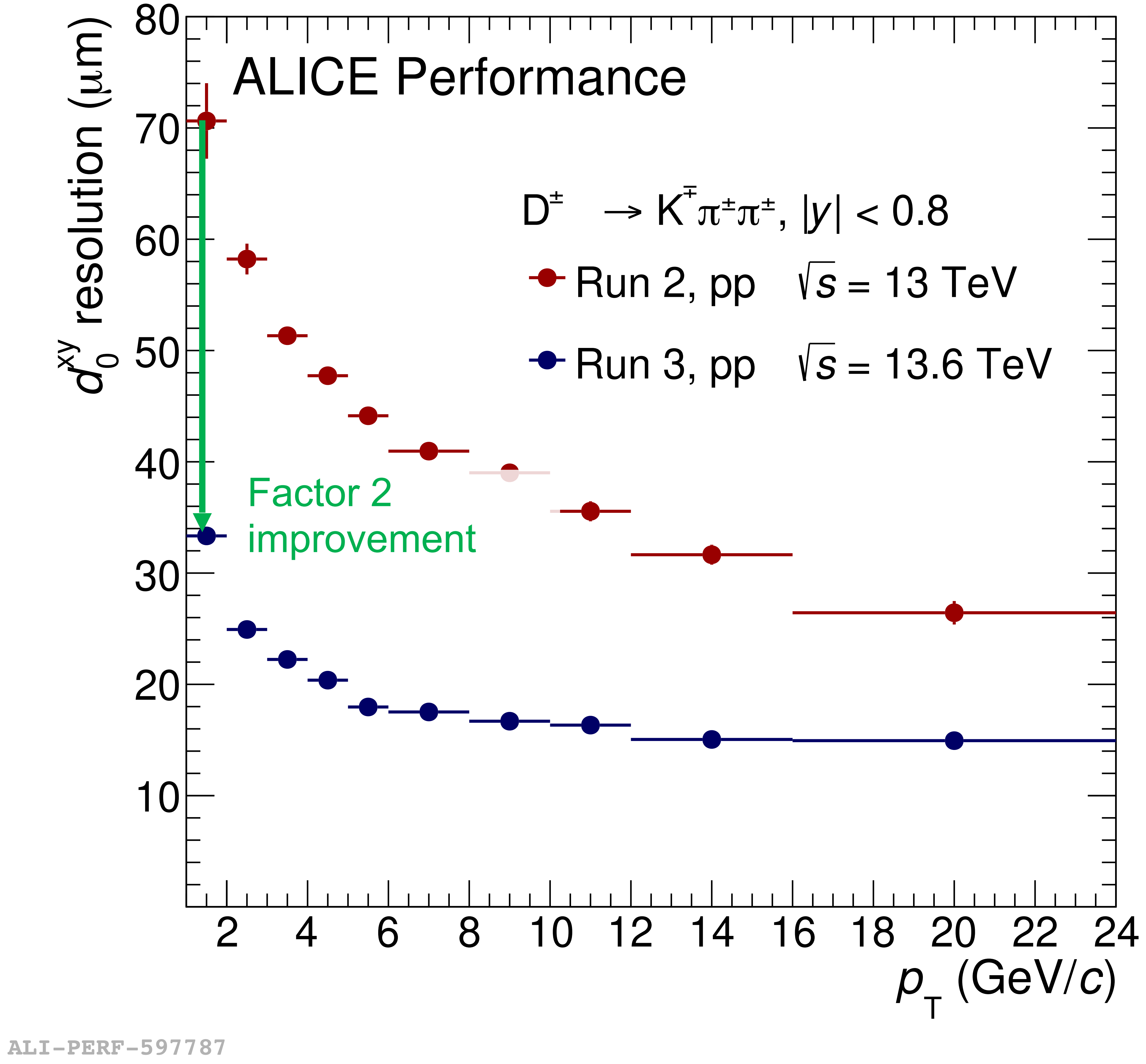
- Total: 192 Readout Units
- Distribute trigger and control signals
- Interface data links to ALICE DAQ
- Control power supply of chips
- Radiation level low enough to use (selected!) off-the-shelf electronics + soft-error mitigation techniques

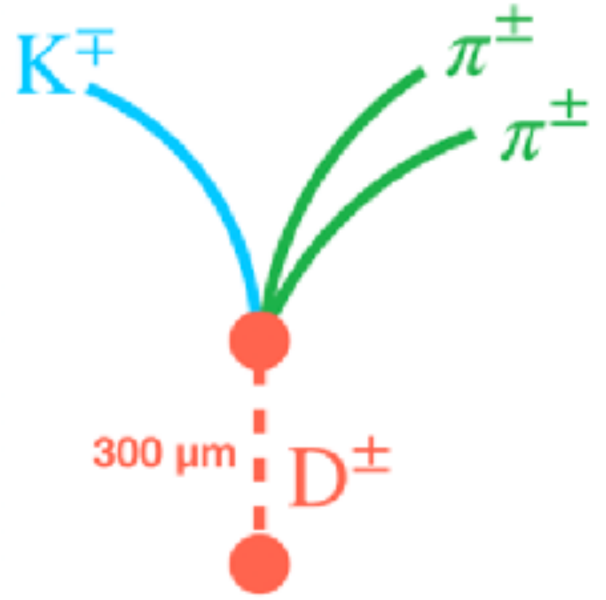
Integration of as much as possible into ALPIDE simplified system
Still, radiation at position of readout unit requires work


ALICE
ALICE
Pb-Pb 5.36 TeV
LHC22s period
18th November 2022
16:52:47.893

Resolution improvement



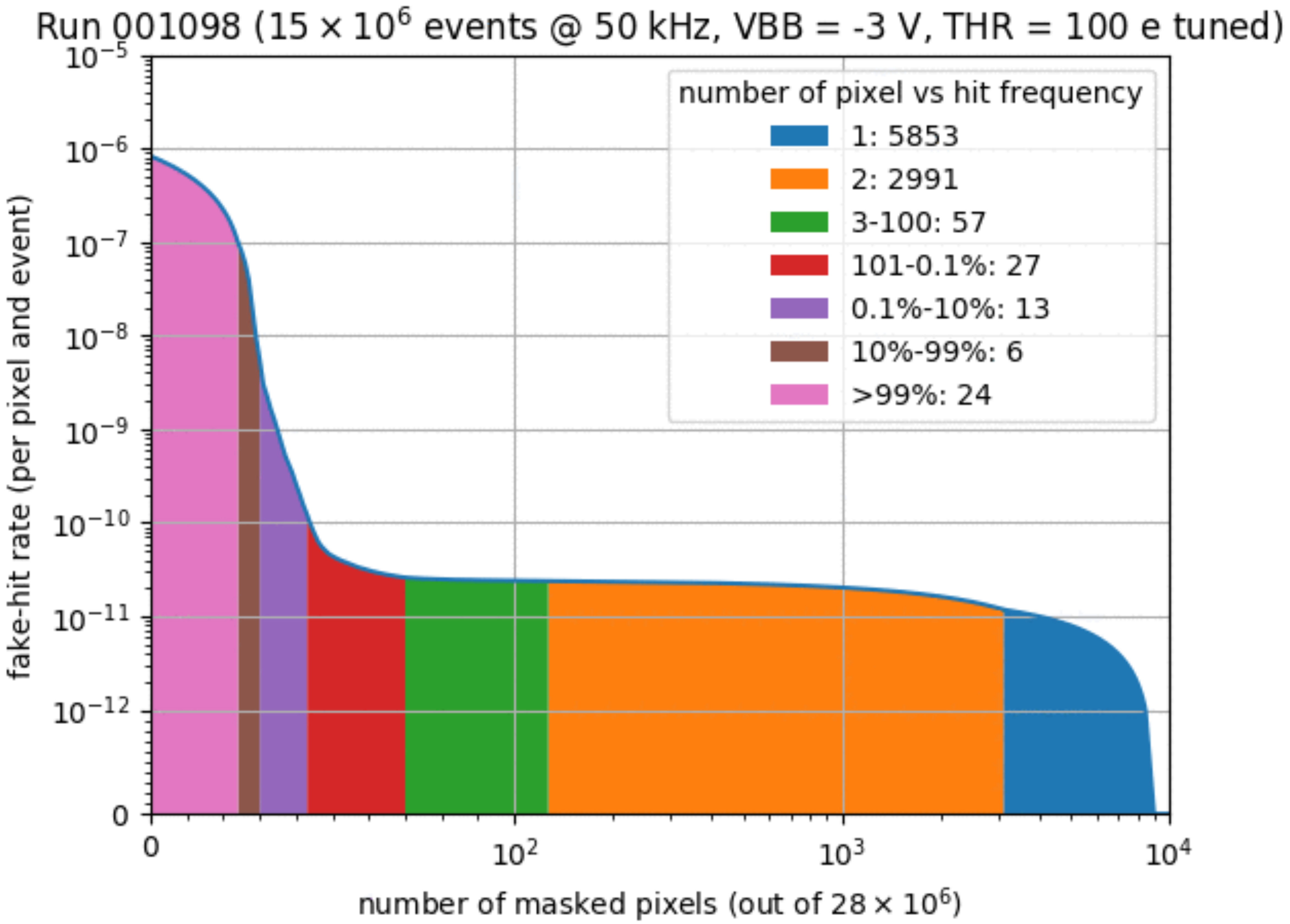




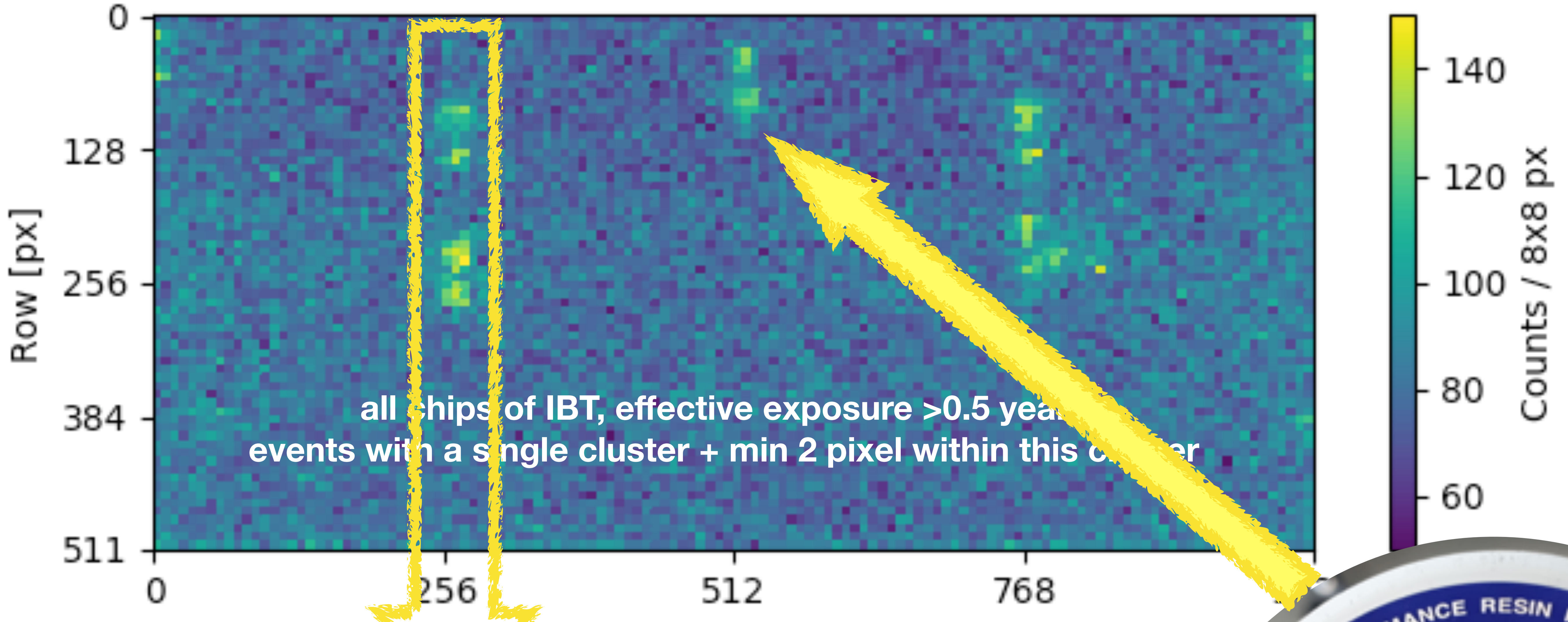
Improved impact parameter resolution for charged tracks and $D^{\pm}$ mesons

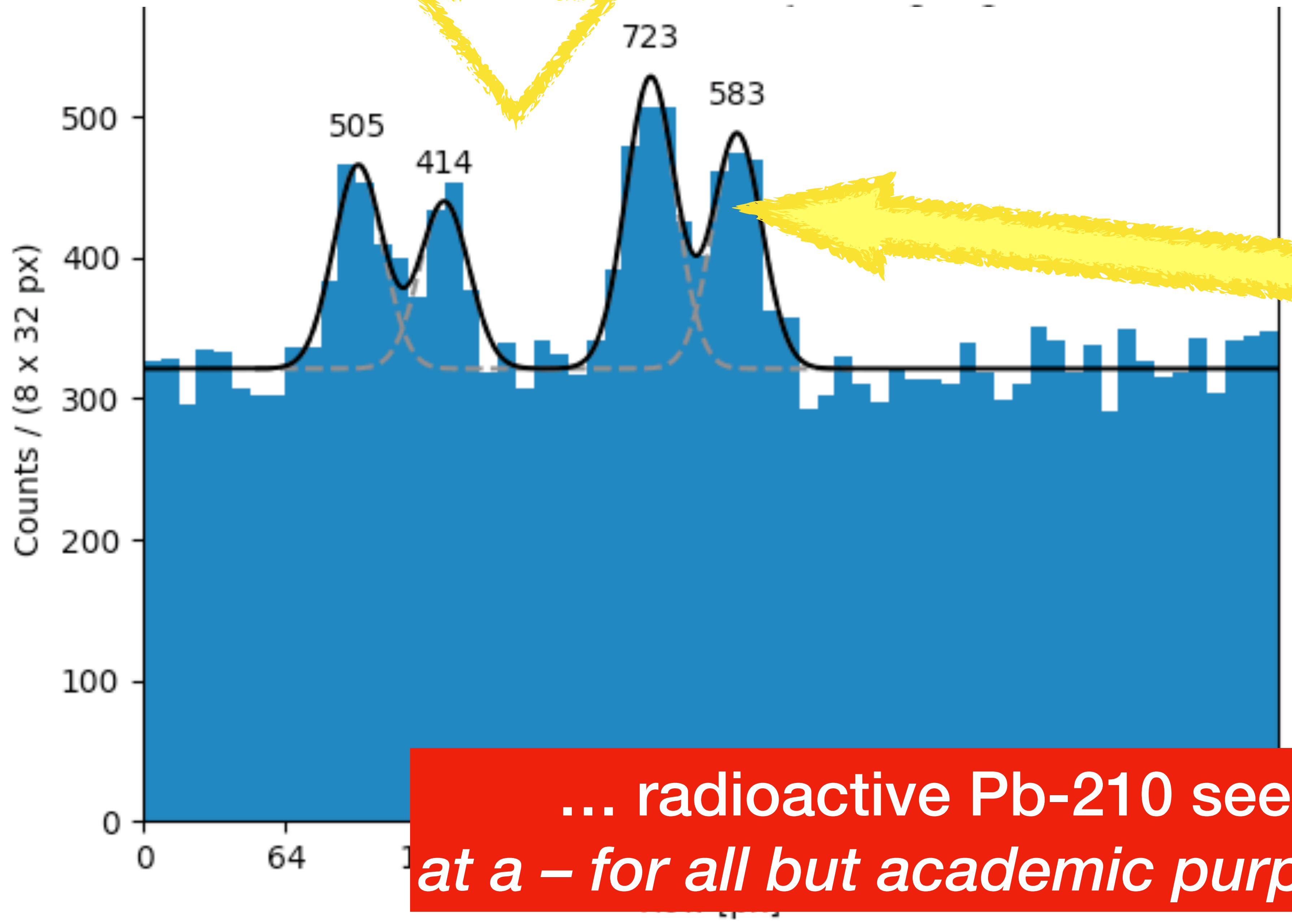
ALICE ITS2

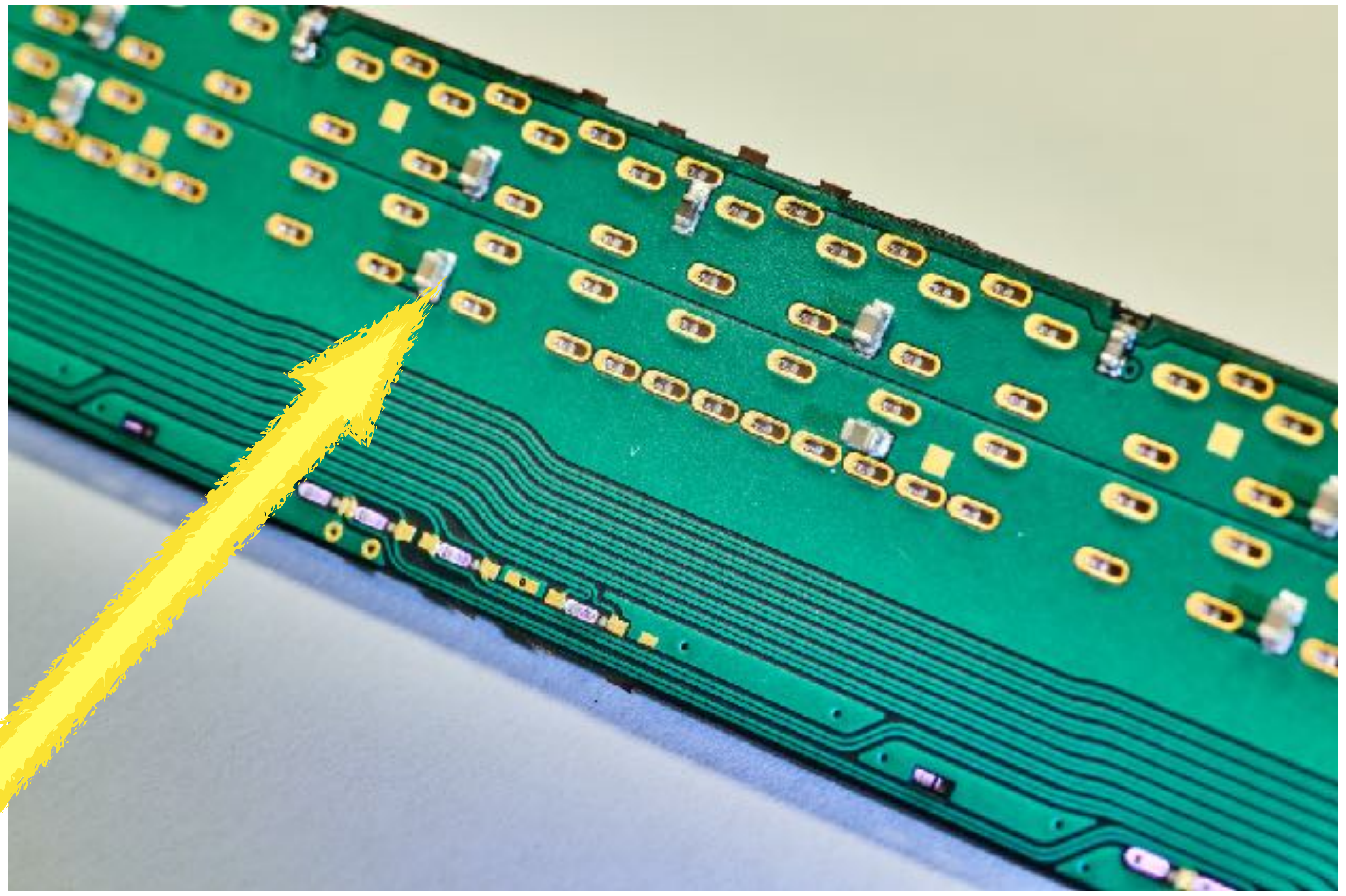
- This is the real rate measured on-detector, including final services
- Essentially, apart from a hand-full pixels per chip, the detector is **noise-free**
- Biggest contributor is natural radiation (which is *not* excluded here)
- Indeed, mitigation of Random Telegraph Signal noise (RTS noise / RTN) was a major achievement in the APIDE R&D

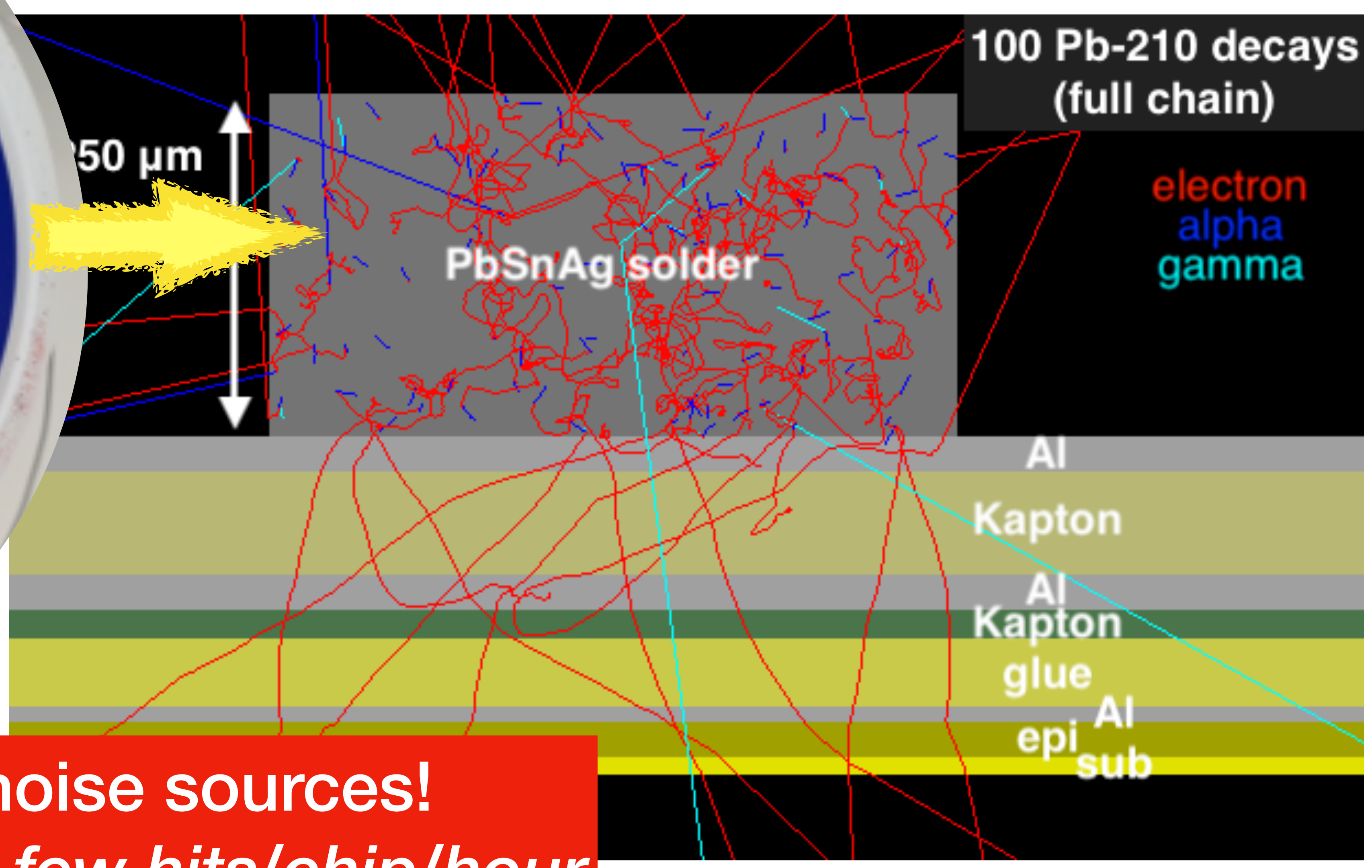


ITS2 performance





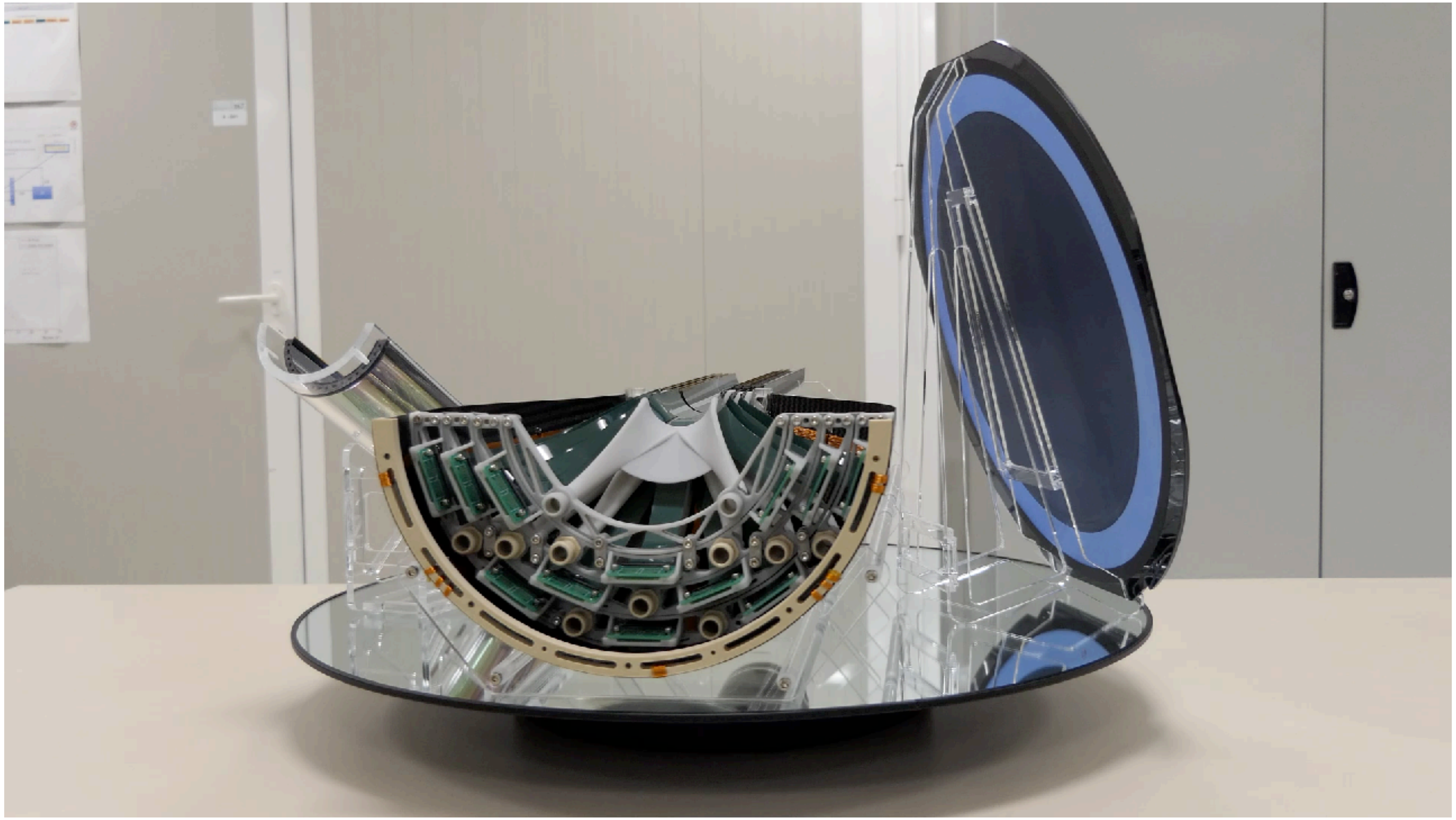




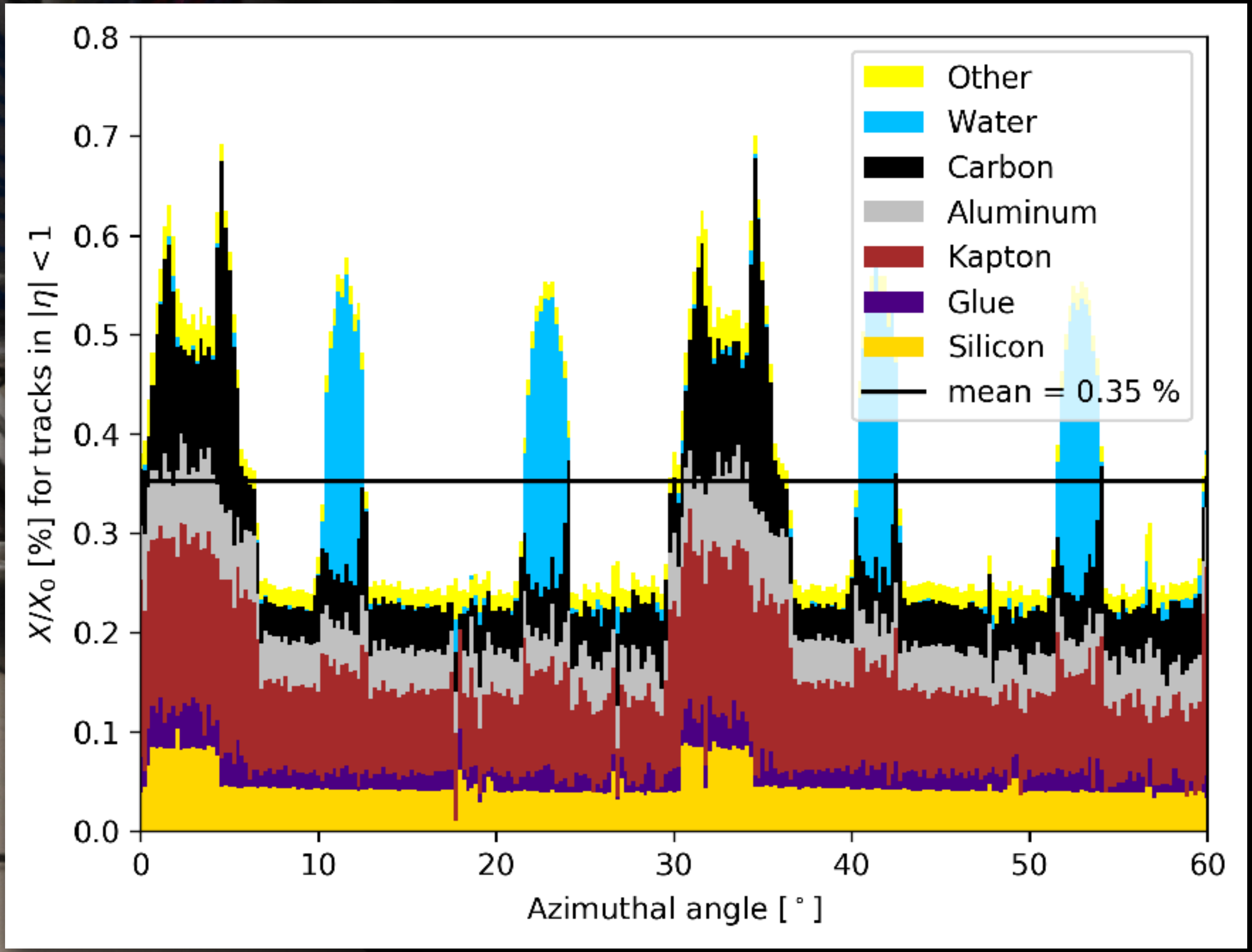
… radioactive Pb-210 seems to be one of the main real noise sources!
at a – for all but academic purposes – negligible rate of totals few hits/chip/hour

[TDR: ALICE-TDR-021]

ITS3



ITS2 Inner Barrel

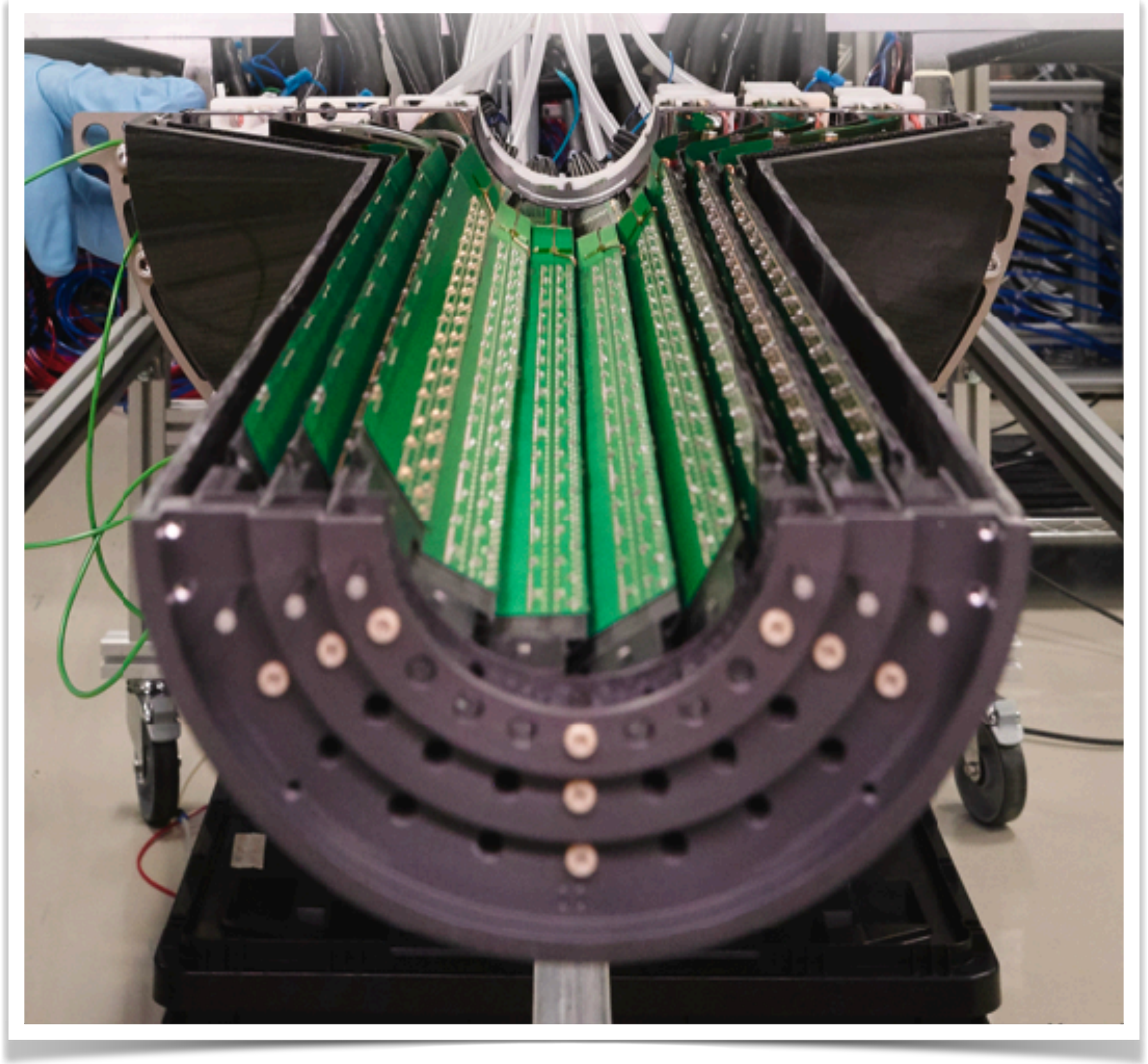


Very light detector (0.35% X0)

Yet, dominated by support structures

ALICE ITS3

conceptional idea

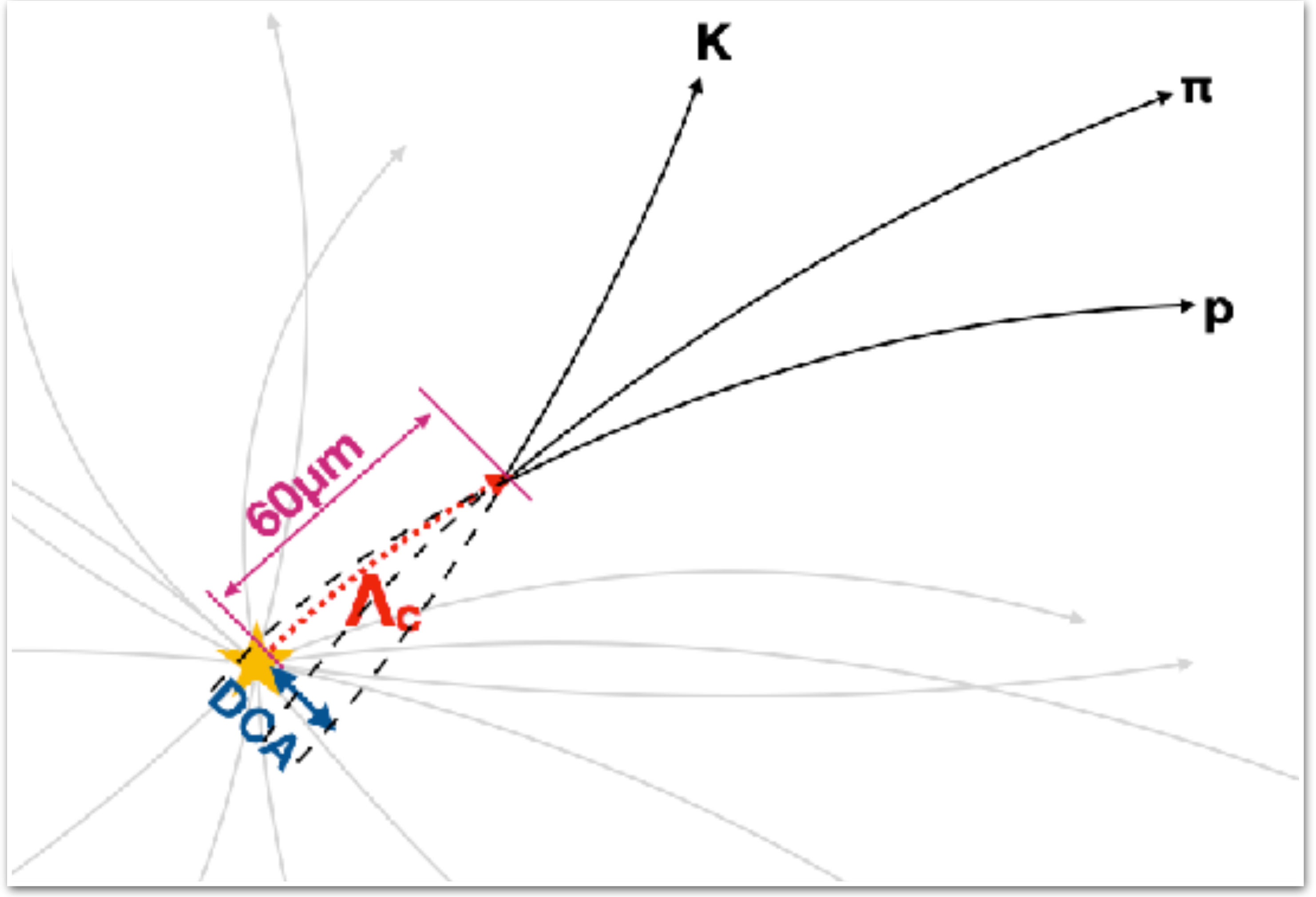


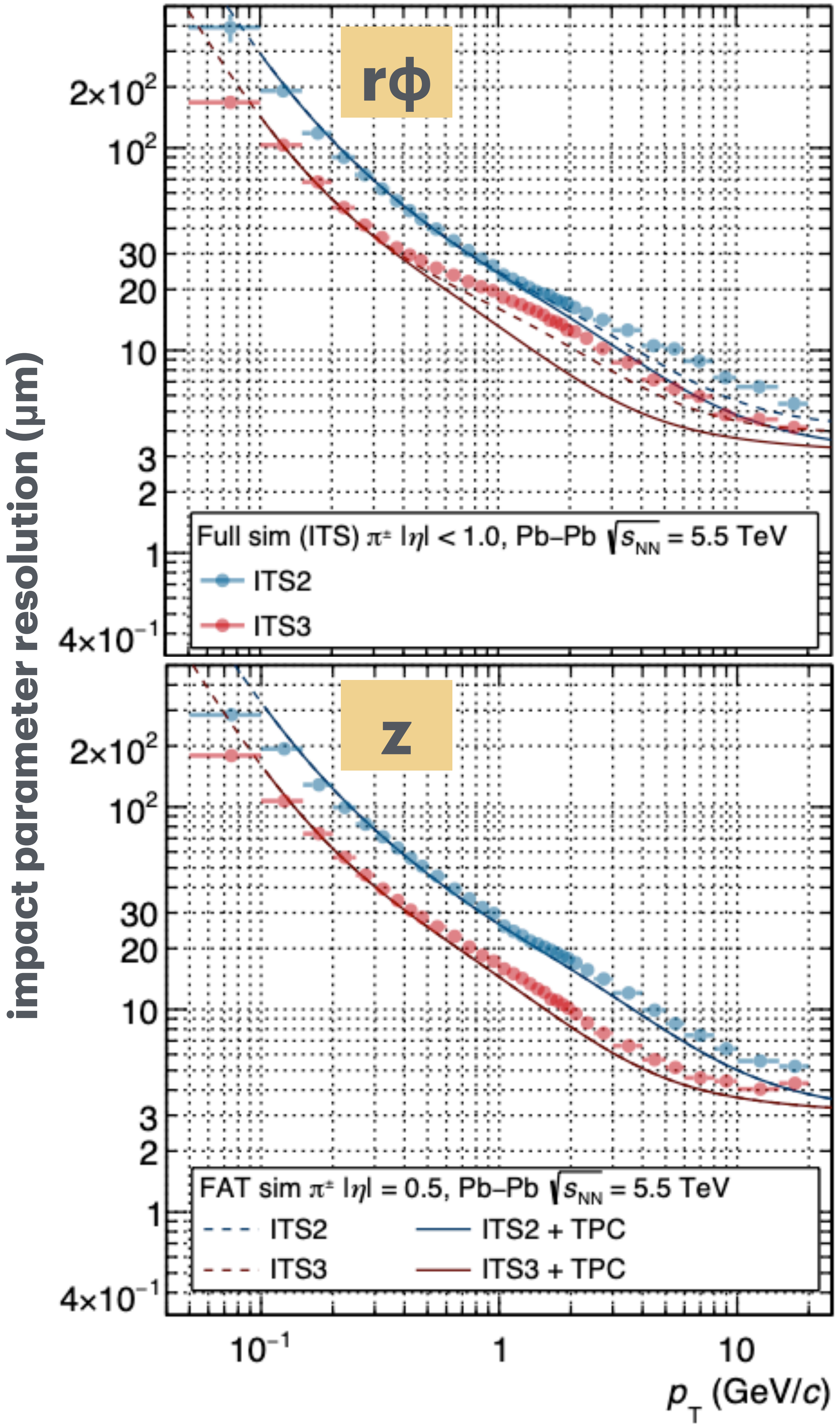
Only 1/7th of the material budget!

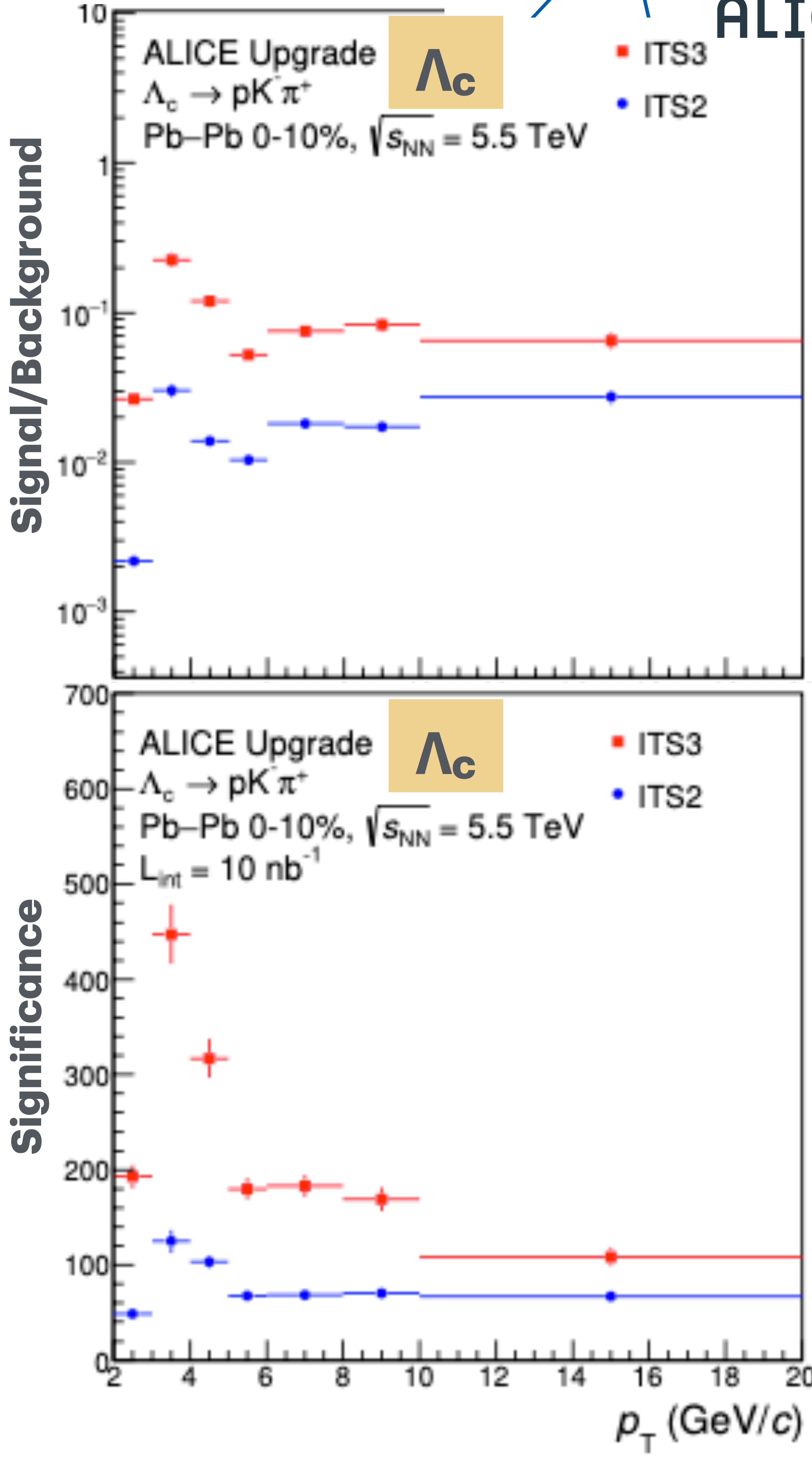
- Replacing the barrels by real half-cylinders (of **bent, thin** silicon)
- Rely on **wafer-scale sensors** (1 sensor per half-layer) in **65 nm** technology
- **Minimized material budget** → large improvement of vertexing precision and physics yield ("**ideal detector**")

Projected performance boost

- Improvement of pointing resolution by:
  - drastic reduction of **material budget** (0.3 → 0.07% X0/layer)
  - being **closer** to the interaction point (24 → 19 mm)
  - thinner and smaller **beam pipe** (700 → 500 μm; 18 → 16 mm)
- Directly boosts the ALICE core physics program:
  - low momenta
  - secondary vertex reconstruction
- E.g. Λ_c S/B improves by factor 10, significance by factor 4

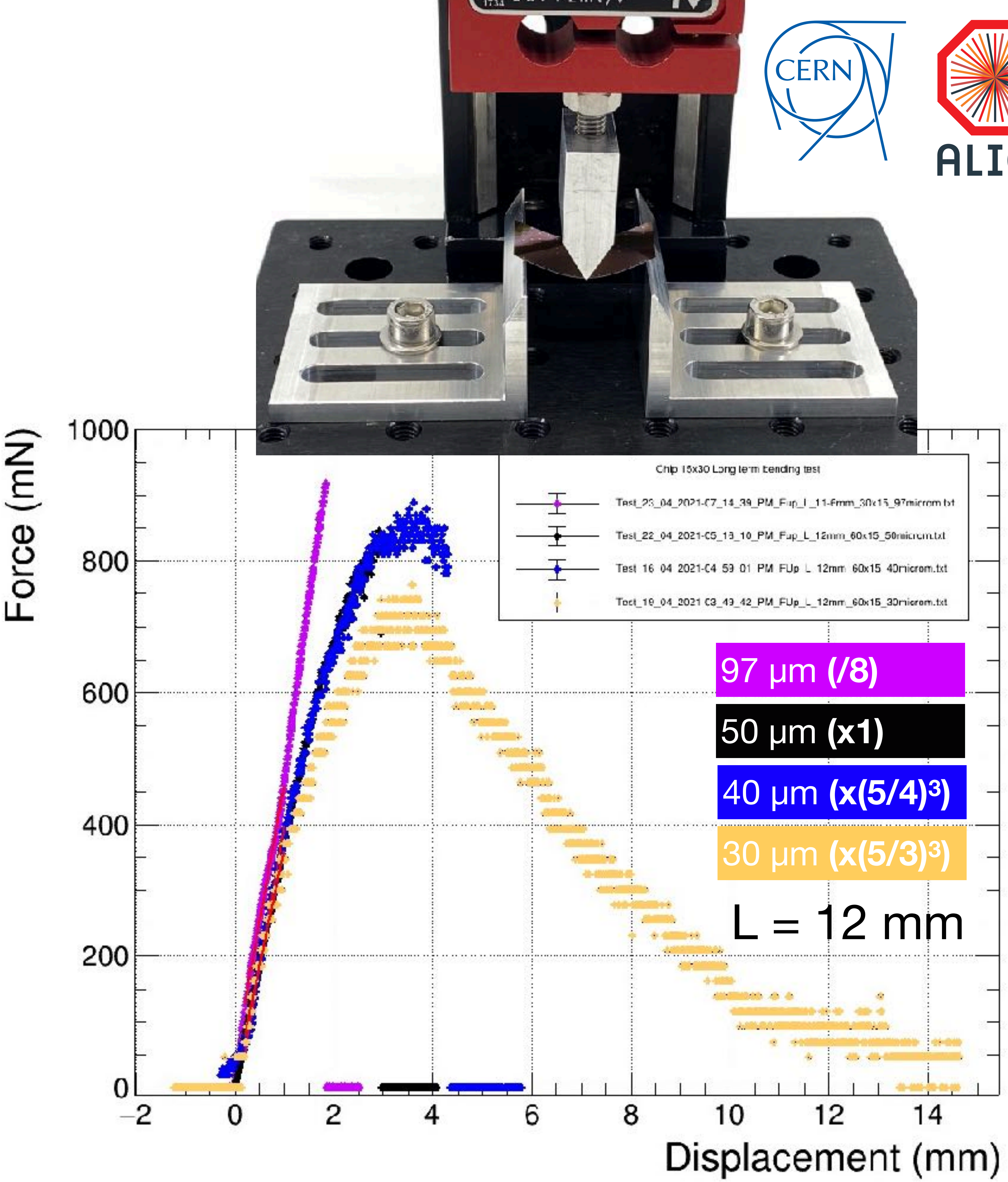






Flexibility of silicon

- **Monolithic** Active Pixel Sensors are quite flexible
- Bending force scales as (thickness)$^{-3}$
  - large benefit from thinner sensors



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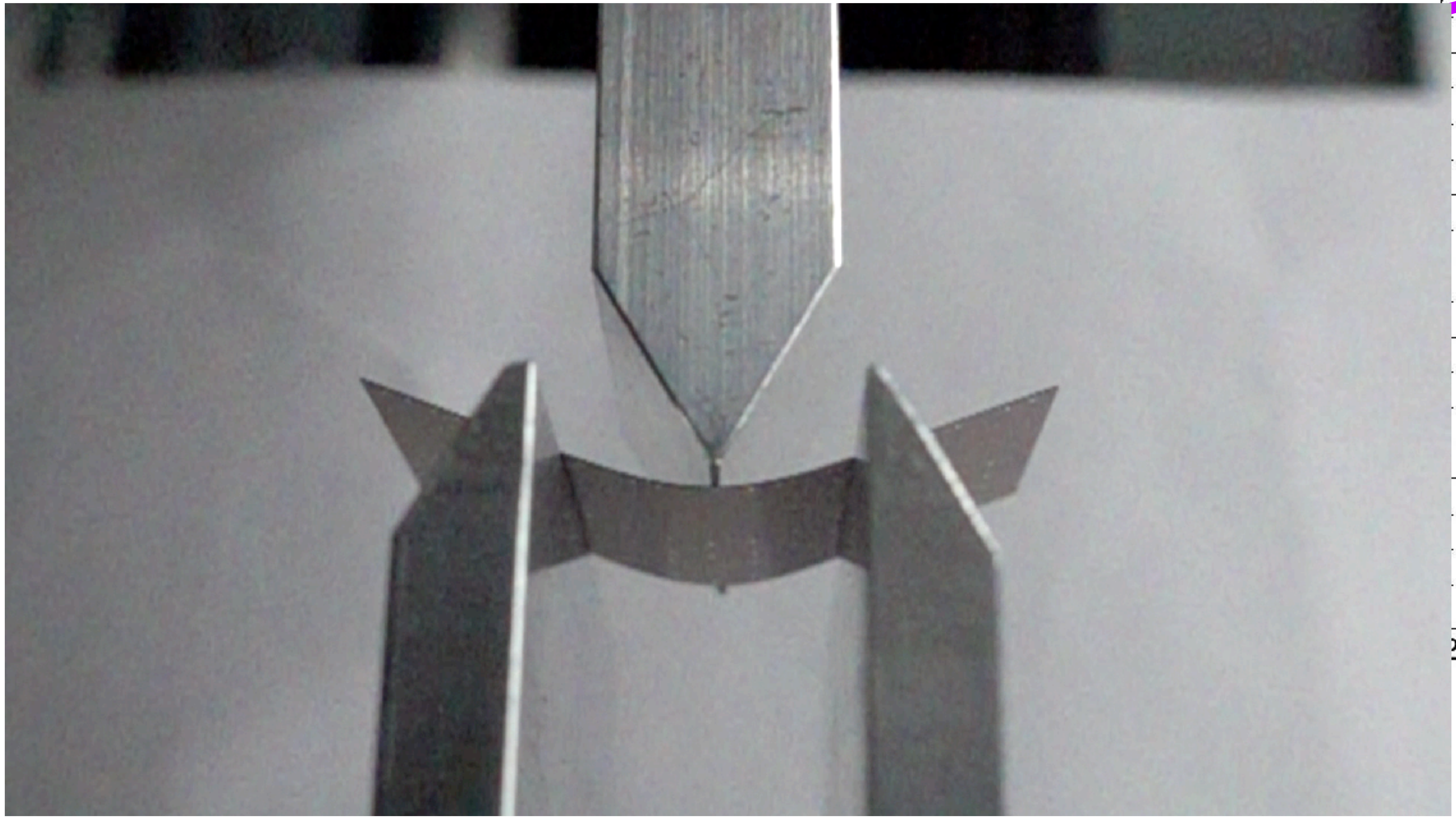

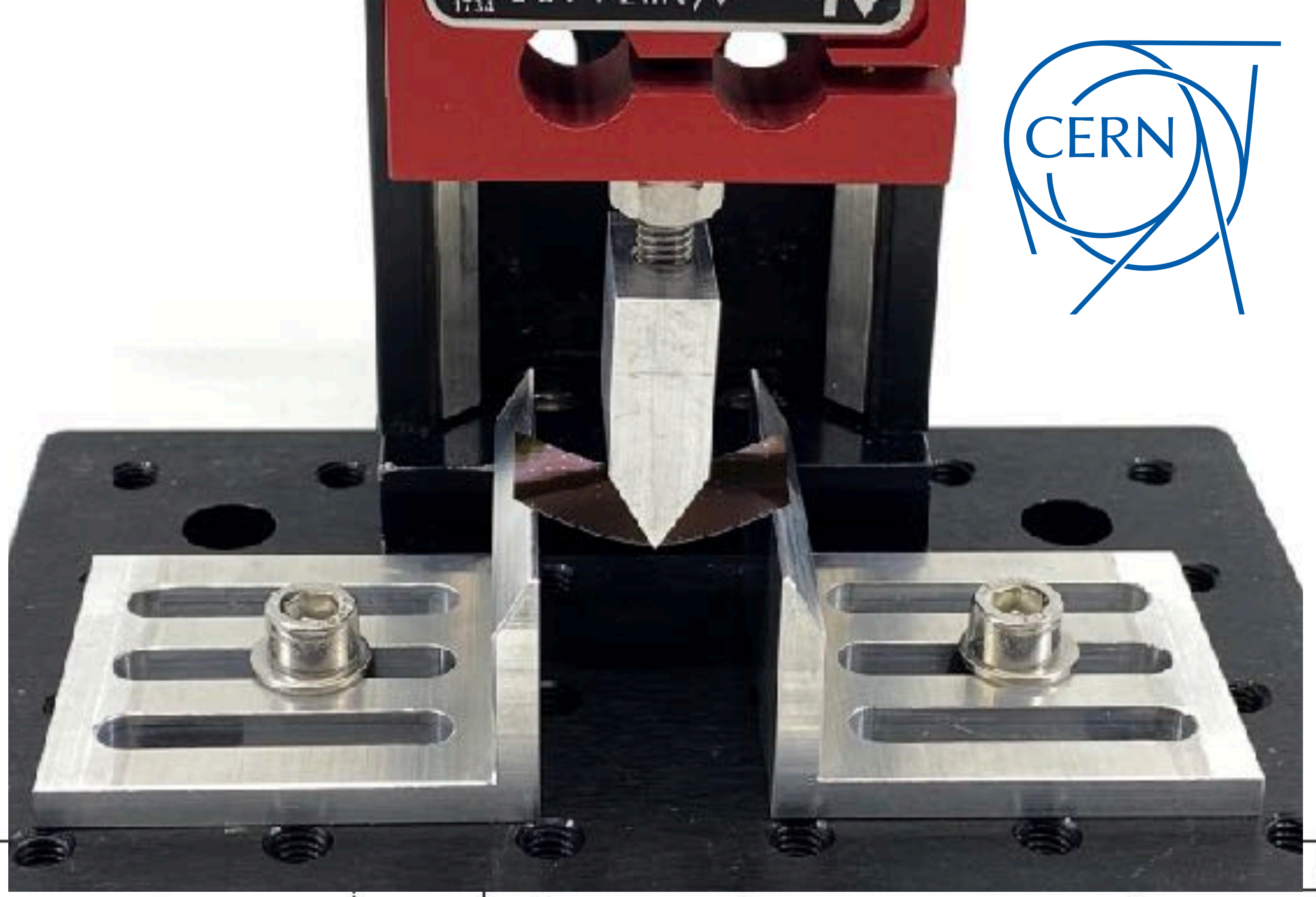

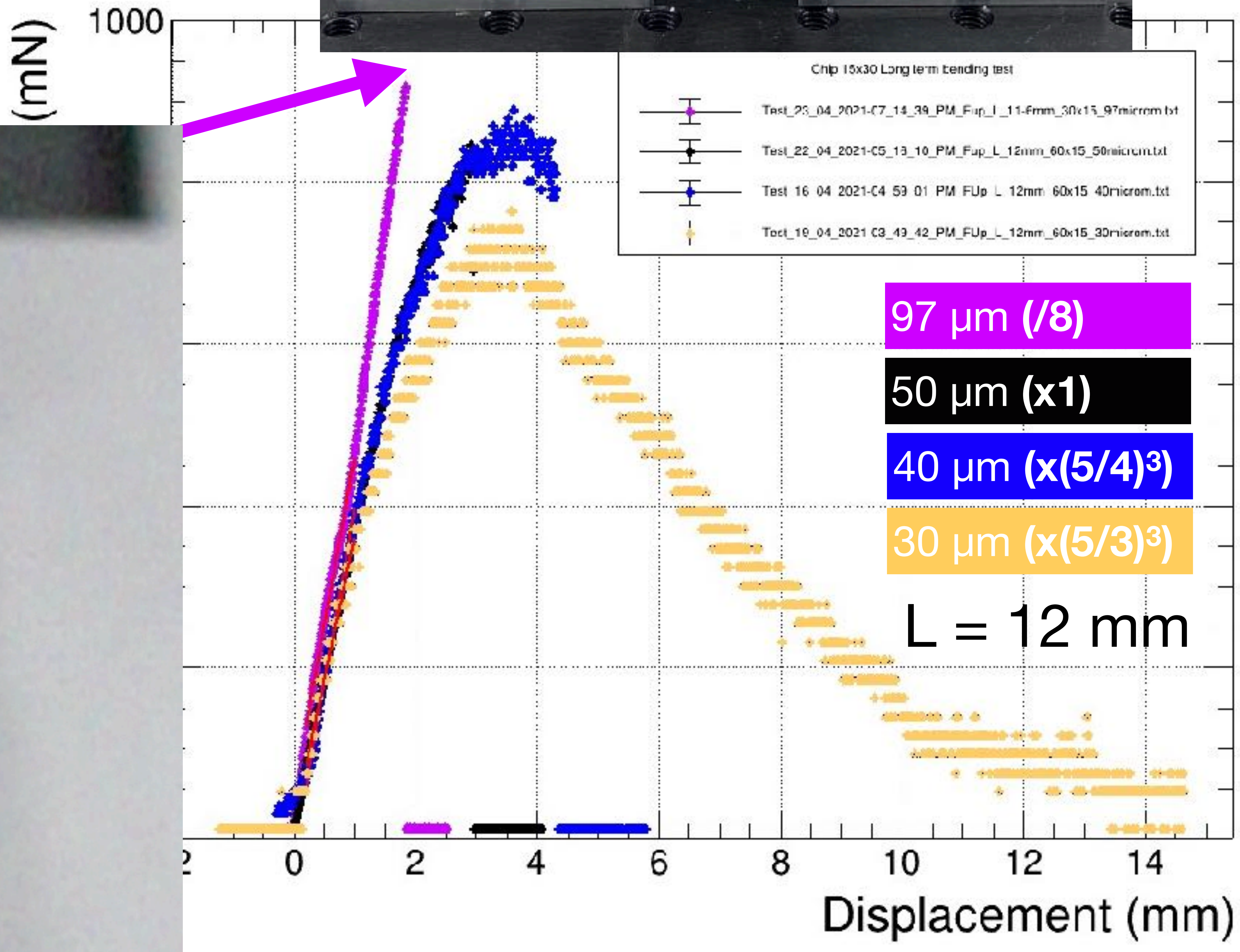

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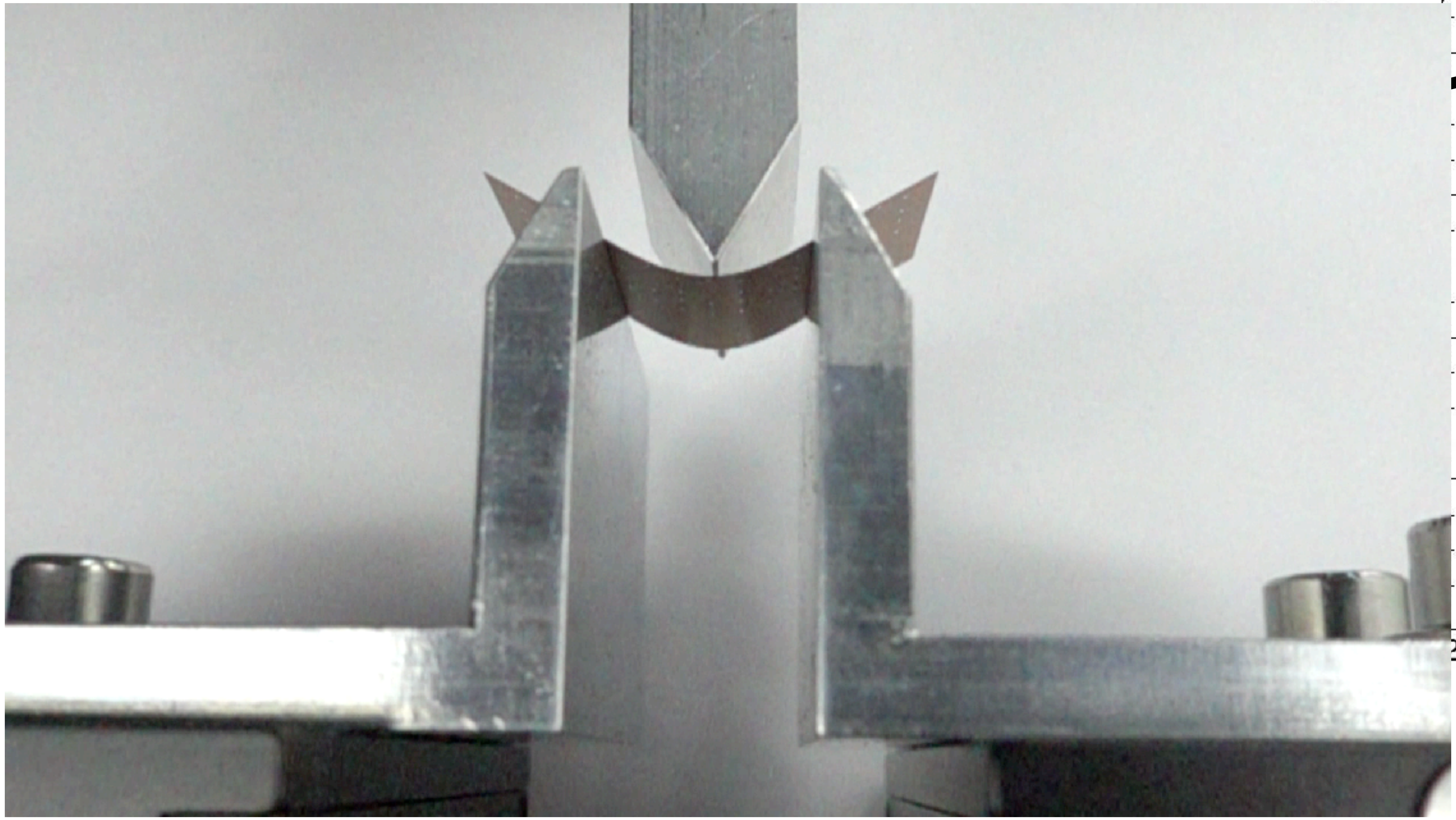

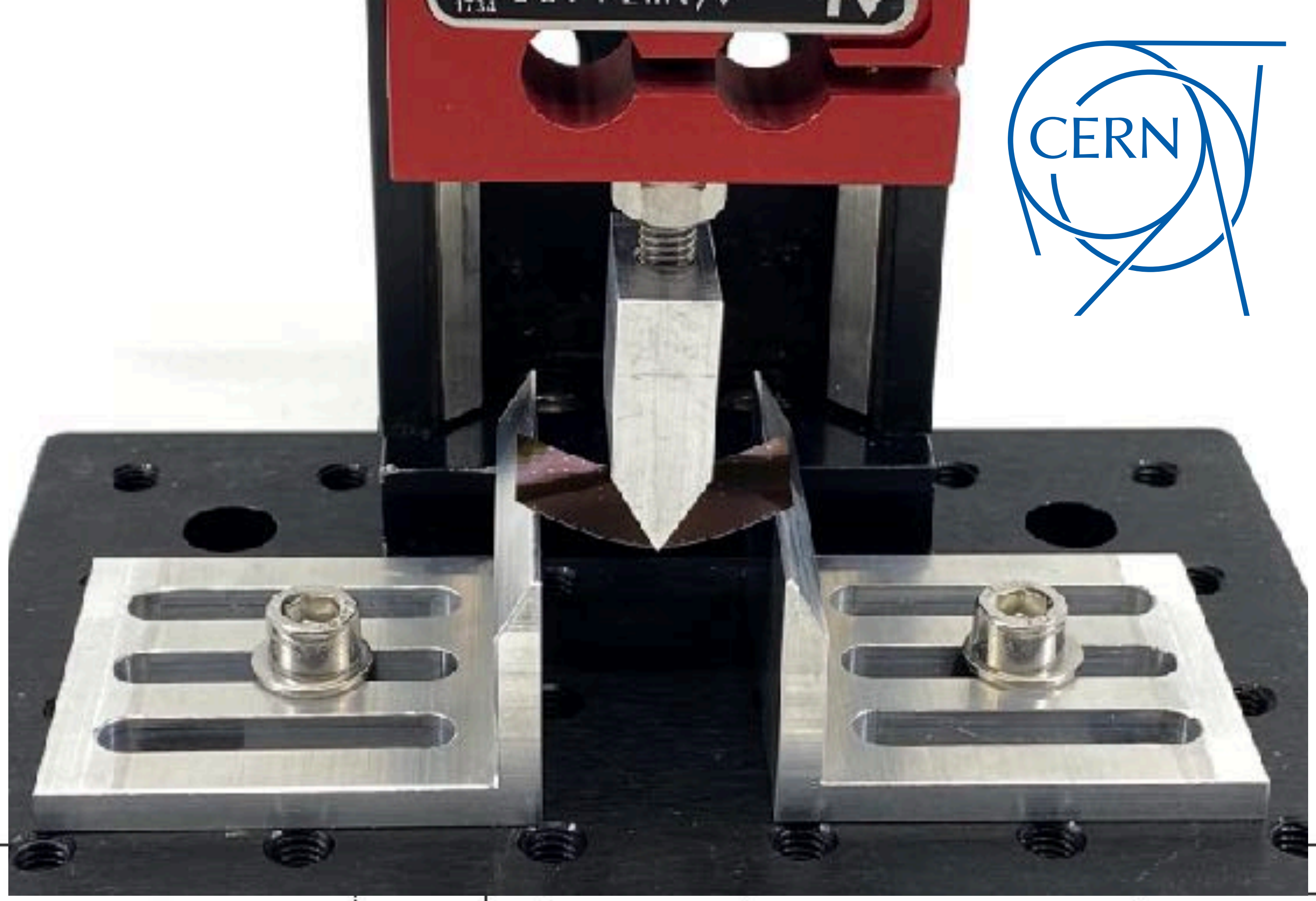

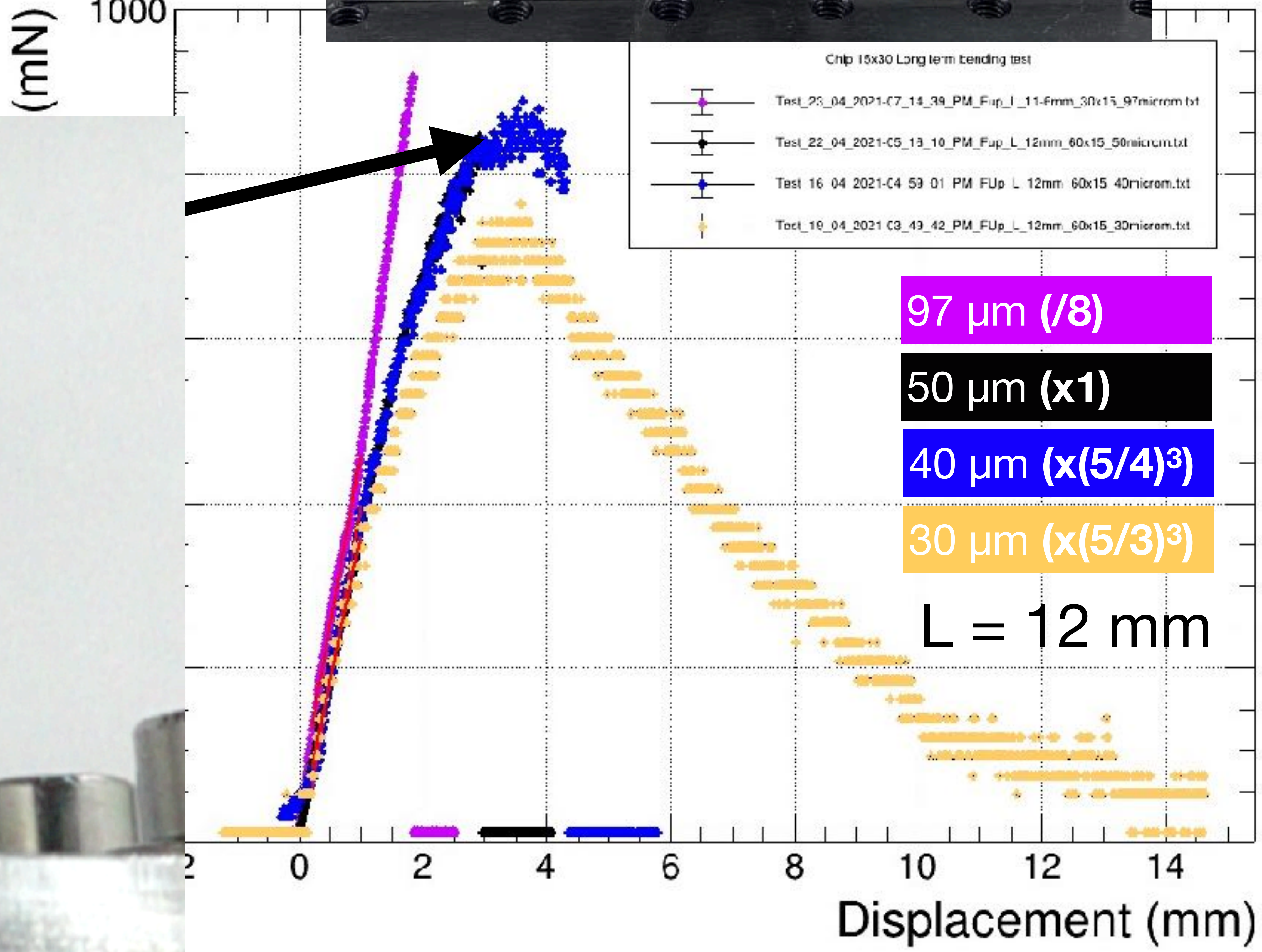

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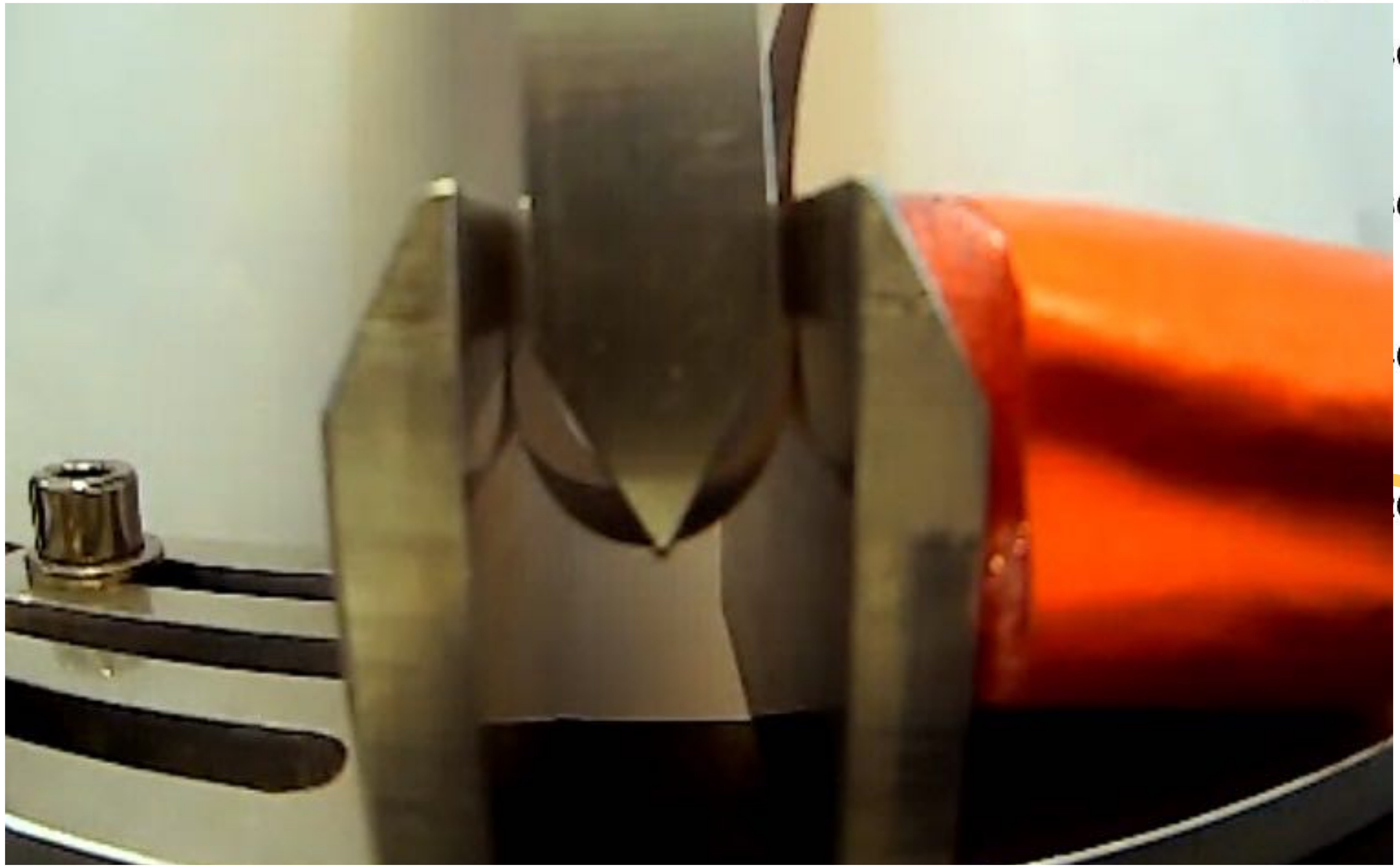
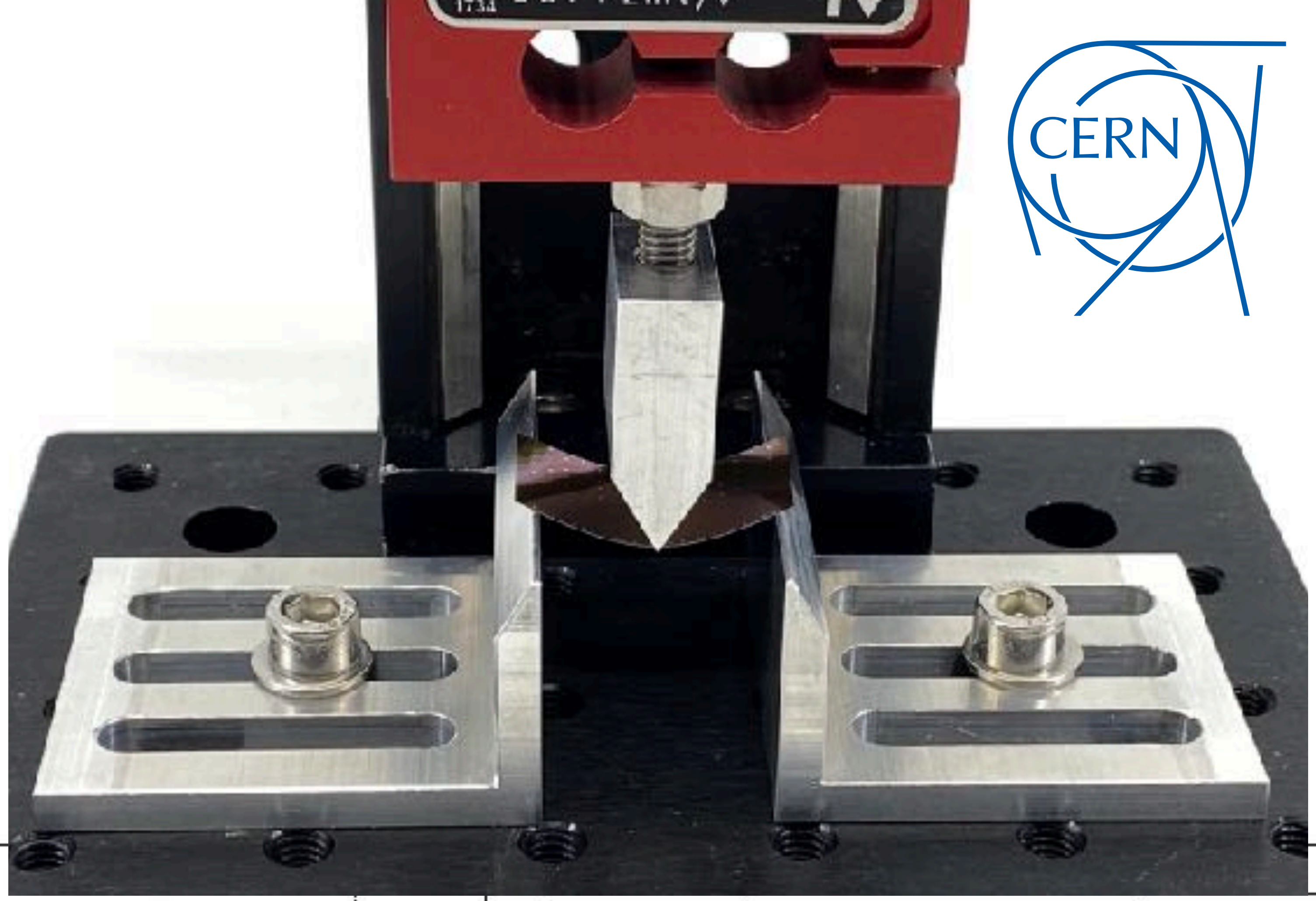
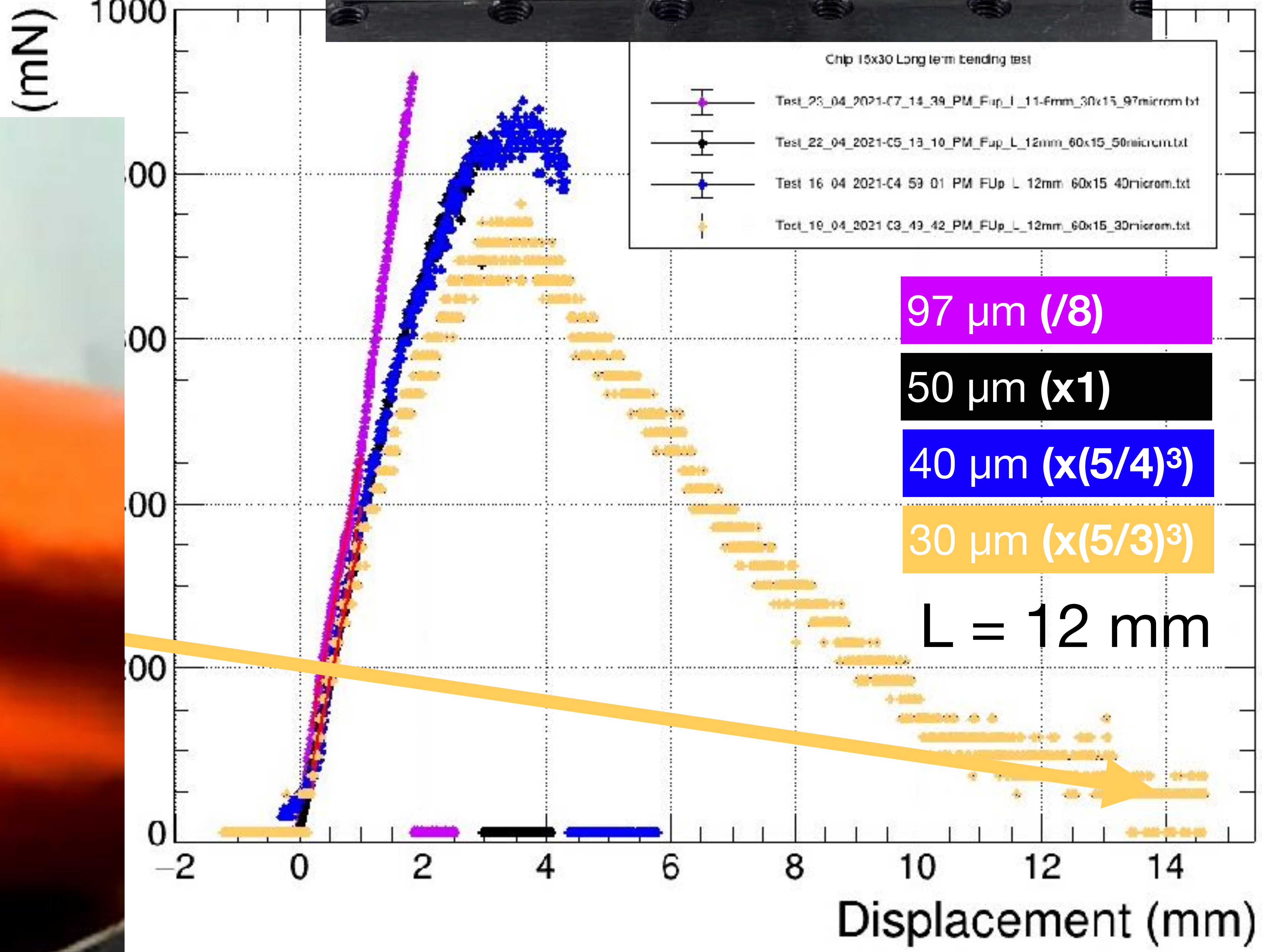


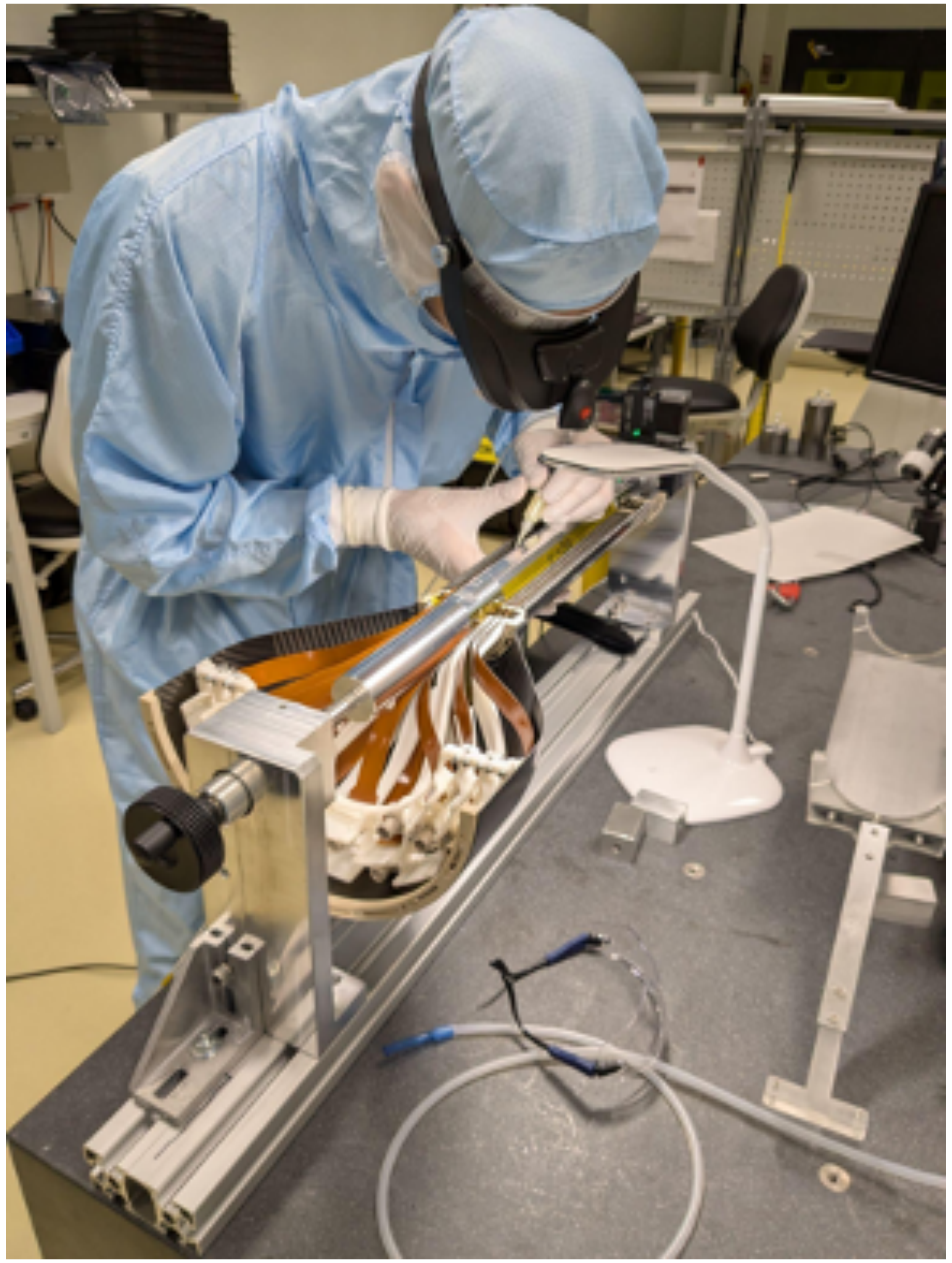
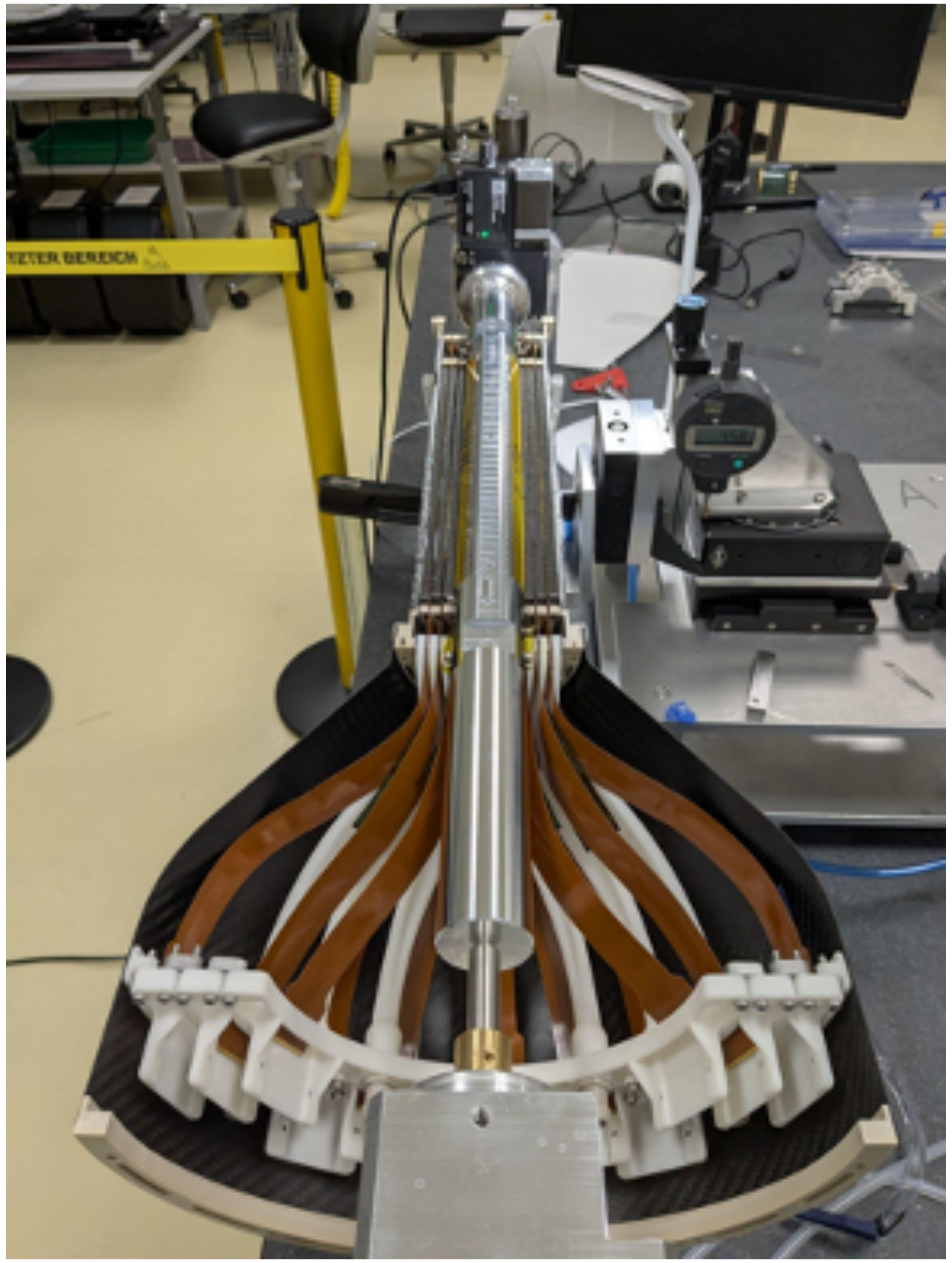




Bending of fully processed wafers

R = 18 mm
50 µm fully
processed silicon

Engineering Models
including services


X-ray tomography

Next technology node: 180 nm → 65 nm

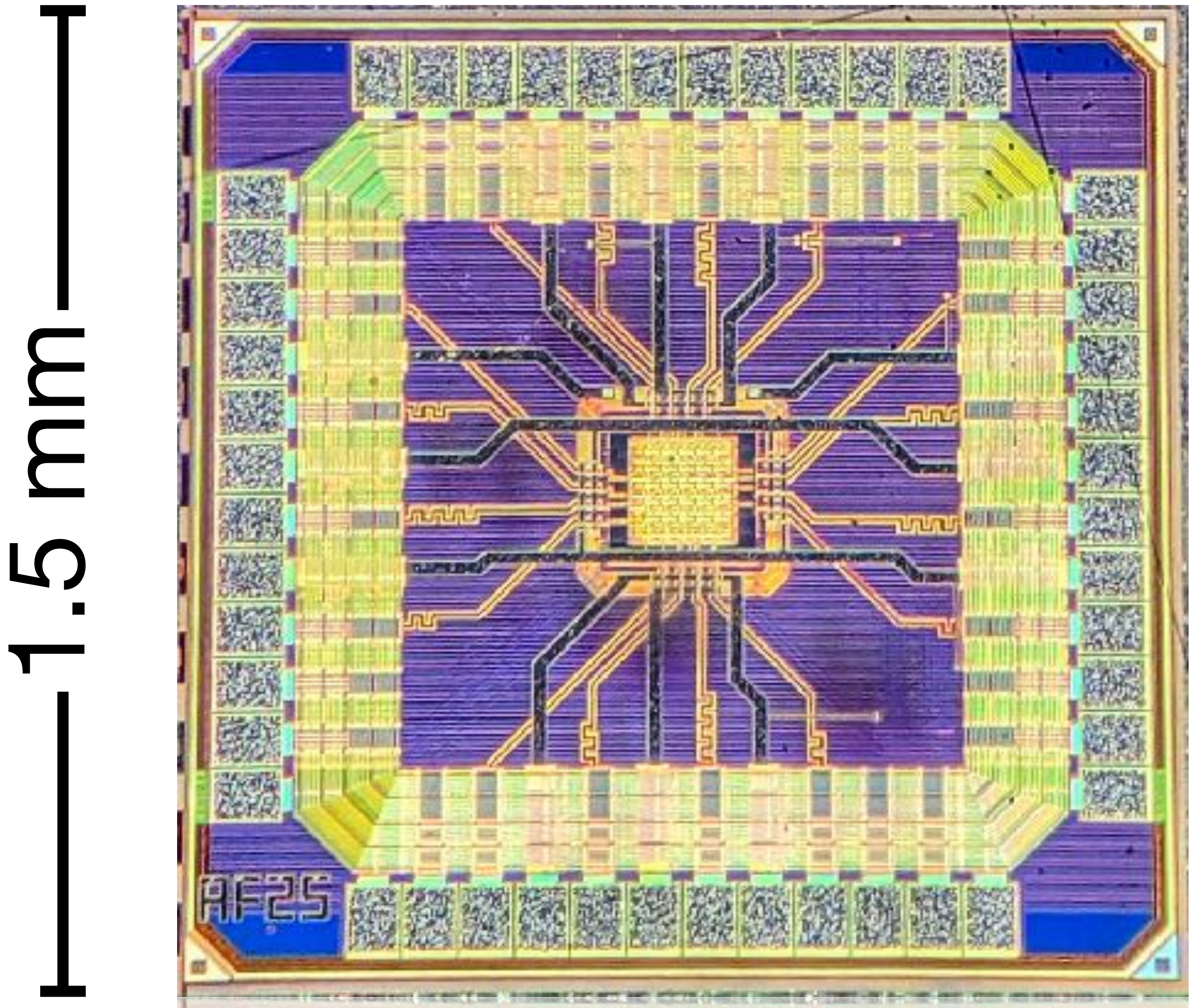
- **Key benefits:**
  - smaller features/transistors: higher integration density
  - smaller pitches
  - lower power consumption
  - larger wafers

- ALICE ITS3 together with CERN EP R&D
  - leverages on experience with 180 nm (ALPIDE)
  - excellent links to foundry

- Works excellently!

65 nm technology qualification

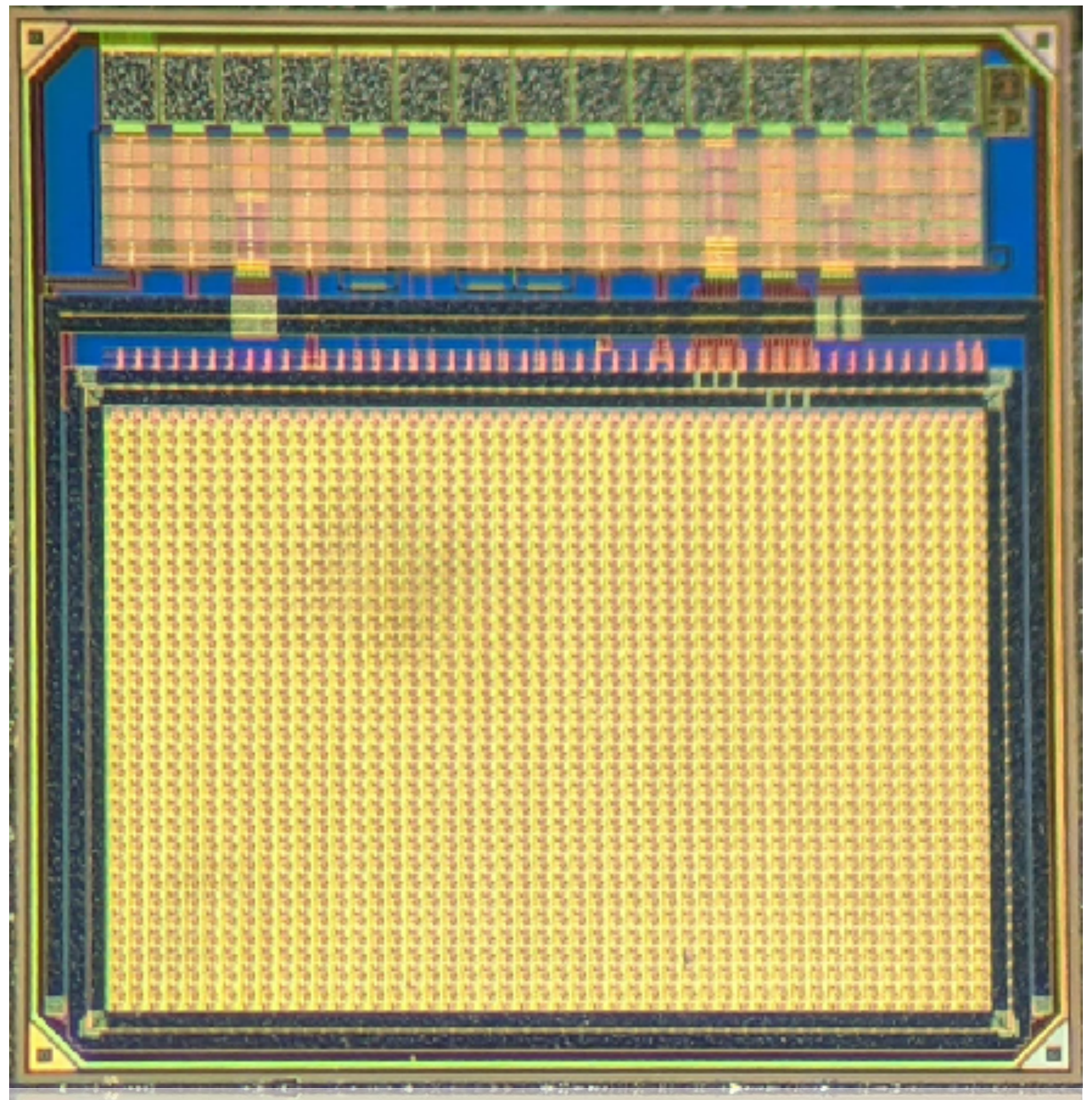
APTS



- **matrix:** 6x6 pixels
- **readout:** direct analog readout of central 4x4
- **pitch:** 10, 15, 20, 25 μm
- **total:** 34 variants

[doi:10.1016/j.nima.2024.169896]
[doi:10.1016/j.nima.2024.170034]
[doi:10.48550/arXiv.2512.13339]

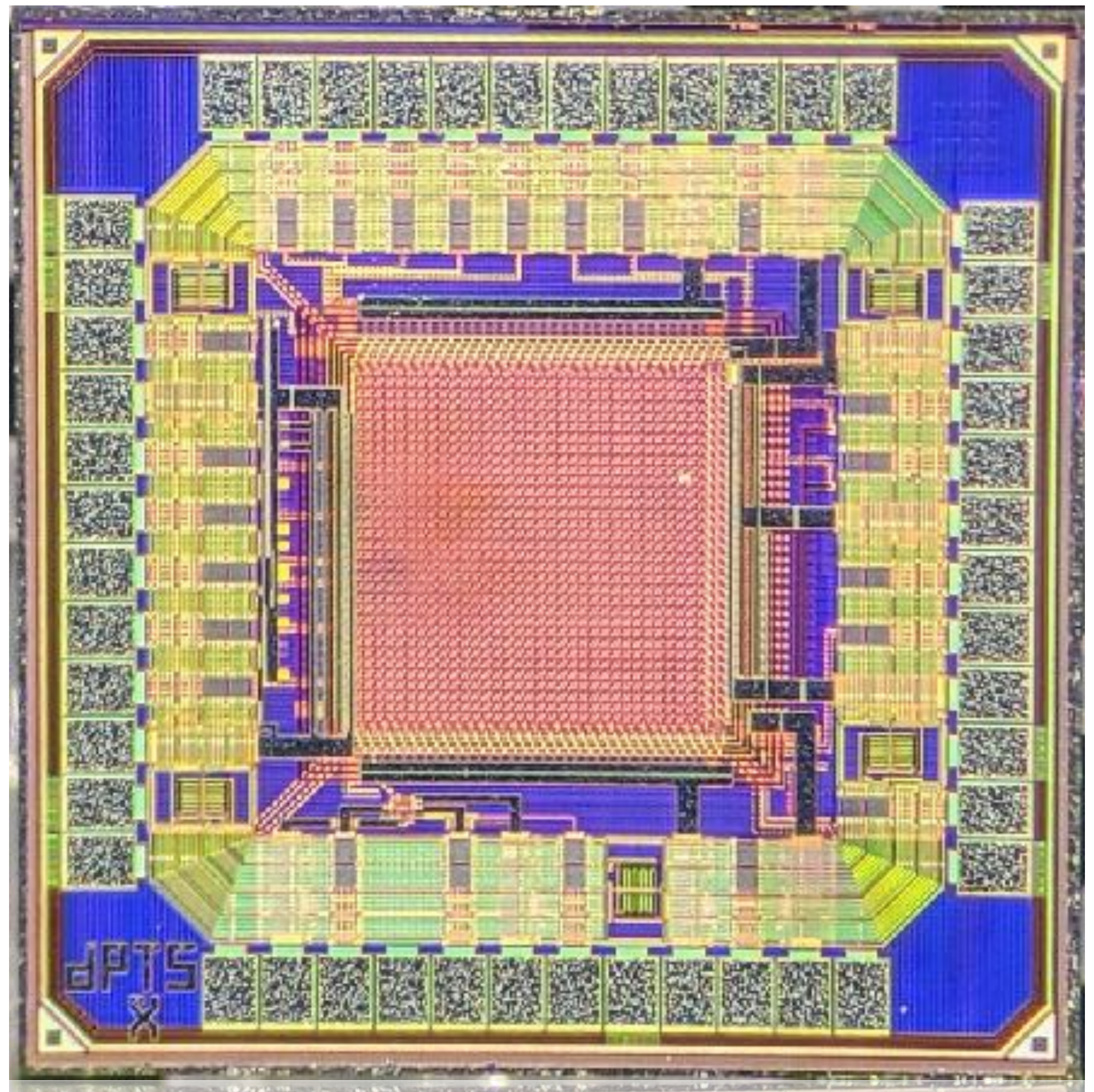
CE65



- **matrix:** 64x32, 48x32 pixels
- **readout:** rolling shutter analog
- **pitch:** 15, 25 μm
- **total:** 4 variants

[doi:10.1016/j.nima.2022.167213]
[doi:10.1088/1748-0221/20/03/C03033]

DPTS



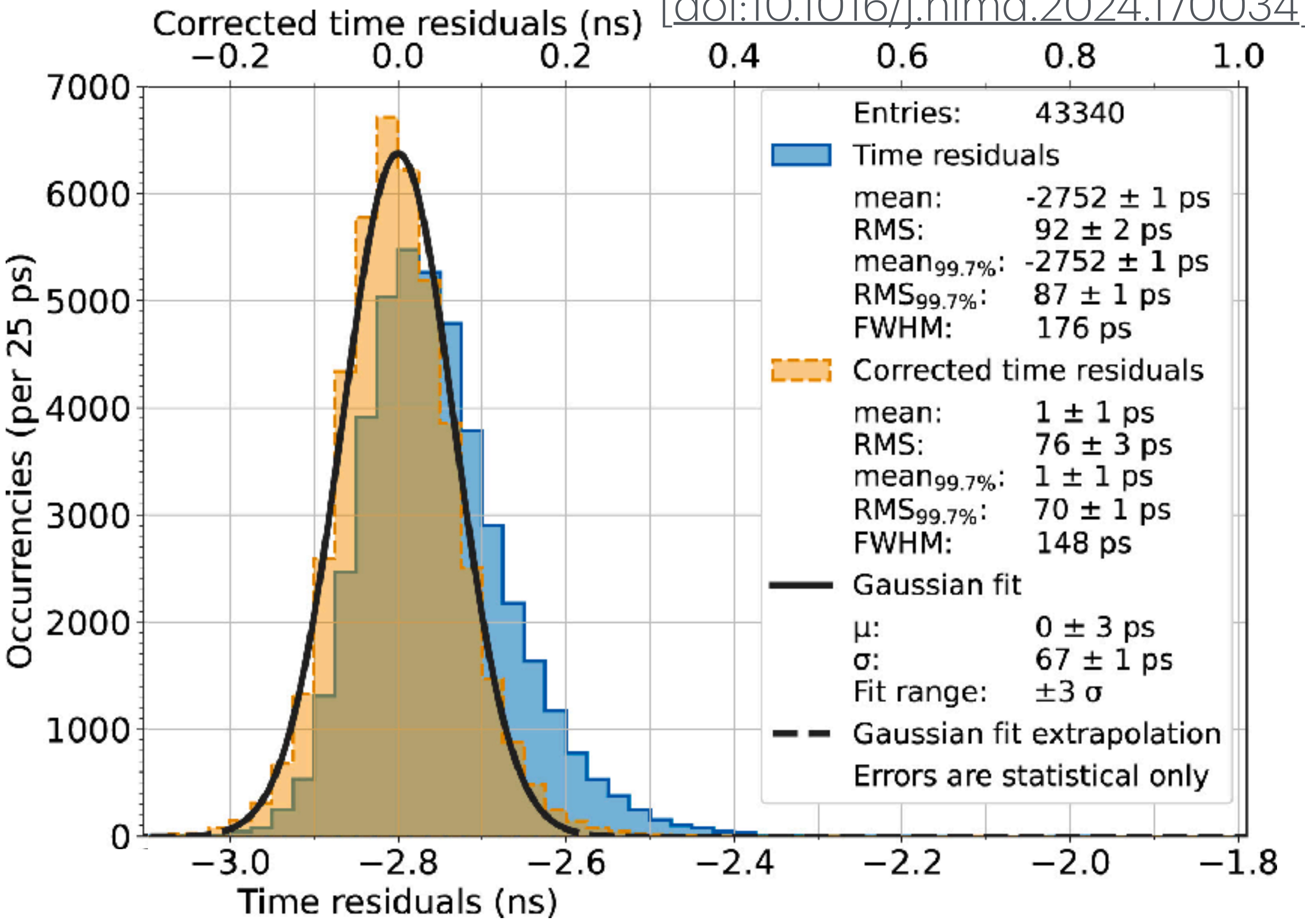
- **matrix:** 32x32 pixels
- **readout:** async. digital with ToT
- **pitch:** 15 μm
- **total:** 3 variants

[doi:10.1016/j.nima.2023.168589]
[doi:10.48550/arXiv.2505.05867]

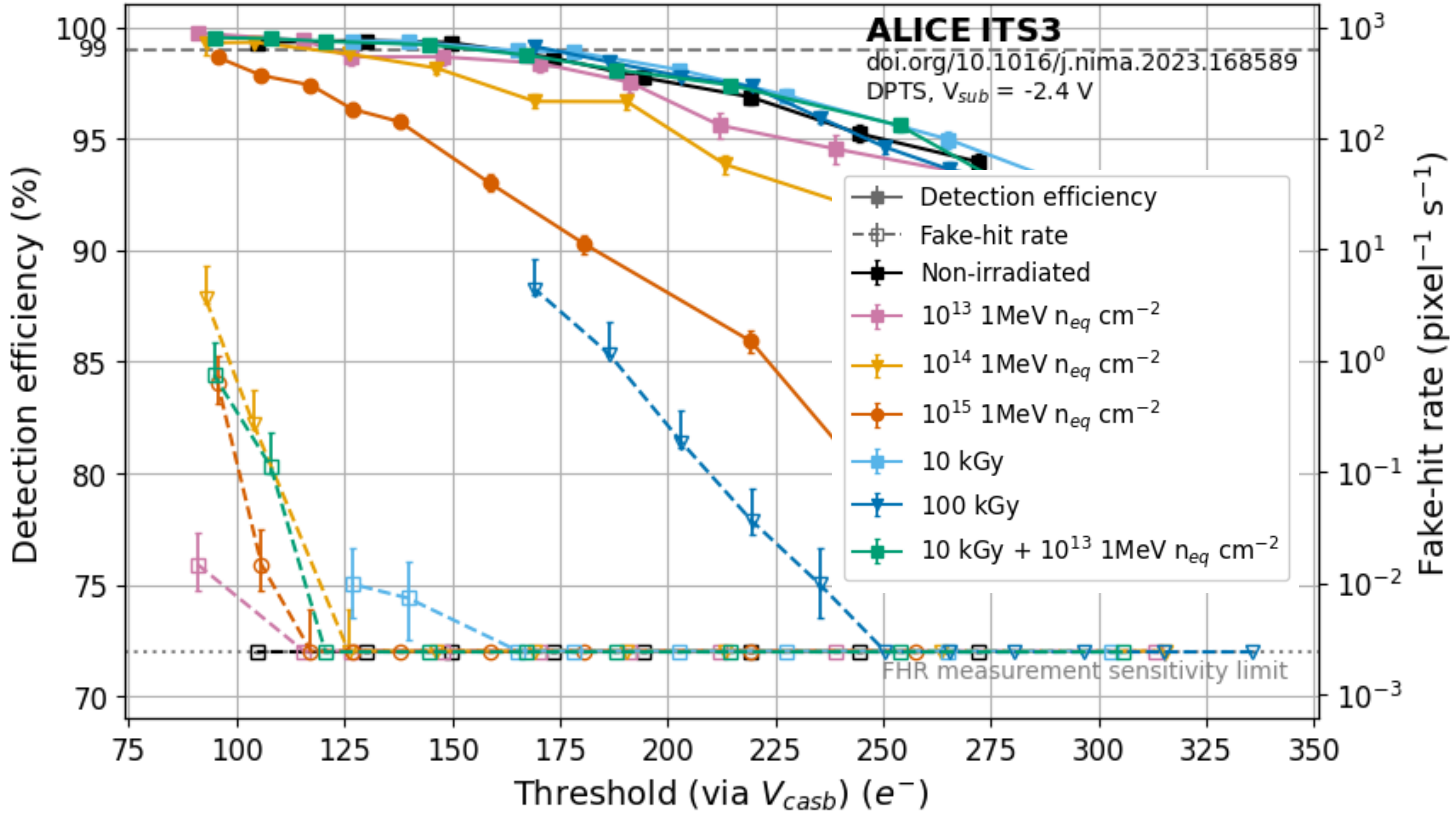
65 nm technology qualification

- Intrinsic time resolutions of 67 ps for 10 µm pixels
- >99% detection efficiency even after 10^{15} NIEL for 15 µm pixels at room temperature

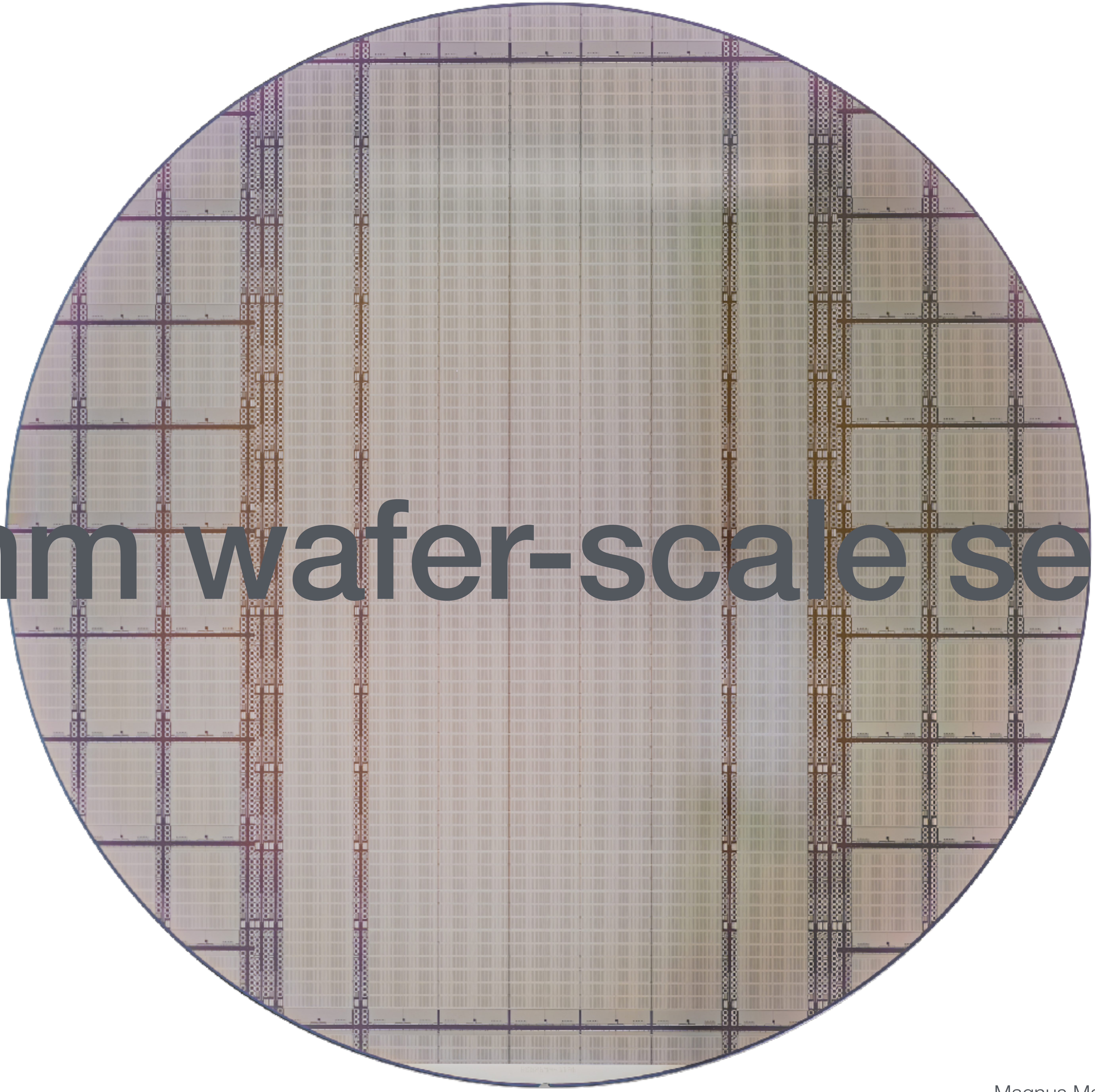
[doi:10.1016/j.nima.2024.170034]



[doi:10.1016/j.nima.2023.168589]



Excellent performances of the 65 nm technology have been established experimentally

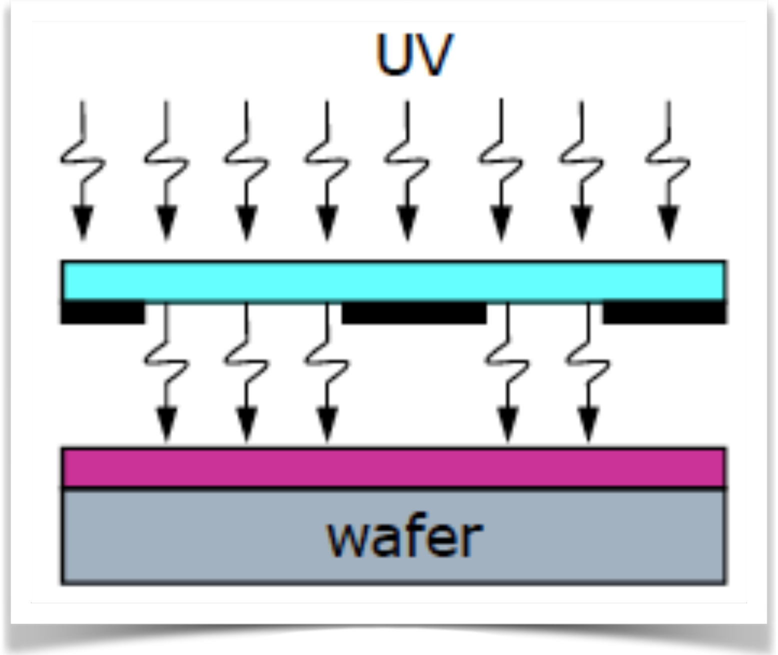


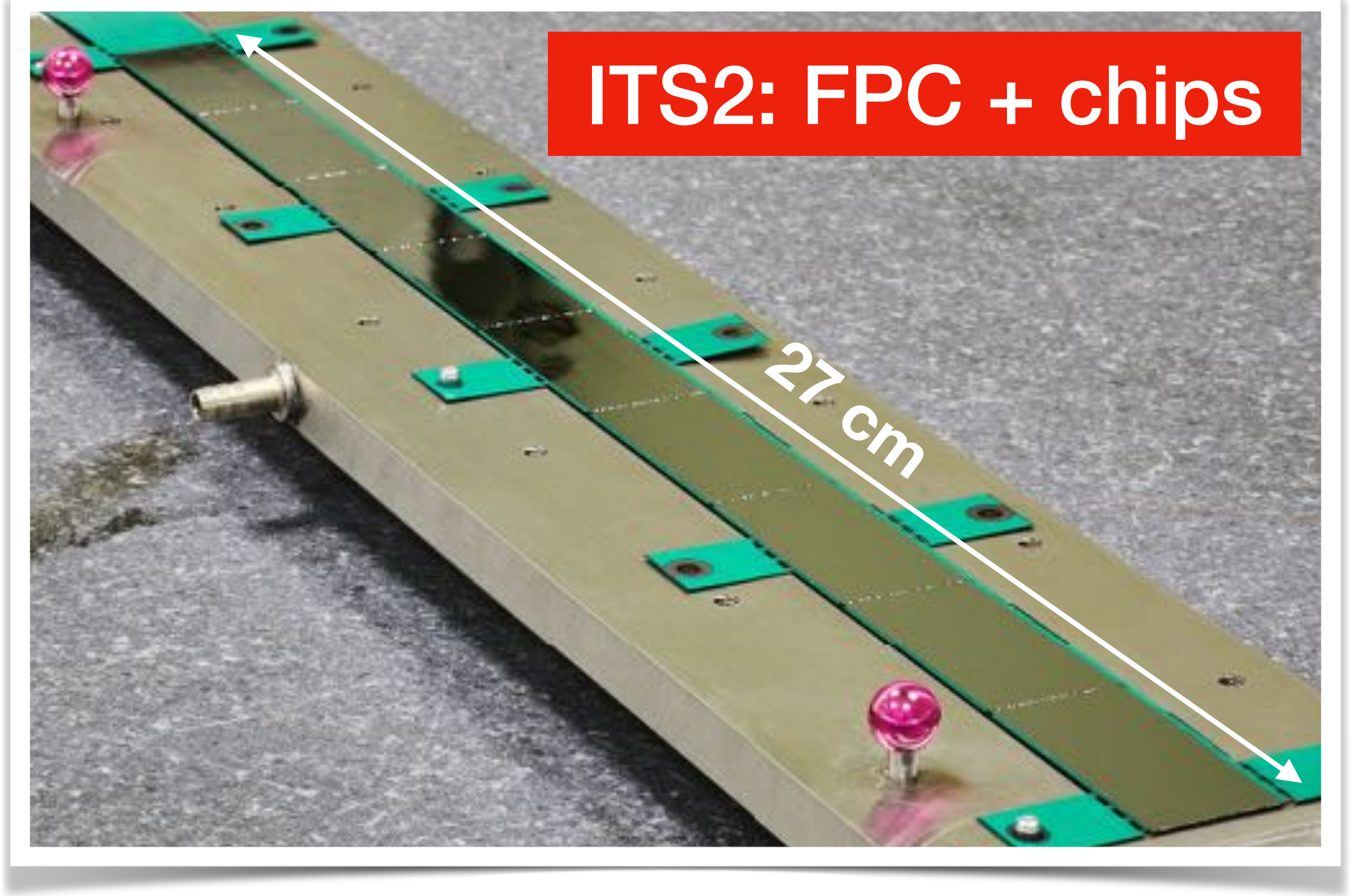
300 mm wafer-scale sensors

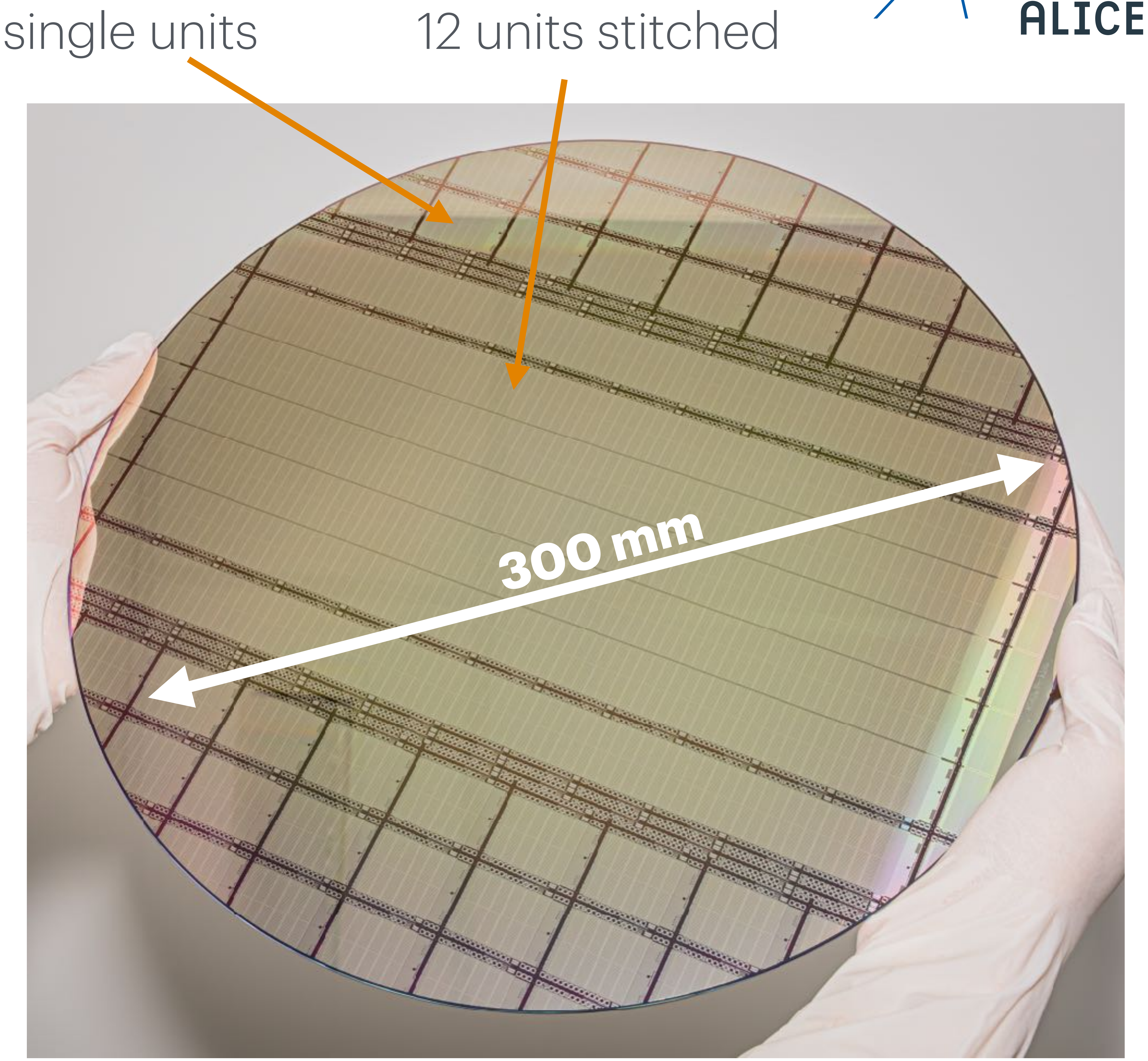
Wafer-scale sensors

concept

- **Previous** chip sizes are *O*(1-3 by 1-3 cm^2)
  - dictated by mask size
  - masks are exposed once for each chip
  - chips diced out and qualified/selected
  - interconnection on circuit boards (“modules”)
- **Wafer-scale** “chips”/sensors: stitching of exposures
  - same mask exposed in a precisely aligned fashion
  - design is made periodic (metal lines stitch together)
  - *chip is a module*

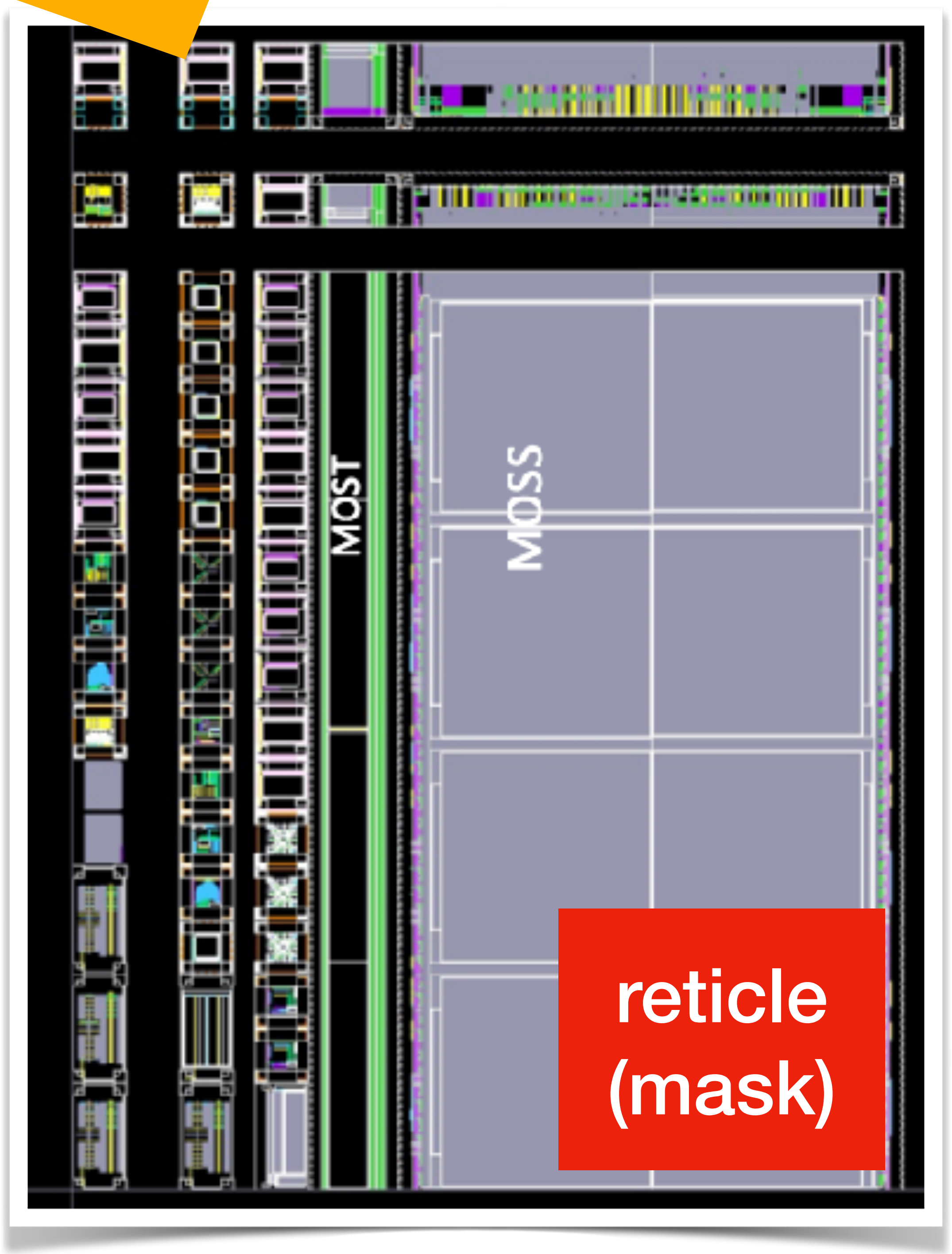




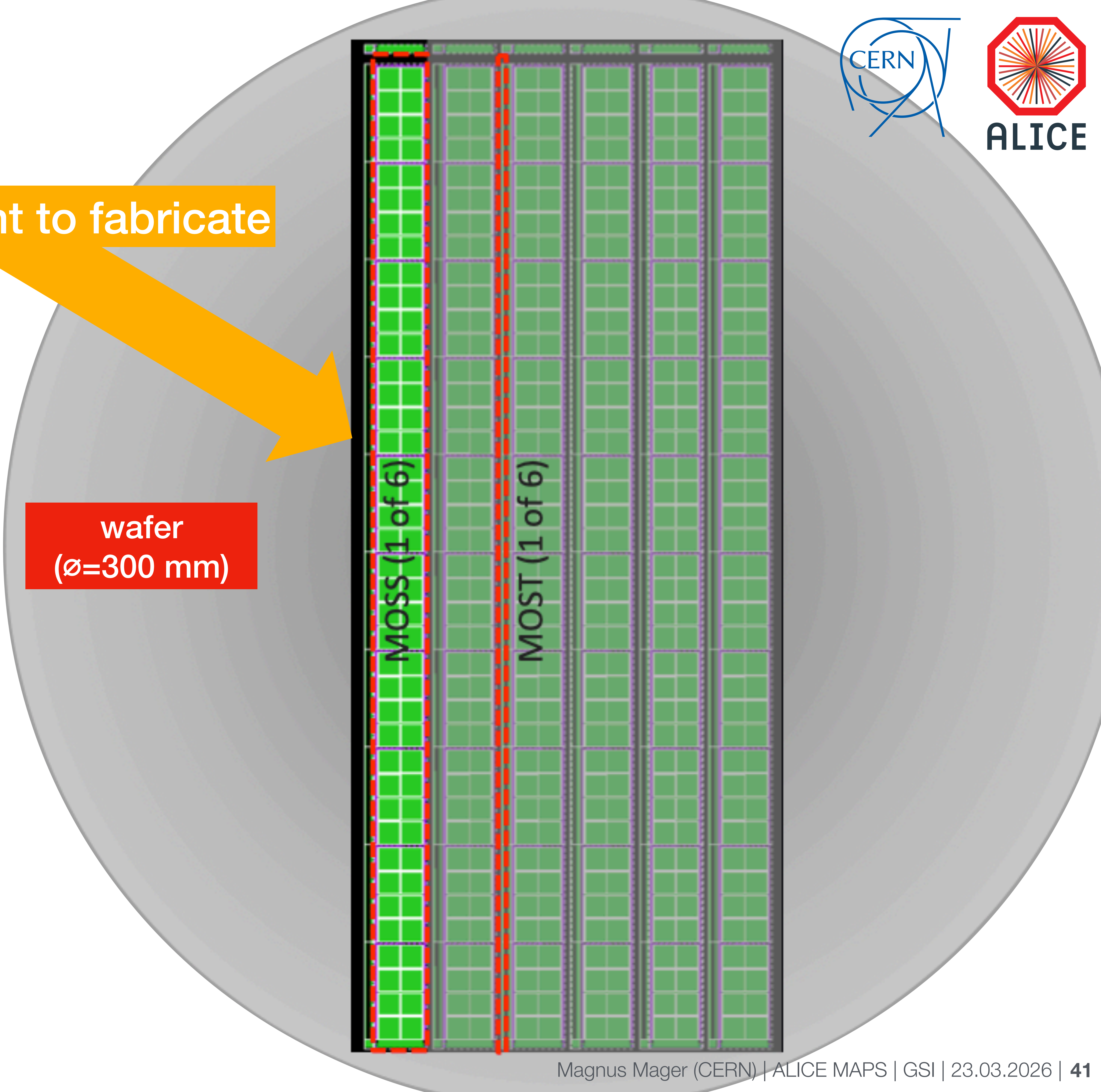


Stitching
rough principle

what we "design"

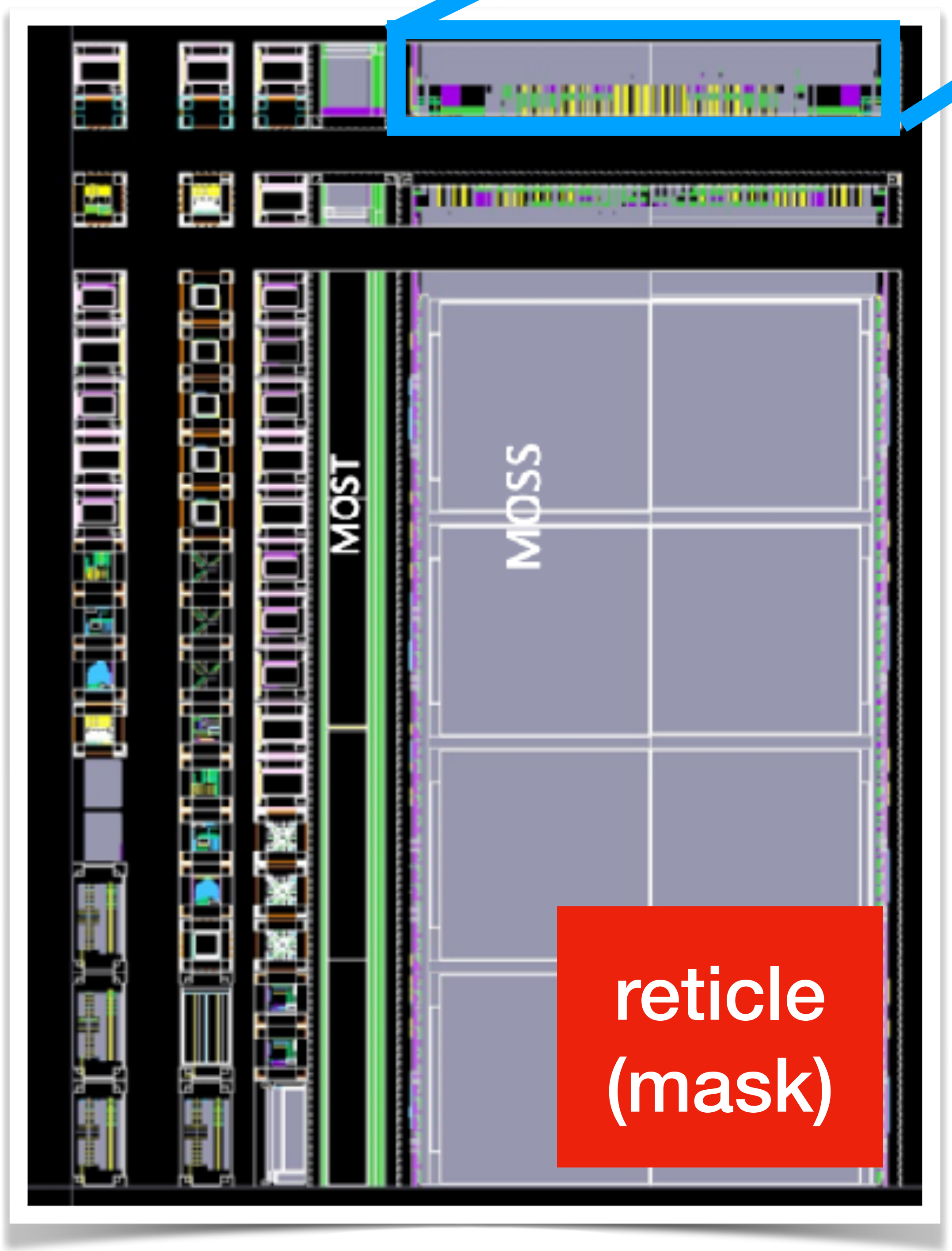


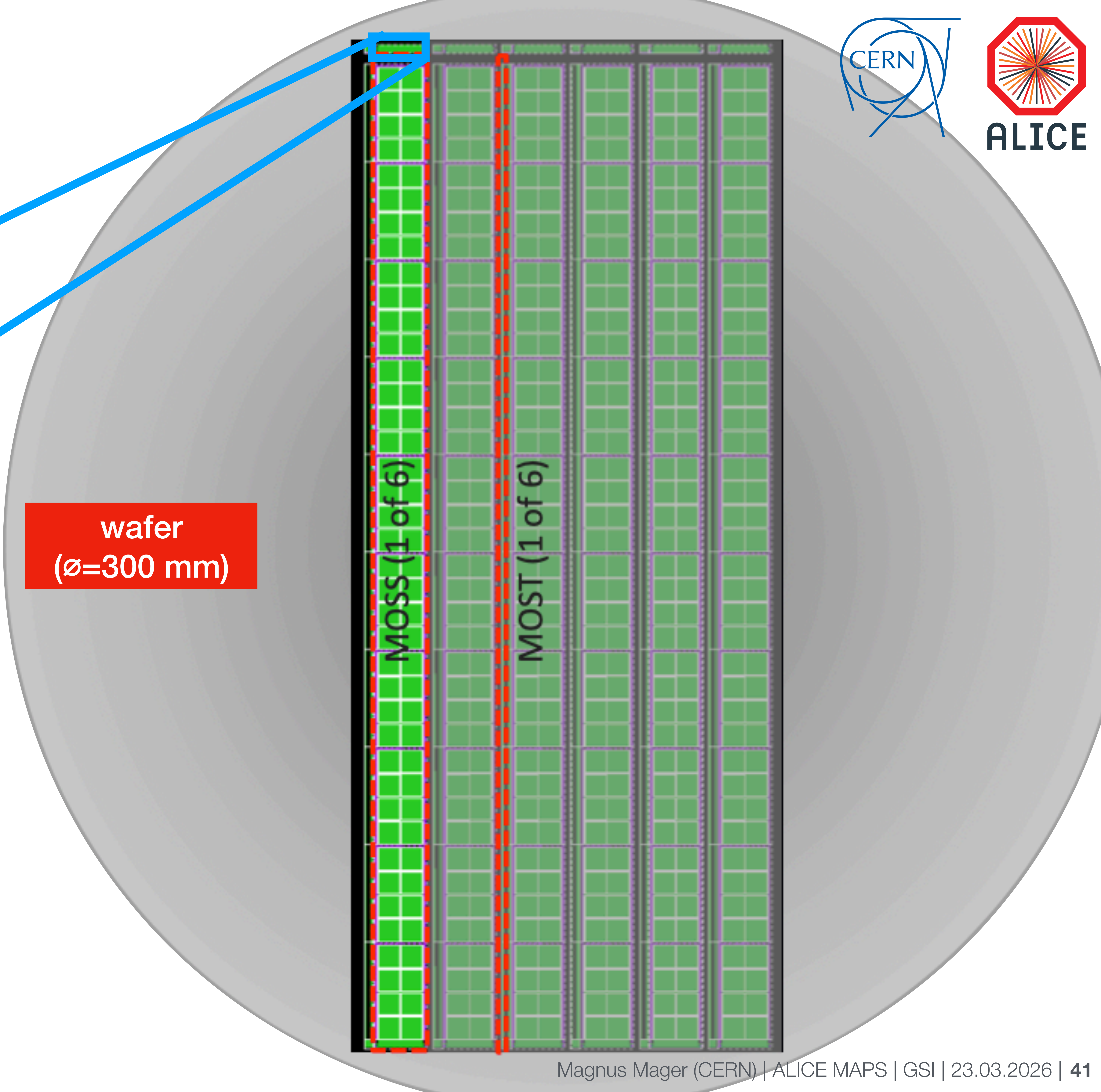
what we want to fabricate



Stitching
rough principle

- top part

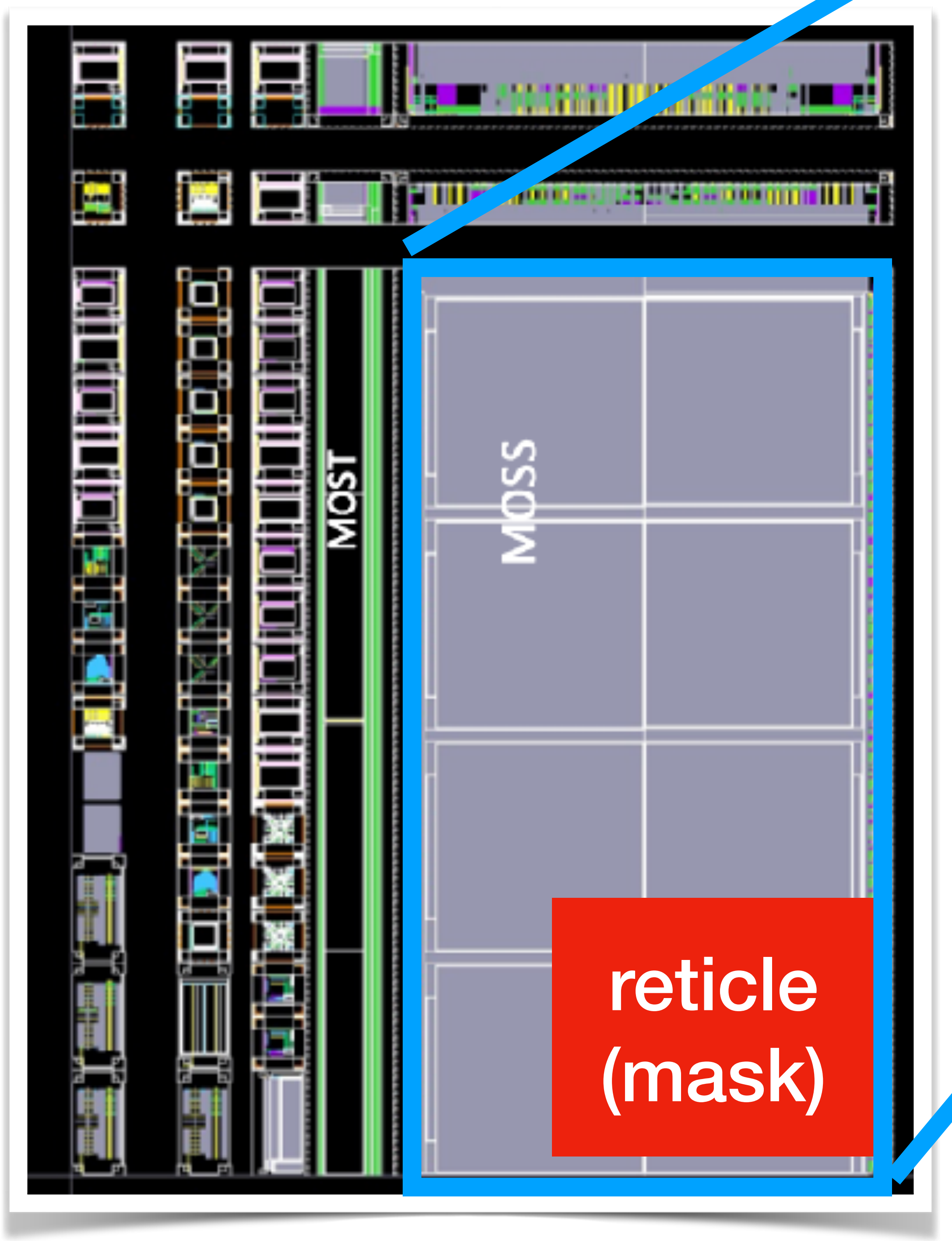


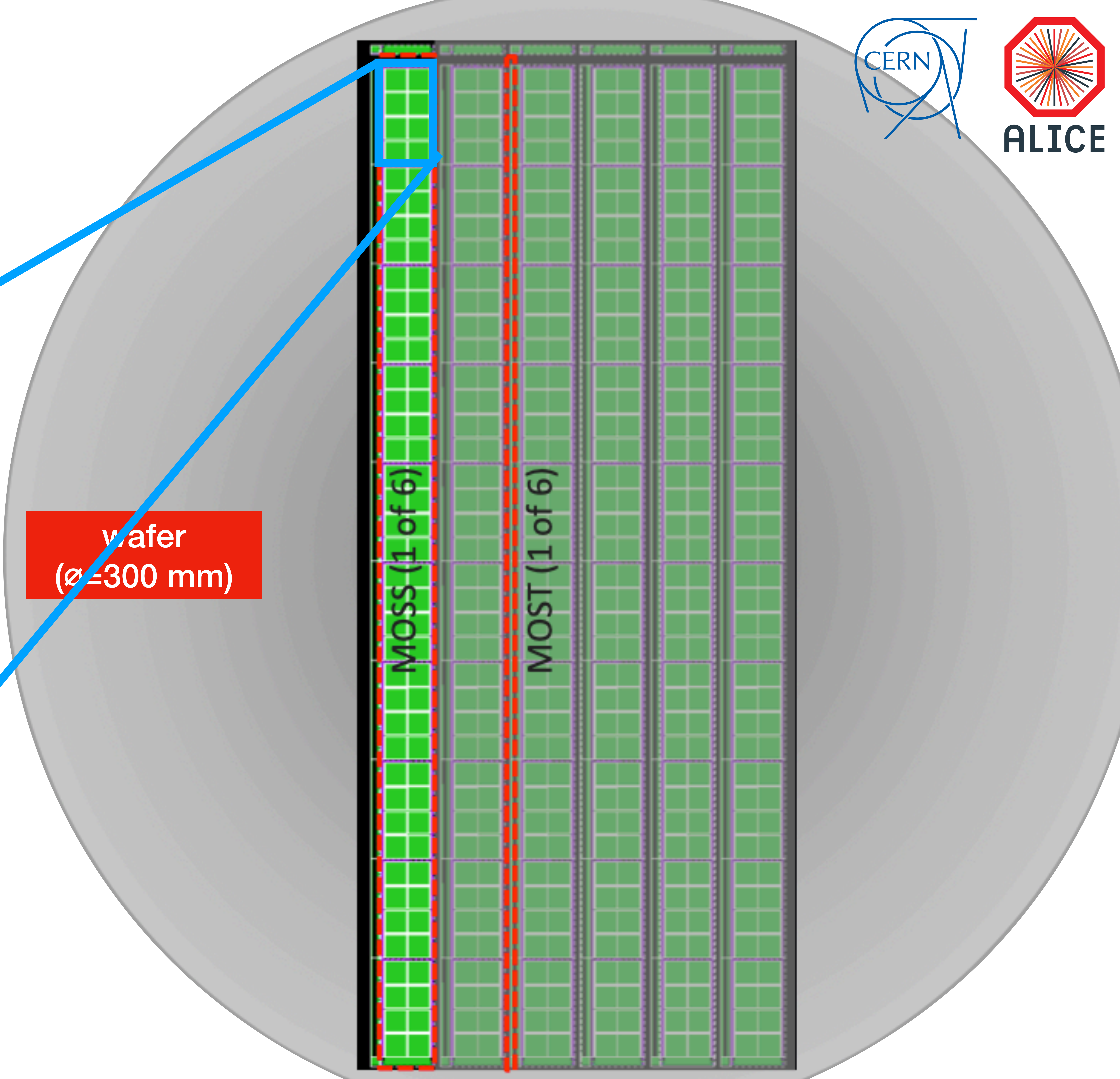


Stitching

rough principle

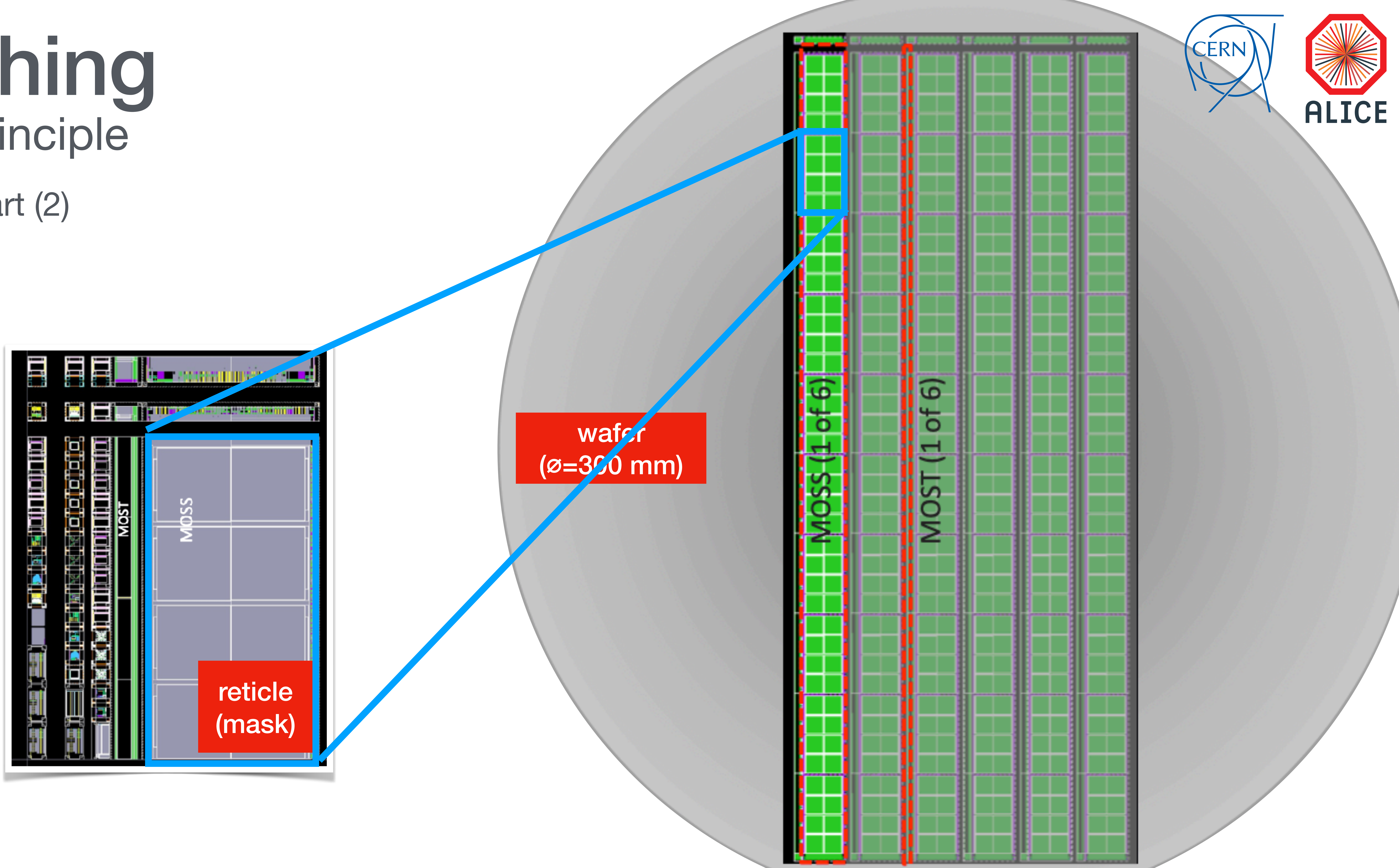
- central part (1)





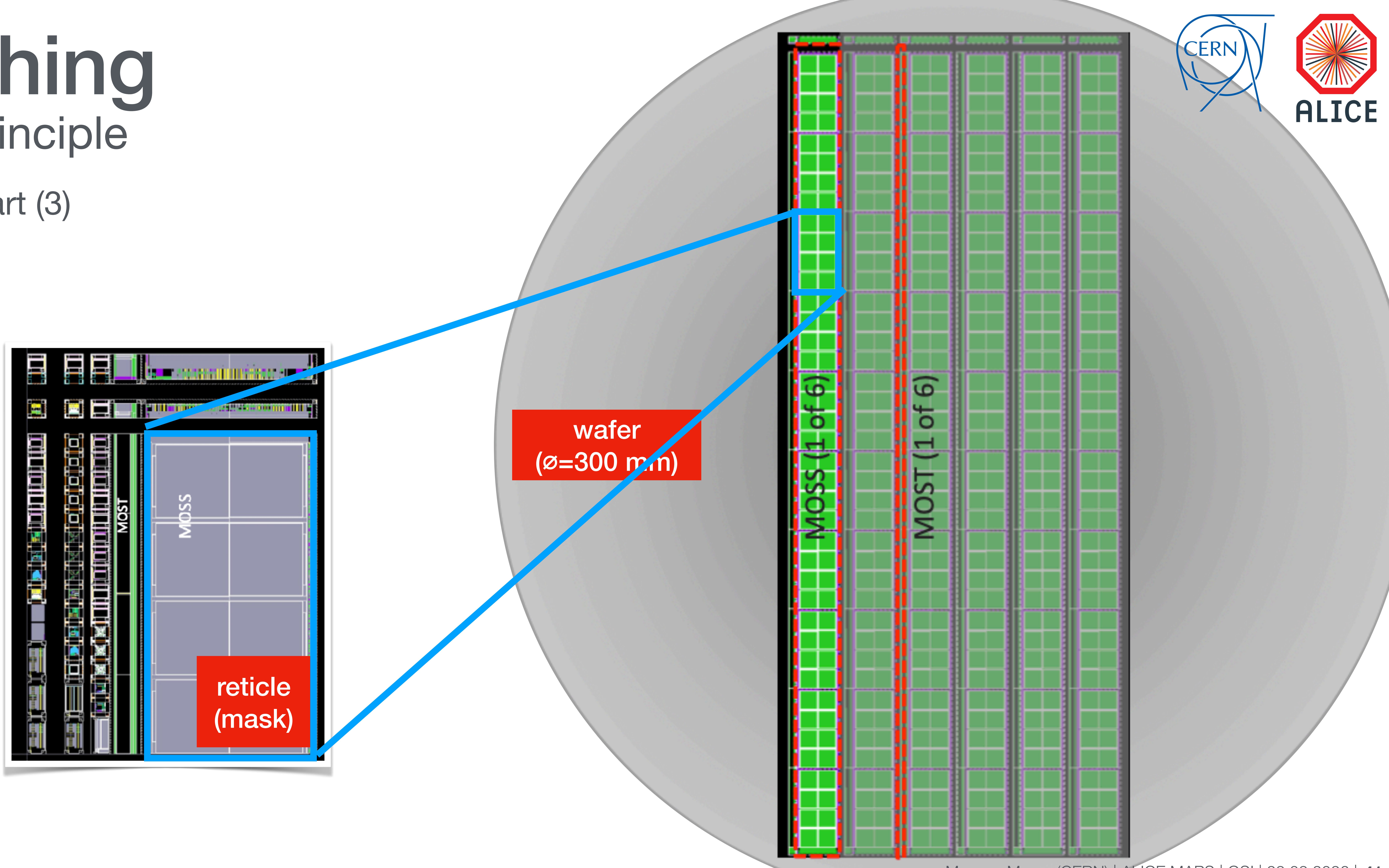
Stitching
rough principle

- central part (2)



Stitching
rough principle

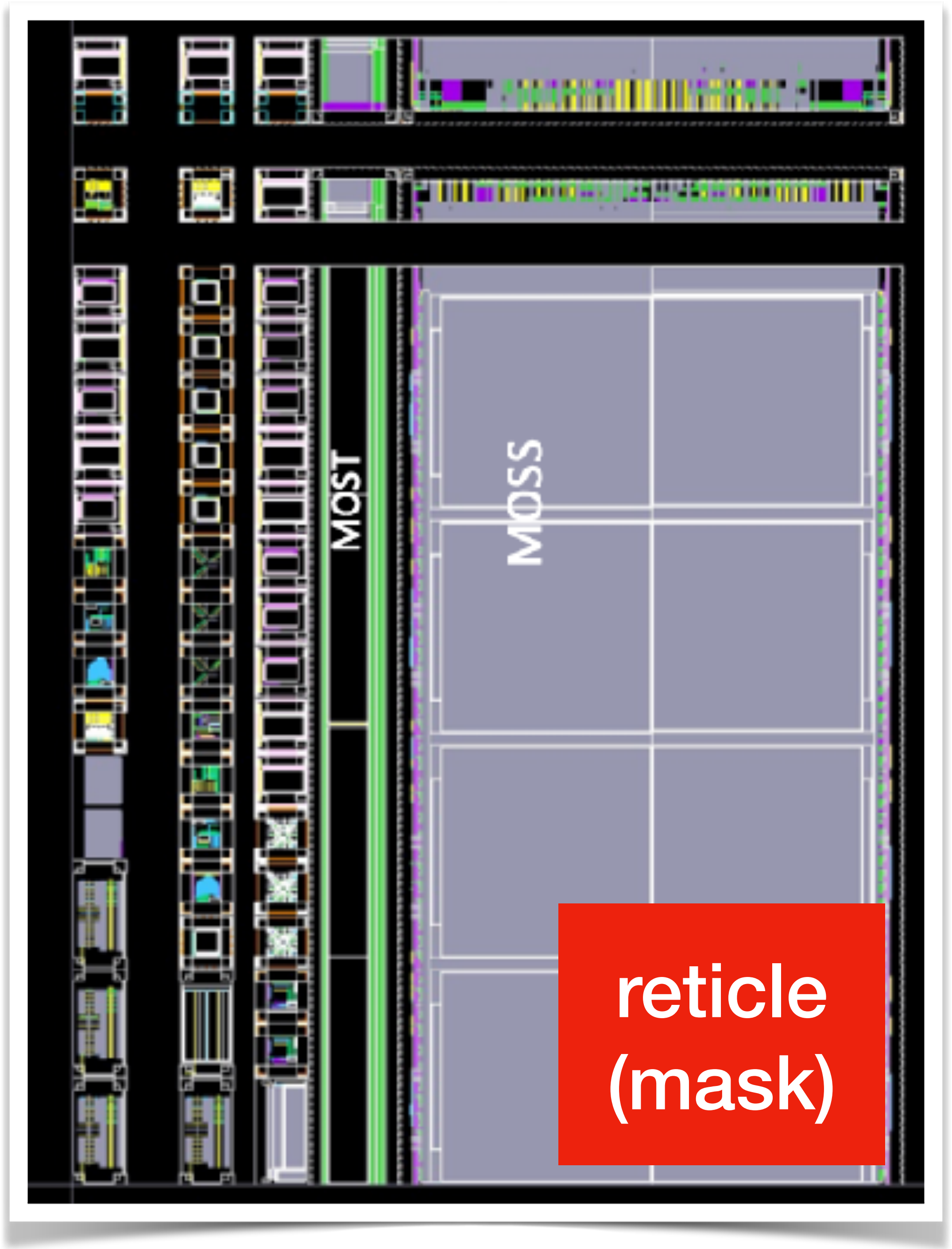
- central part (3)

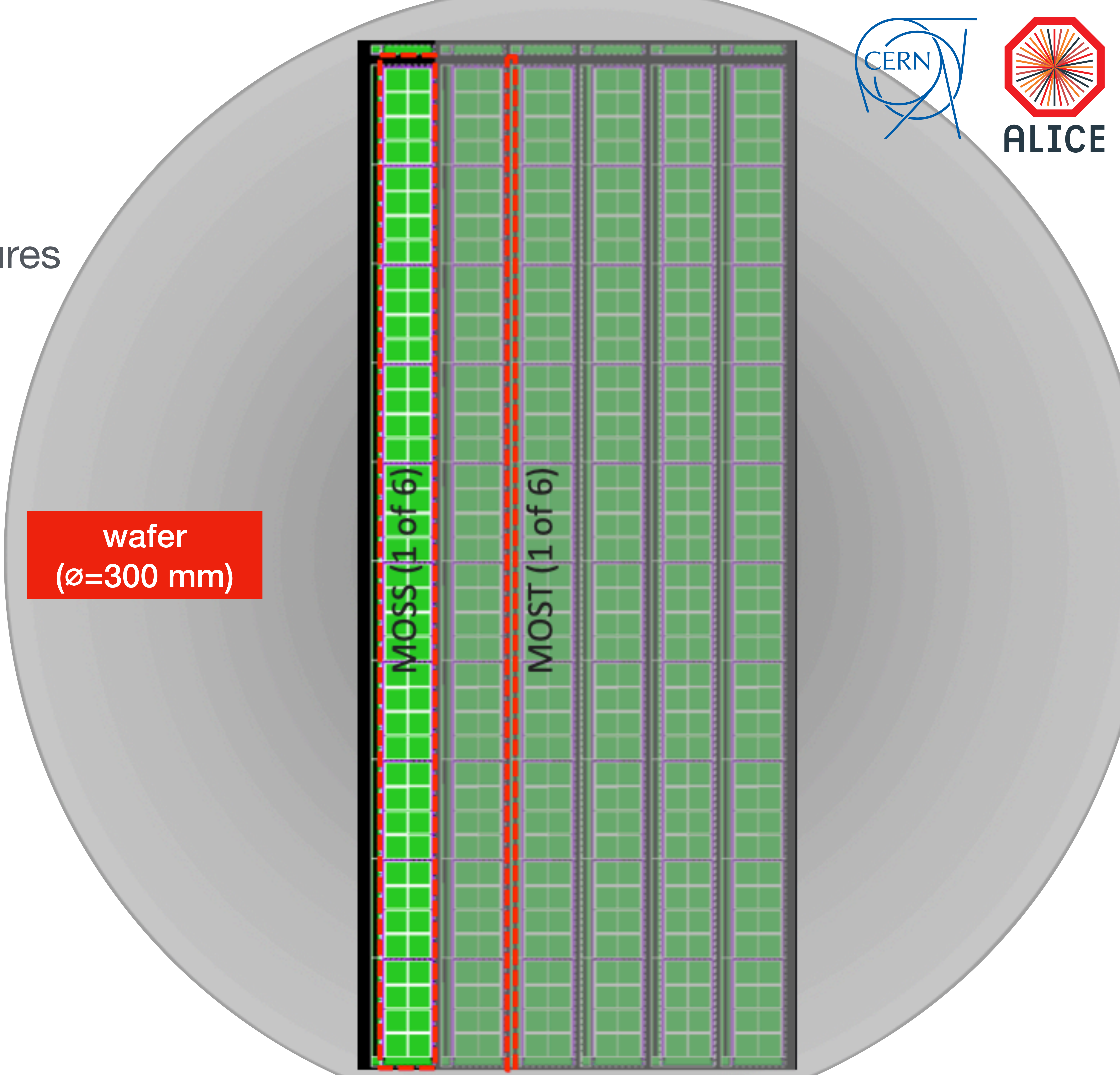


Stitching

rough principle

- final chip is the concatenation of all exposures





ITS3 chip development roadmap

past

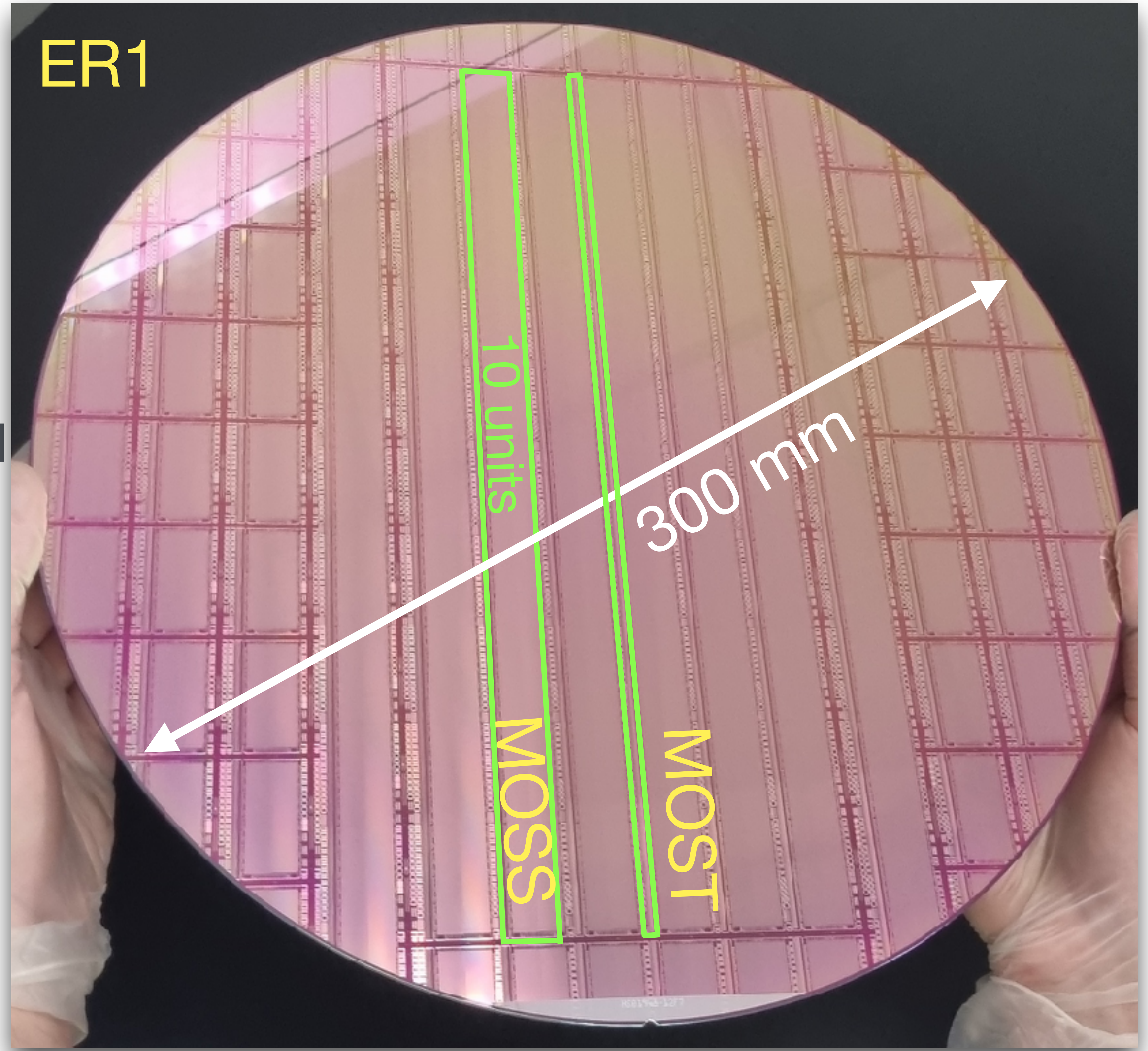
- **MLR1: first MAPS in TPSCo 65nm** (2021)
  - successfully qualified the 65nm process for particle detectors

present

- **ER1: first stitched MAPS** (2023)
  - large design “exercise”
  - “**MOSS**”: 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm²): conservative design, different pitches
  - “**MOST**”: 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm²): more dense design
- **ER2: “MOSAIX”** (2025)
  - full-scale, fully functional prototype
  - *currently being tested*

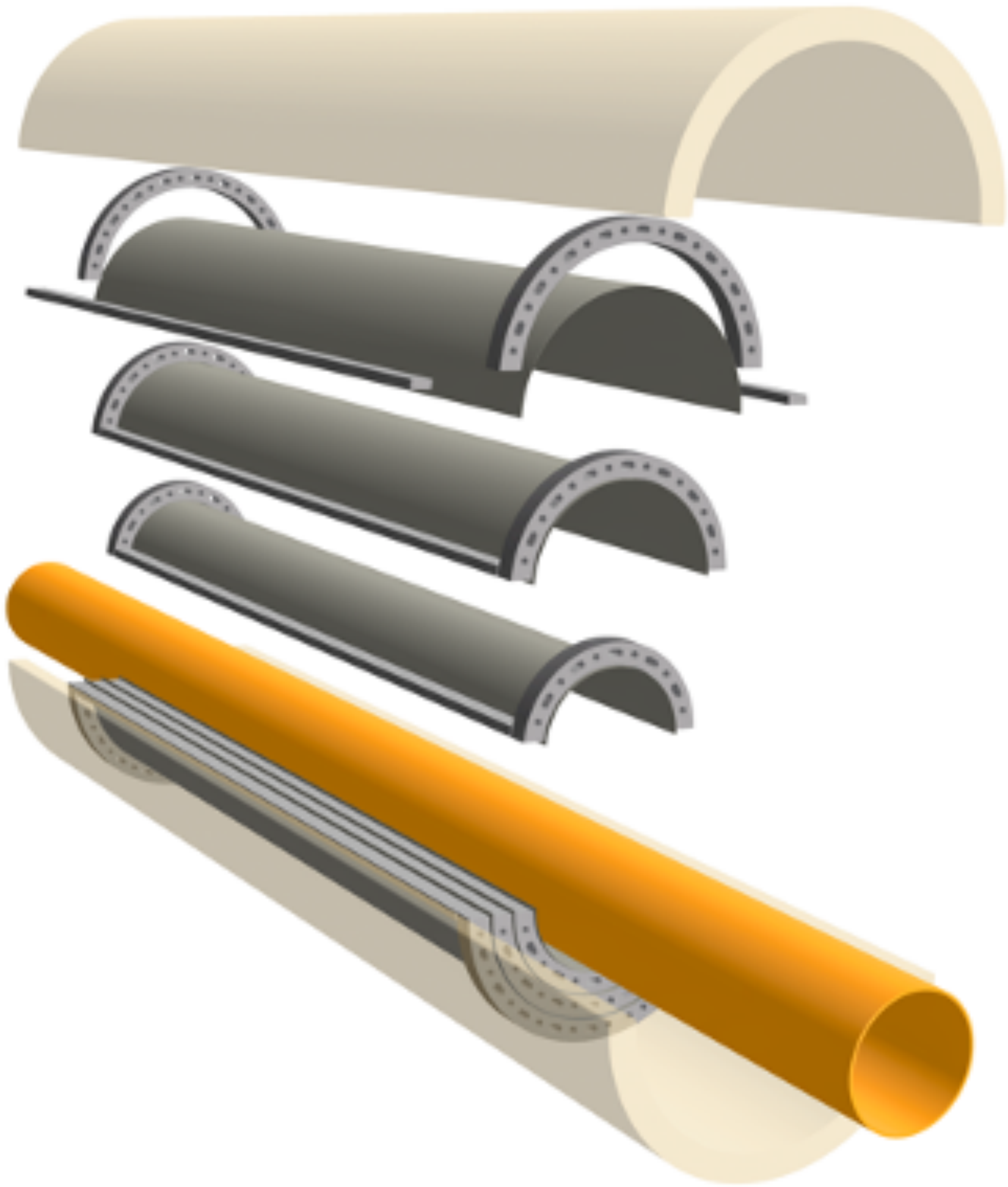
future

- **ER3: ITS3 sensor production** (2026)

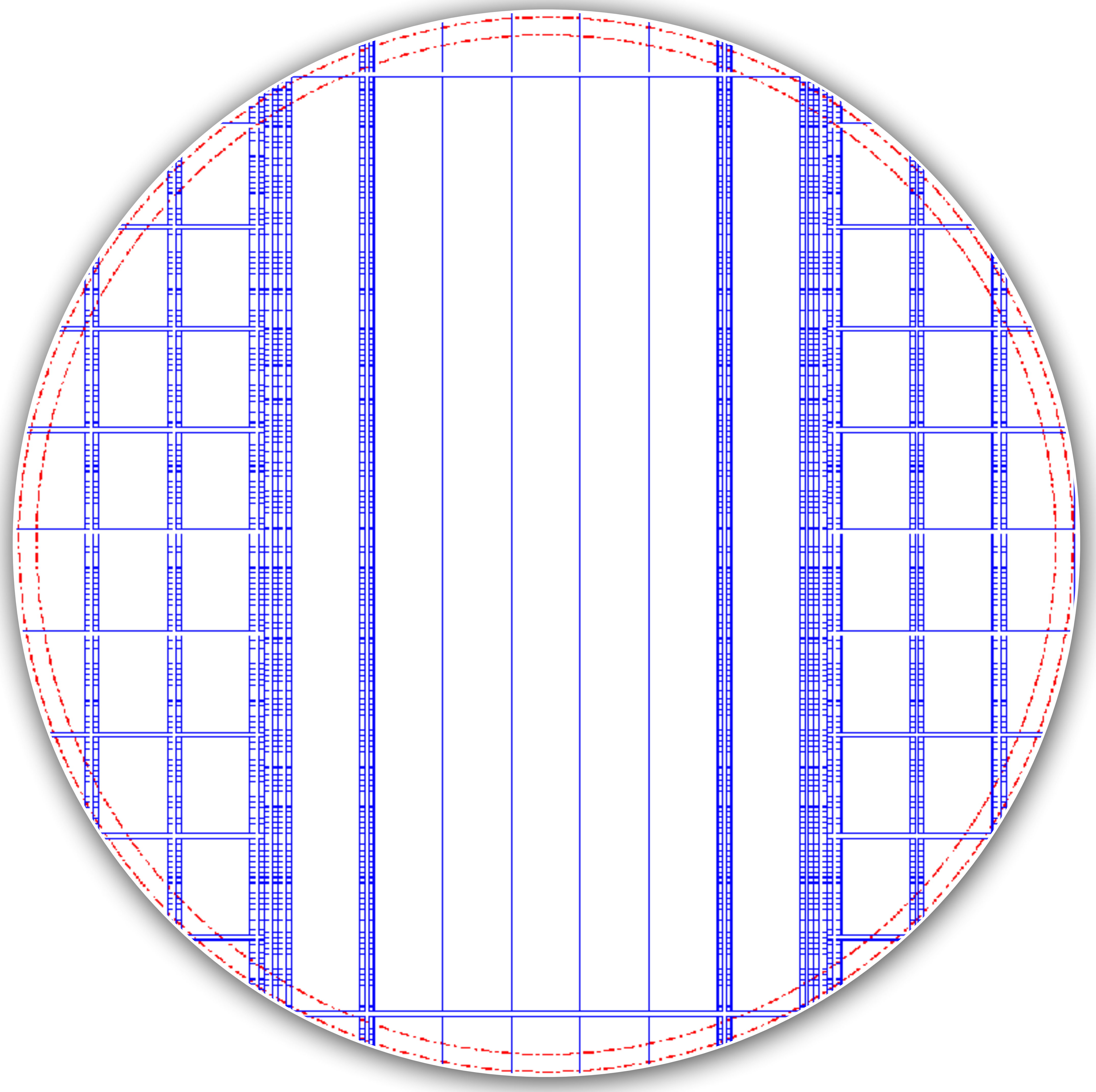


ER2: MOSAIX

the full-scale prototype

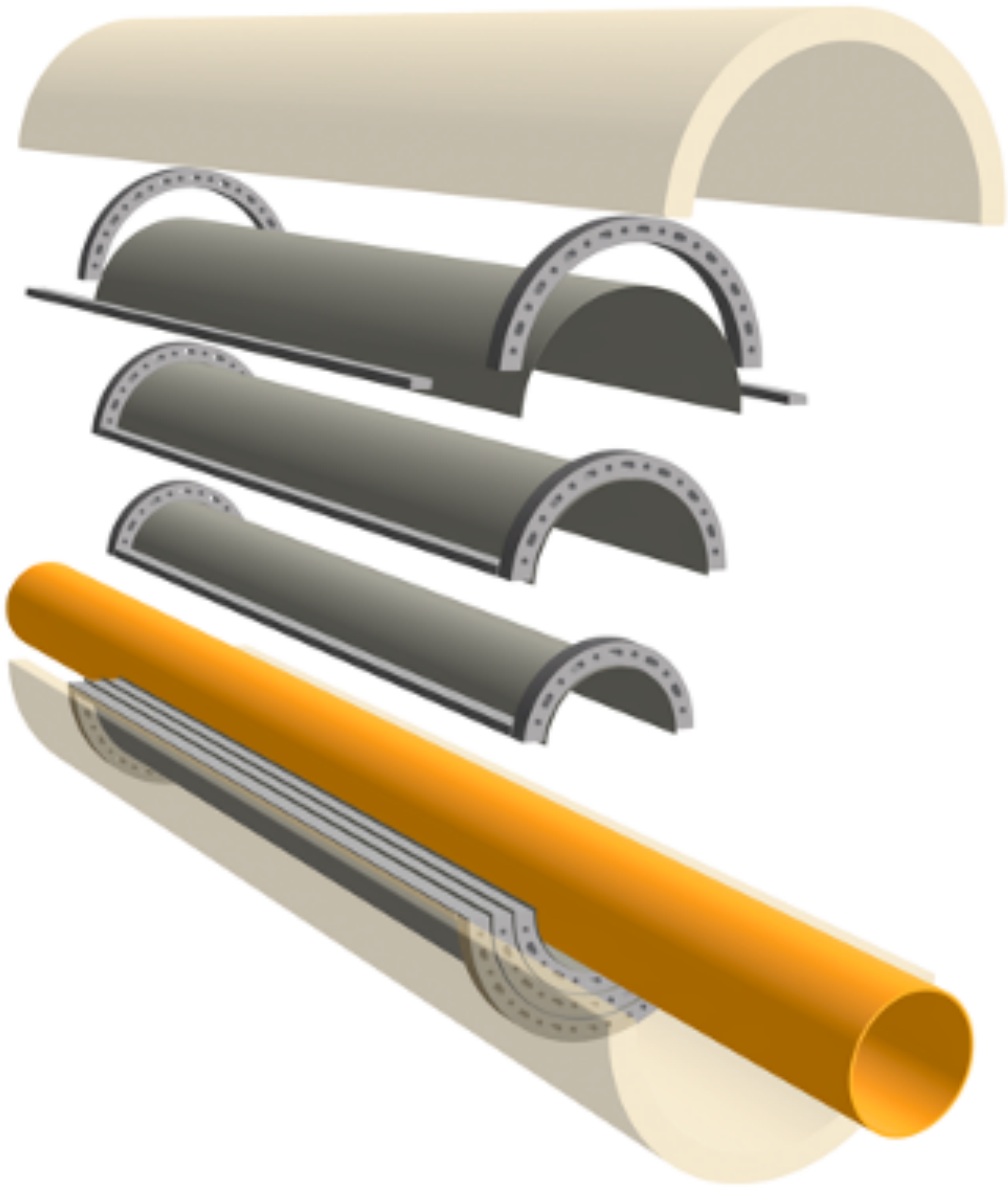


ER2 wafer layout

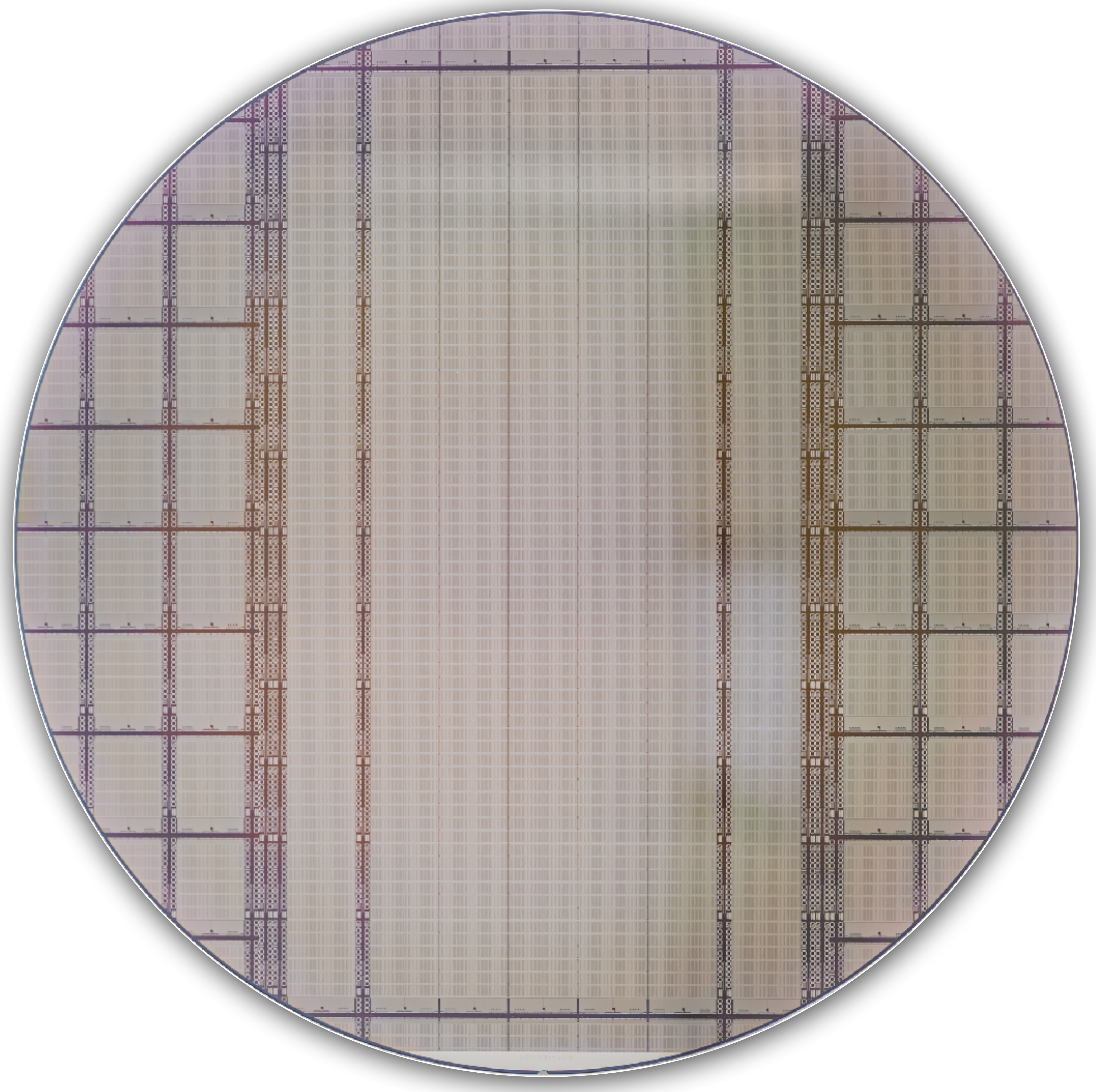


ER2: MOSAIX

the full-scale prototype

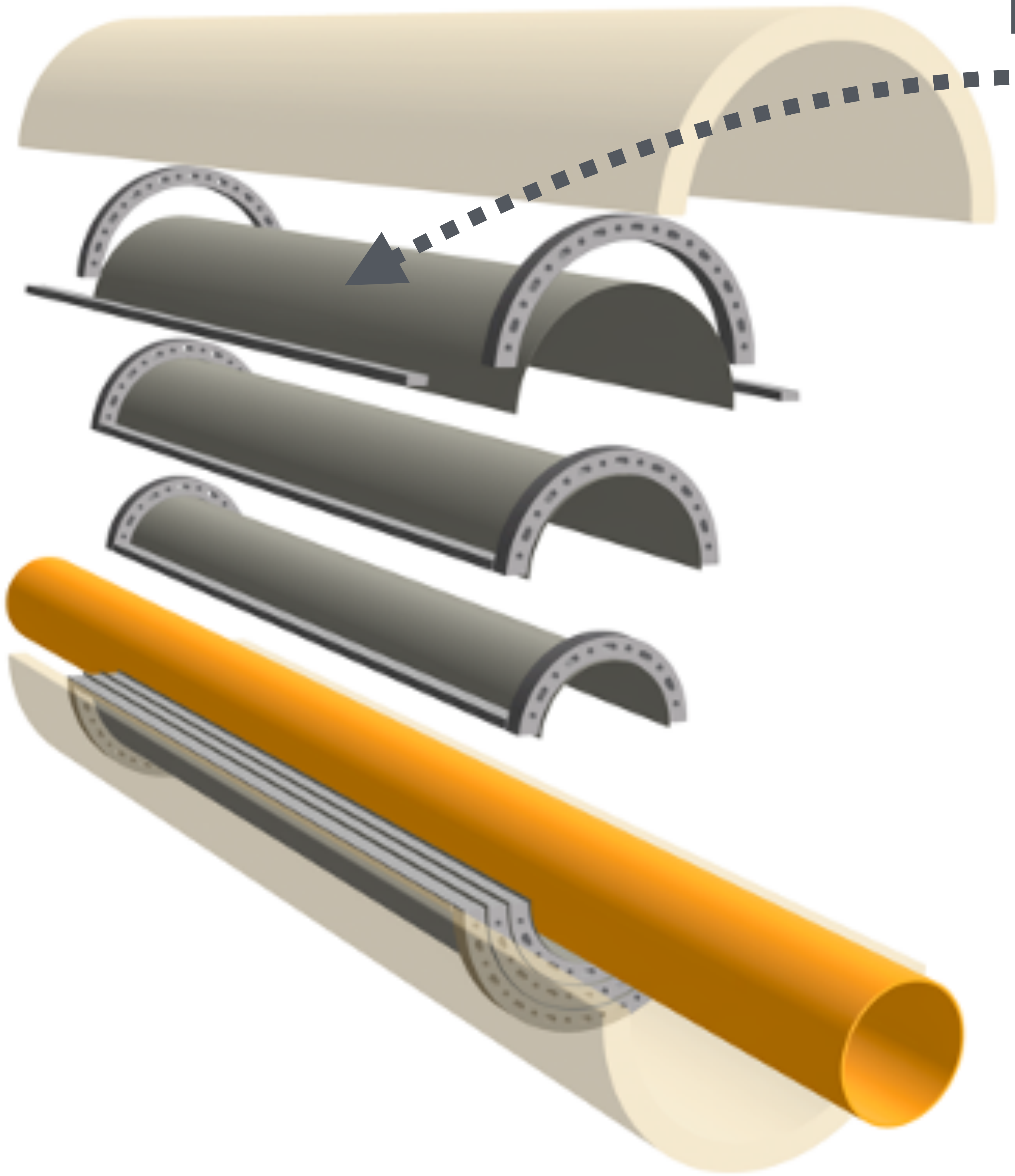


ER2 wafer layout



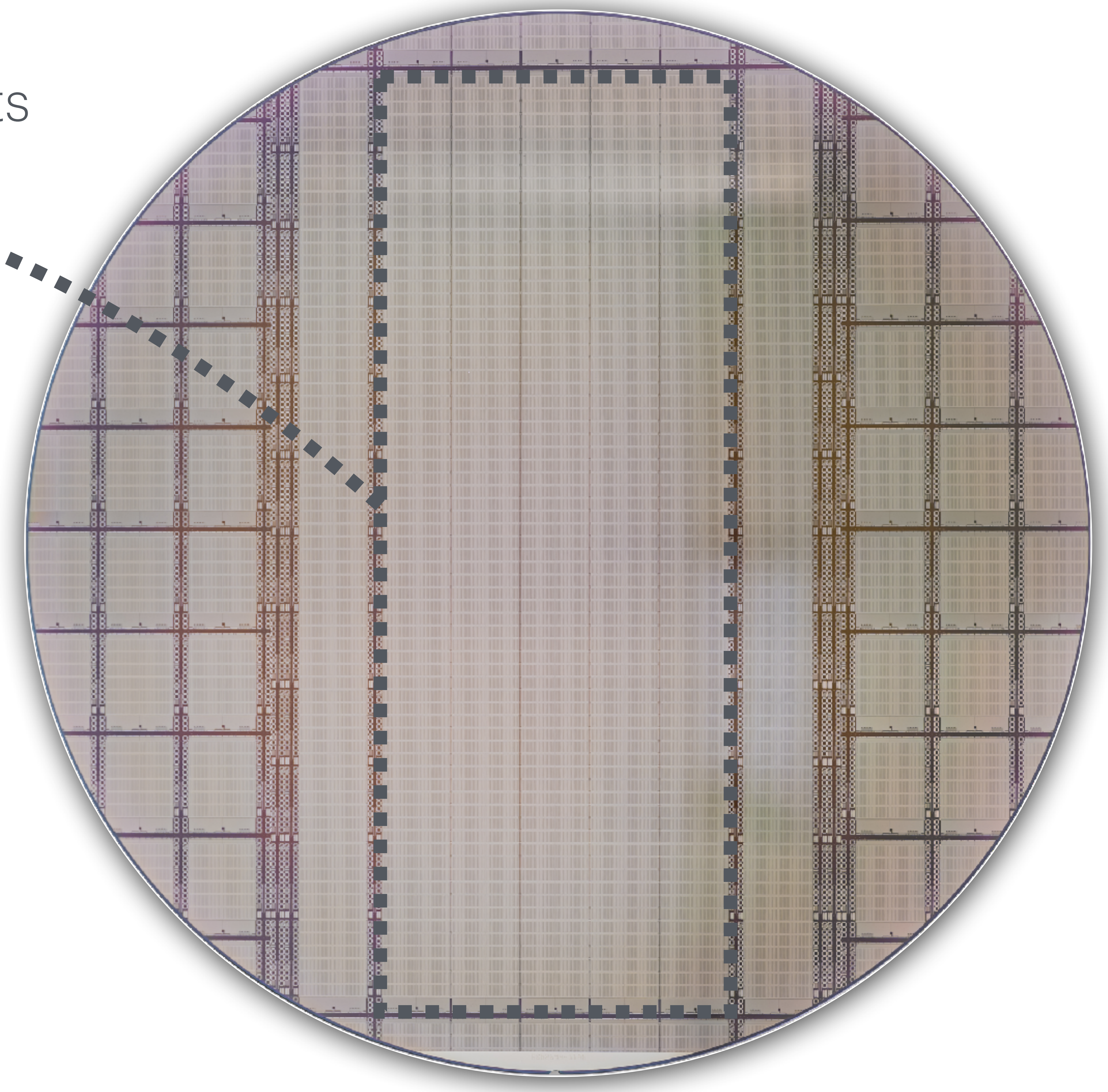
ER2: MOSAIX

the full-scale prototype



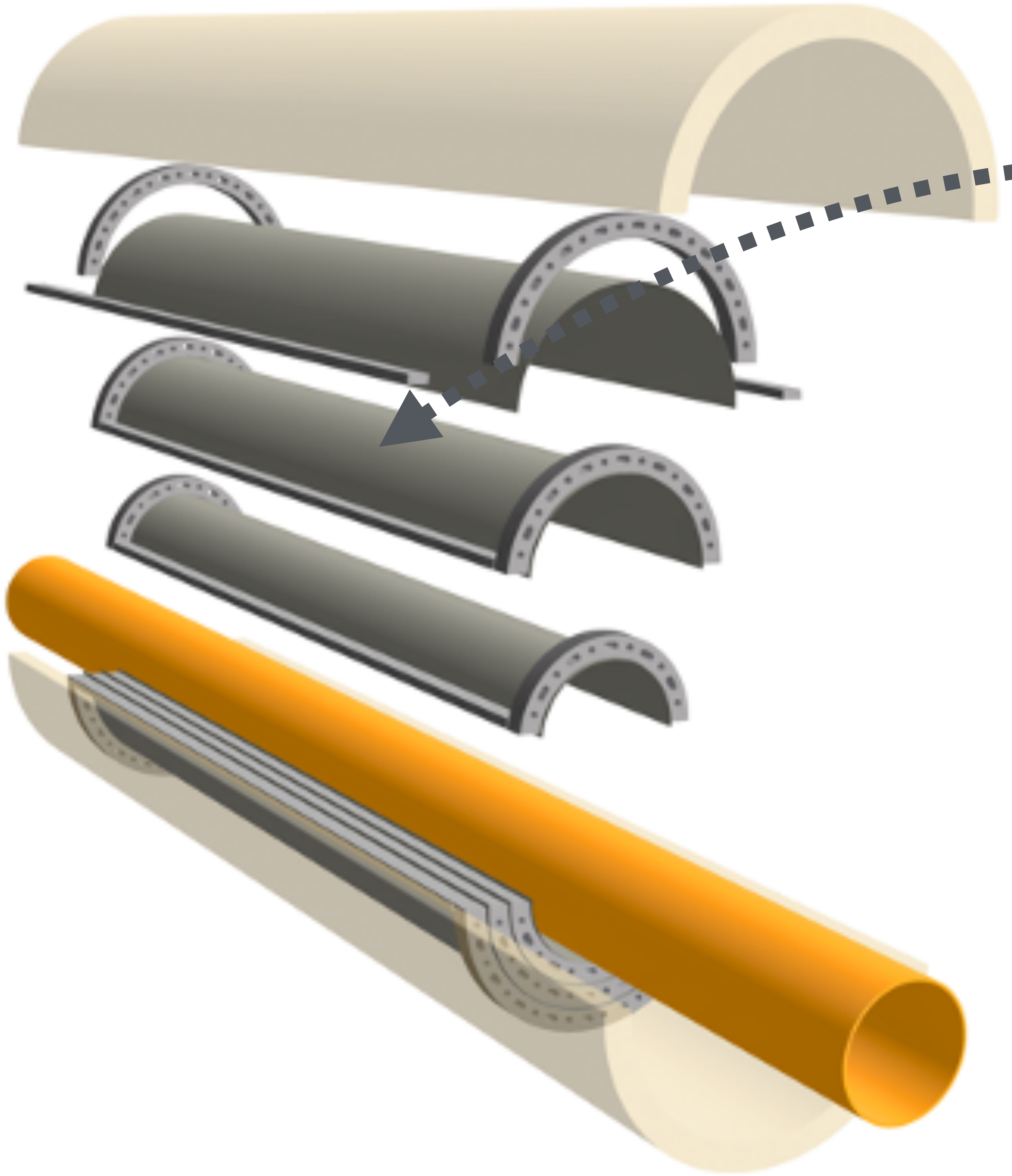
Layer 2: 5 segments

ER2 wafer layout



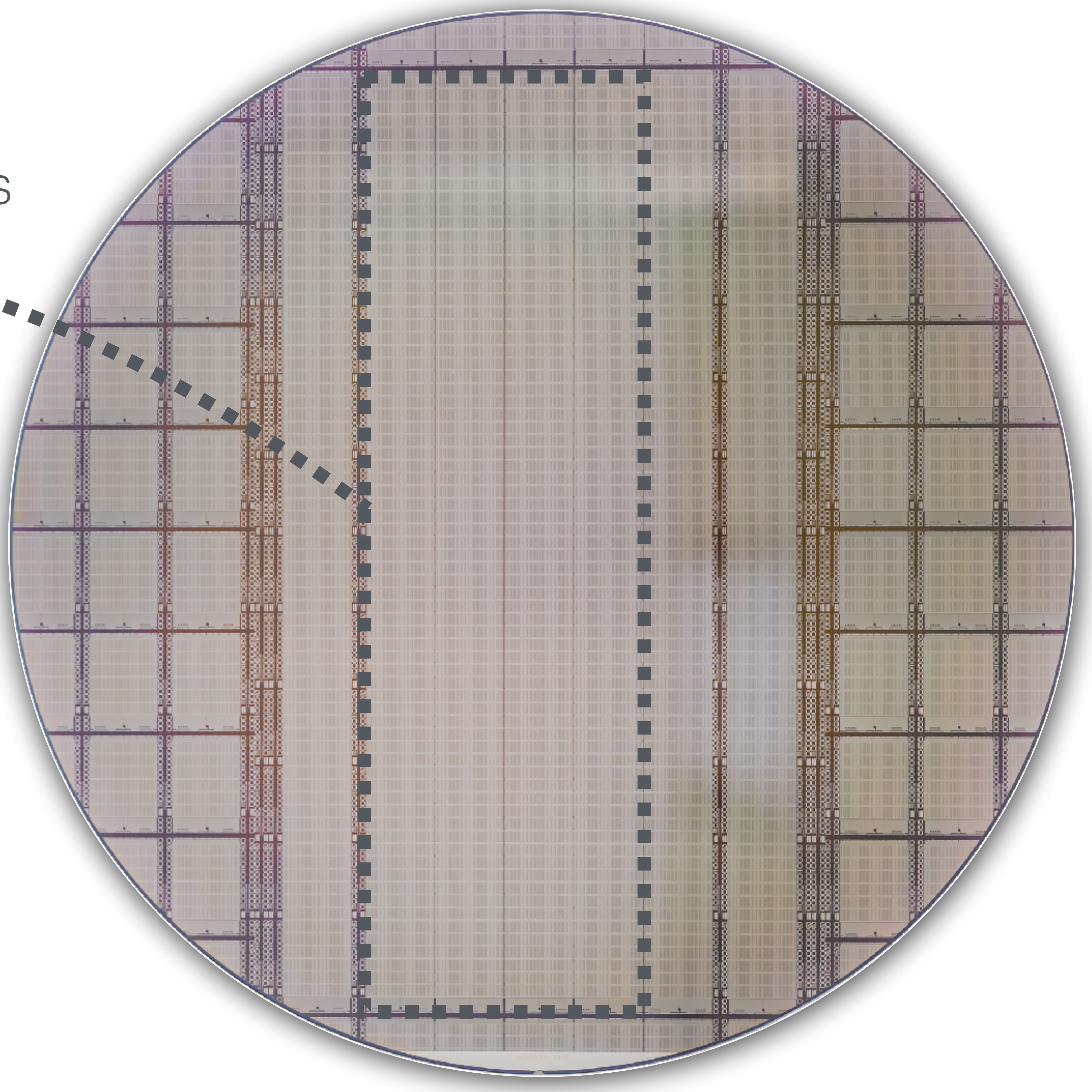
ER2: MOSAIX

the full-scale prototype



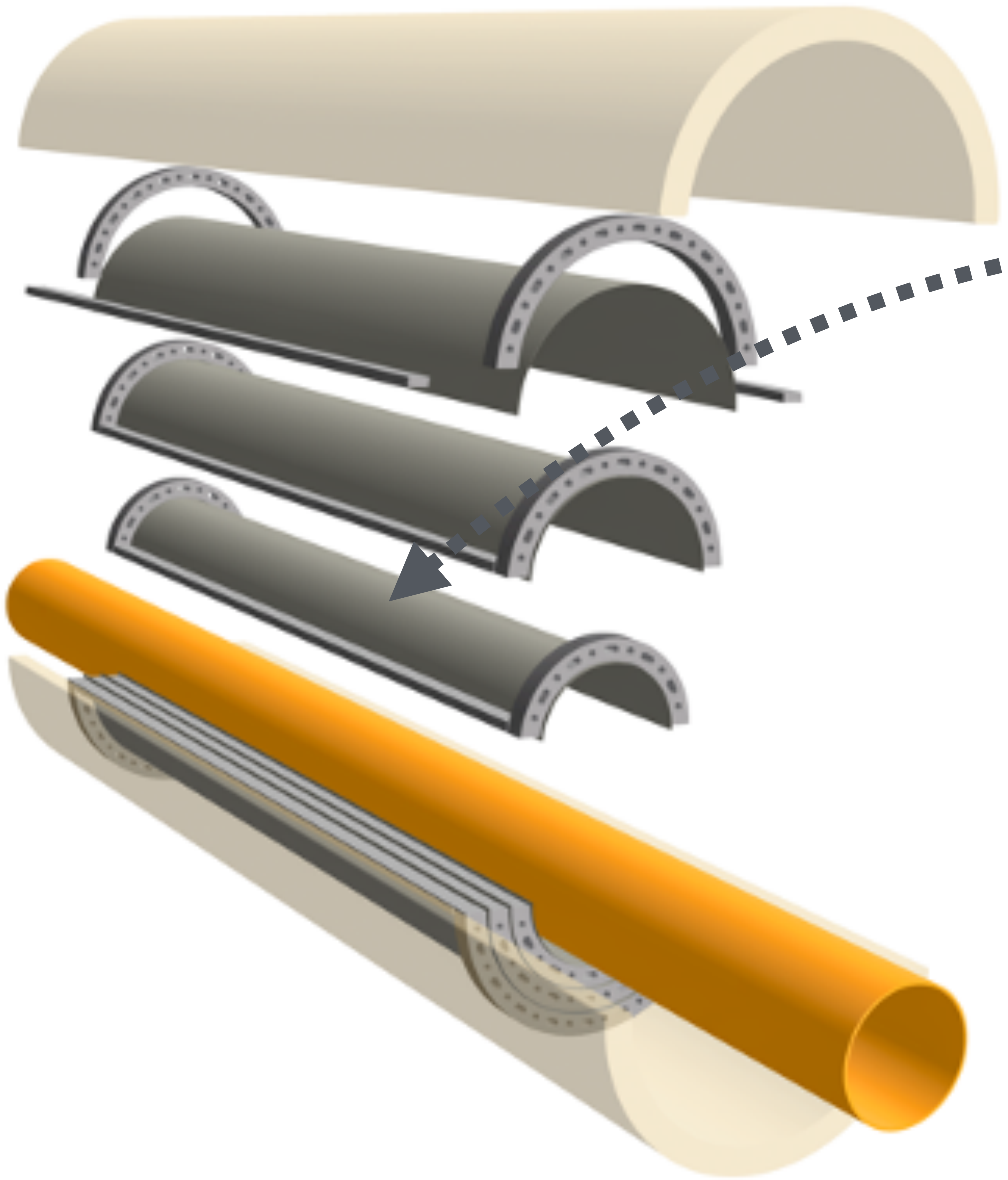
Layer 1: 4 segments

ER2 wafer layout



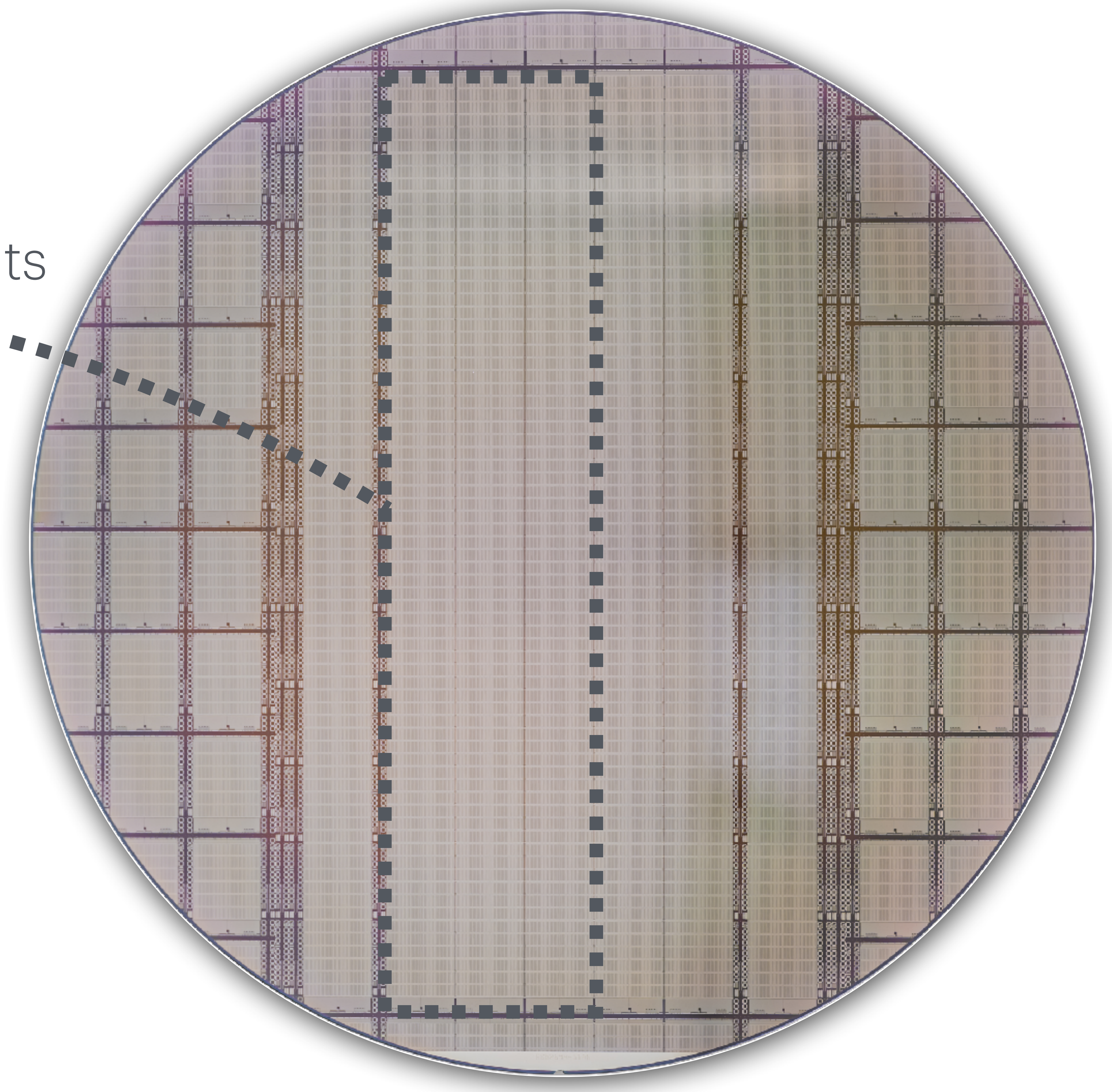
ER2: MOSAIX

the full-scale prototype



Layer 0: 3 segments

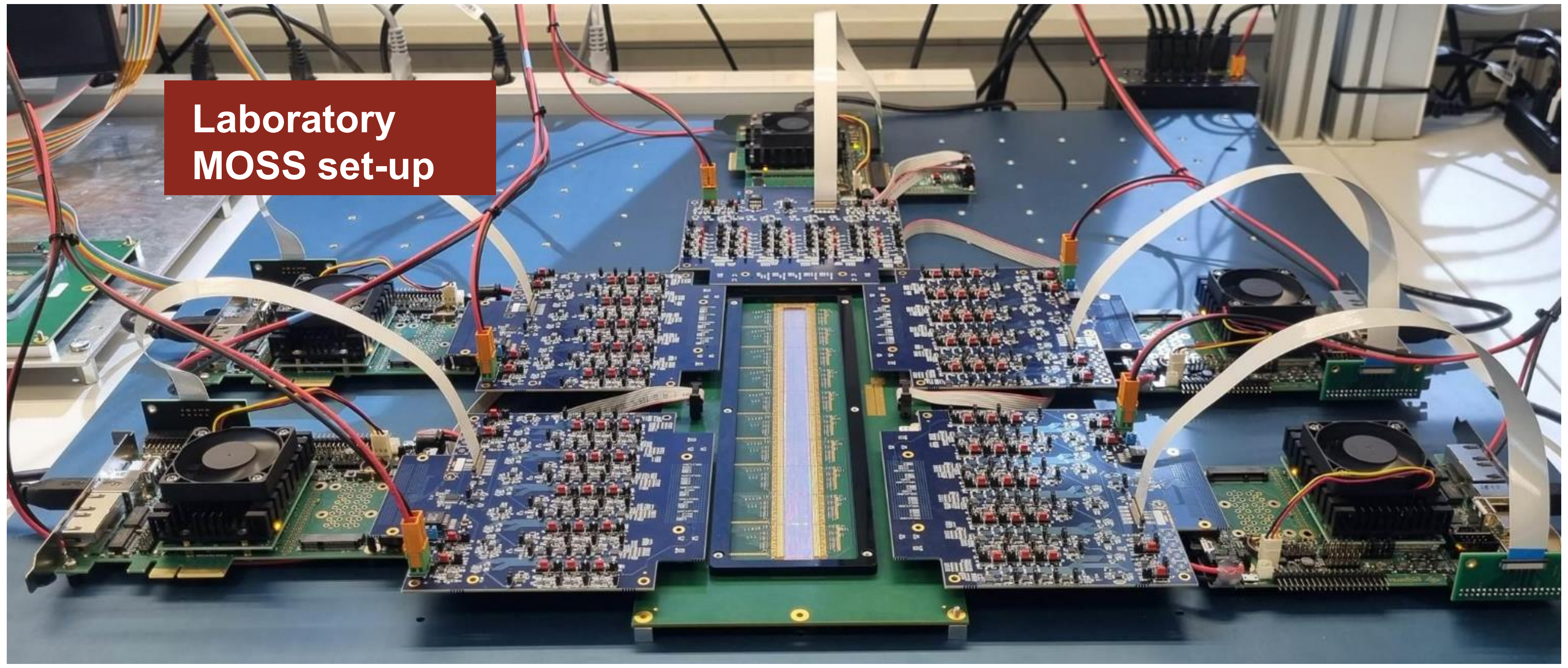
ER2 wafer layout



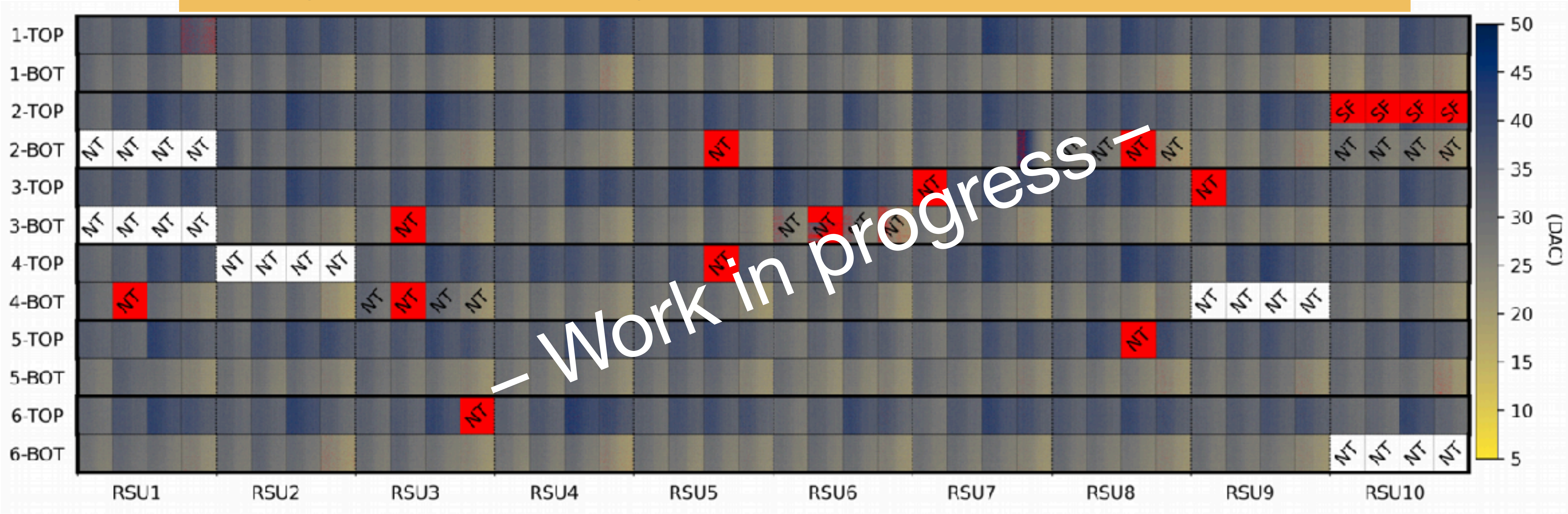
ER1: MOSS

understanding of yield

- **Detailed understanding** of yield is gained with first prototypes
- **Mitigation** strategy based on:
  - hardening critical circuitry
  - fine-grained isolation of eventually malfunctioning blocks
- **Very encouraging** results
  - extrapolated functional yield >98%



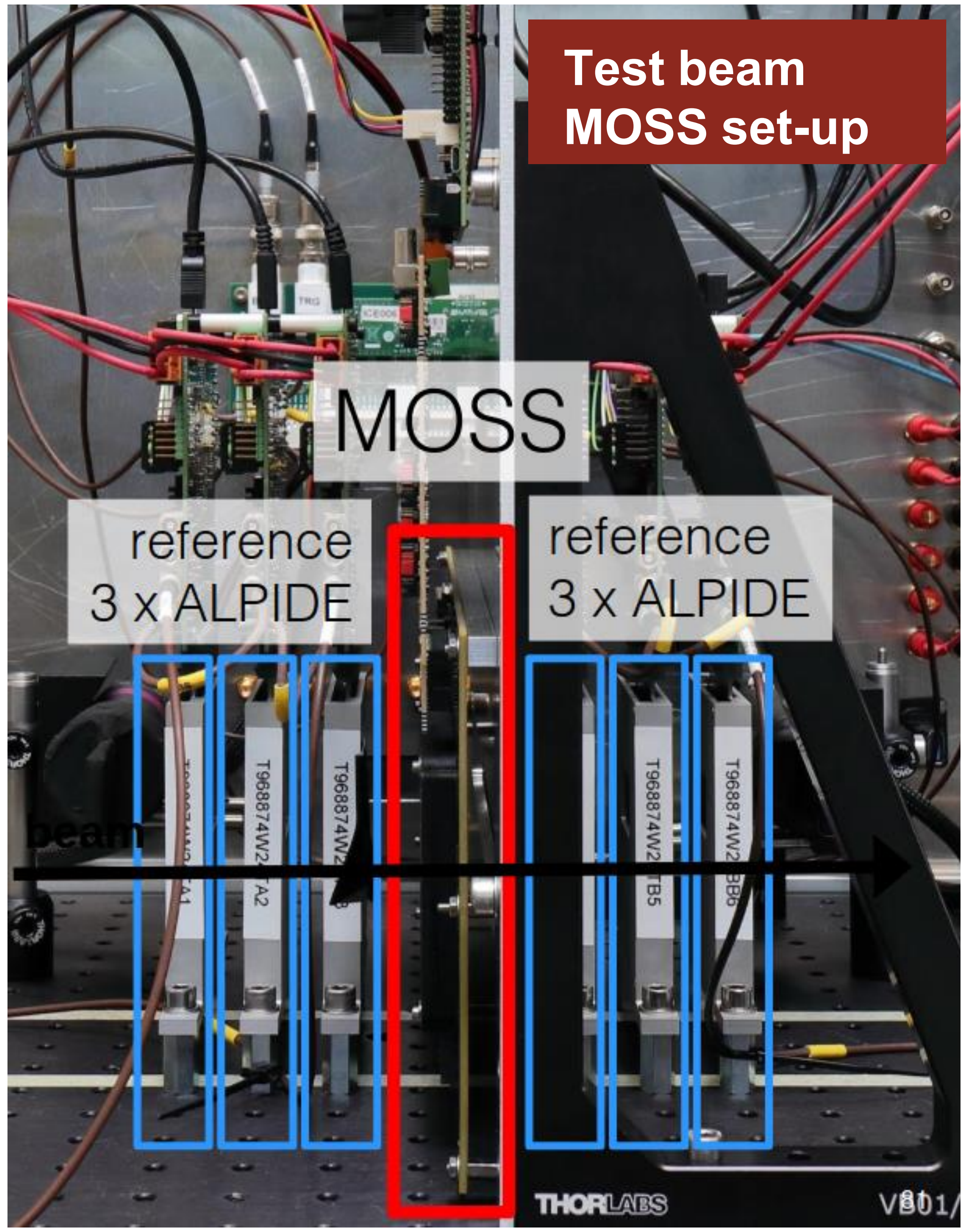
Example threshold map of 40 MPixel over 10x26 cm of silicon

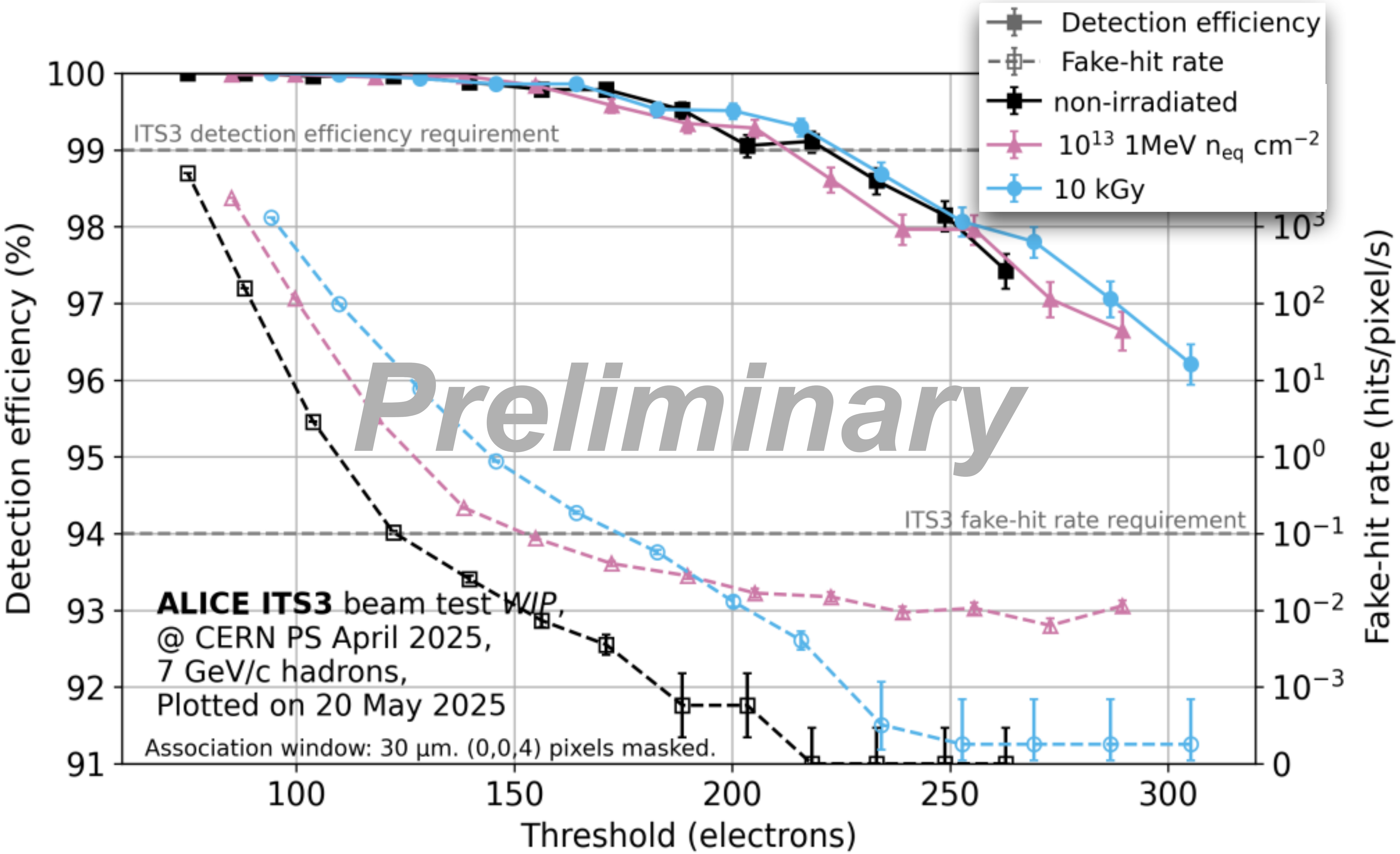


[doi:10.1016/j.nima.2026.171297]

[doi:10.1109/TNS.2026.3671605]

ER1: MOSS
operation in beam tests



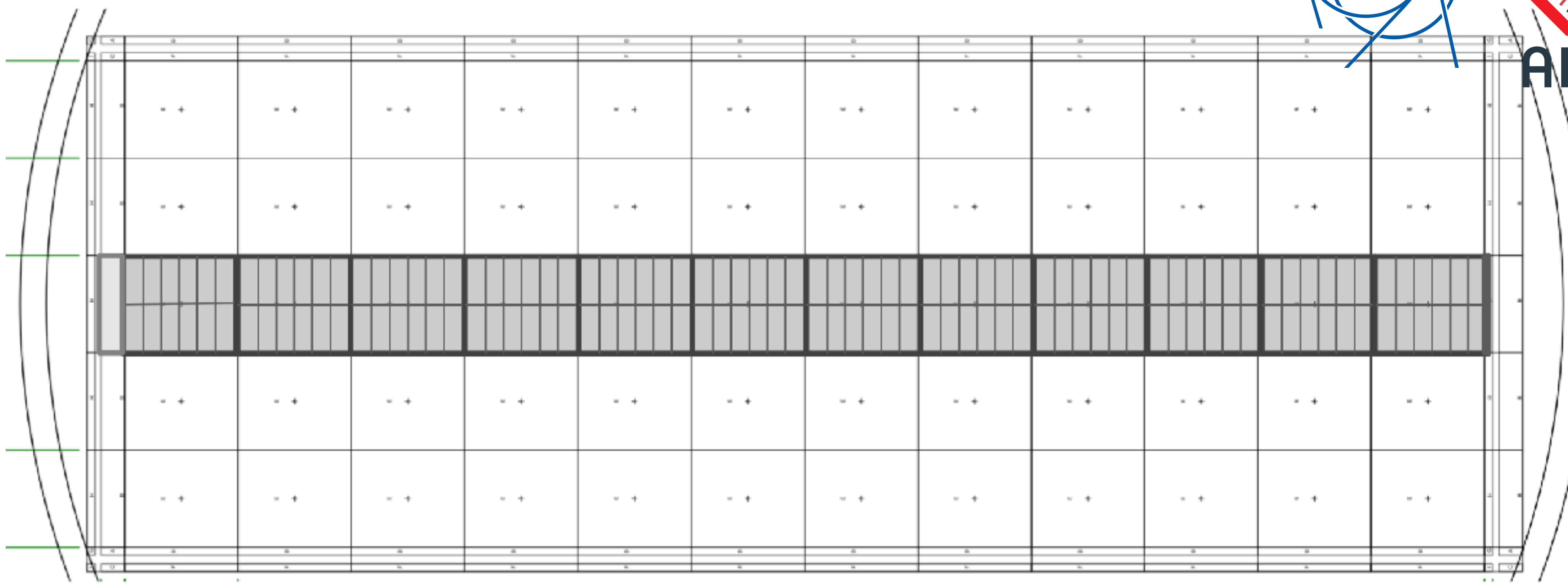


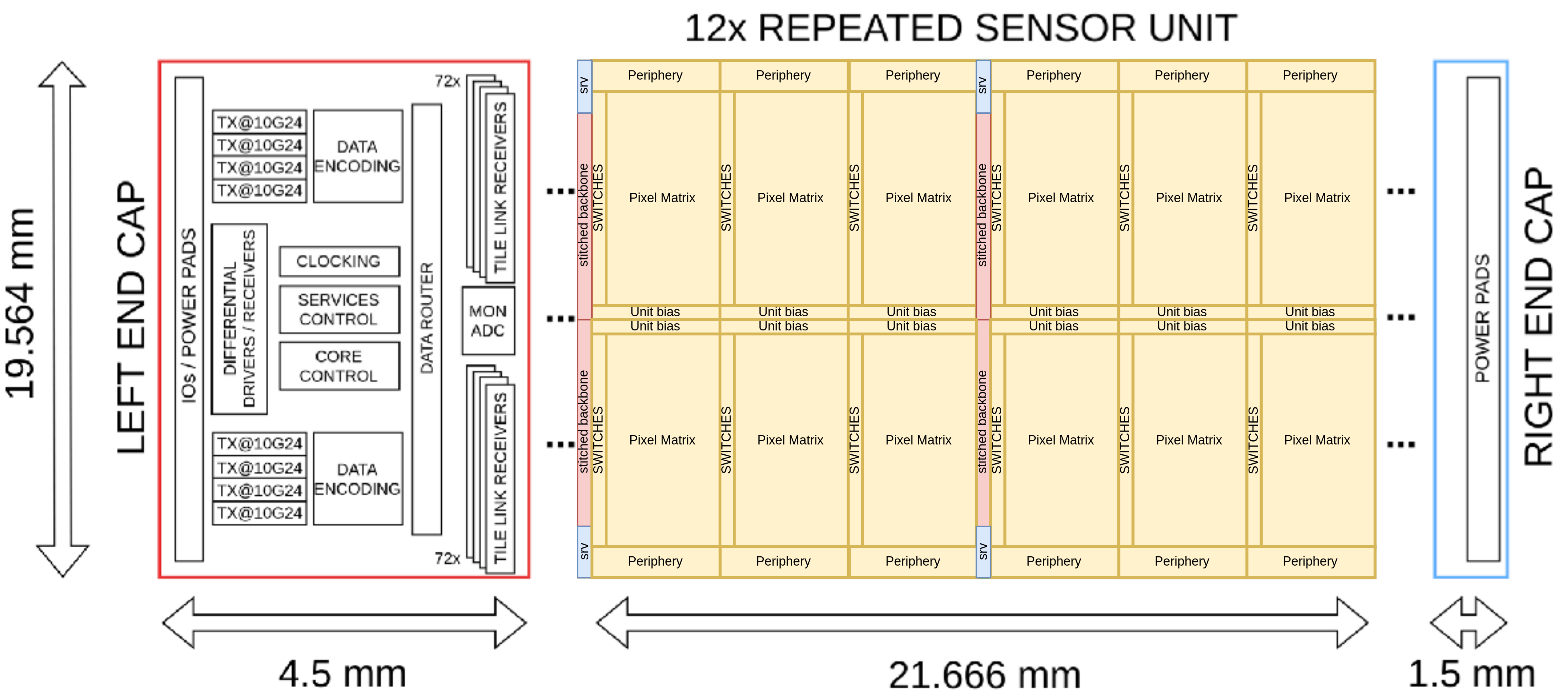
- Prototypes **work well** in beam tests
- **Operational margin** (efficiency >99% and fake-hit rate <10^{-6}) is maintained at ALICE radiation levels

ER2: MOSAIX

architecture

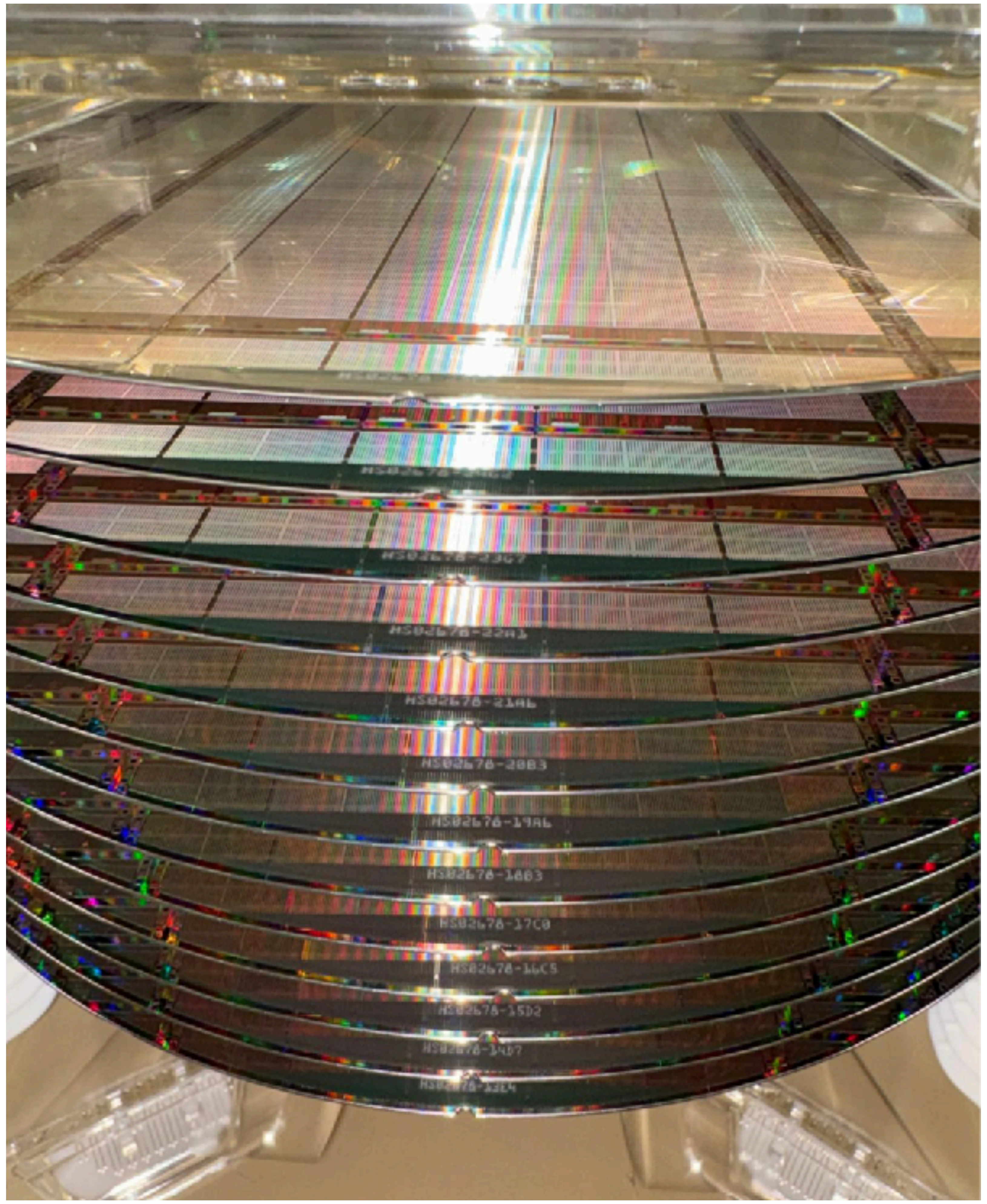
- Same size and full functionality of final chip
  - "module on a chip"
  - including data/event management and high-speed links
- High-granularity power network
  - 144 units can individually be switched off in case of malfunctioning
- 12 different pixel/matrix variants to fine tune operational margins
  - pitch: 20.8 × 22.8 μm²
- Wafers back from production!

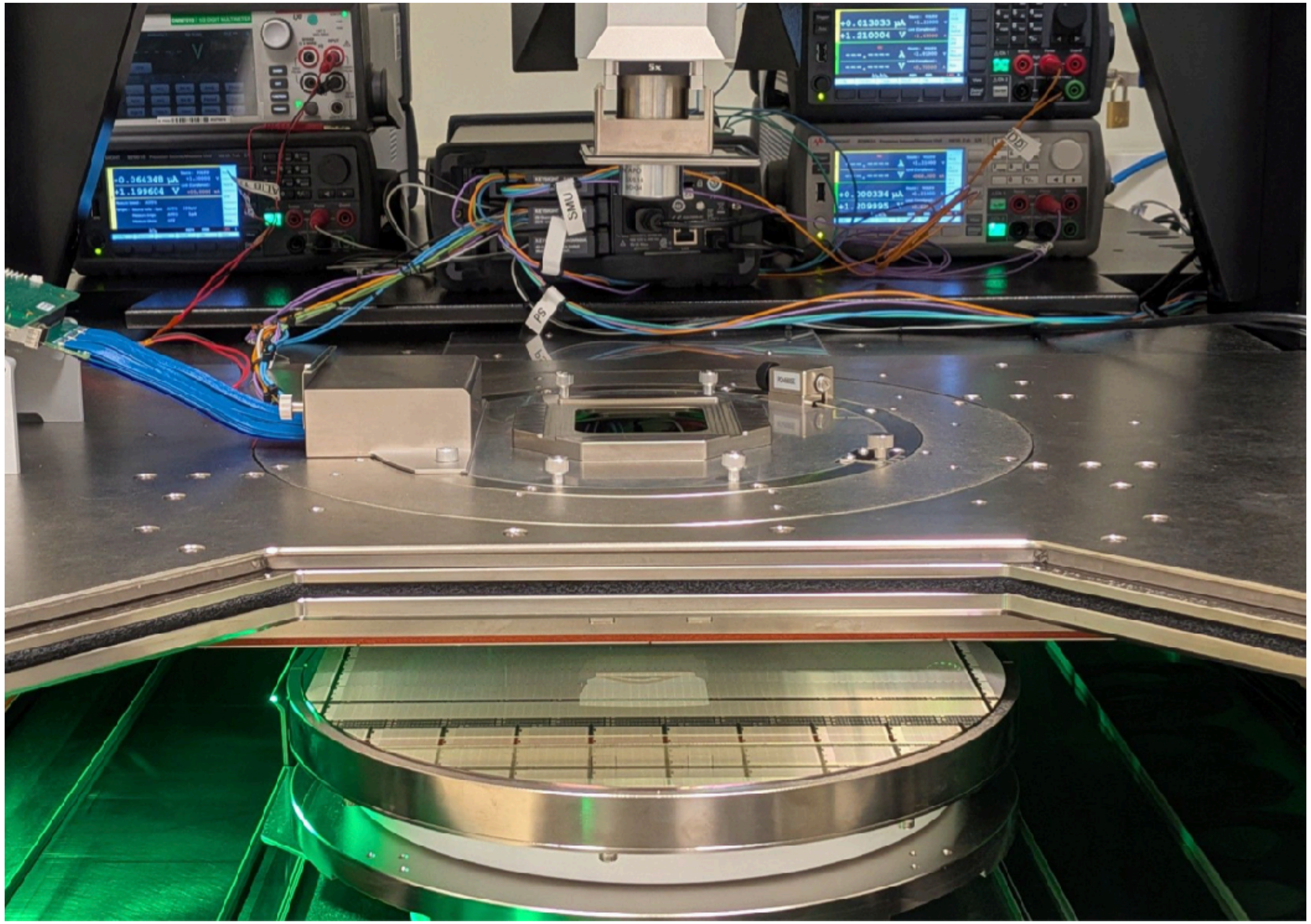




ER2 tests

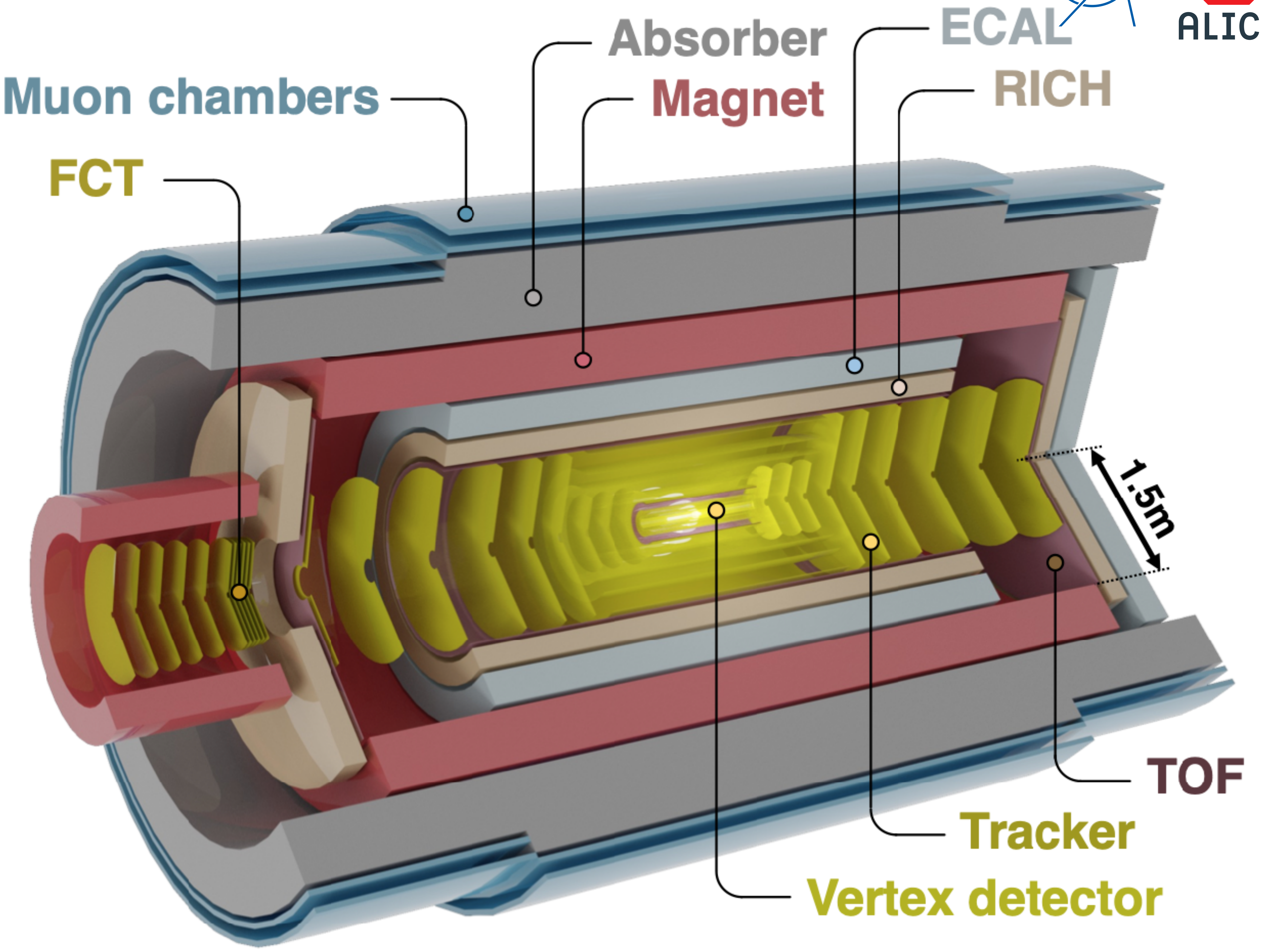
- are ongoing ;)





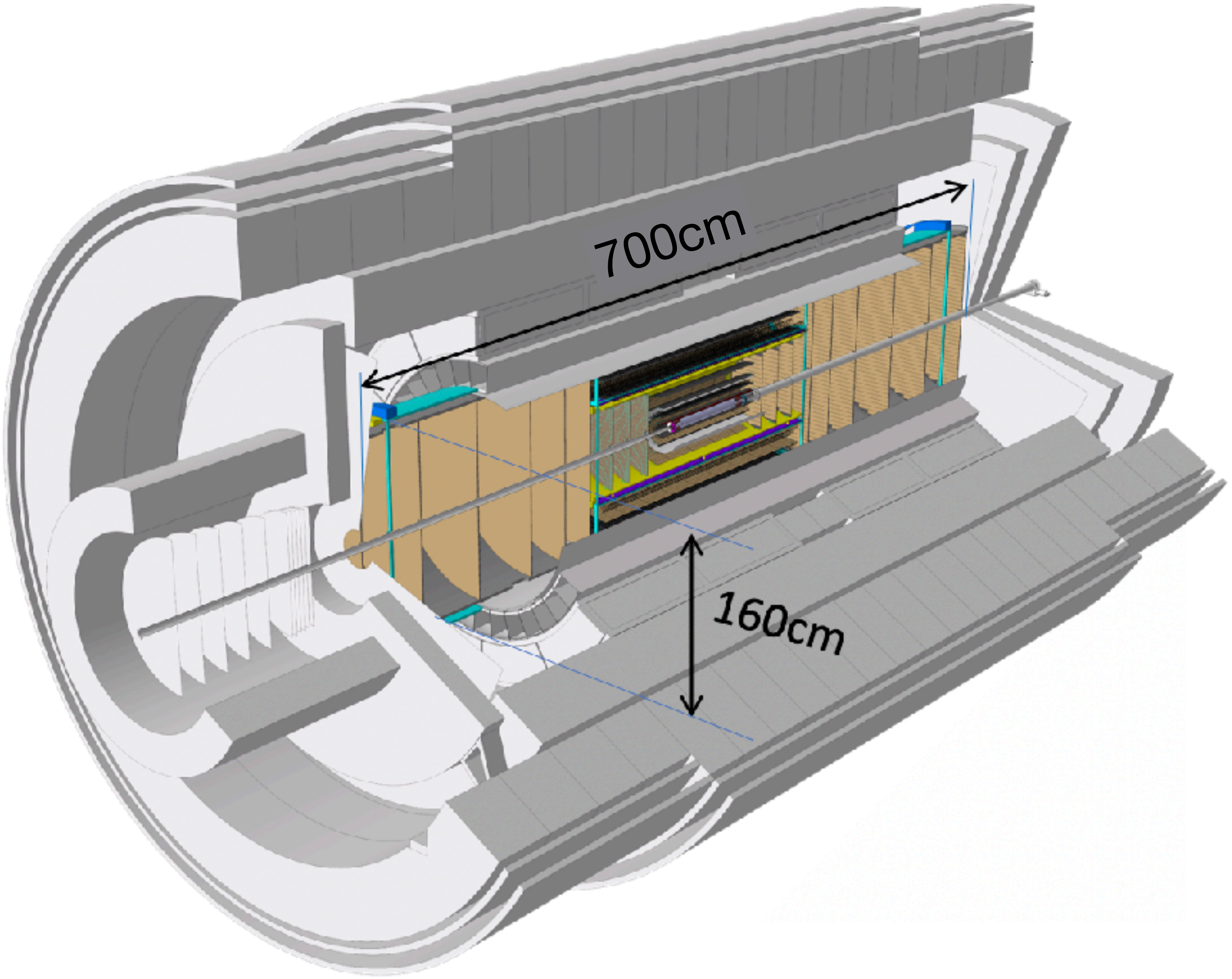
ALICE 3

[LOI: doi:10.48550/arXiv.2211.02491]



ALICE 3

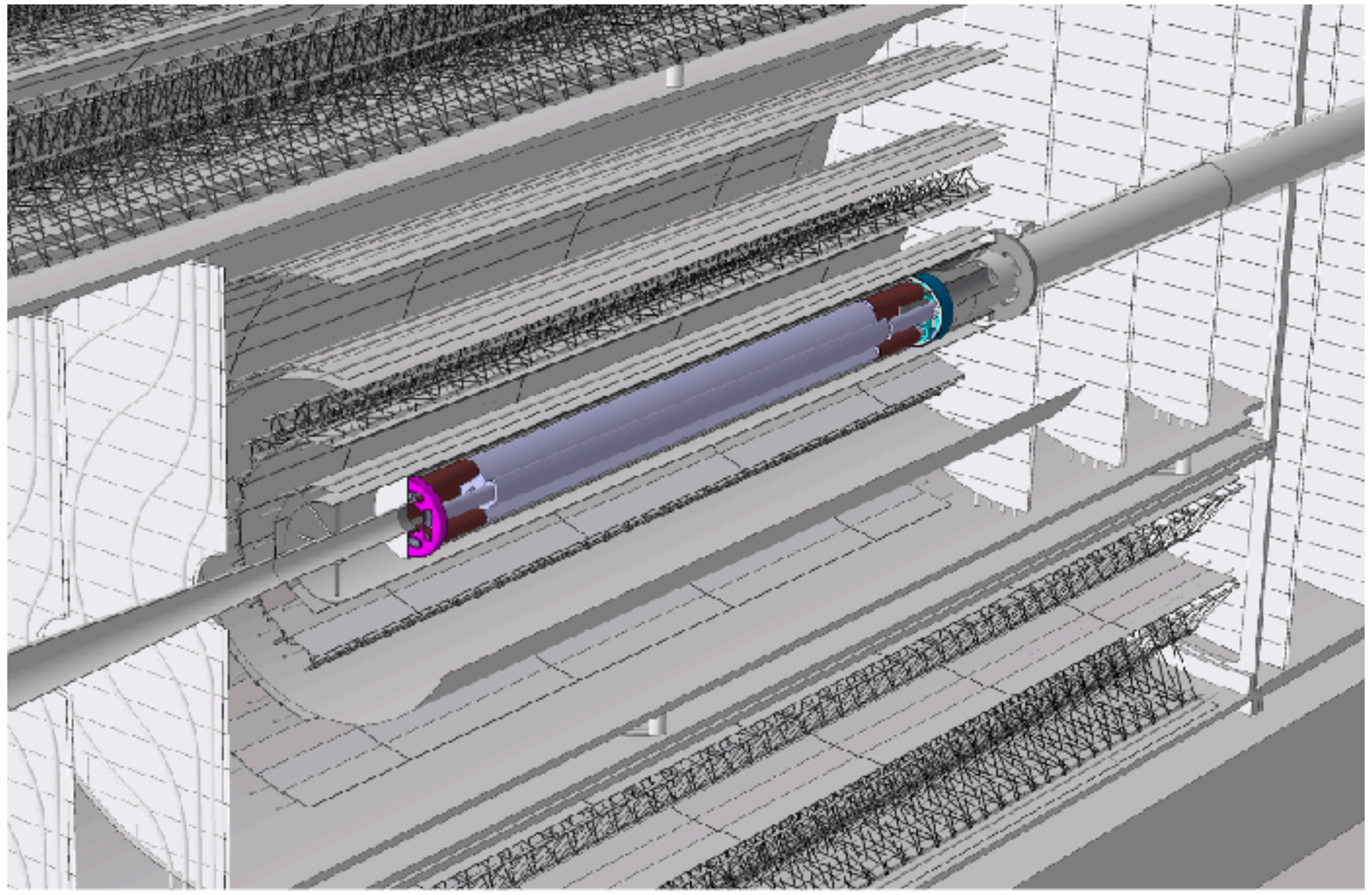
Middle and Outer Layers

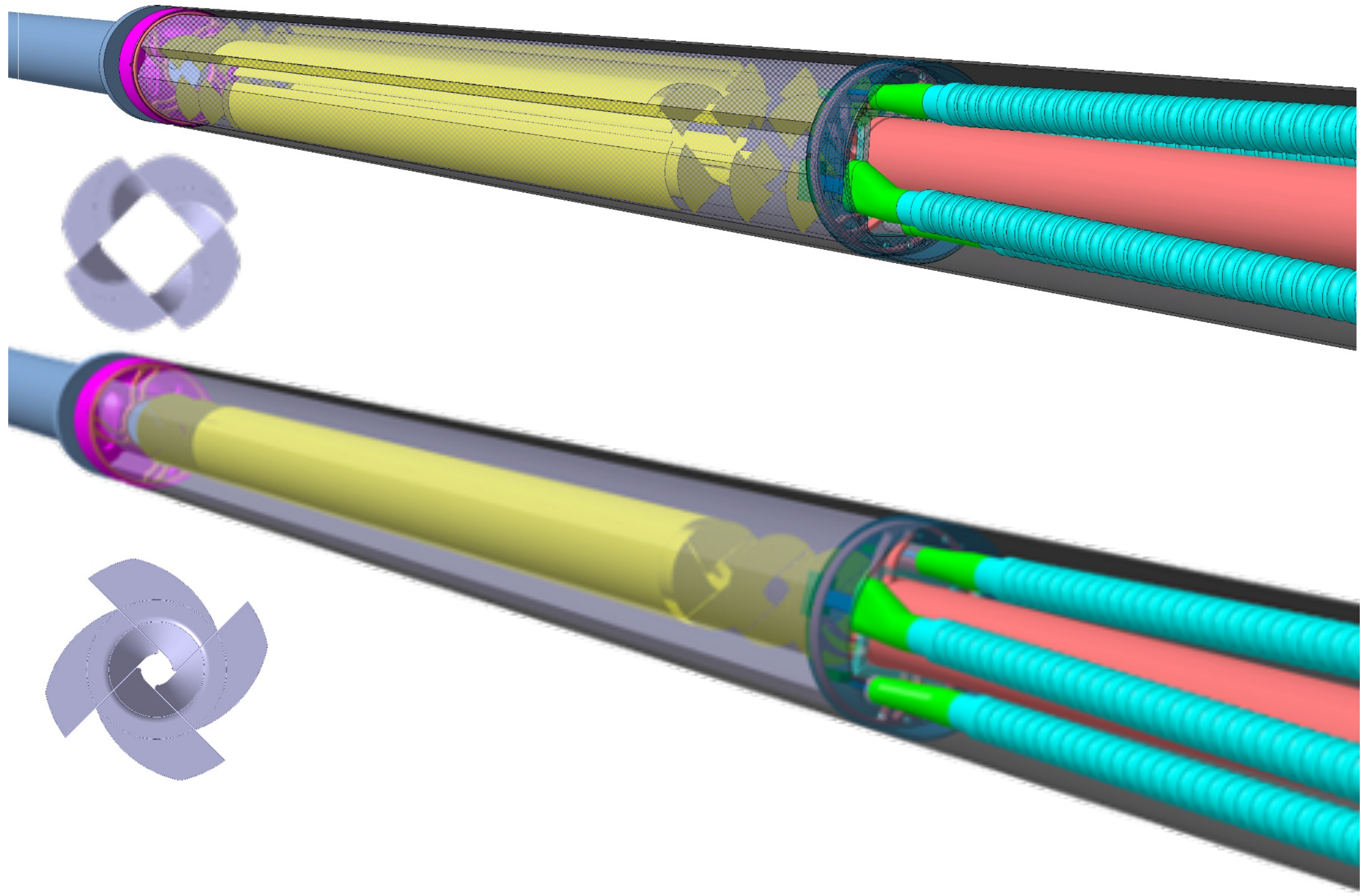


- **40-60 m²** silicon pixel detector
  - large coverage: ±4η
  - high spatial resolution: ≈ 10 µm
  - very low material budget:
    X/X_0 (total) ≲ 10%
  - time resolution: 100 ns
  - low power: ≈ 20 mW/cm²
- **Main R&D challenge**: its size
  - power consumption and distribution (both ways) are critical
  - module design for industrial production is necessary
- Relies on maturity, reliability and availability of a large quantity of MAPS
  - largely leverages from ITS2 and ITS3

ALICE 3

Vertex Detector





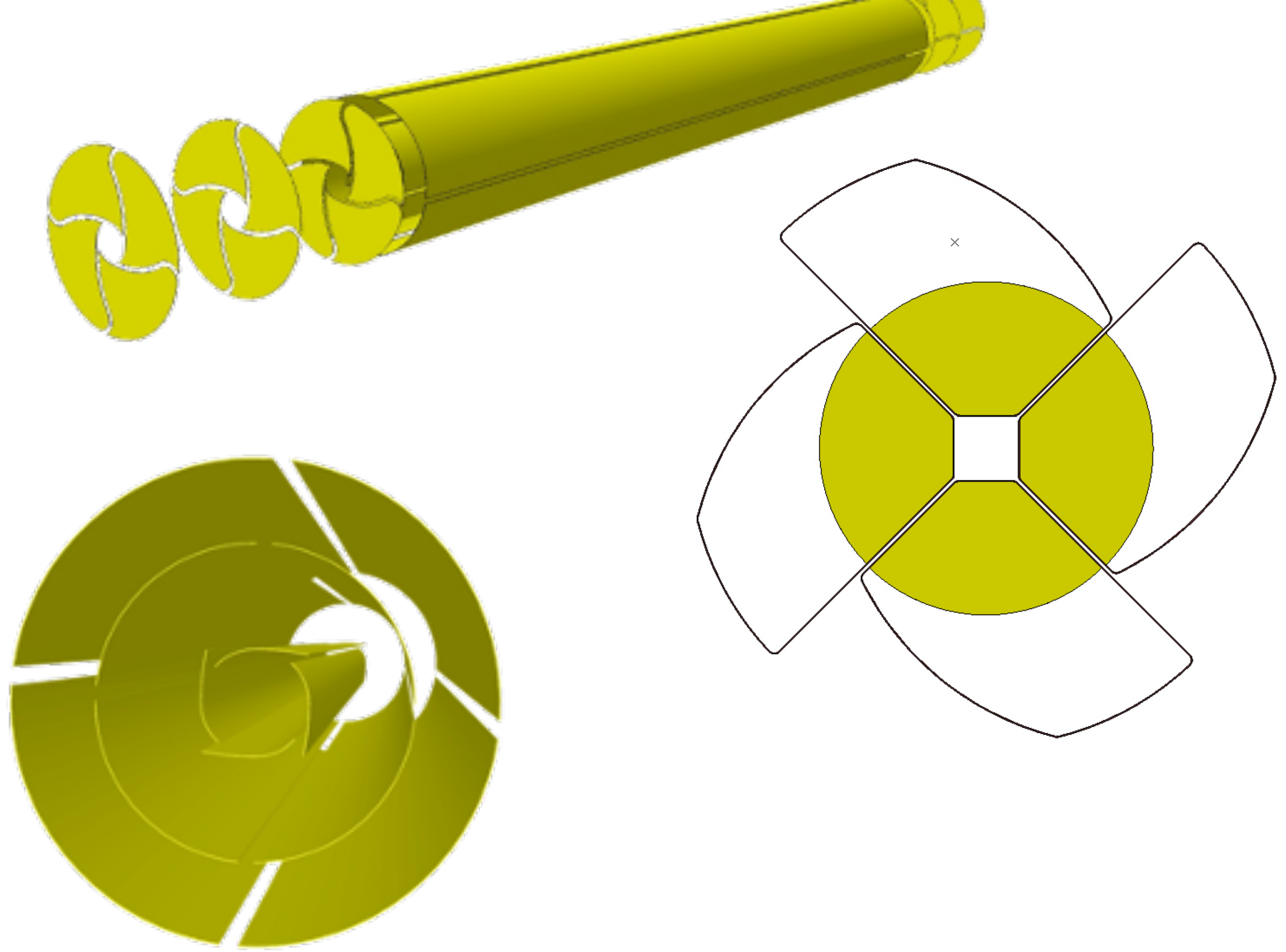
- **Based on wafer-scale, ultra-thin, curved MAPS**
  - radial distance from interaction point: 5 mm (inside beampipe, retractable configuration)
  - unprecedented spatial resolution: ≈ 2.5 µm
  - … and material budget: ≈ 0.1% X_0/layer
  - at radiation levels of: ≈ 10^{16} 1MeV n_{eq}/cm^2 + 300 Mrad
  - and hit rates up to: 94 MHz/cm^2

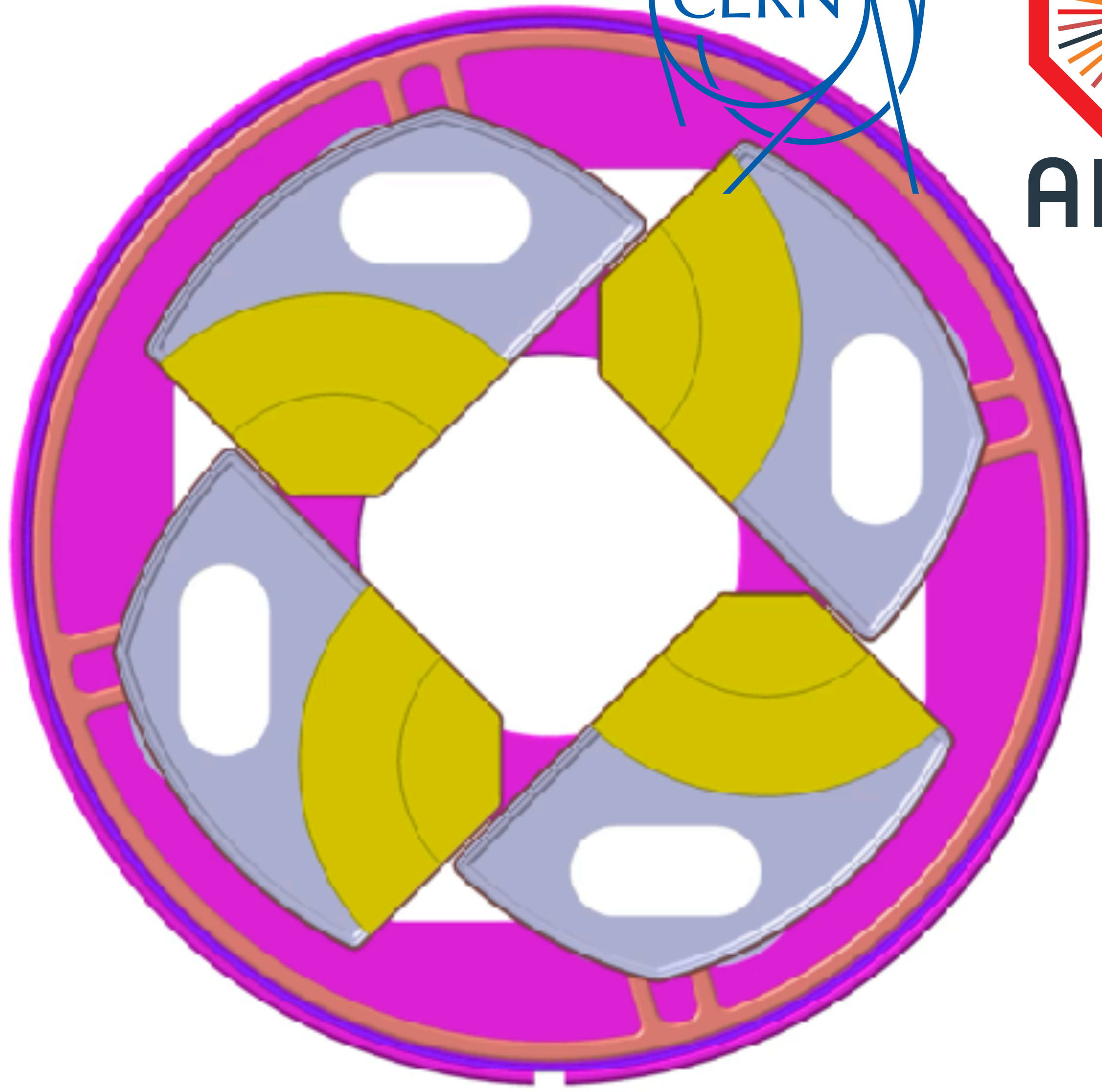
- Unprecedented performance figures
  - largely leverages on the ITS3 developments
  - pushes the technology on a number of fronts

- **R&D has started**

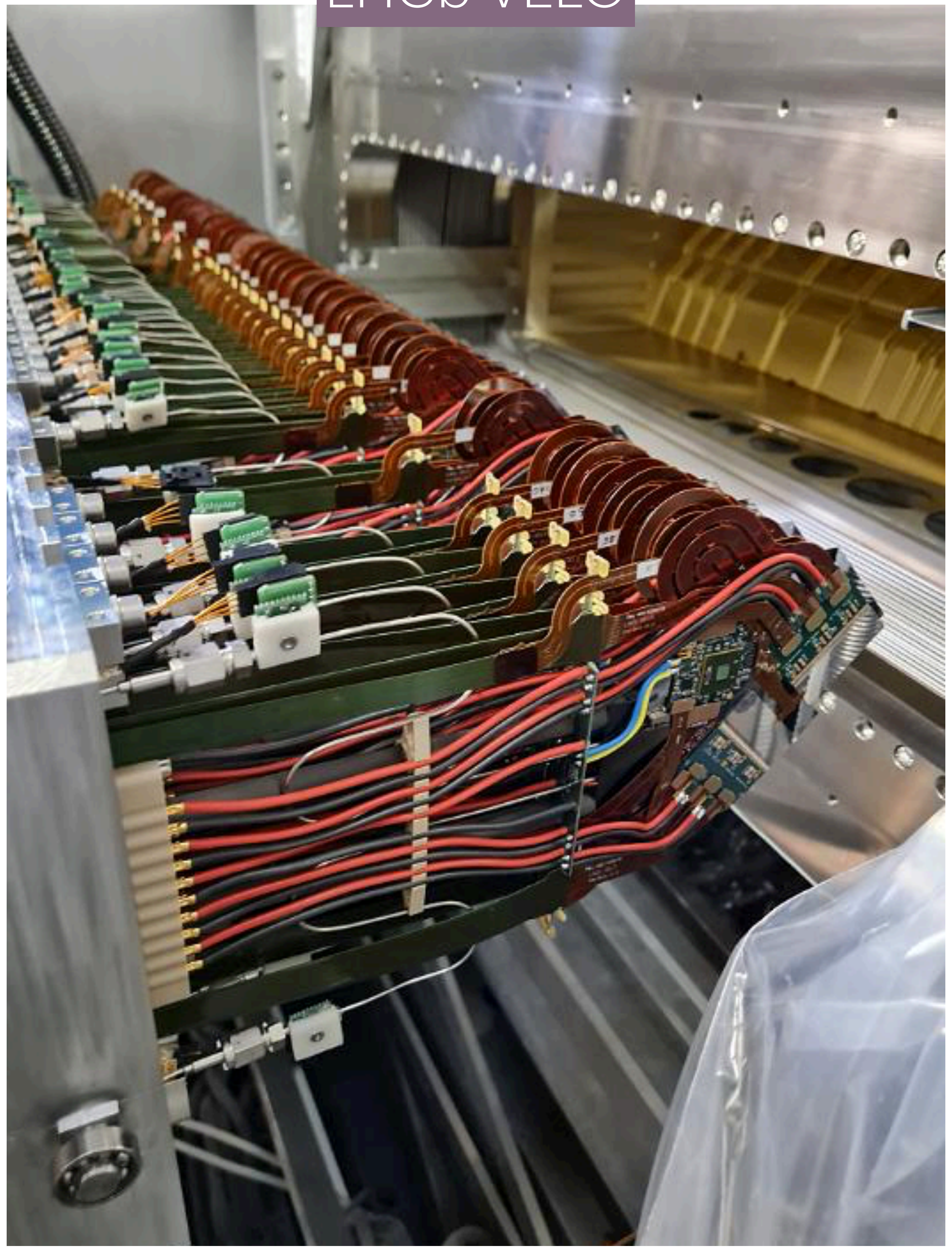
ALICE 3

in beam pipe: iris mechanics

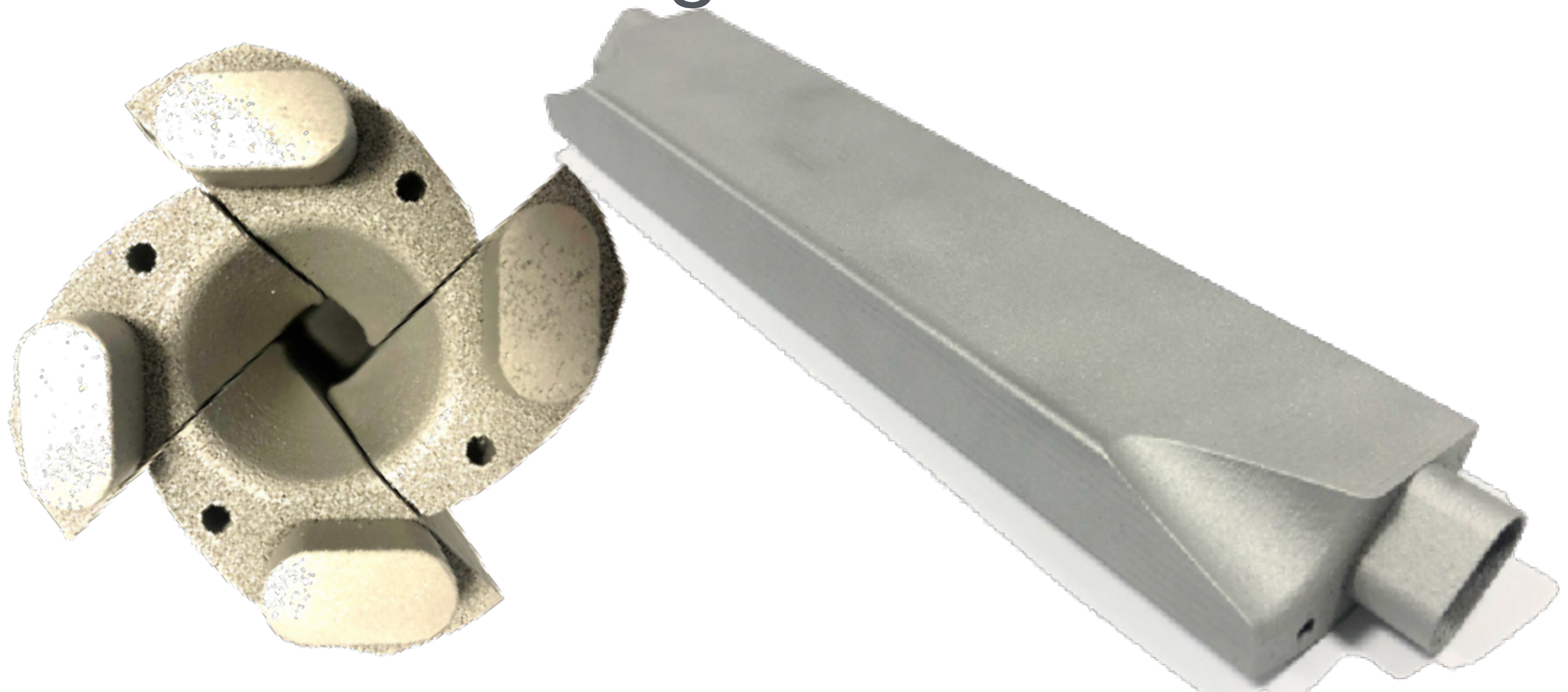


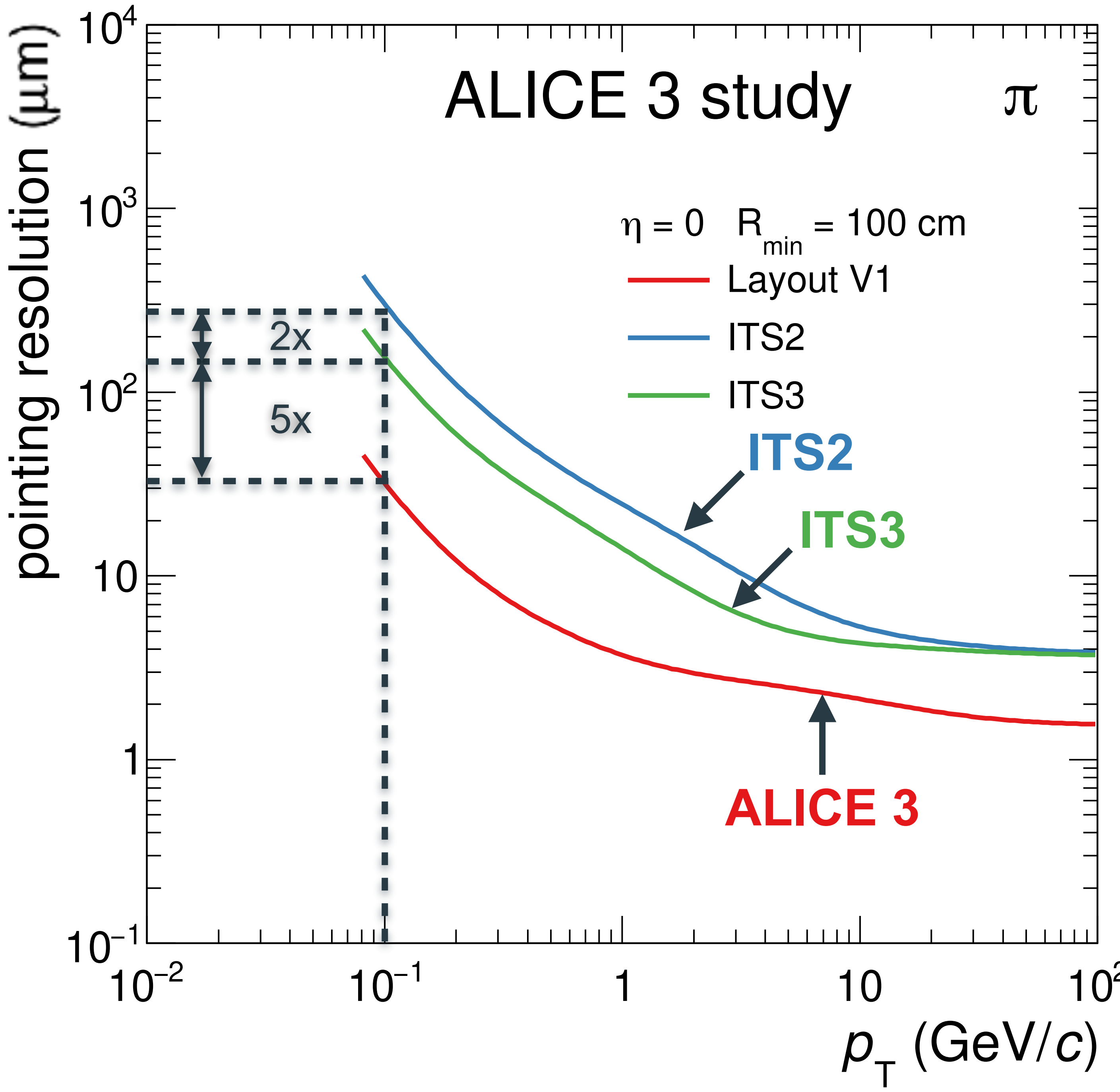


LHCb VELO



- Ultimate tracking resolution obtained by minimizing the extrapolation length (lever arm) → **in beam pipe**
- Needs to be retracted during beam injection
  - Similar concept to LHCb VELO, but in barrel configuration





ALI-SIMUL-491785

Future sensor requirements

	Vertex Detector	Middle Layers	Outer Tracker	ITS3
Pixel size (μm^2)	$O(10 \times 10)$	$O(50 \times 50)$		$O(20 \times 20)$
Position resolution (μm)	2.5	10		5
Time resolution (ns RMS)	$O(100)$	$O(100)$		$O(1000)$
In-pixel hit rate - barrel / forward (Hz)	94	42 / 12	1 / 16	54
Fake-hit rate (/ pixel / event)		$< 10^{-7}$		
Power consumption (mW / cm^2)	70		20	35
Particle hit density - barrel / forward (MHz / cm^2)	94	0.6 / 0.6	0.06 / 0.6	8.5
Non-Ionising Energy Loss (1 MeV n_{eq} / cm^2)	3×10^{15}	4×10^{13} / 4×10^{13}	3×10^{13} / 4×10^{13}	4×10^{12}
Total Ionising Dose (Mrad)	110	3 / 3	0.5 / 3	0.4

- Challenging, but ITS3 provides a great starting point
  - indeed, a lot of ITS3 R&D supports the feasibility of several parameters

MAPS for ALICE 3 tracker
(working proposal)

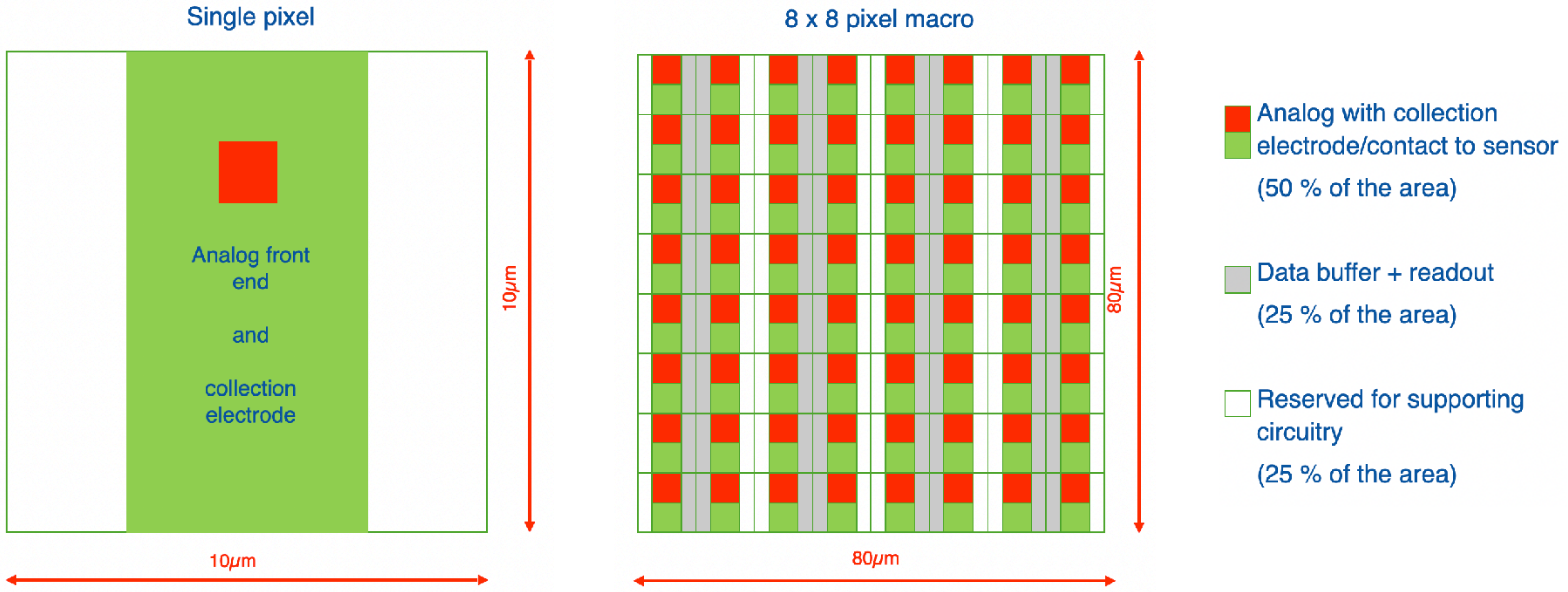
- **Background:** attempt a unified approach to the sensor development, even if requirements differ for different parts of the detector
- **Common design approach:** modular pixel matrix unit (1×1 cm^2), identical layout and circuits for all layers
- **Two variants:**
  - 10 µm pitch for the Vertex Detector (VD), driven by spatial resolution
  - 20 µm (or larger) pitch for Middle and Outer Layers (ML/OL)
- **Readout strategy:** higher frequency for VD, lower for ML/OL
- **Integration:** multiple matrix units assembled into large-area sensors (up to ~2×3 cm^2 for ML/OL, larger sensors for VD)
- **Performance targets:**
  - Spatial resolution: 2.5 µm -> 10 µm pitch (VD) , ~10 µm (ML/OL)
  - Power density: ~70 mW/cm^2 (VD), 20-30 mW/cm^2 (ML/OL)
  - Radiation tolerance: 3×10^{15} 1 MeV n_{eq}/cm^2
- **Engineering / R&D challenge:** internal routing with analog signals crossing digital regions, and vice versa

Global architecture

working ideas

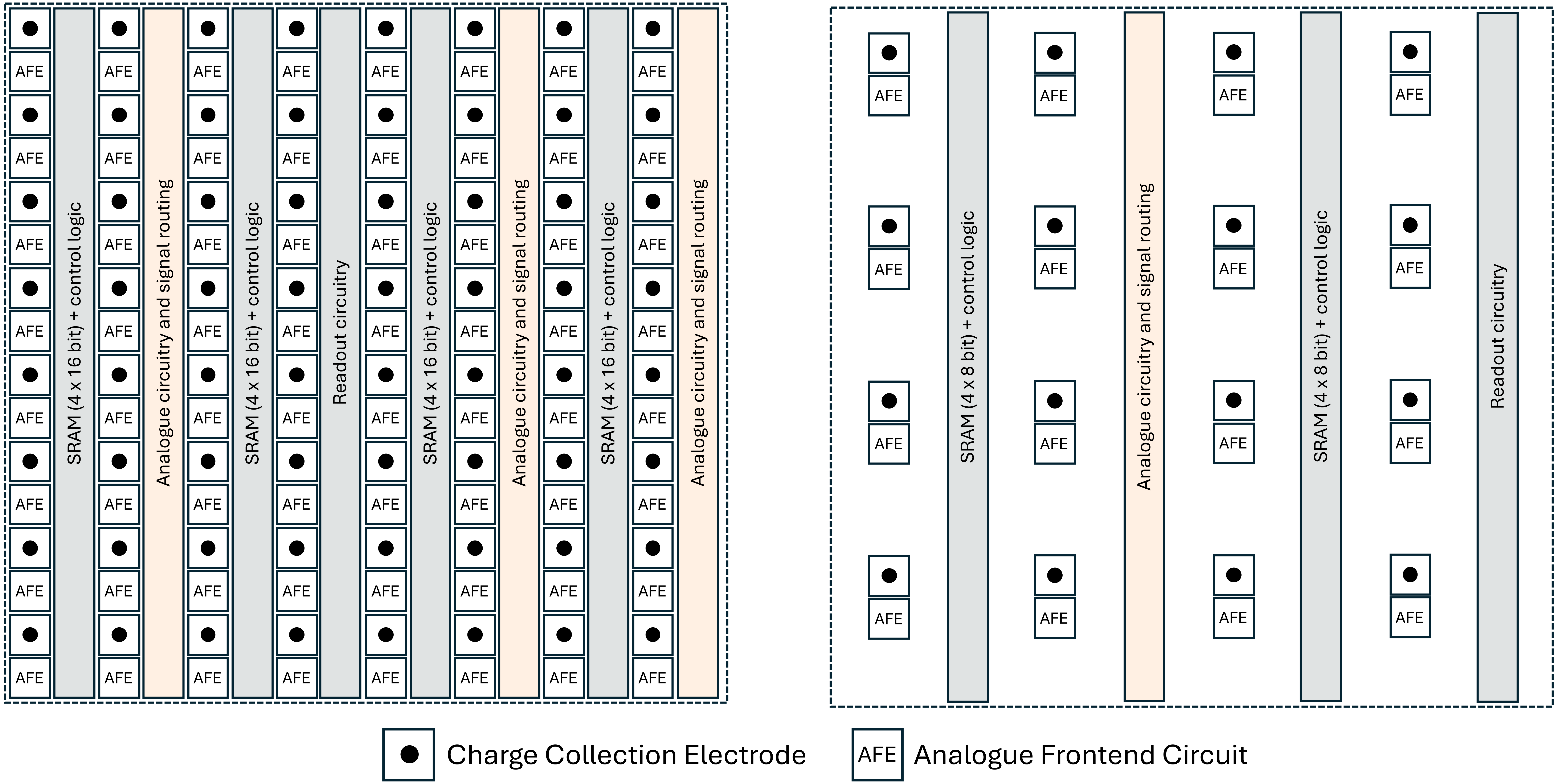
- **Central concept:** build sensors from a modular Pixel Macro (e.g. a 80 µm × 80 µm block)
- **Pixel pitch flexibility:** 10 µm × 10 µm or 20 µm × 20 µm (extendable to larger pitches)
- **Matrix Core:**
  - 128 × 128 Pixel Macros → 1 cm × 1 cm matrix
  - Peripheral logic for control, aggregation, serialization
- **Scalability:**
  - Tile Matrix Cores into larger sensors (e.g. 2 × 3 cm for ML/OL)
  - Larger sensors for VD, stitching (if needed) limited to periphery
- **Technology baseline:** 65 nm CMOS, 7 + 1 metal layers, including thick layer(s) for power grid

10 µm pixels



- **R&D:** internal routing with analog signals crossing digital regions, and vice versa

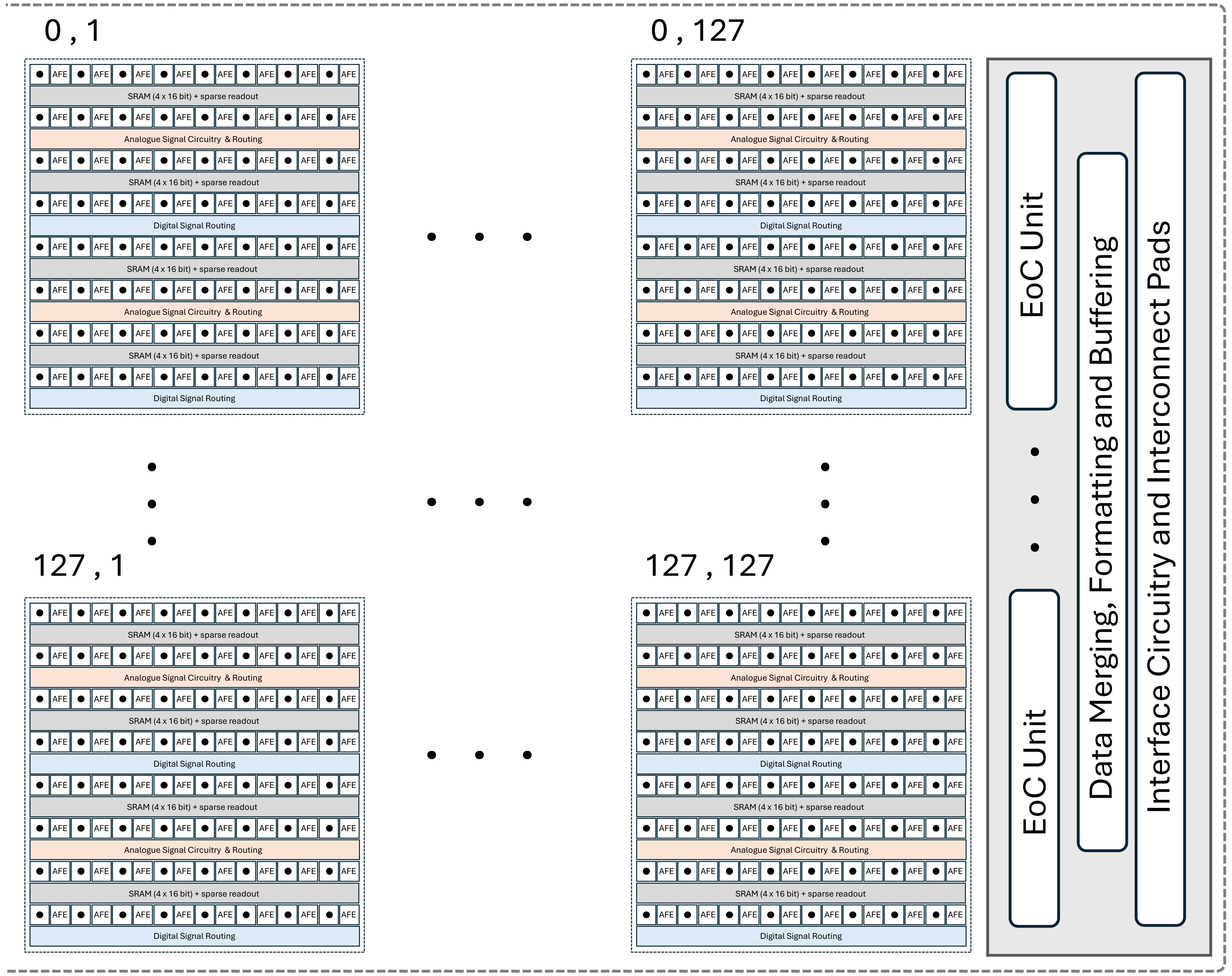
Modular: 10 µm → 20 µm



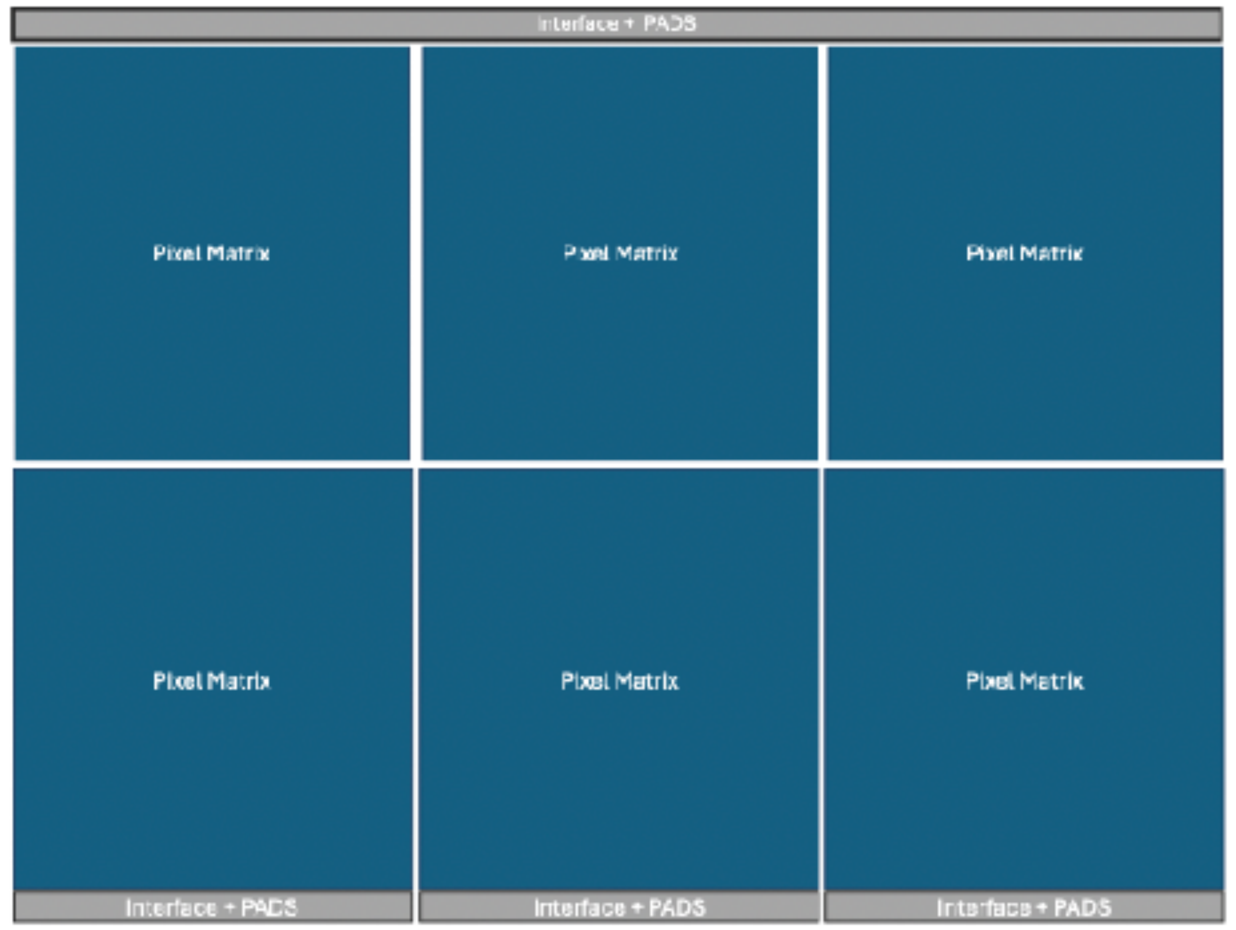
- Simplification to larger pitches possible (e.g. Outer Tracker), potentially yielding:
  - higher yield
  - lower power

Sensor assembly

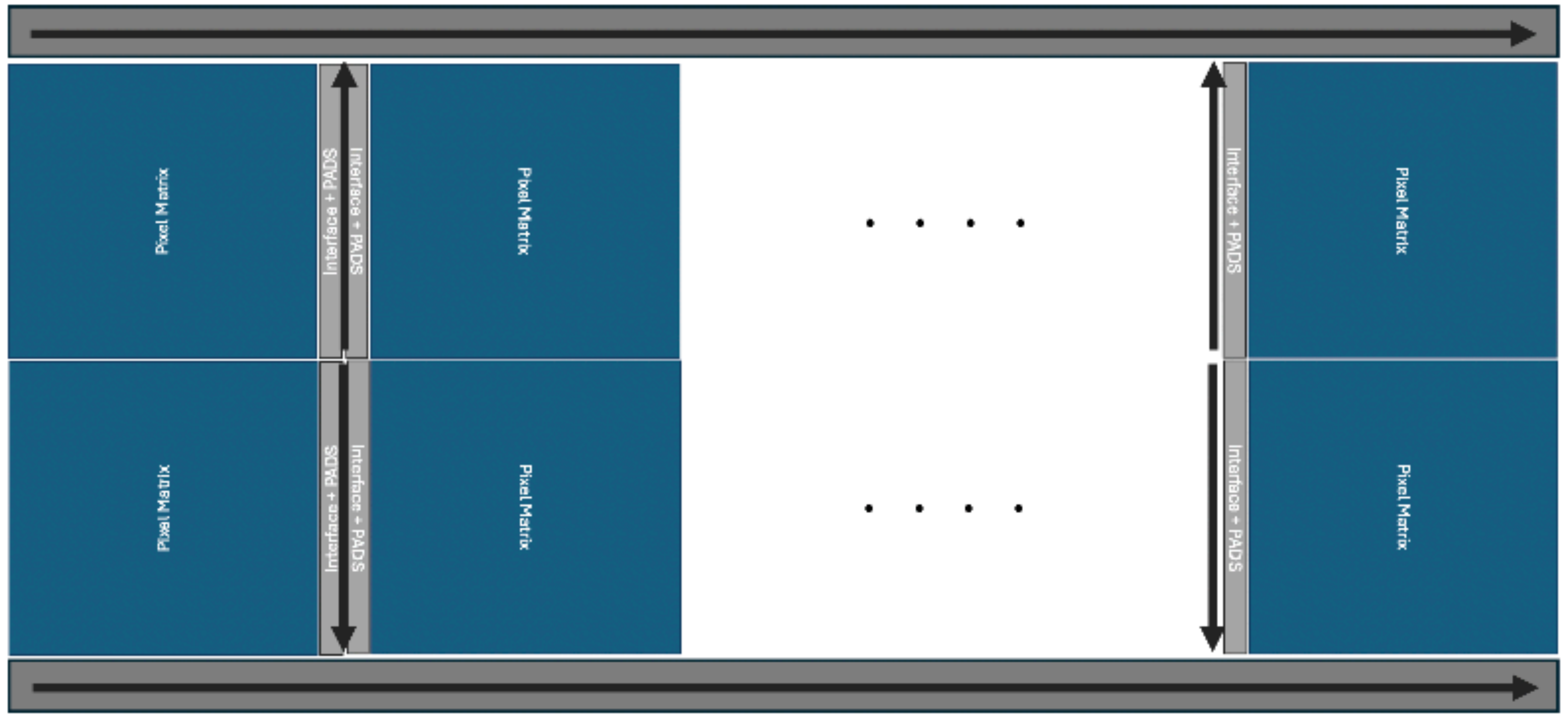
- Pixel macros will be instantiated to build the full matrix
- Different arrangements possible to serve different detector requirements



Option for reticle-size sensor

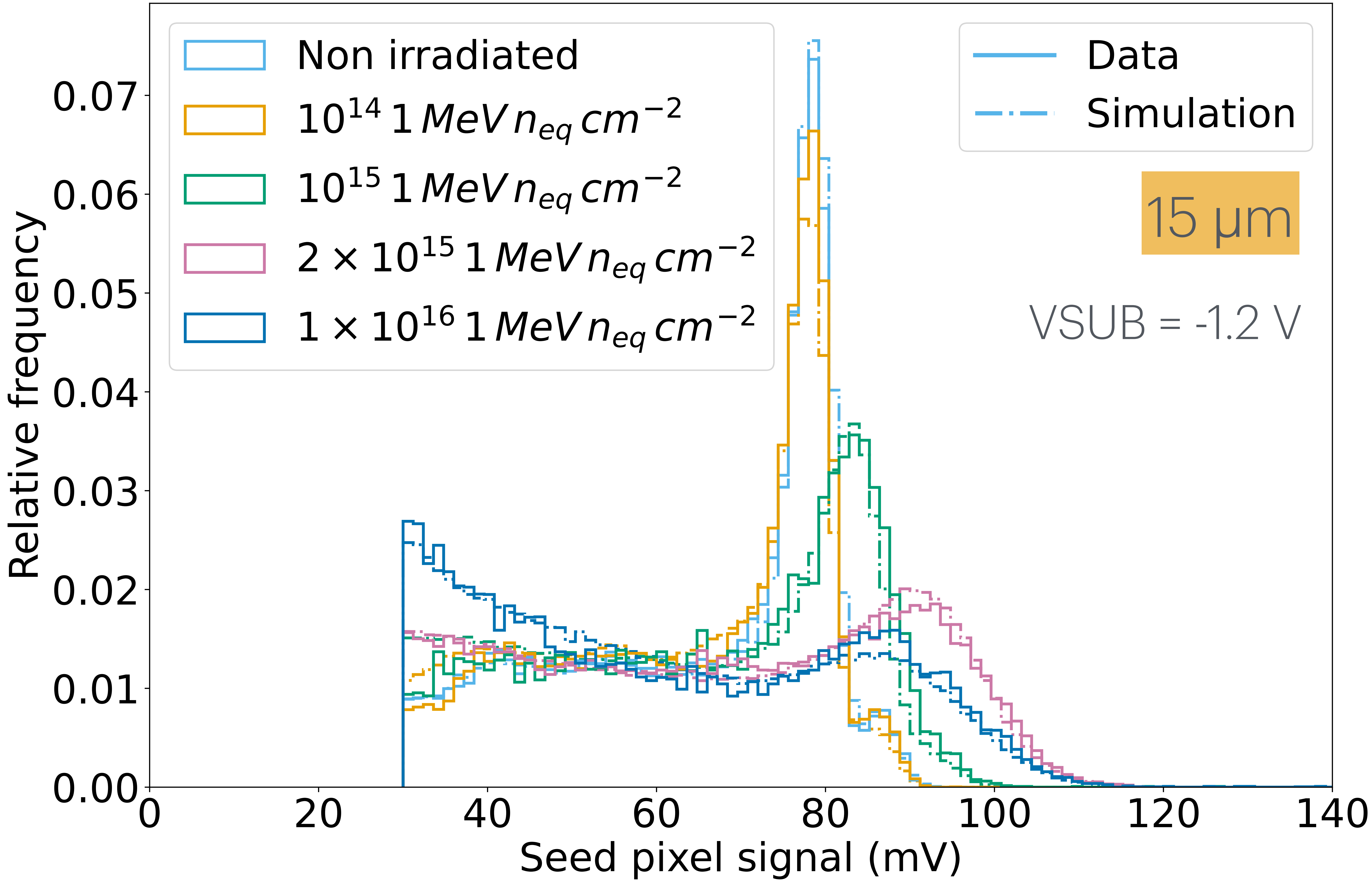


Option for stitched sensor



Radiation hardness

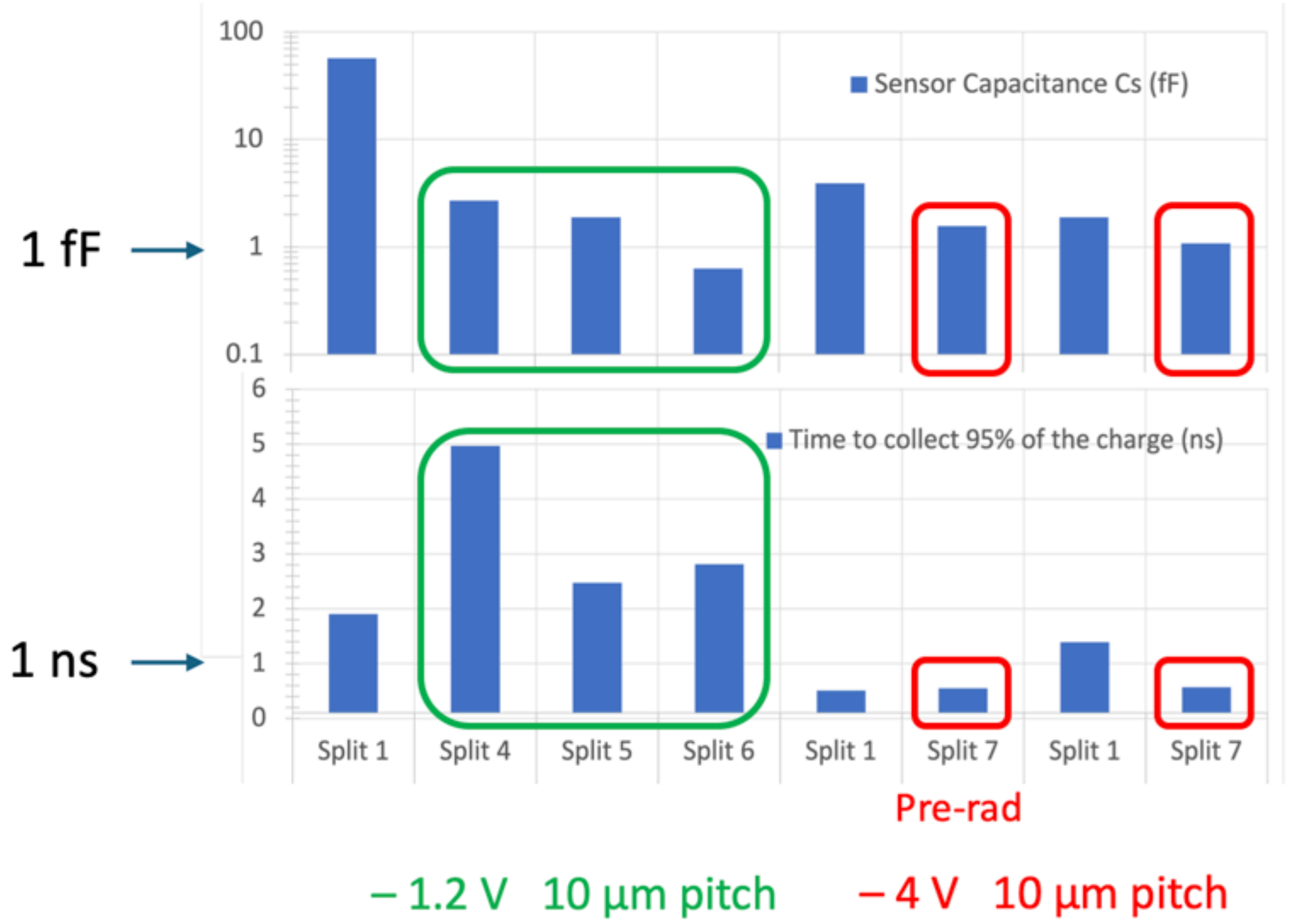
- Main principle challenge
- Already assessed with ITS3 prototype chips
- Excellent starting point
- Further improvements by:
  - reduction of pixel pitch
  - further process optimization



Process optimization

for radiation hardness

- Continued improvement over the last decade
  - MLR1 Dec. 2020: split 1 (std) - split 4
  - ER1 Dec. 2022: split 4
  - ER2 Aug. 2025
- Different optimizations:
  - split 4-6 for -1.2 V and 20 µm pitch optimized for ITS3 and outer layers
  - split 7 for -4 V and 10 µm pitch towards higher radiation tolerance circuit to be compatible with -4 V
- TID in TPSCo 65 nm:
  - No showstopper, typical transistor radiation tolerance for a 65 nm technology
  - However, in MOSS a sensitivity to TID observed (increased fake hit rate)
  - topology dependent, to be investigated for the new front end

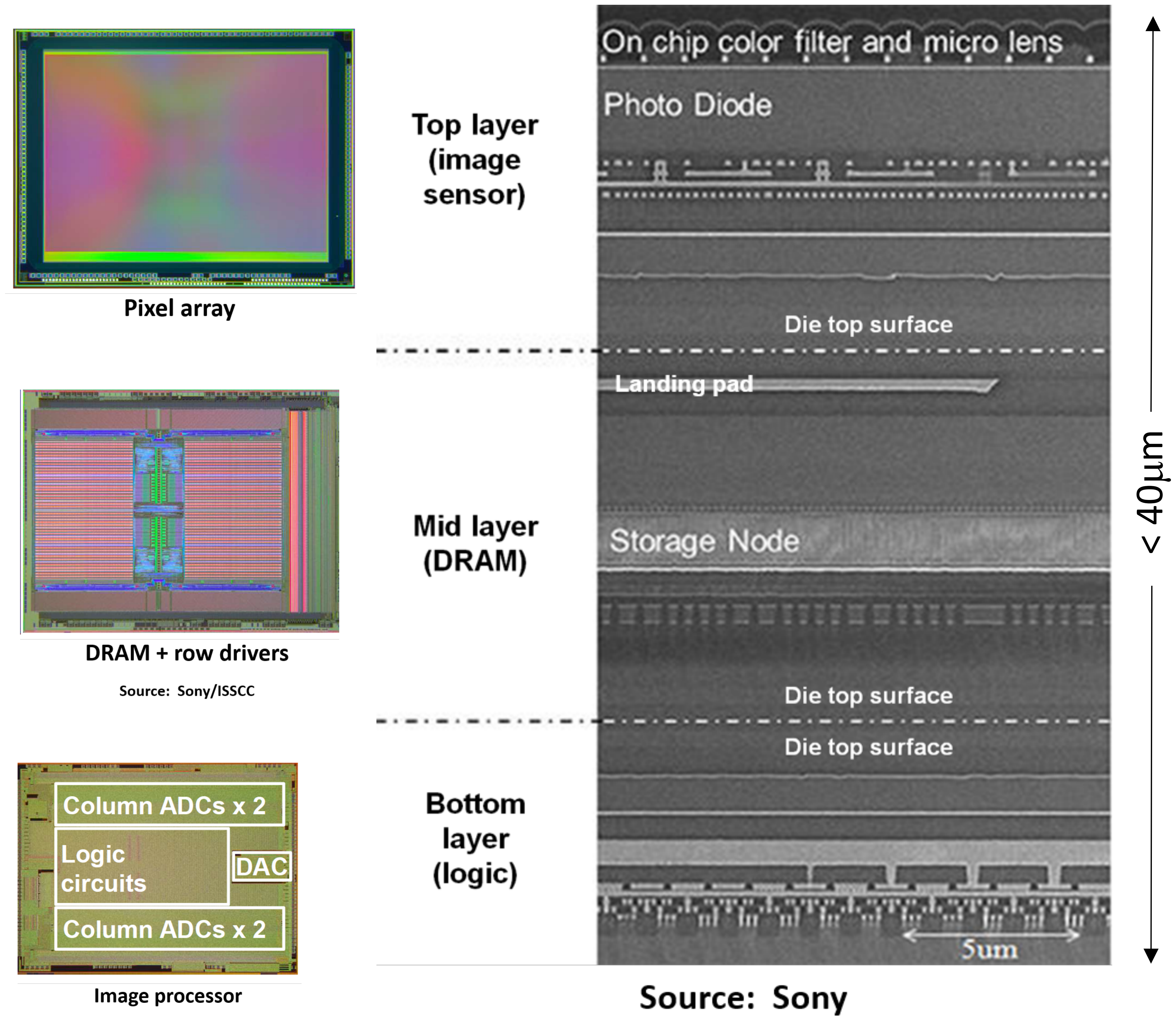


More future opportunities

personal selection

Wafer stacking

“monolithic hybrids”



- Many modern (optical) pixel sensors are **stacks of different chips**
- Smears the boundaries between monolithic and hybrid detectors
  - but: stays an industrial process
- Optimized choice for technology for each function can be taken, e.g.
  - sensor + first level amplification
  - readout
- NB: sensor layer can still be “MAPS”-like, i.e. contain active elements

Time over threshold

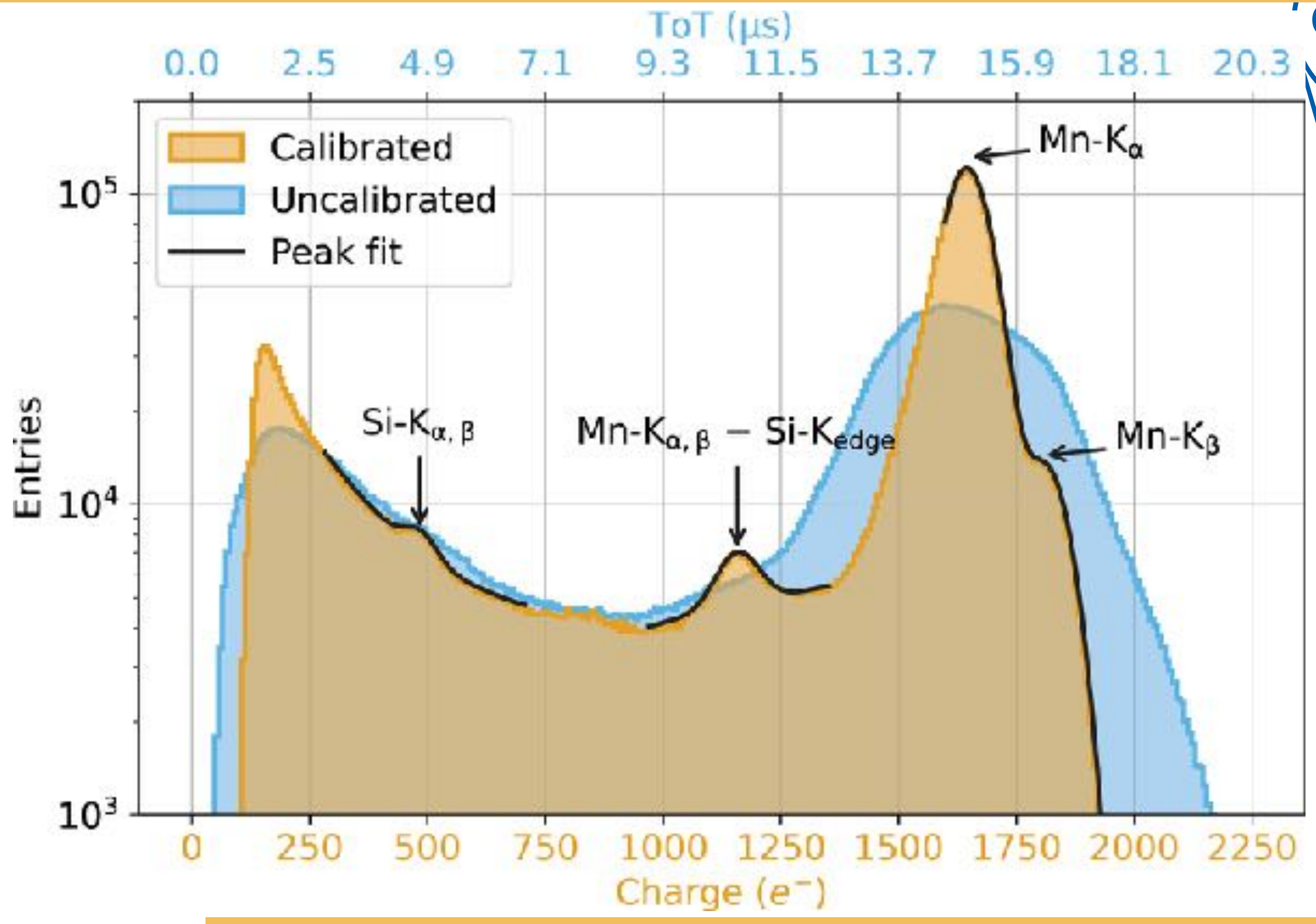
dE/dx, PID

- Pixels with binary (yes/no) readout can still measure charge by looking at how long the signal is seen by the electronics (~Wilkinson ADC): **time over threshold, ToT**

- **Potential benefits**
  - position resolution: measurement of charge sharing
  - time resolution: time walk correction
  - particle identification: specific energy loss, dE/dx

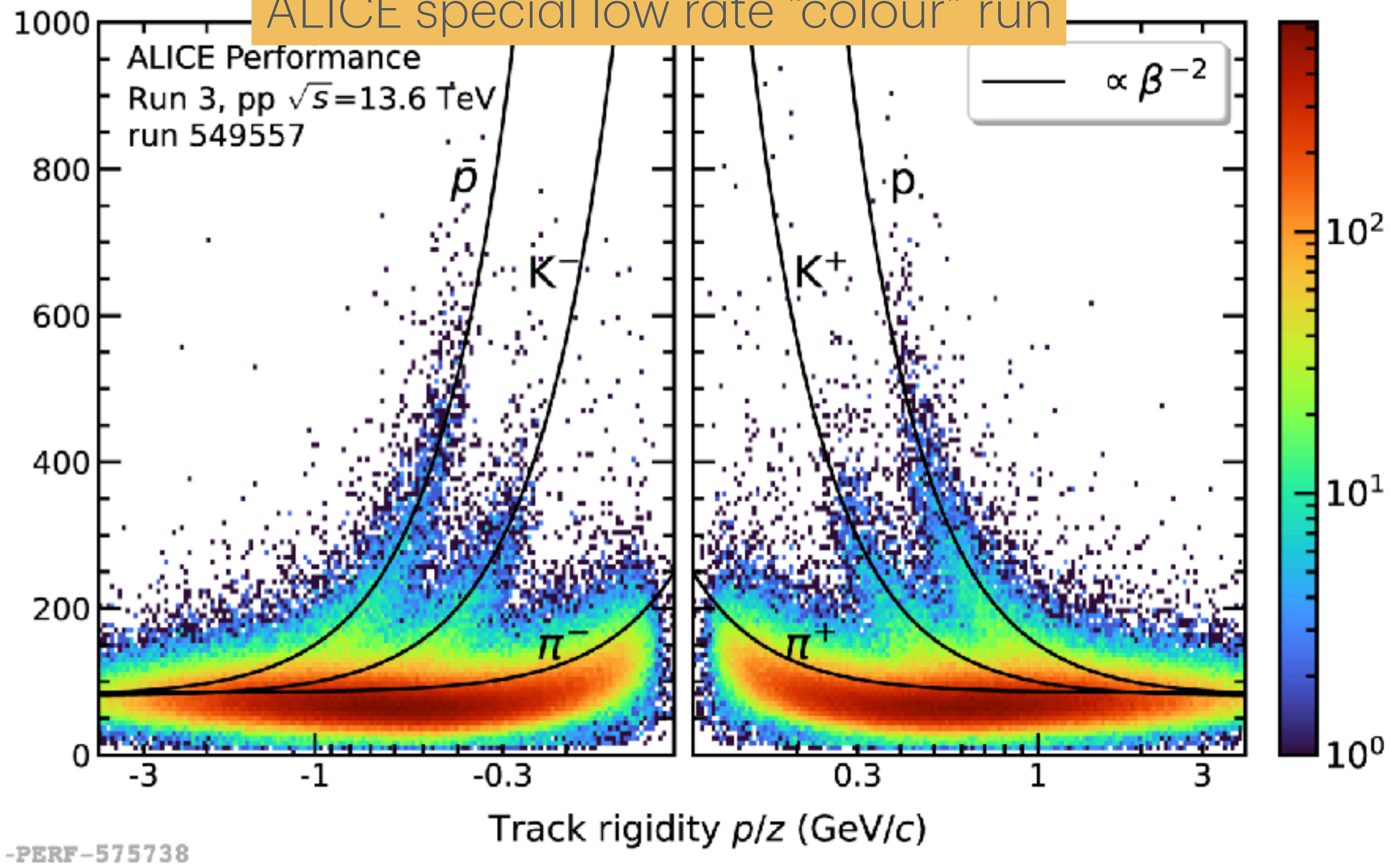
- **Particle identification** with silicon
  - (+) good ratio of ionization potential to multiple scattering
  - (-) too coarse segmentation (too few measurement points): Landau tails difficult to remove
  - still: applicable for low momentum particles

low energy X-ray spectra from 65 nm prototypes



[doi:10.1016/j.nima.2023.168589]

ALICE special low rate "colour" run

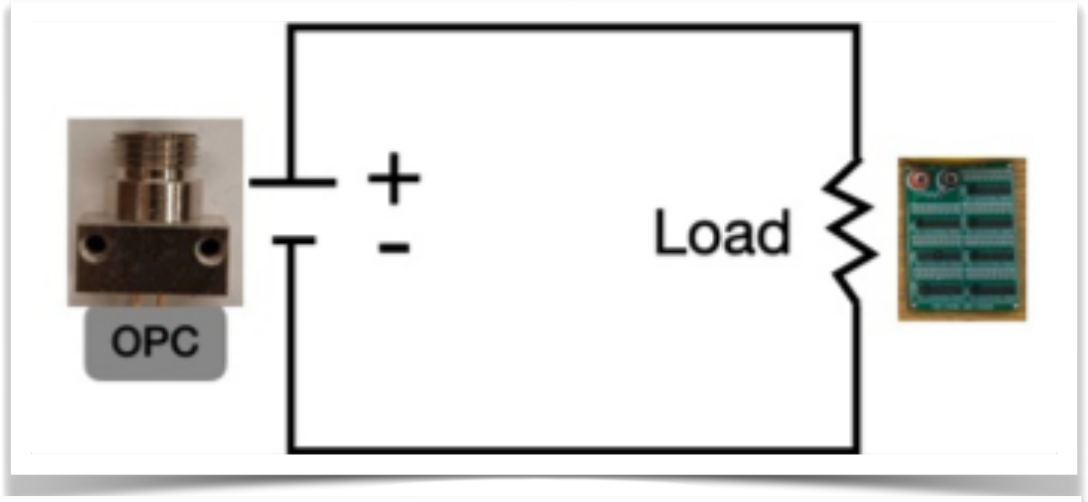


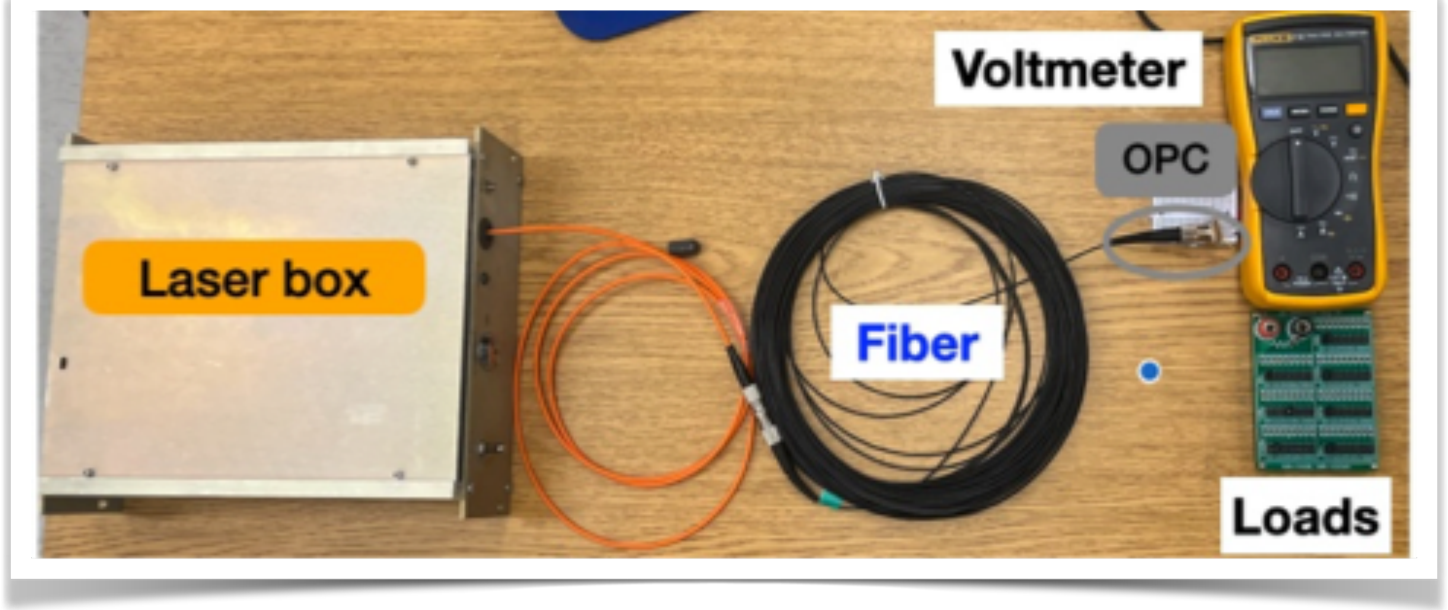
[doi:10.1088/1748-0221/20/01/C01030]

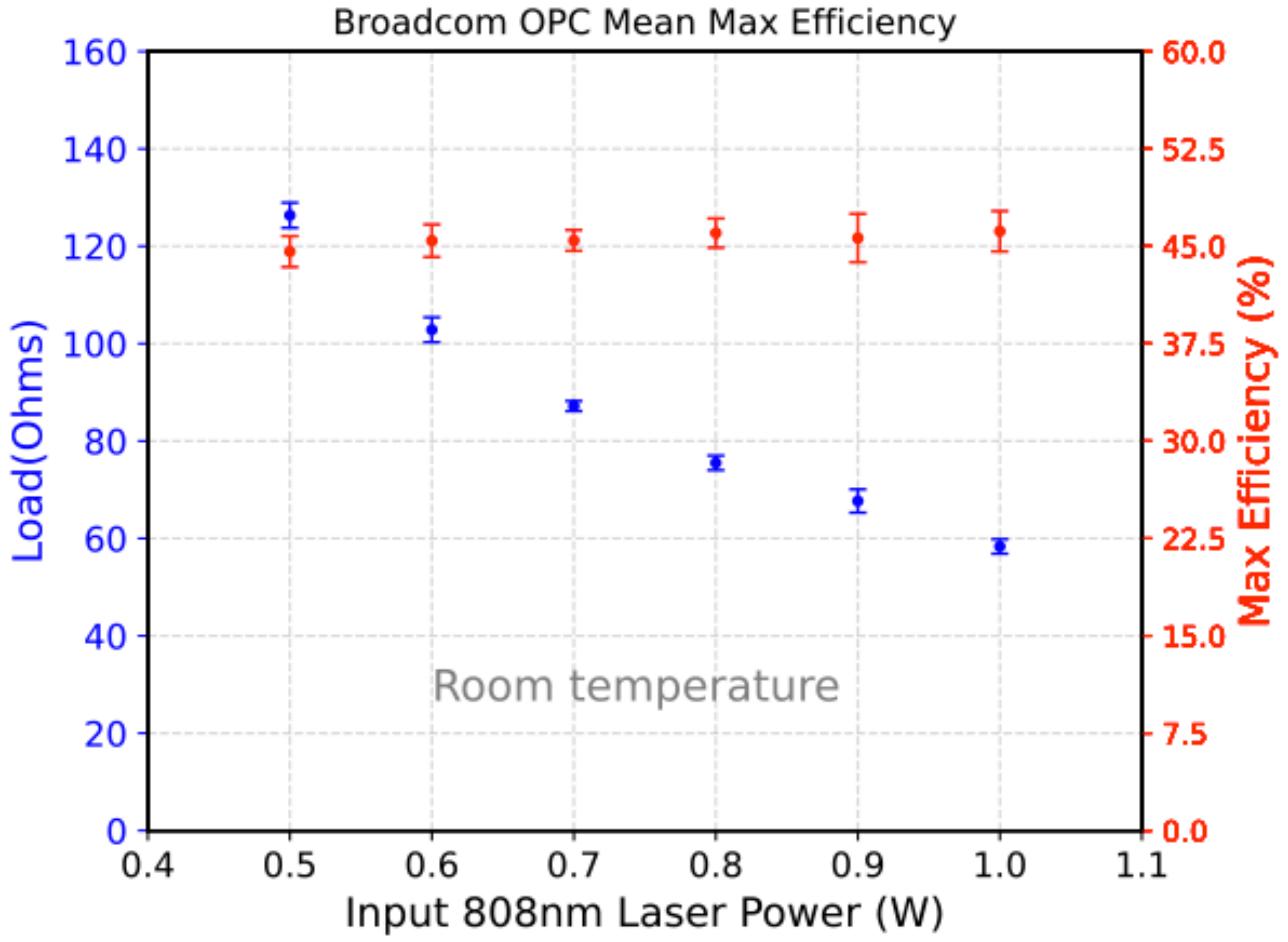
Future trends

powering (serial, optical, mechanical, chemical, nuclear)

- **Powering is one of the key difficulties** in the design of low mass detectors
- **Novel ideas and solutions are necessary** to get to large-scale low mass detectors
- **Serial powering**
  - put detectors in series instead of parallel
  - employed in LHC upgrades
  - to be ported to CMOS detectors (planned for ALICE 3)
- **Optical powering ("power over fibre", POF):**
  - shoot a laser onto a photocell
  - commercially available solutions exist
  - used e.g. by DUNE
- **More "exotic" ideas:** use fuel cells, piezo transformers, batteries, …







[doi:10.48550/arXiv.2405.16816]

Summary and outlook

- CMOS Monolithic Active Pixel Sensors (**MAPS**) are an **established technology**
  - provide excellent spacial resolution at lowest material budgets
  - ALICE is currently operating 24k sensors on its inner tracking system (ITS2)
  - rapid development over last 2 decades
- **ITS3** project **introduced *and* proved feasibility** of a new class of ultra-light vertex detectors
  - **bent MAPS** work very well
  - **65 nm** process is established for HEP applications
  - **Stitched** (wafer-scale) design and associated yield is understood
  - **Bent, large, thin** sensors can be handled and mechanically integrated
  - **Air cooling** is proved to be sufficient
  - to be installed in LHC Long Shutdown 3
- **ALICE 3 sensor R&D** is starting
  - further process optimizations to reach higher radiation hardness
  - conceptional road towards 10 μm pitch laid out

MAPS have a bright future and will