

# Pixels in CBM

## The Micro Vertex Detector and Beyond

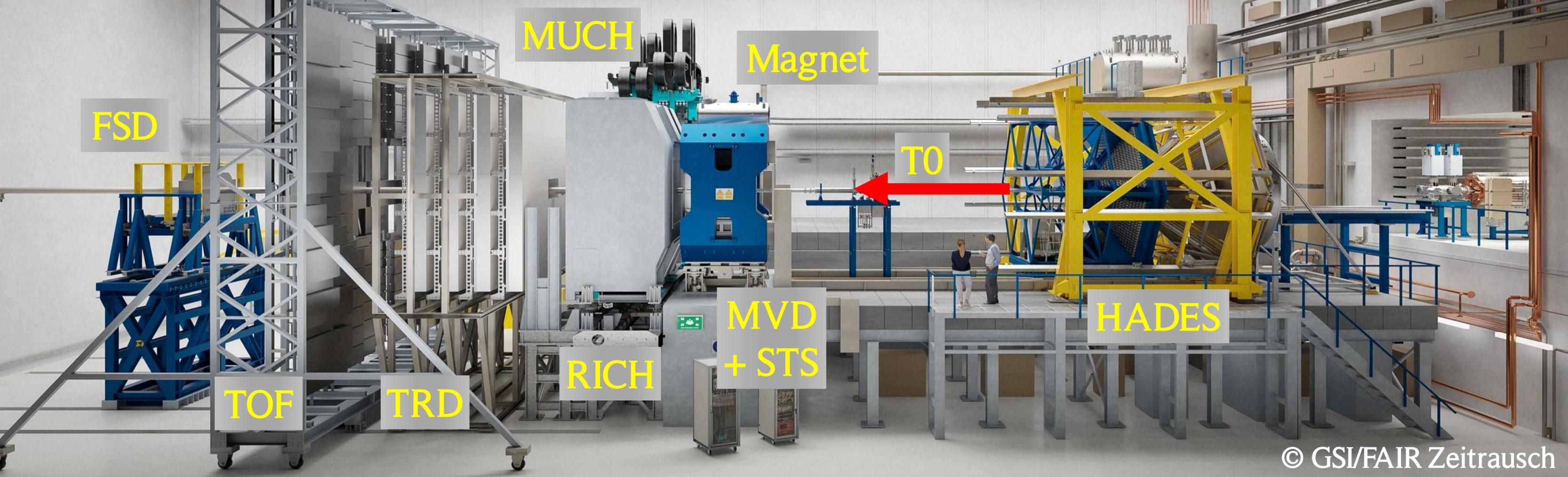
Franz A. Matejcek for the CBM Collaboration

1<sup>st</sup> GSI Pixel Platform Workshop, GSI, 23.03.2026



Chapter 0

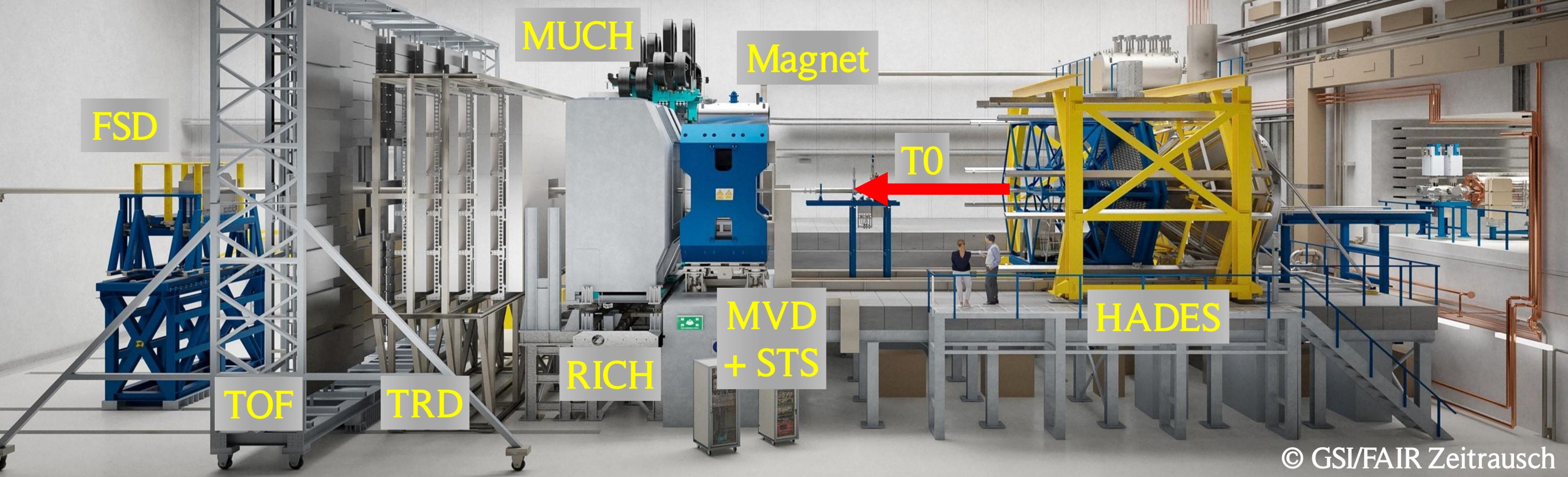
# Introduction



## Compressed Baryonic Matter Experiment

Fixed Target A-A at  $\sqrt{s_{NN}} = 2.9, \dots, 4.9$  GeV

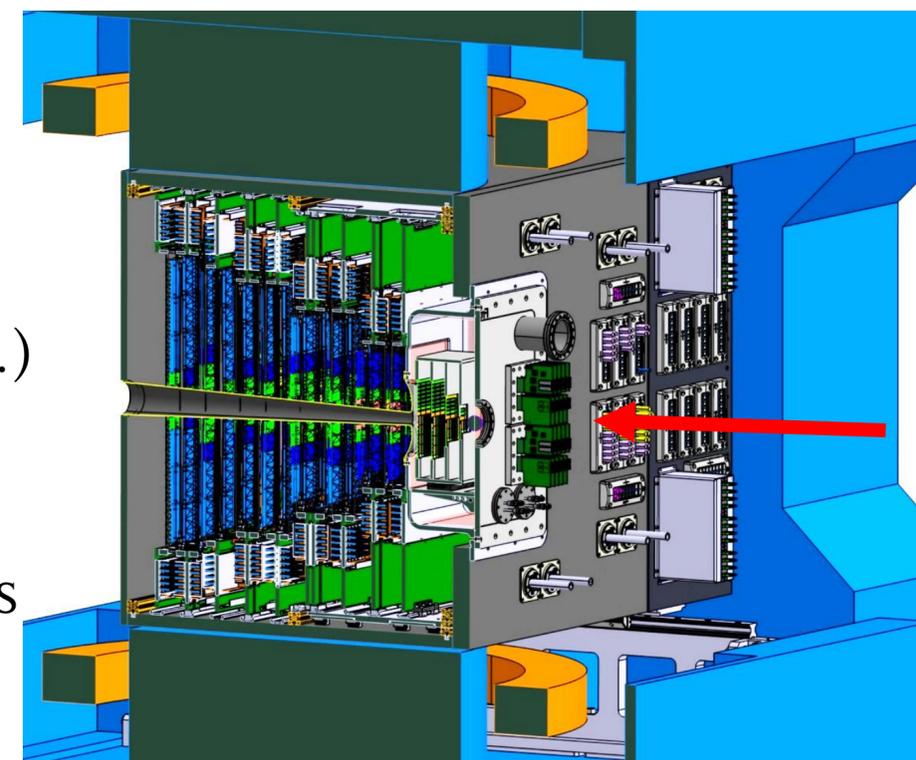
- First-order chiral phase transition
- Exotic phases (soft deconfined, quarkyonic, ...)
- EoS at neutron star core densities
- In-medium properties of hadrons
- Strangeness and Charm production, properties



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### Compressed Baryonic Matter Experiment

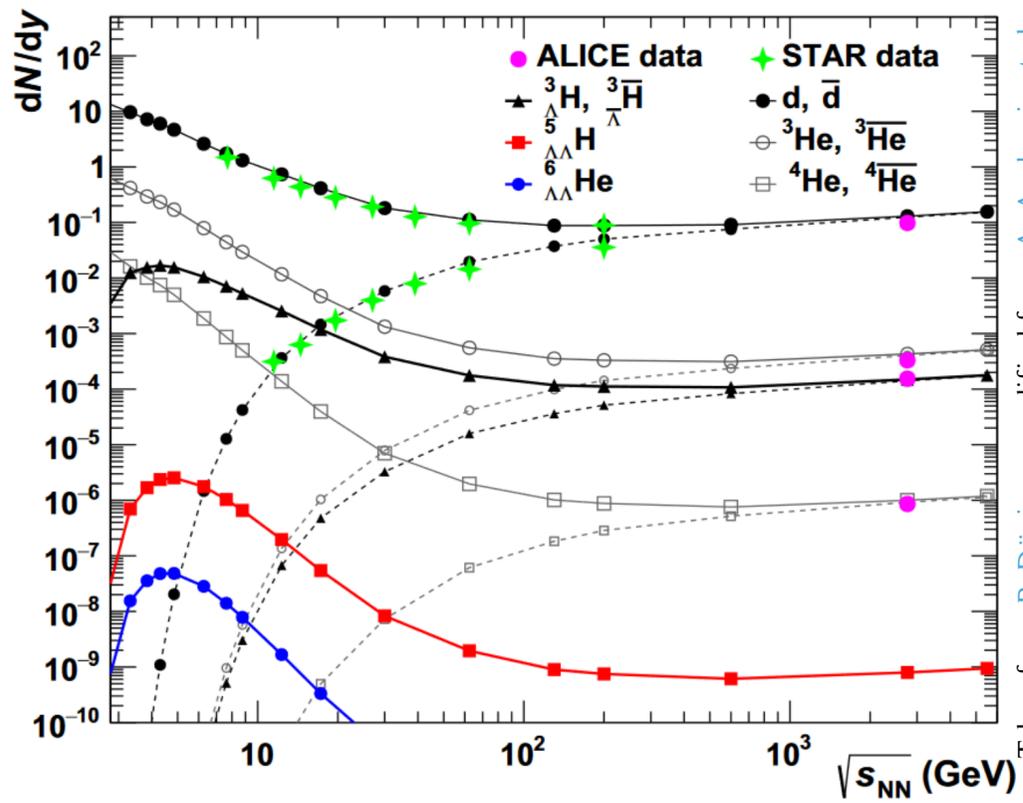
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### The Inner Tracker

- Inside 1 T·m magnet dipole field
- 2.5 – 25° polar acceptance (full azimuth)
- MVD:** 4 layers CMOS MAPS
- $z = 8 - 20$  cm (in vacuum)
- STS:** 8 layers Si-strips
- $z = 30 - 100$  cm (in air)

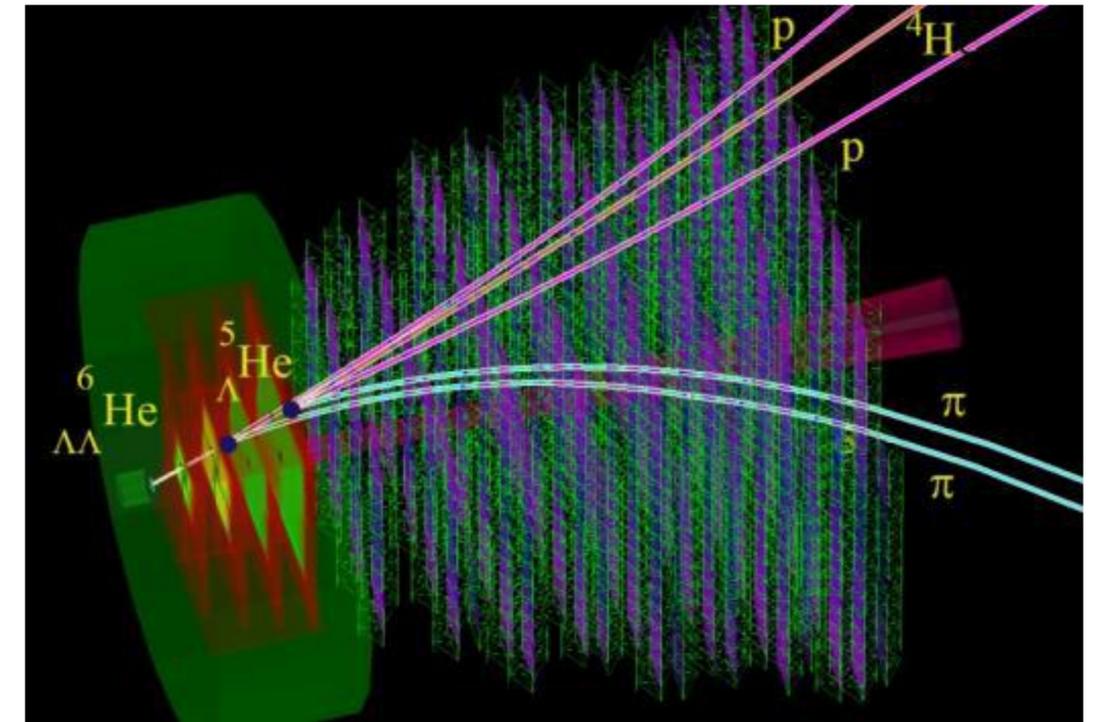
# Physics with the MVD



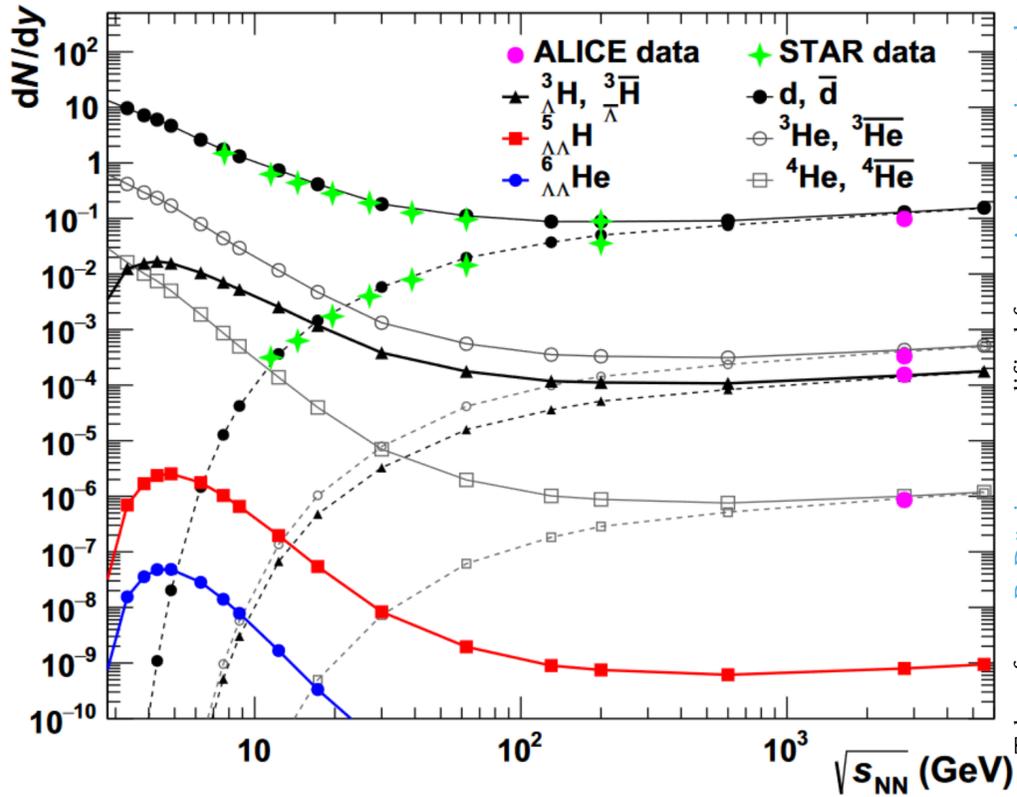
Taken from B. Dönigus, modified from A. Andronic et al.

## Hypernuclei production

Selection w/ KFParticle Finder in CBM



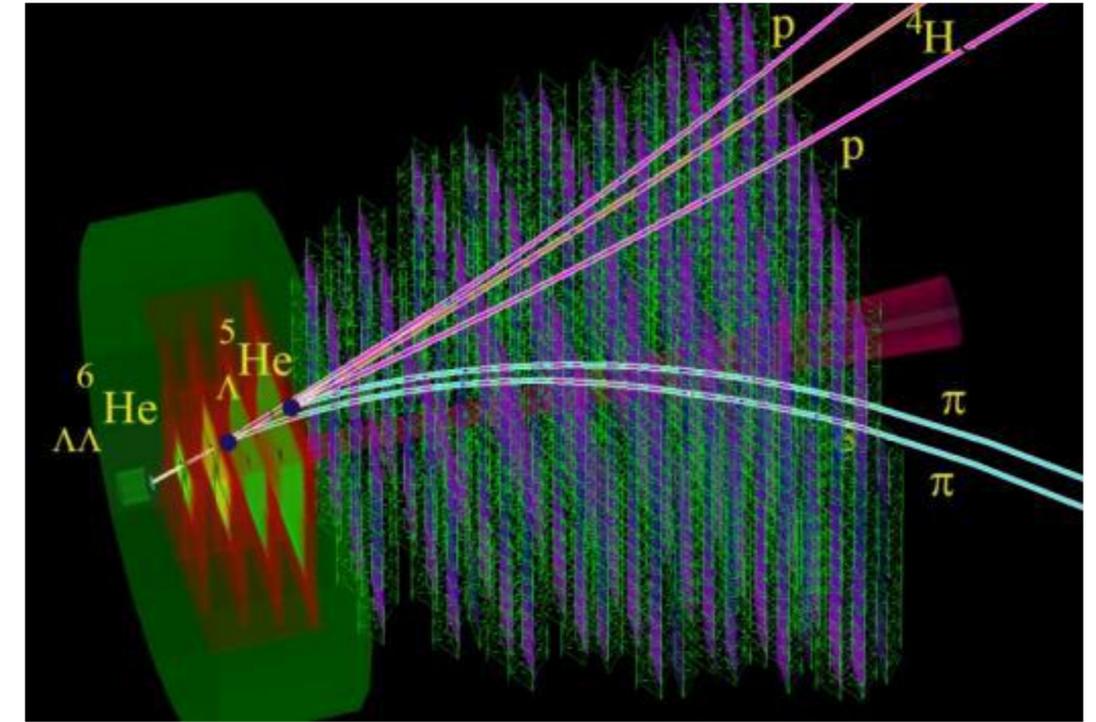
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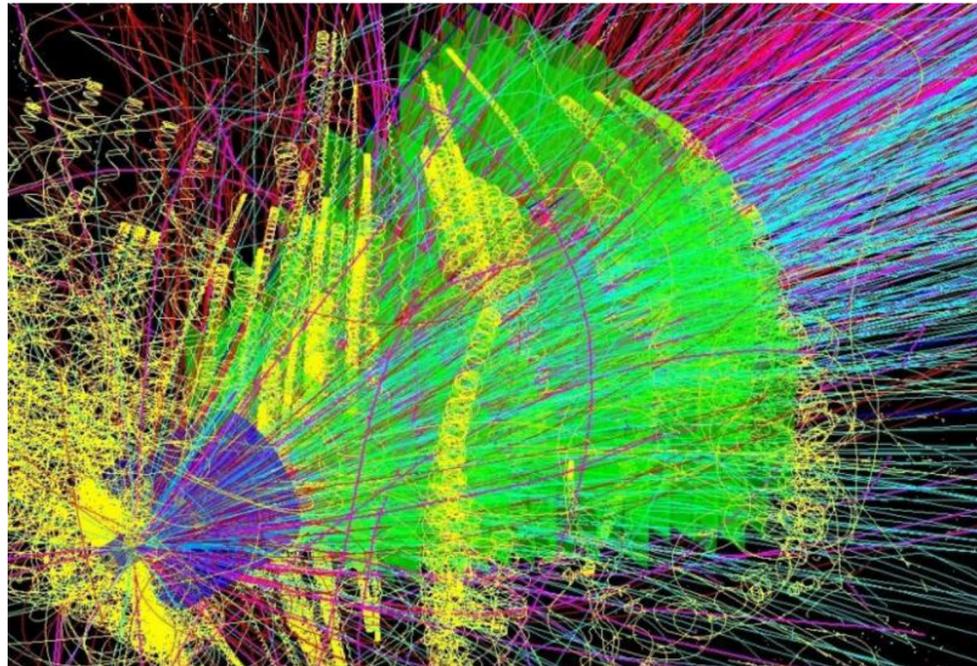
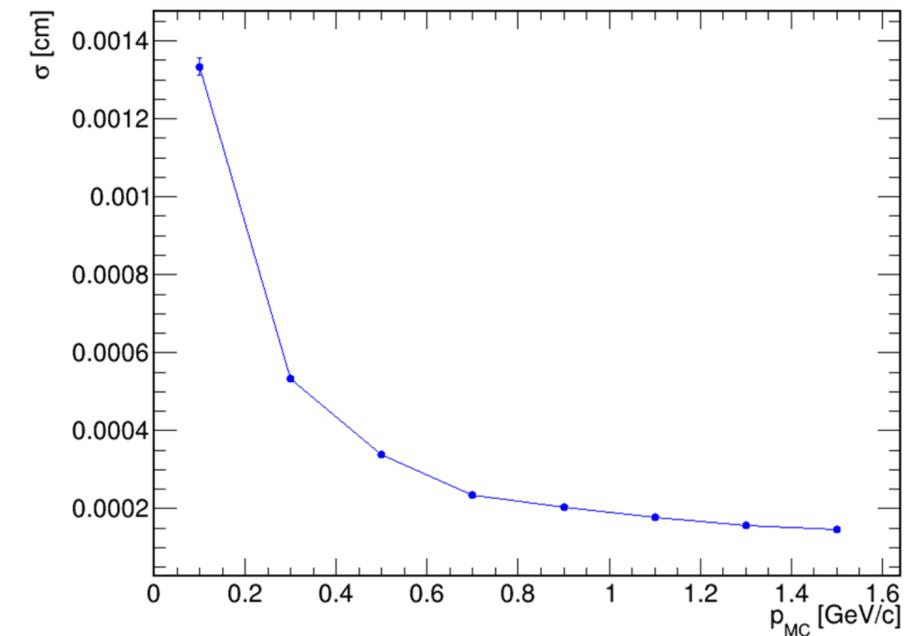
## Hypernuclei production

Selection w/ KFParticle Finder in CBM



Pointing Precision

x-Distance for  $z=0$  [cm]



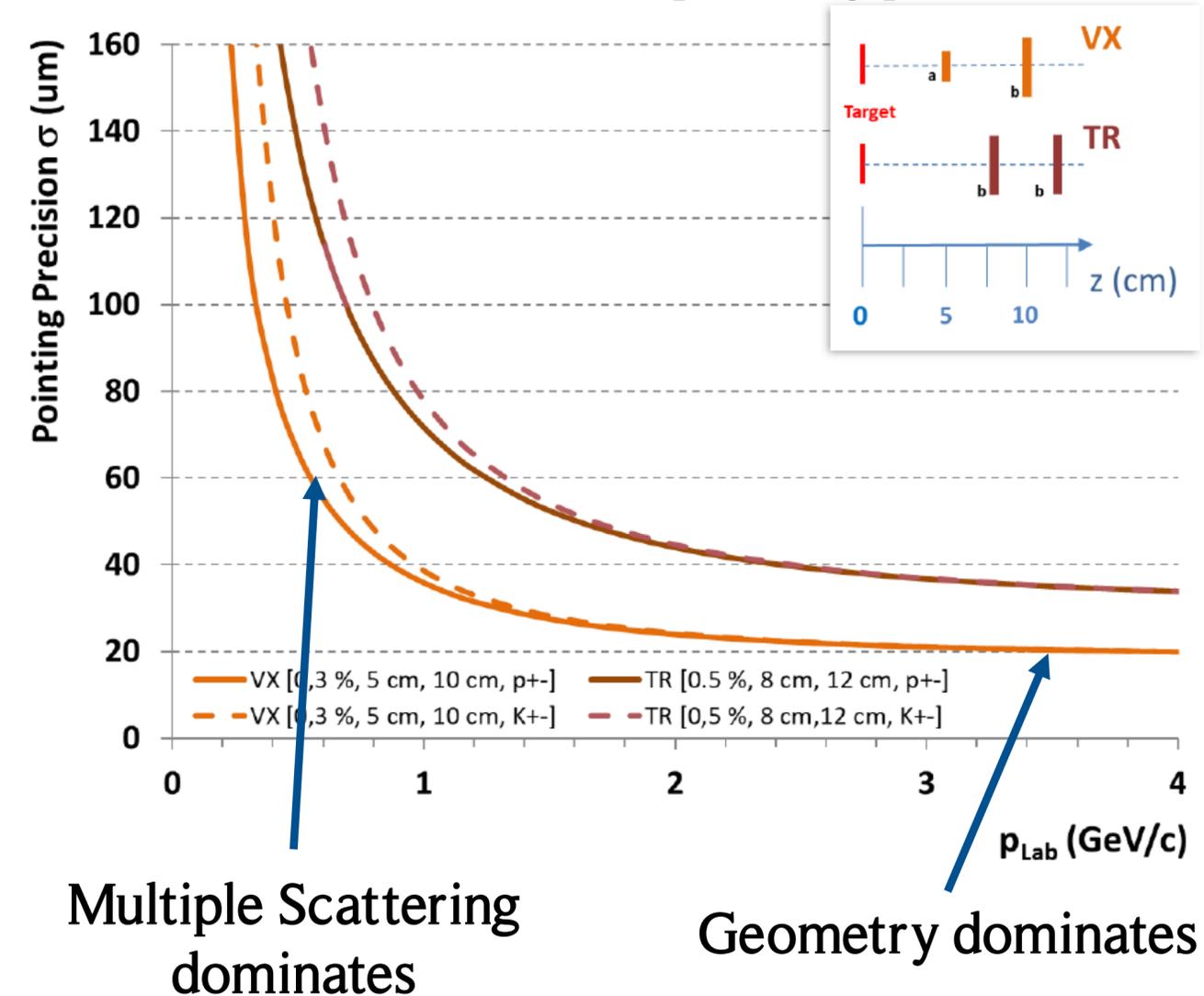
High track density in the Inner Tracker

MVD track seeds minimizing STS ambiguities

# Requirements for Low-p Tracking

$$\sigma_{MS} \sim \frac{1}{\beta \cdot p_{lab}} \sqrt{\frac{x}{X_0}}$$

Generic 2-station pointing precision



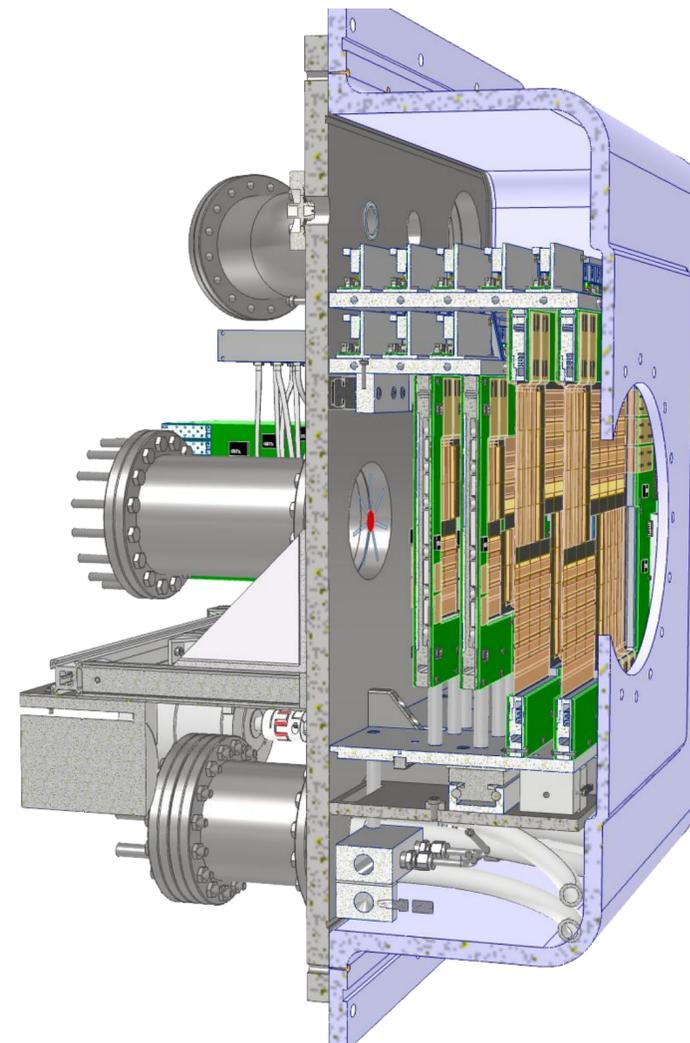
# Requirements for Low-p Tracking

Design driven by material budget

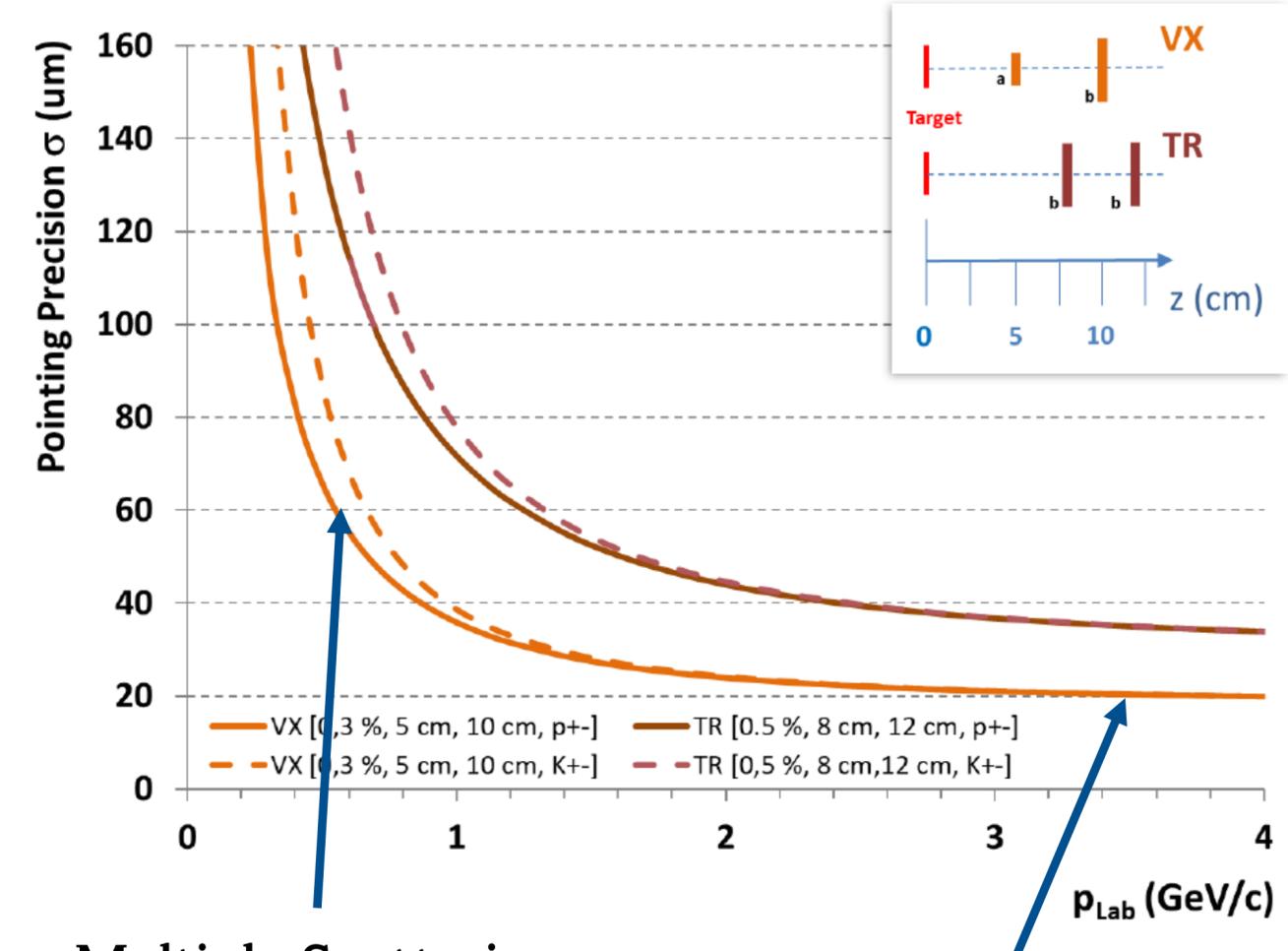
- Multiple Scattering dominated regime
- Technology: (thinned) CMOS MAPS
- Tracking **before** beam window (vacuum operation)



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## Generic 2-station pointing precision



Multiple Scattering  
dominates

Geometry dominates

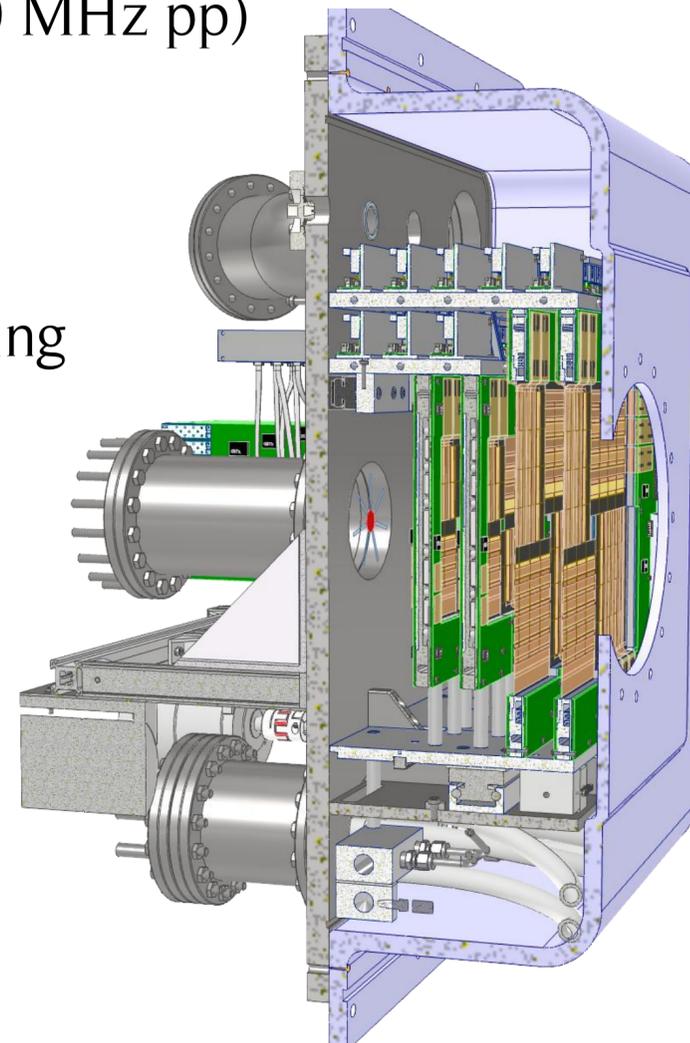
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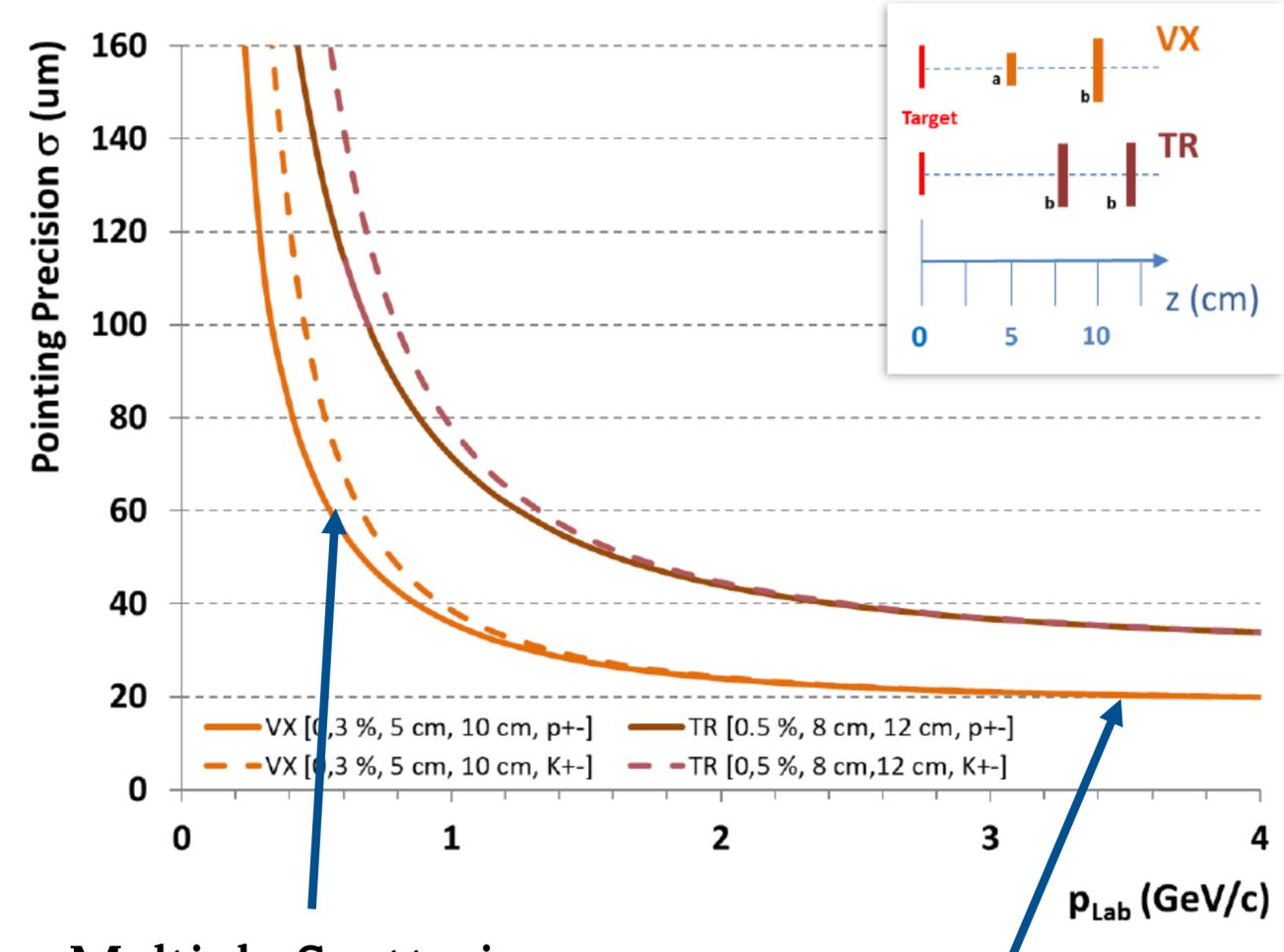
But: No lunch for free

- MVD rate limited to 100 kHz Au+Au (10 MHz pp)
  - Readout speed, radiation hardness
  - 1st station needs annual exchange
- Passive cooling in acceptance
  - Large modules for mechanics and cooling
- Double-sided integration



$$\sigma_{MS} \sim \frac{1}{\beta \cdot p_{lab}} \sqrt{\frac{x}{X_0}}$$

## Generic 2-station pointing precision

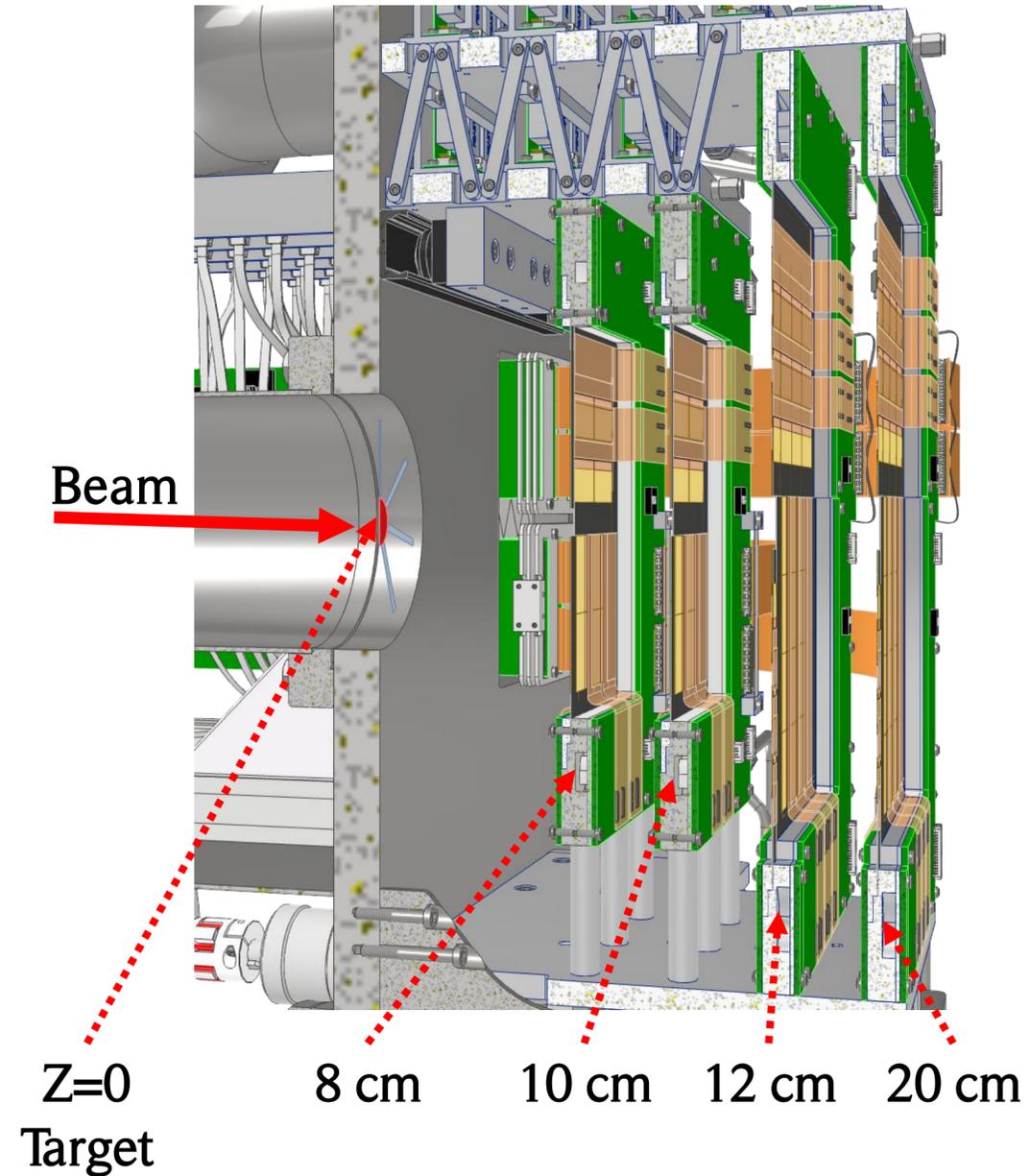
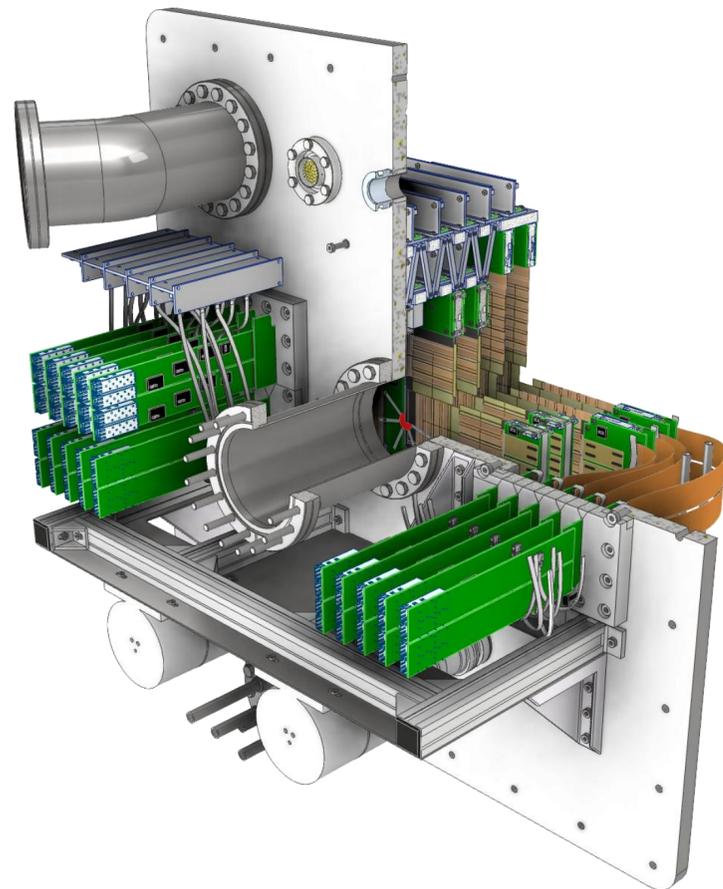


Multiple Scattering dominates

Geometry dominates

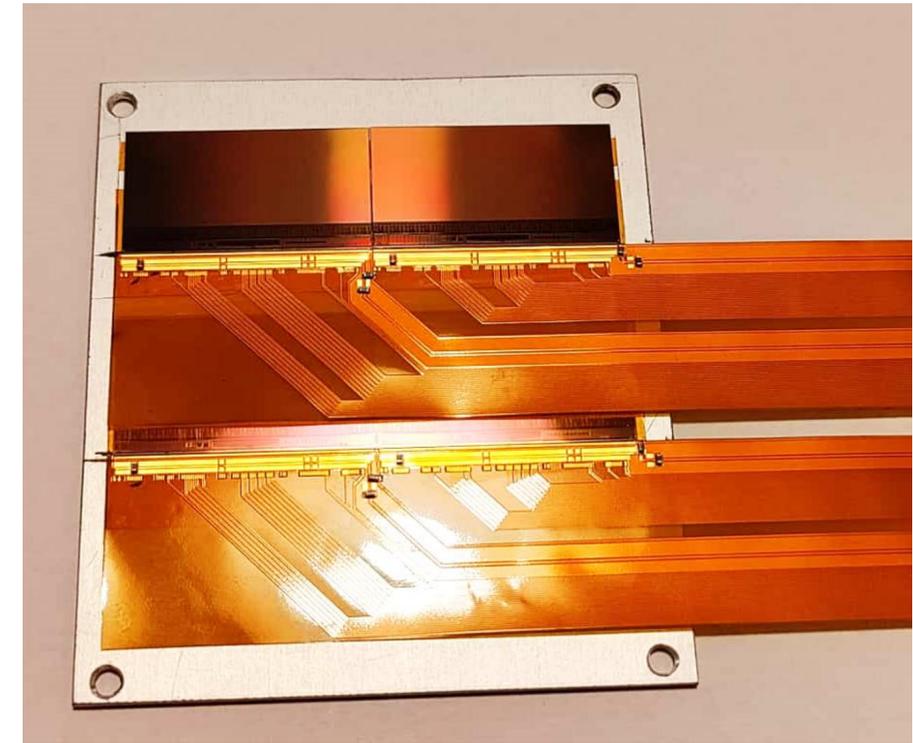
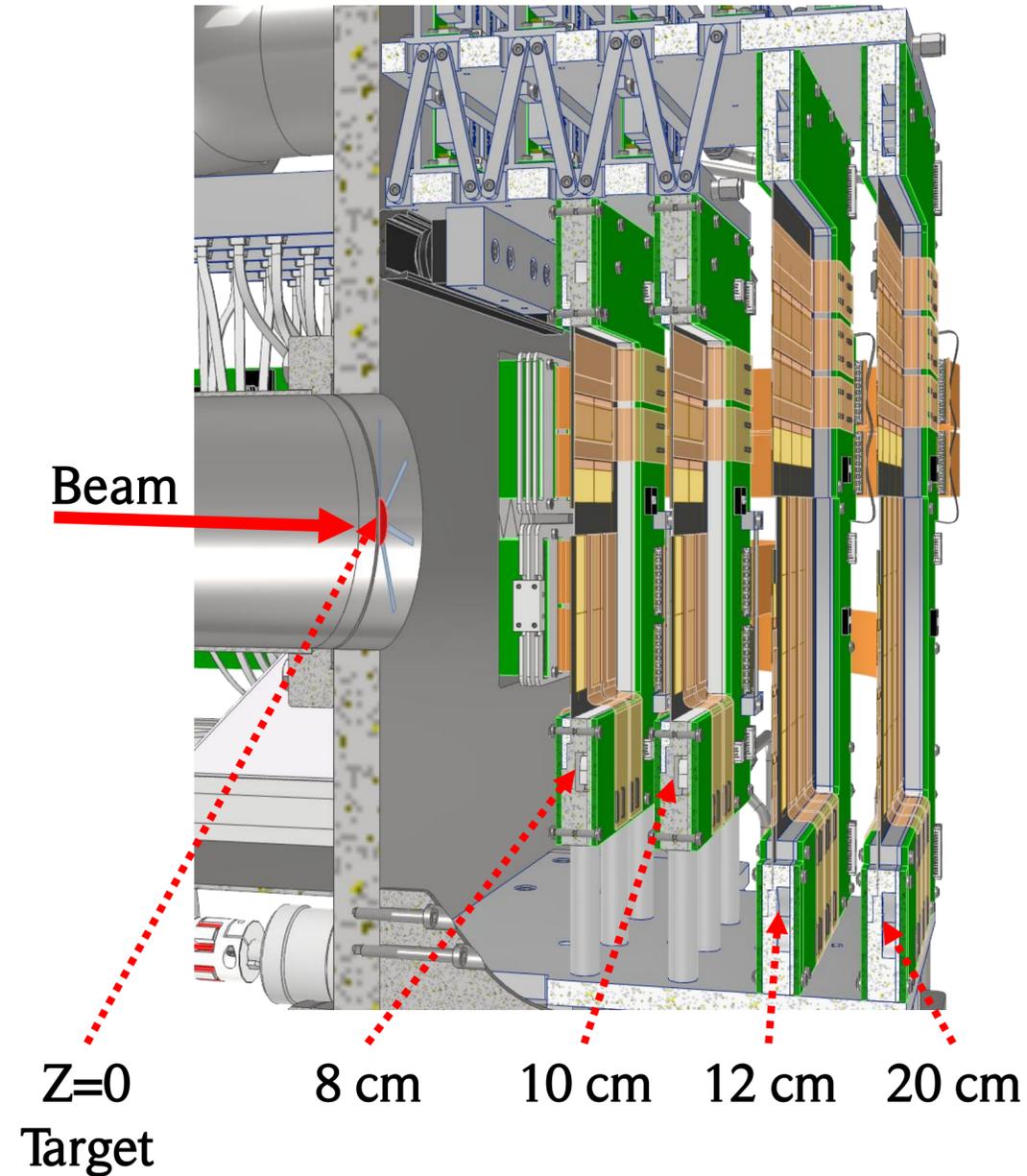
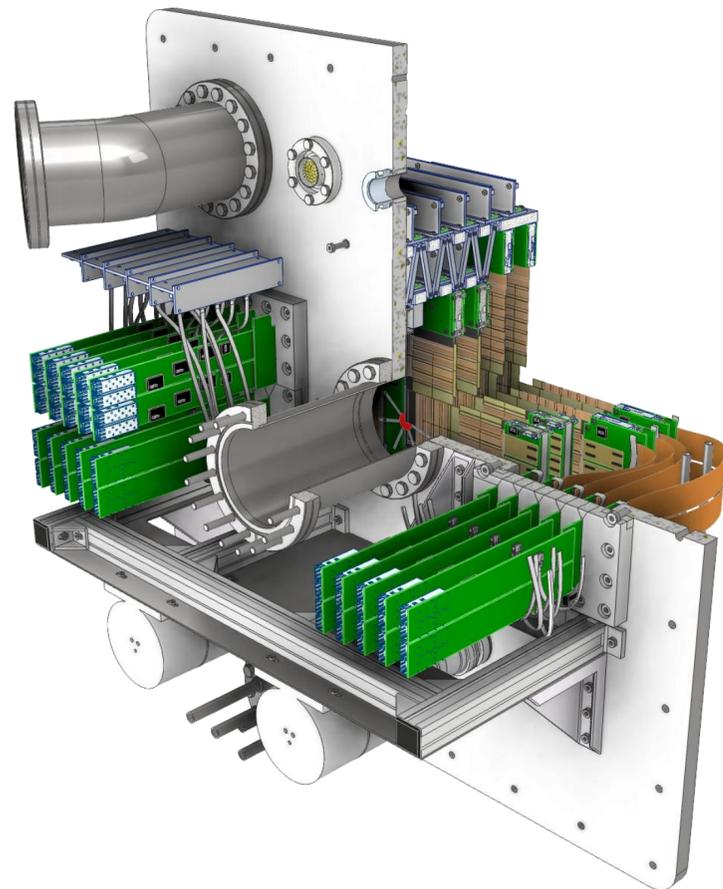
# Overview Micro Vertex Detector

4 planar tracking stations, ~300 sensors  
→ 8 – 20 cm downstream of target



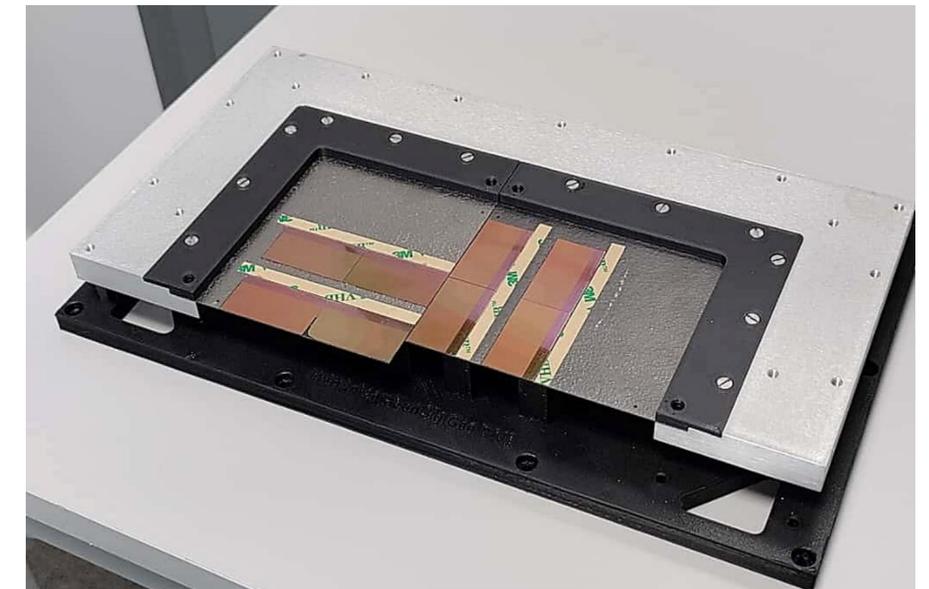
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MIMOSIS-2.1 with MVD FPC

MIMOSIS-2 on TPG



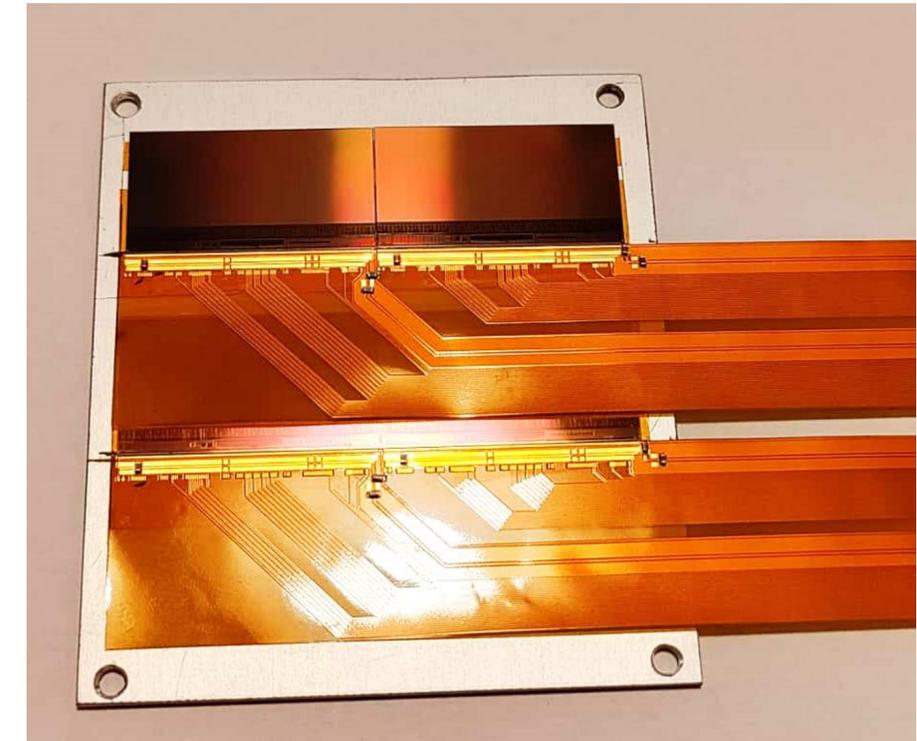
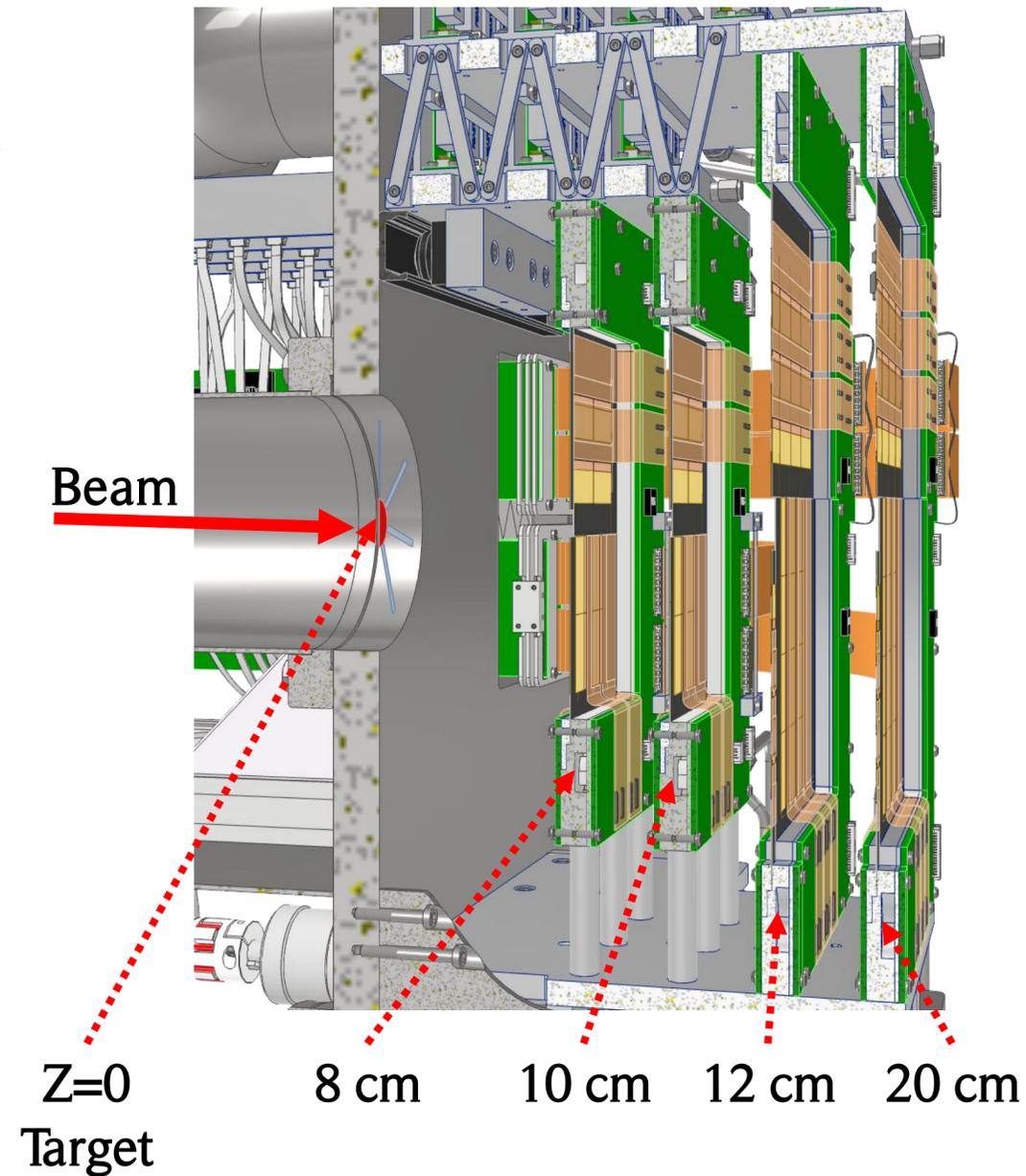
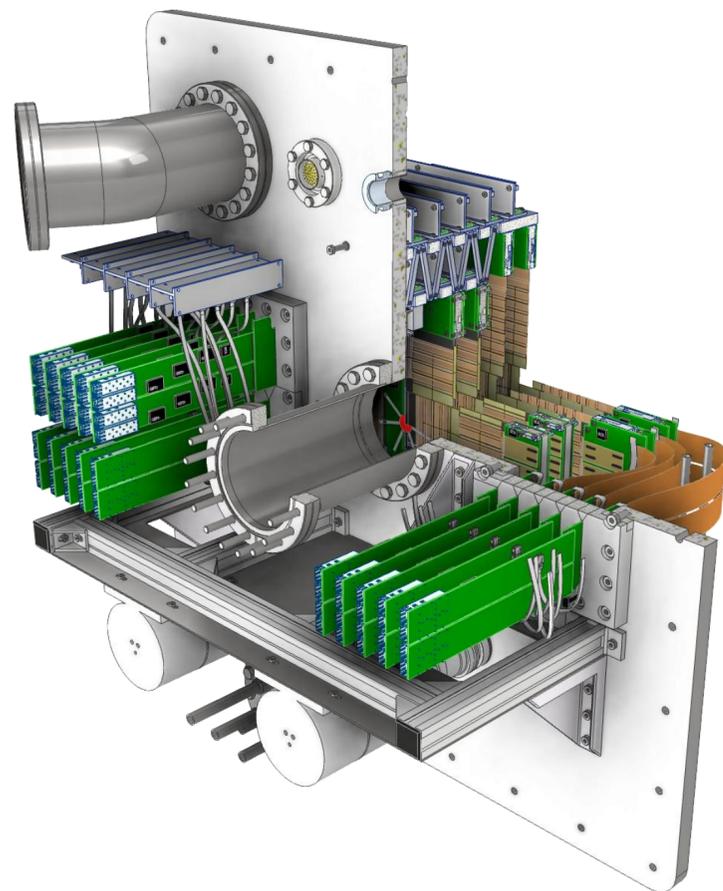
F. Matejcek et al.

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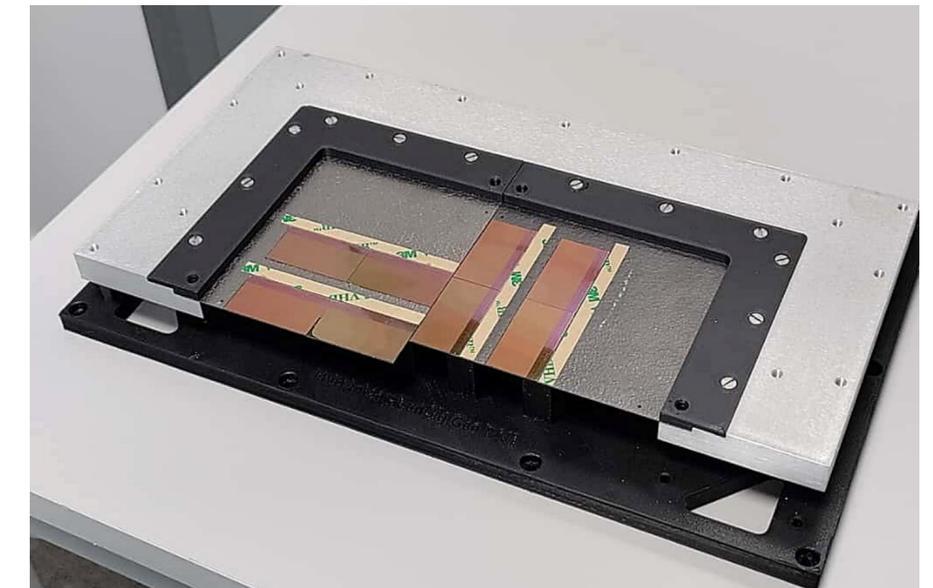
## Key challenges:

- Magnetic field and vacuum operation
- Material budget (0.3% – 0.5%  $X_0$ )
- Double-sided integration



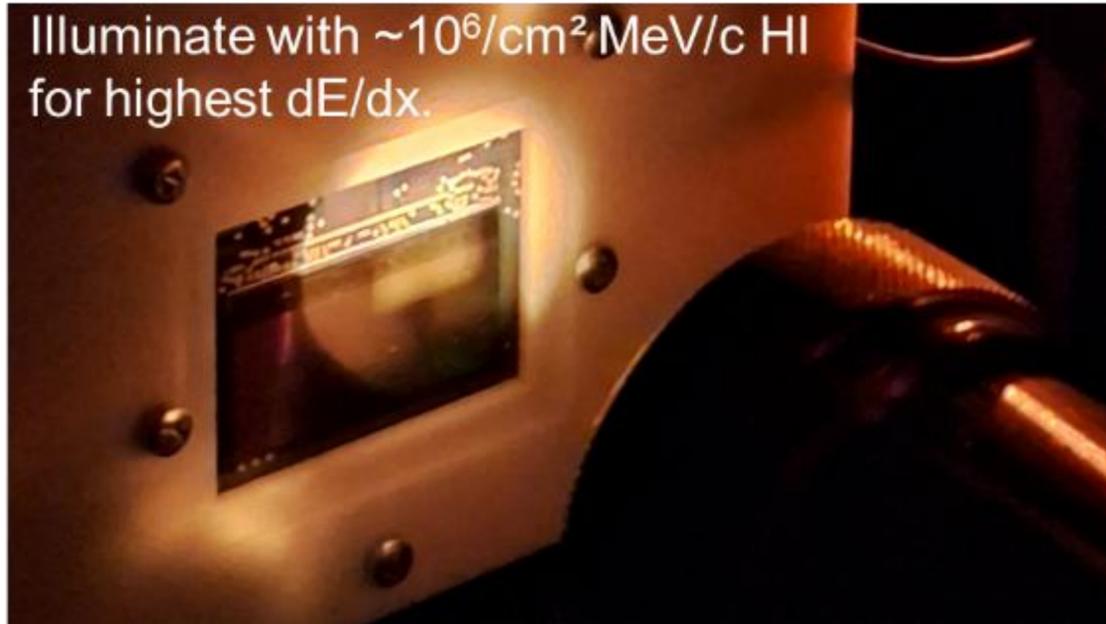
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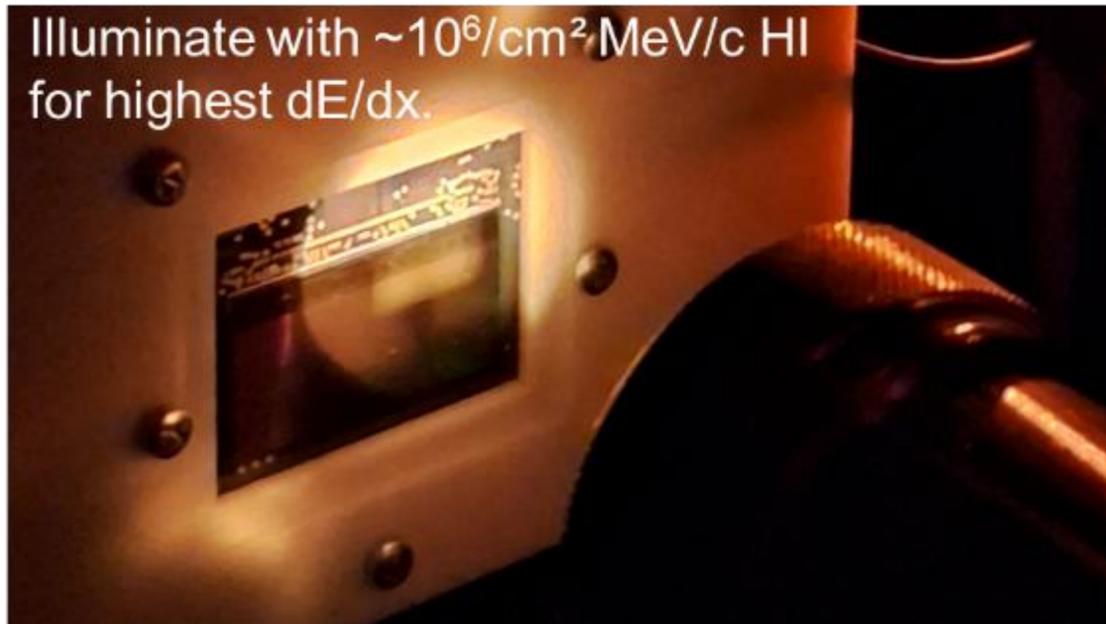
# CBM and the GSI Pixel Platform

Illuminate with  $\sim 10^6/\text{cm}^2$  MeV/c HI  
for highest dE/dx.



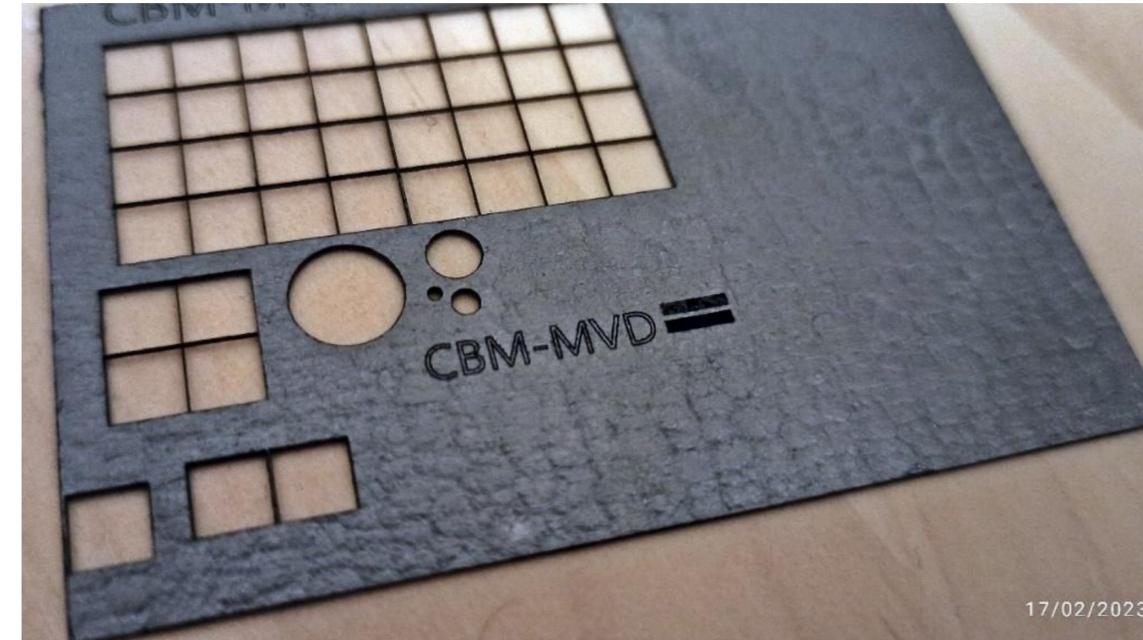
Sensor validation infrastructure  
(SEE tests at UNILAC,  
mCBM@SIS18, ...)

# CBM and the GSI Pixel Platform

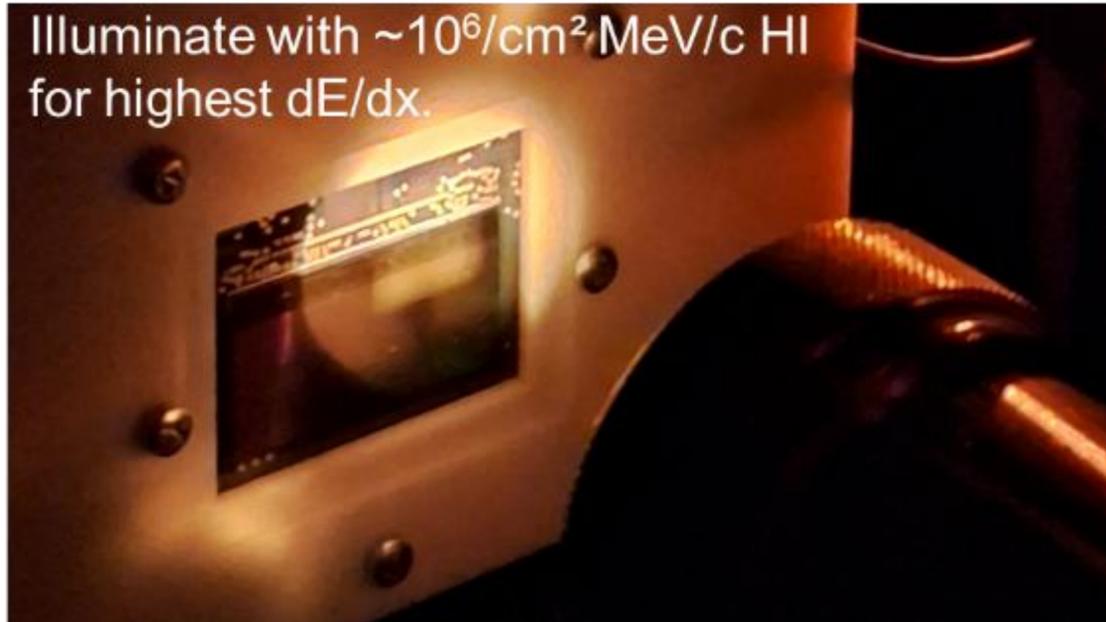


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Integration infrastructure  
(metrology, wire-bonding, probe  
testing, laser-ablation, ...)

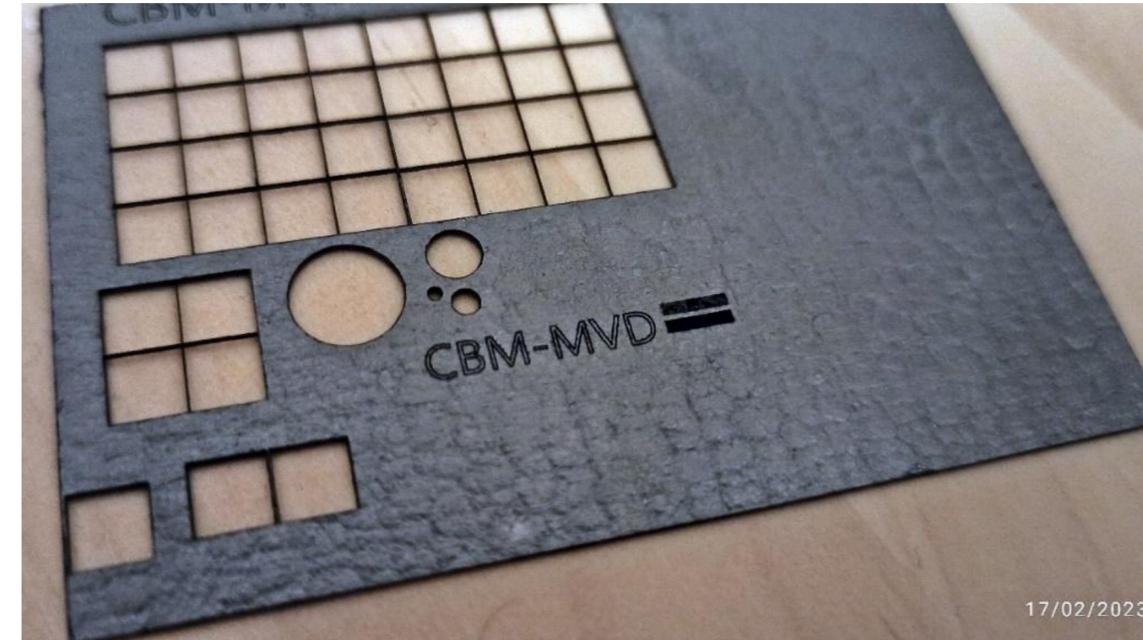


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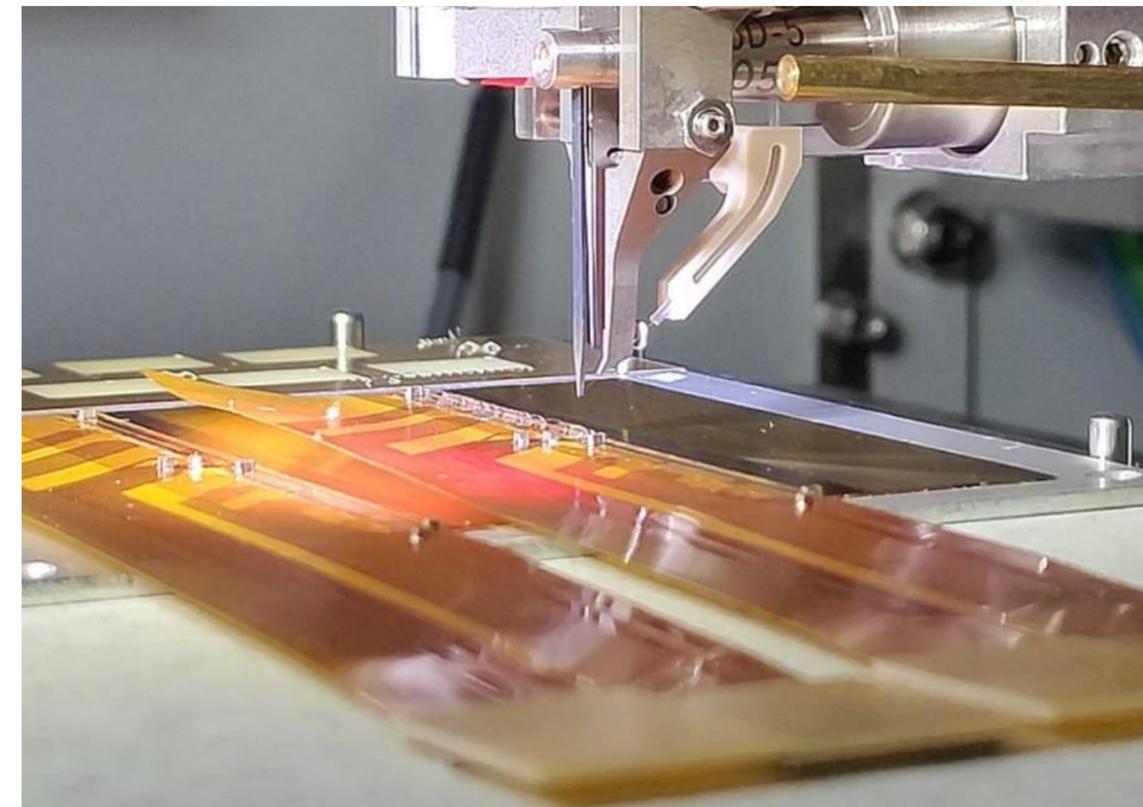


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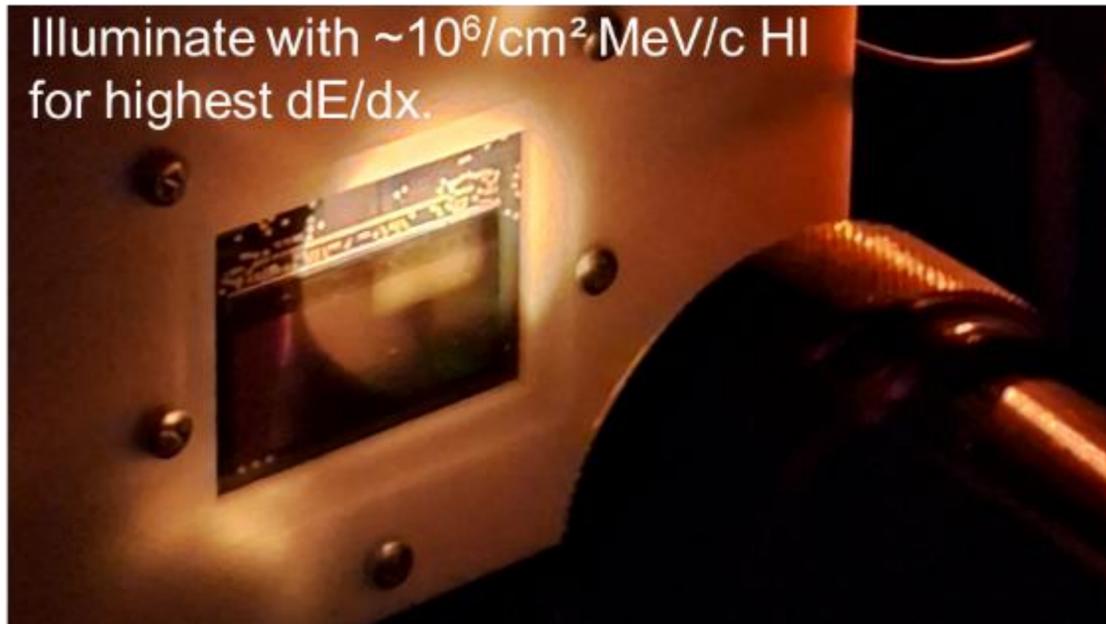
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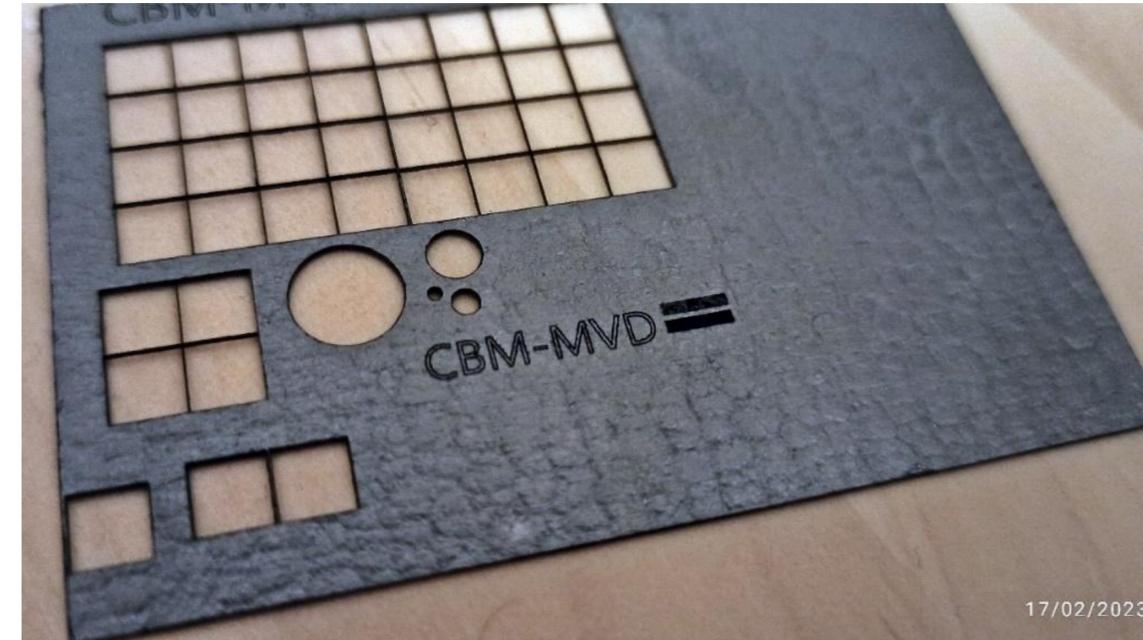
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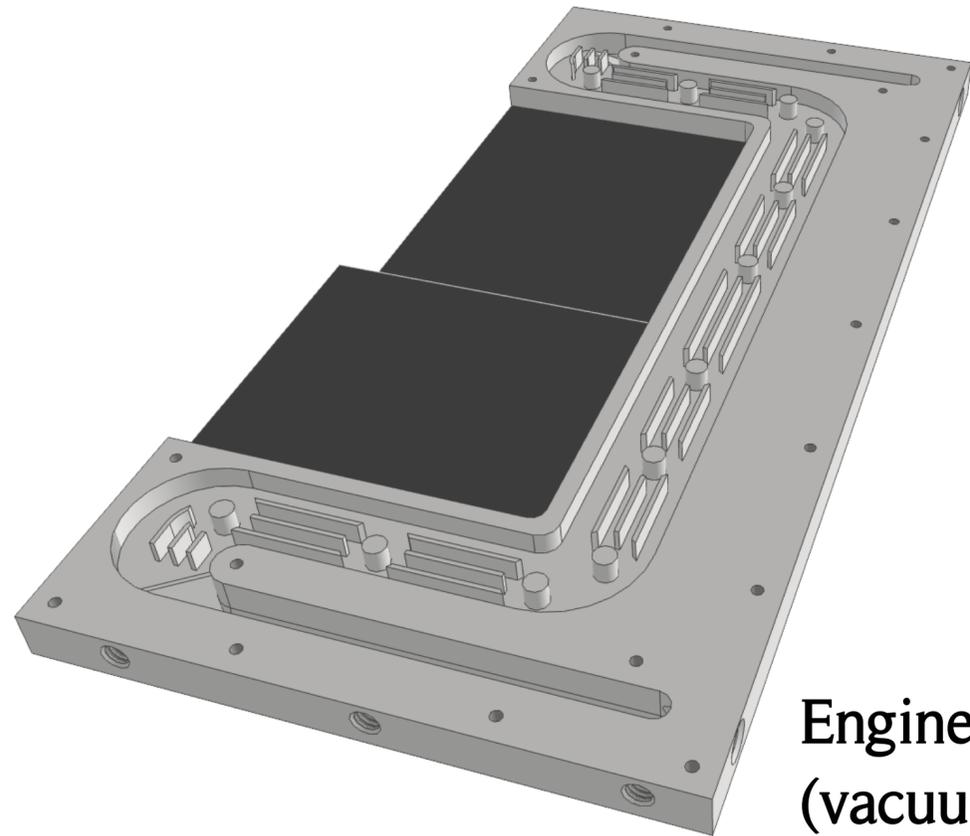
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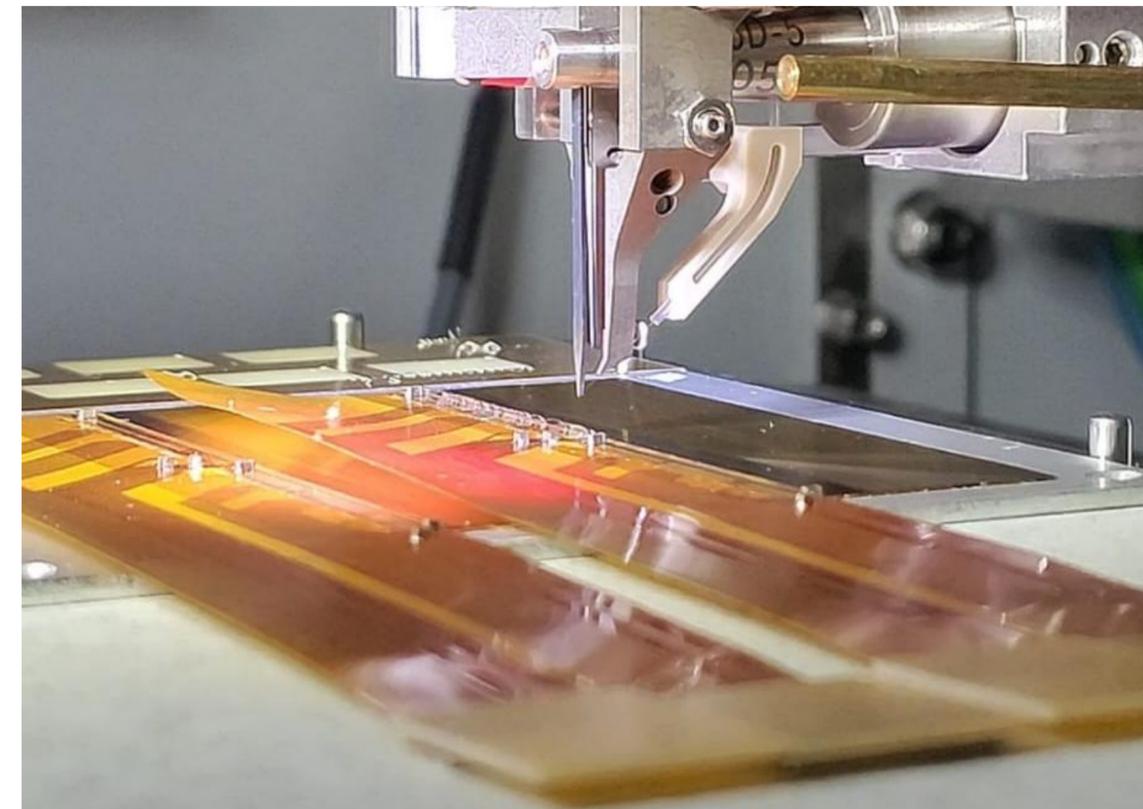


Integration infrastructure  
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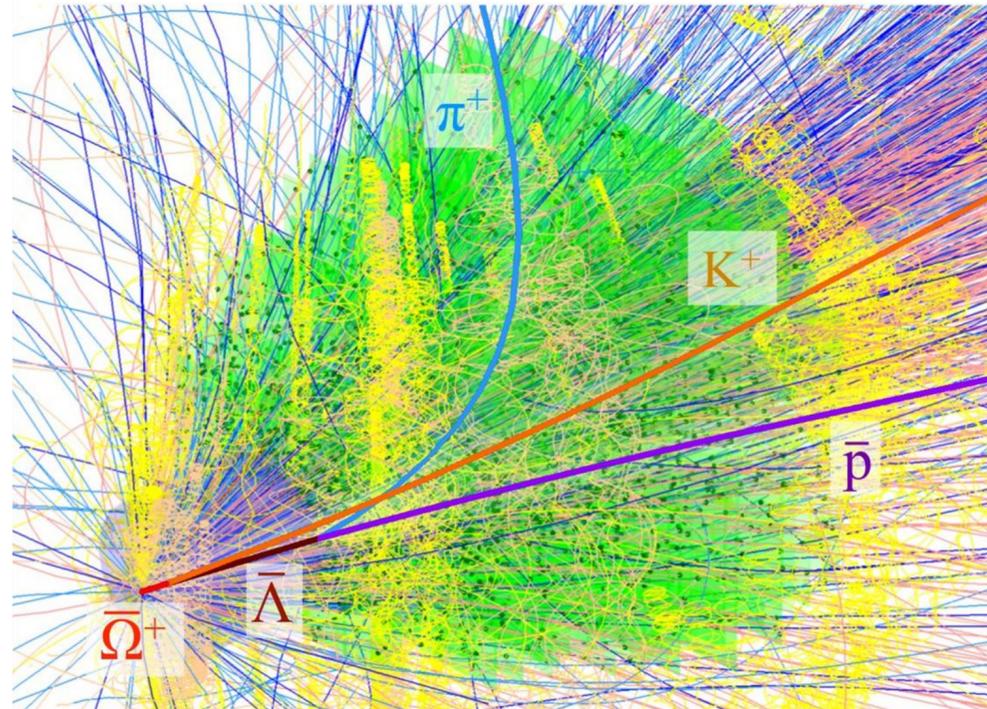
Engineering expertise  
(vacuum feedthroughs, heat sinks, ...)



Chapter 1

# MIMOSIS

# The MIMOSIS Story



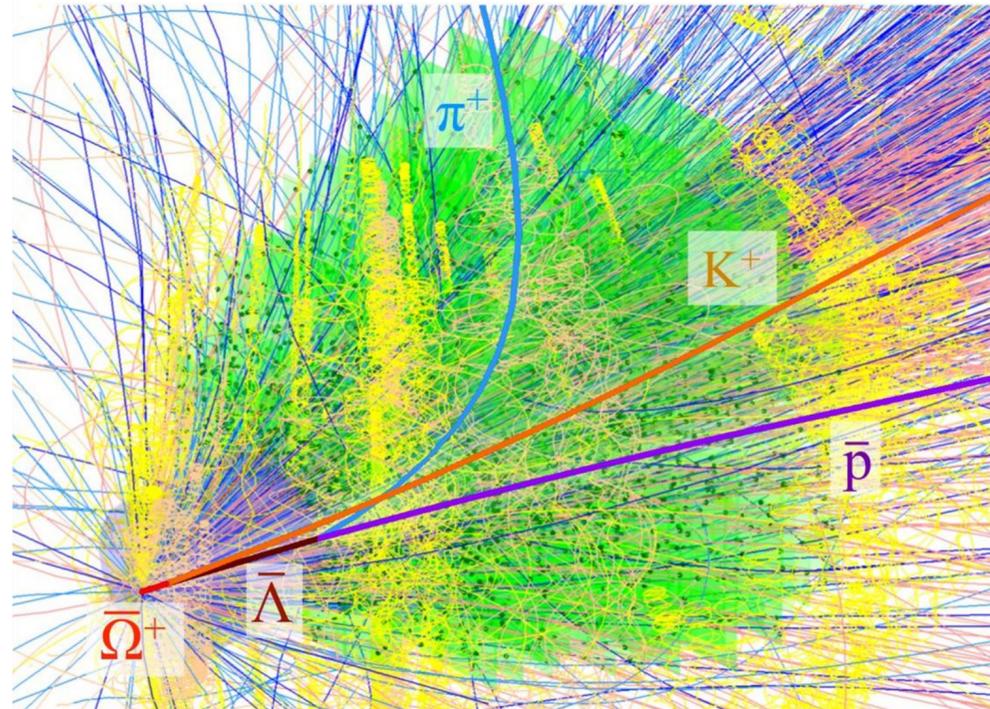
“The needle in the haystack”  
Anti- $\Omega$  in 12 AGeV Au-Au collisions  
in the Inner Tracker

	Requirement
Spatial precision	$\sim 5 \mu\text{m}$
Time resolution	$\sim 5 \mu\text{s}$
Thickness	$\sim 50 \mu\text{m}$
Power dissipation	$< 100 \text{ mW/cm}^2$
Radiation doses (non-ionizing)	$> 7 \times 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$
Radiation doses (ionizing)	$> 5 \text{ Mrad}$
Radiation gradient on chip	$\sim 100\%$
Rate capability avg. (peak)	20 (80) MHz/cm <sup>2</sup>
HI-tolerance	10 Hz/mm <sup>2</sup>

*~10x ALPIDE*

*~20x ALPIDE*

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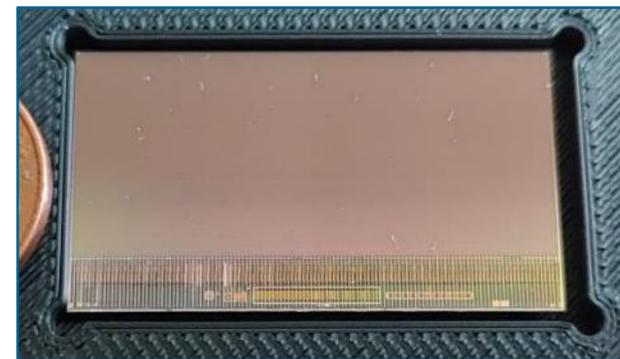
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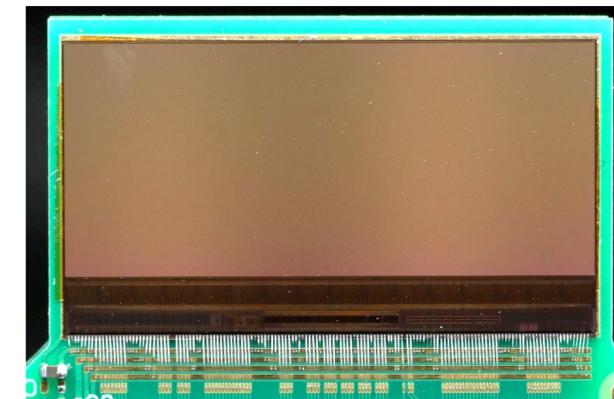
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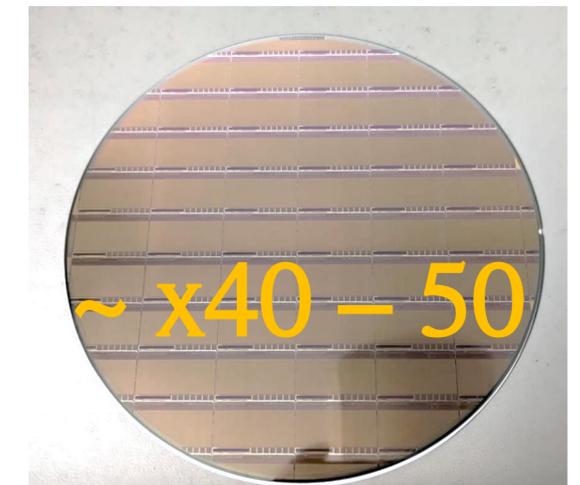
MIMOSIS-0 (2018)



MIMOSIS-1 (2020)



MIMOSIS-2/2.1 (2024)

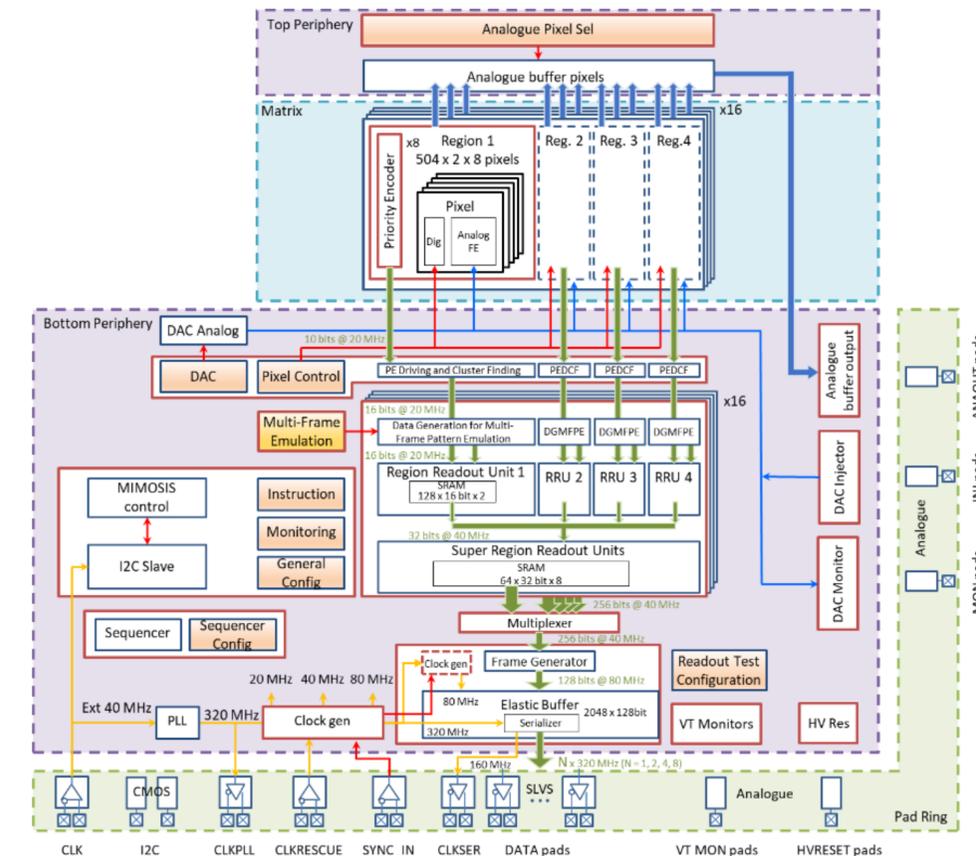
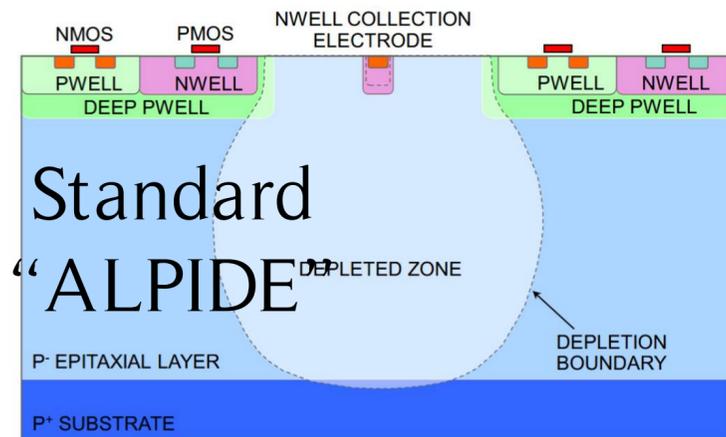


MIMOSIS-3 (2026)

# The MIMOSIS Story

Joint venture: IPHC Strasbourg, University Frankfurt, GSI

→ Starting point: ALPIDE pixel, fully custom digital front-end



# The MIMOSIS Story

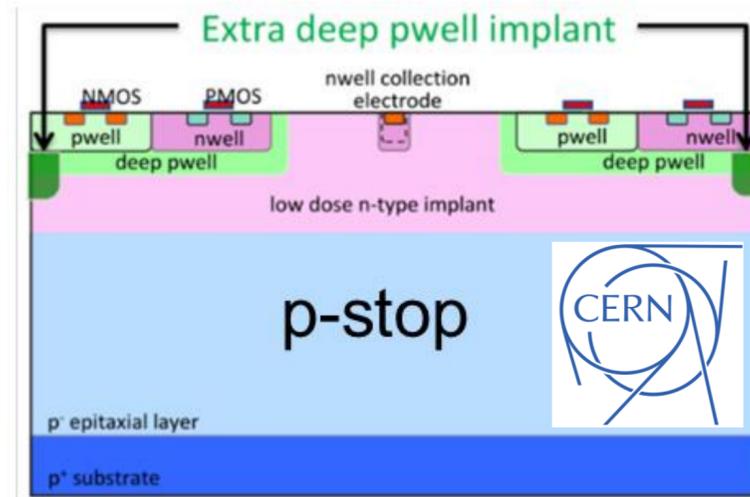
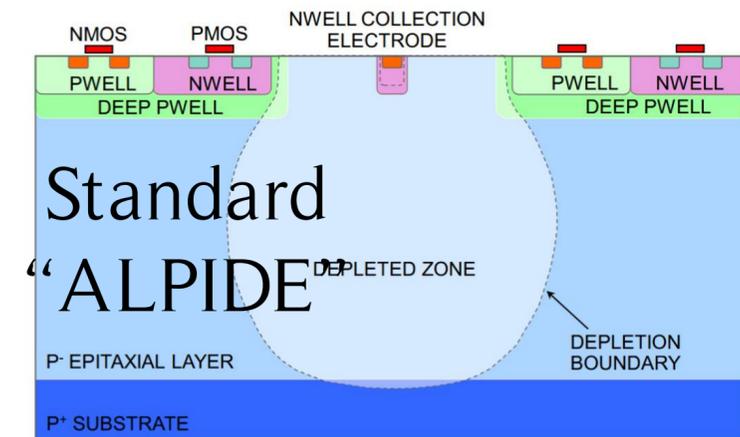
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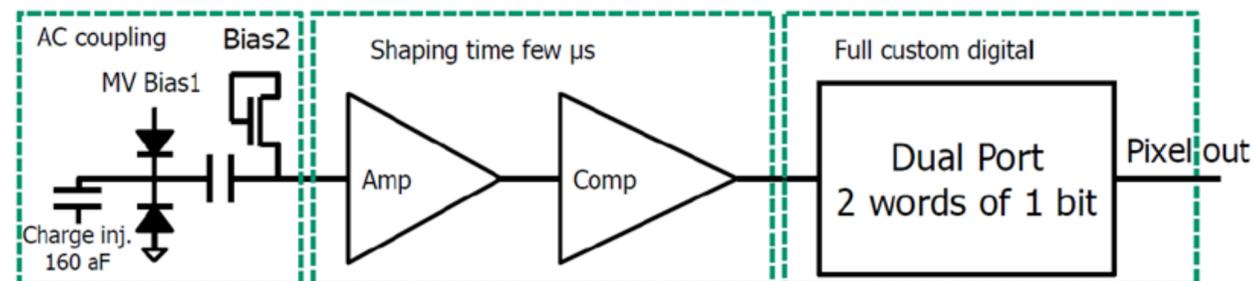
Improved radiation hardness

→ Modified epitaxial layer (“p-stop”)

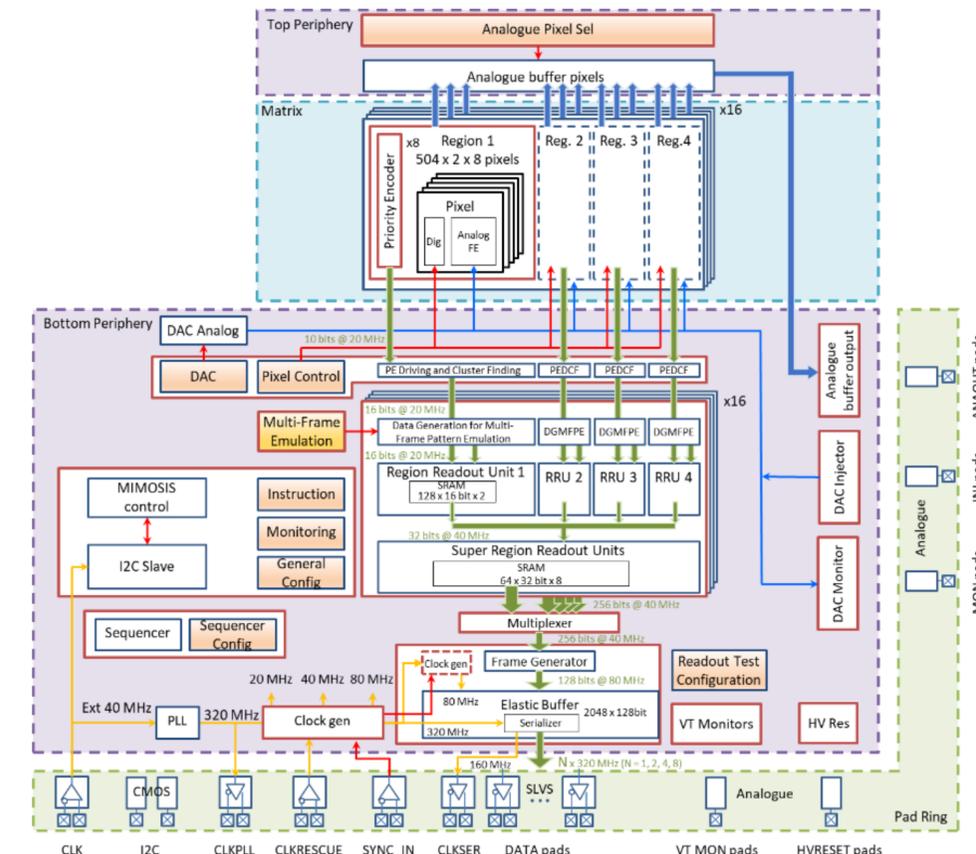
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F. Morel



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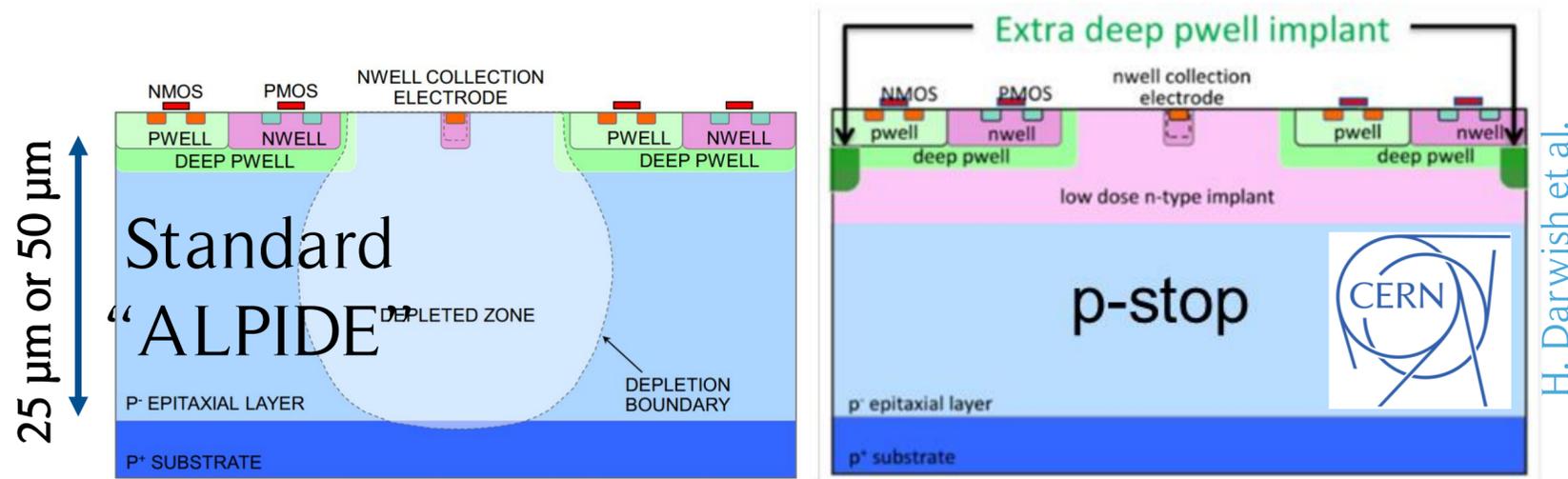
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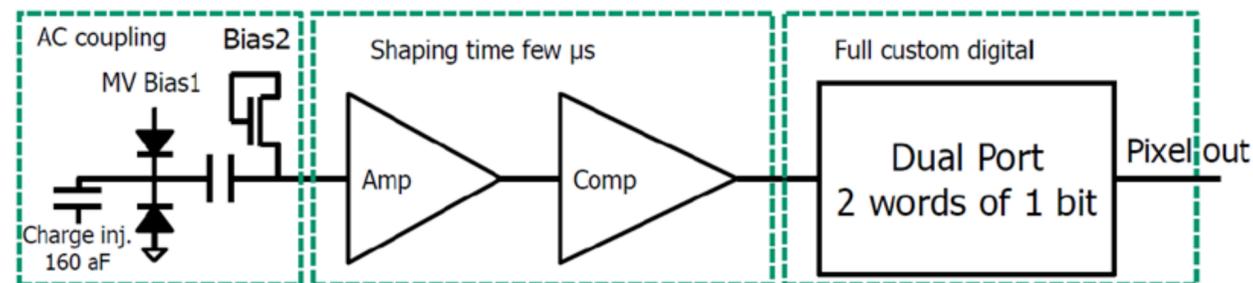
→ Increased diode bias (AC-coupling)

Improved operation range (signal)

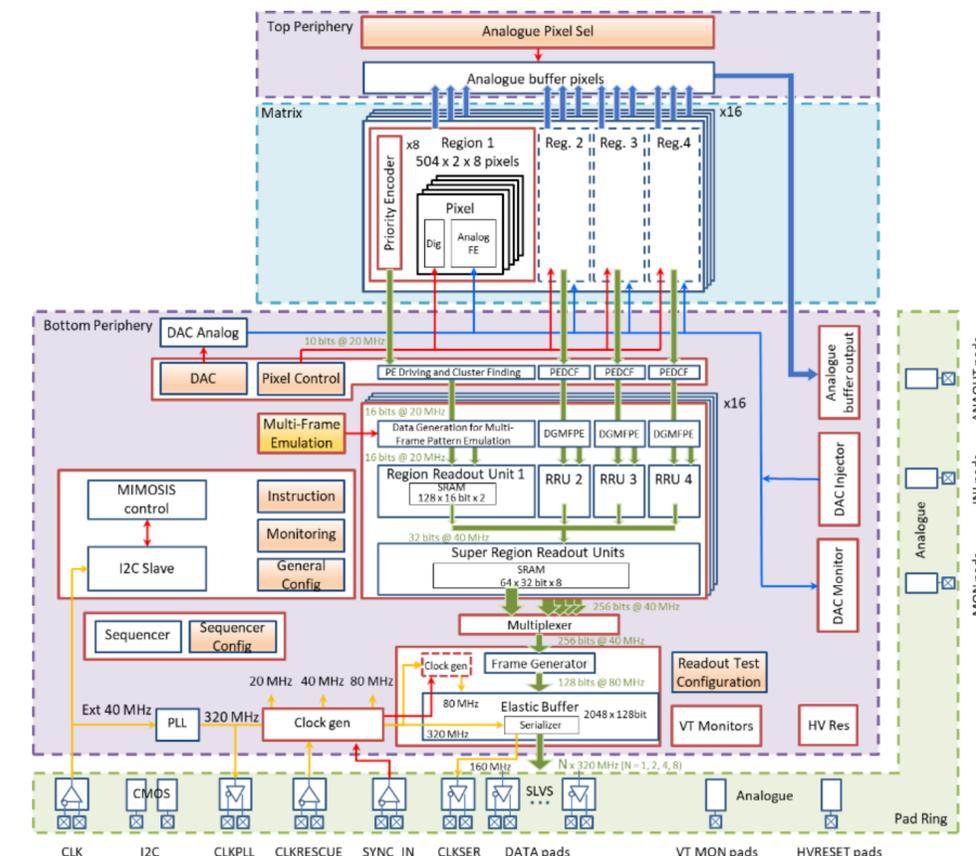
→ 50  $\mu\text{m}$  epi thickness



H. Darwish et al.



F. Morel



# The MIMOSIS Story

Joint venture: IPHC Strasbourg, University Frankfurt, GSI

→ Starting point: ALPIDE pixel, fully custom digital front-end

Improved readout speed

→ 8 x 320 Mbit/s

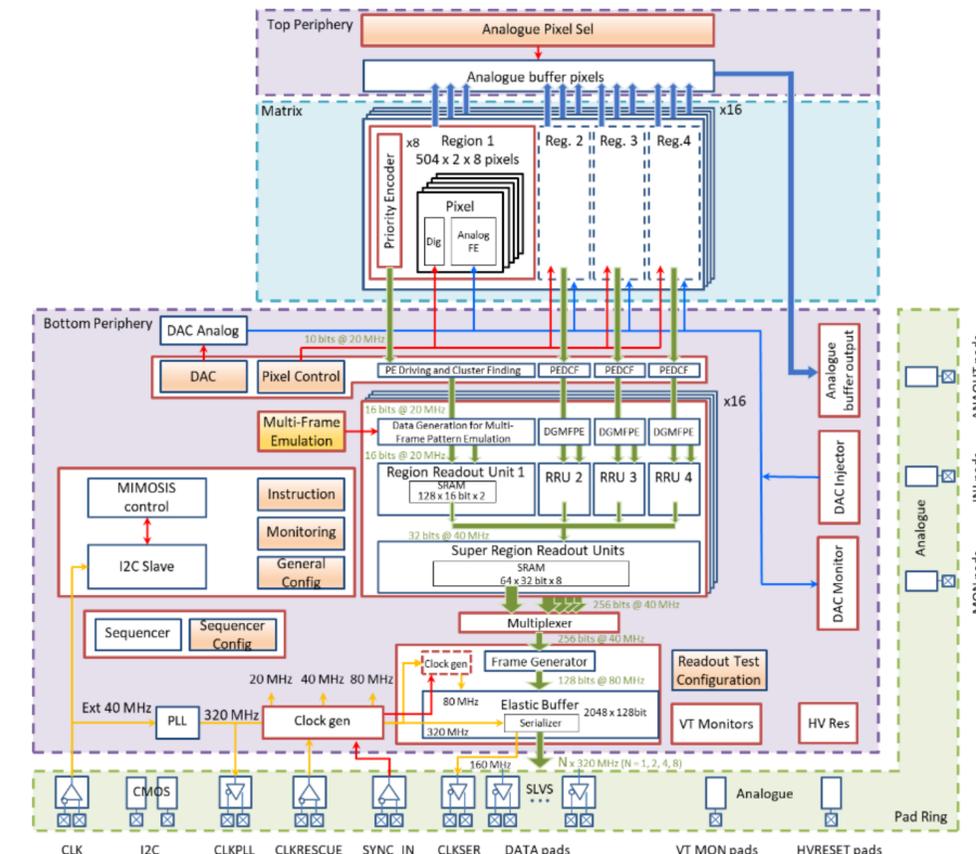
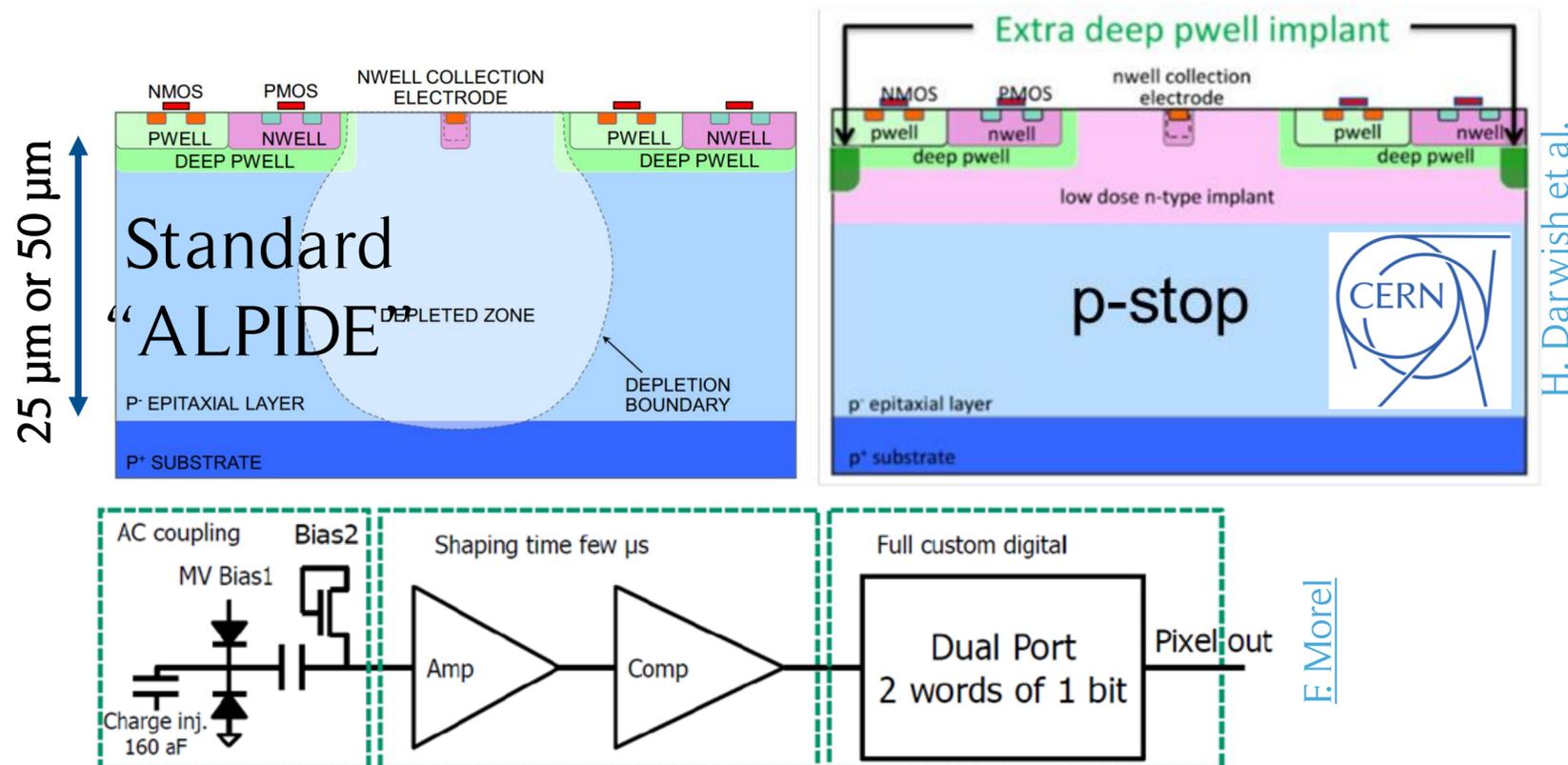
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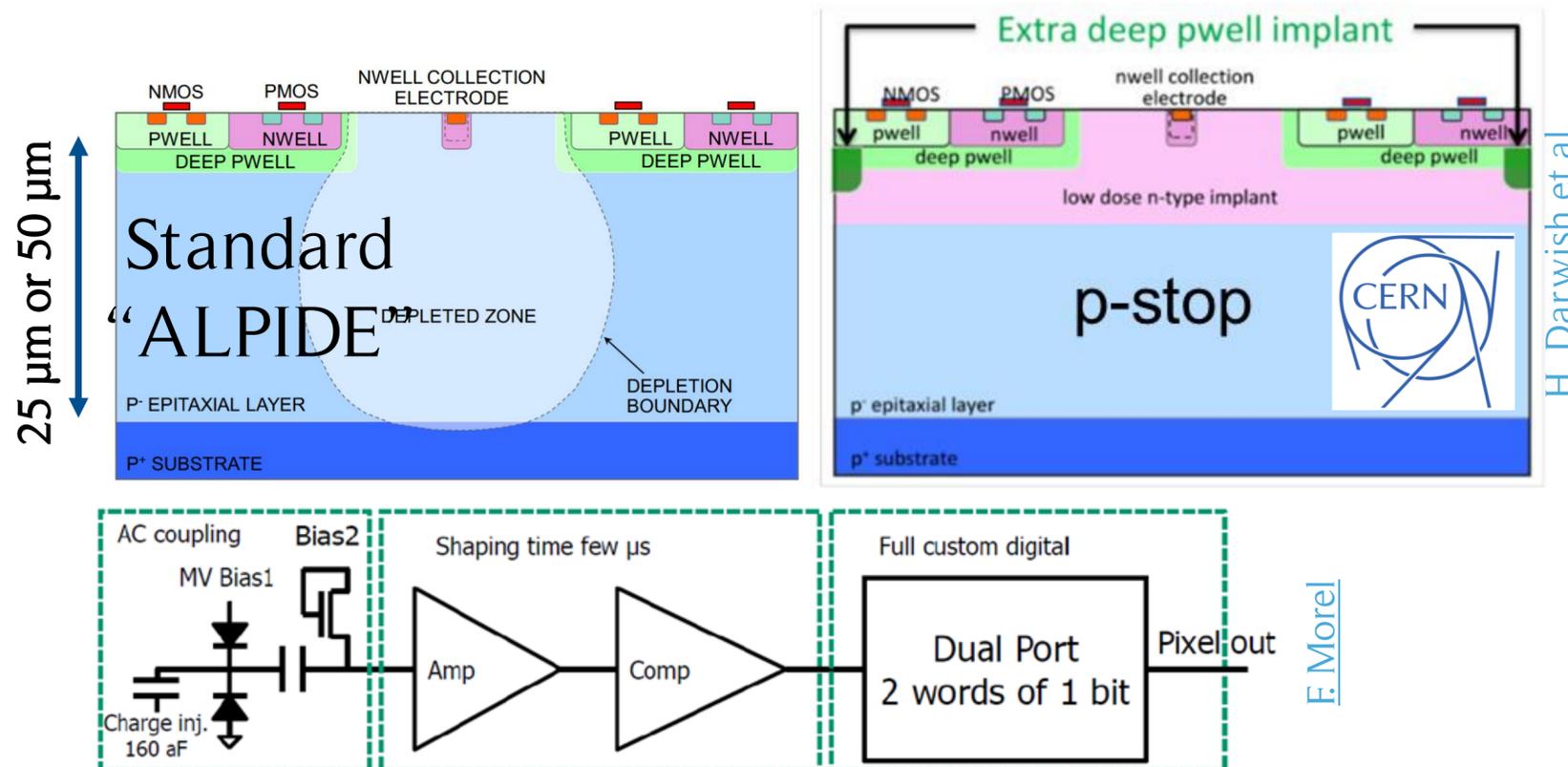
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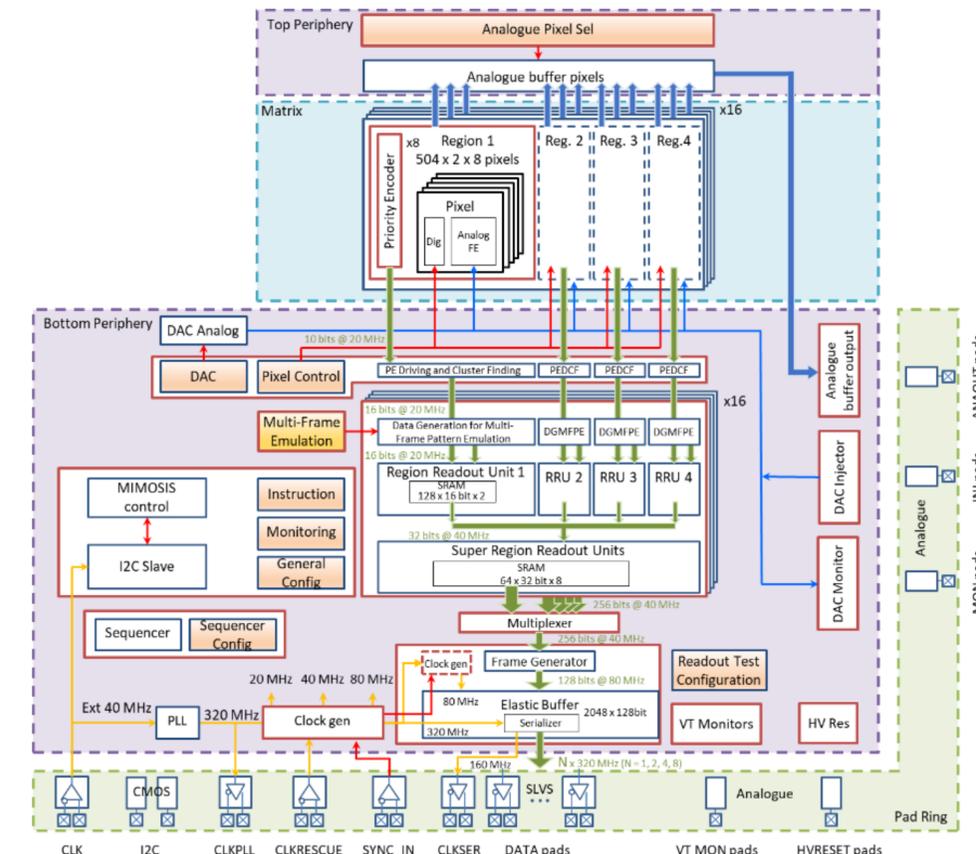
Improved readout speed  
 → 8 x 320 Mbit/s

Improved SEE hardening  
 → Hamming encoding (DACs)  
 → Triple Modular Redundancy



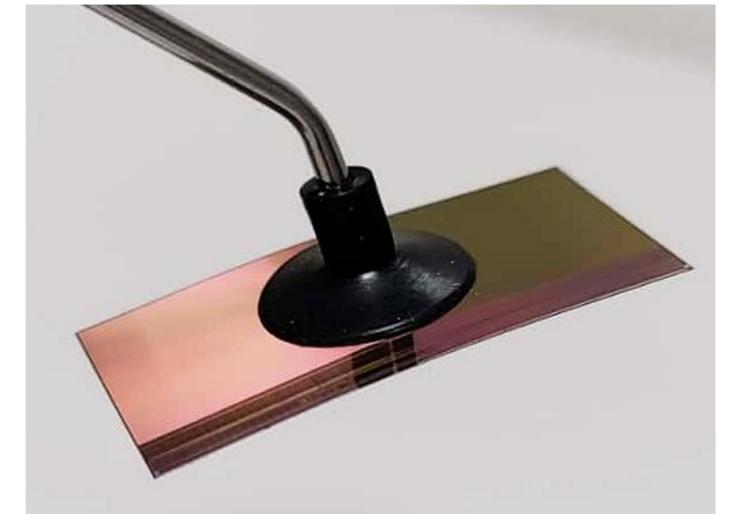
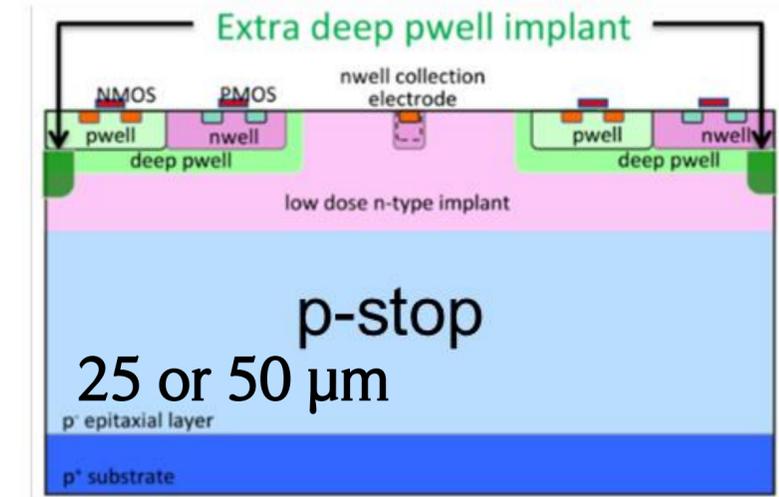
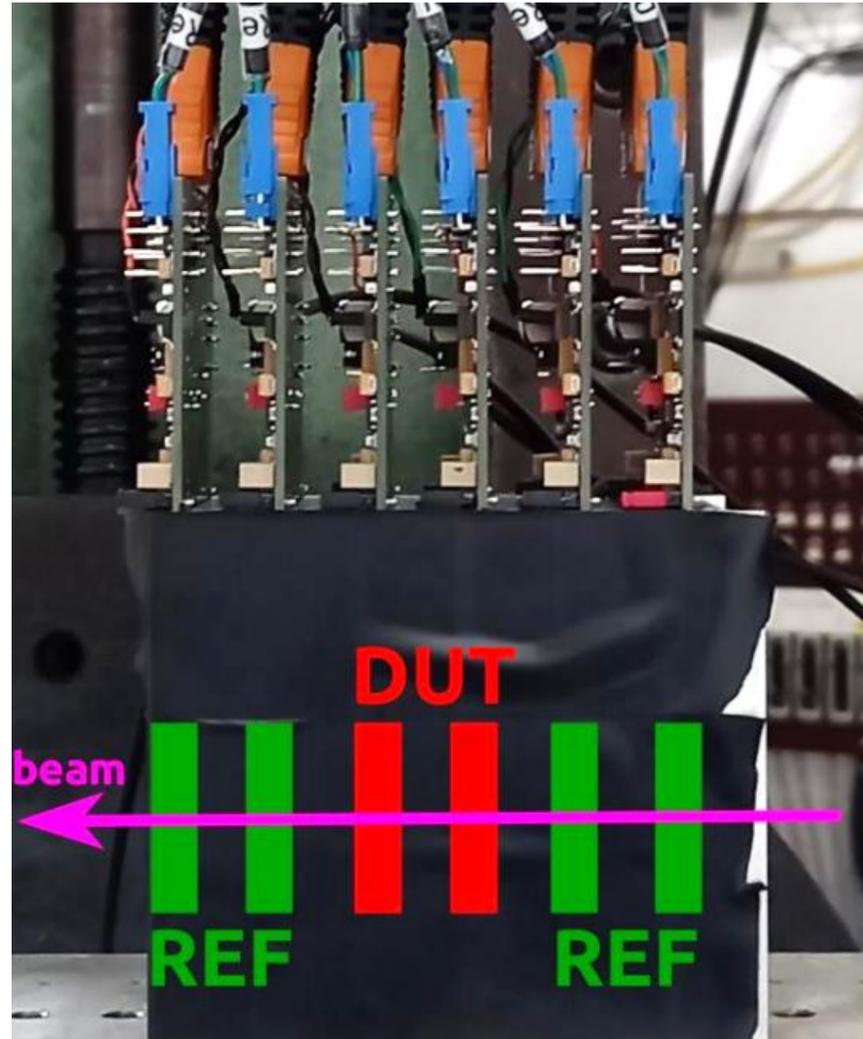
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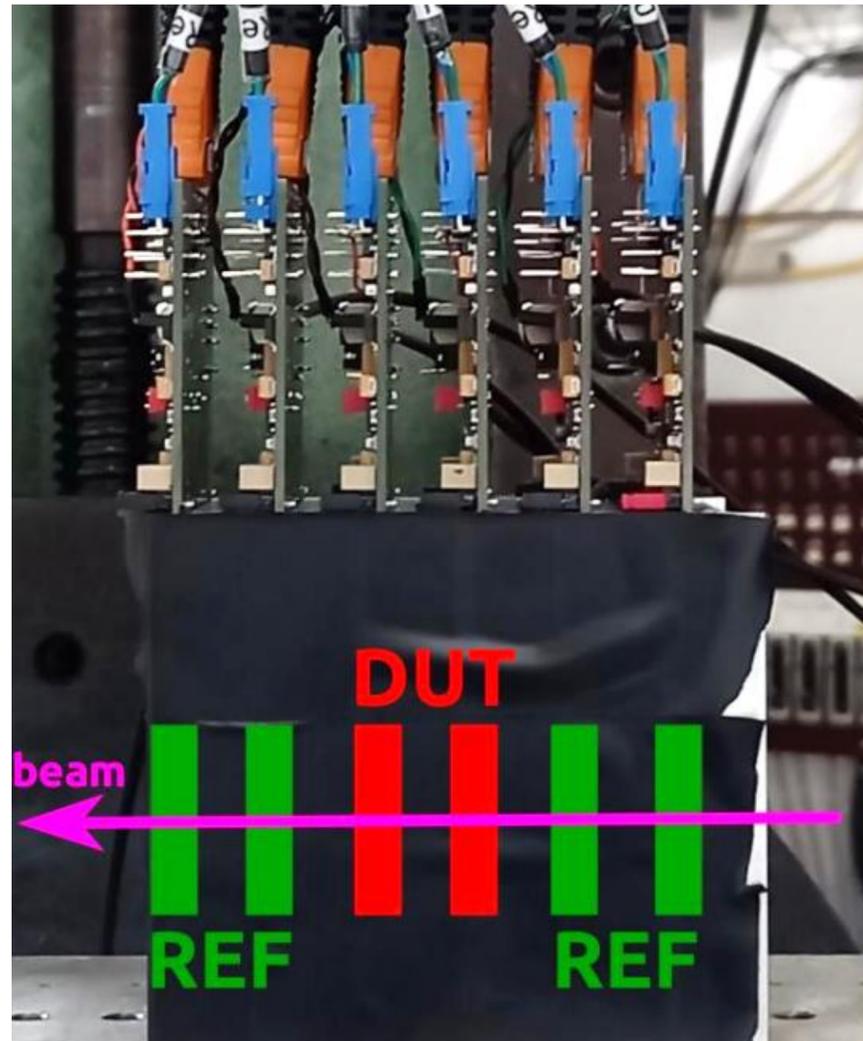
# MIMOSIS-2.1 Performance

- All-MIMOSIS beam telescope
- 4 reference sensors, 2 DUTs
- Controlled room temperature
- Dark rate  $< 10^{-10}$ /pixel/frame

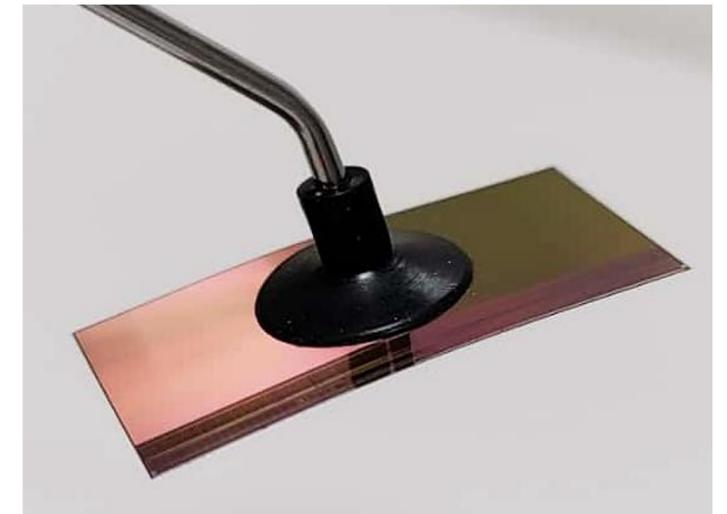
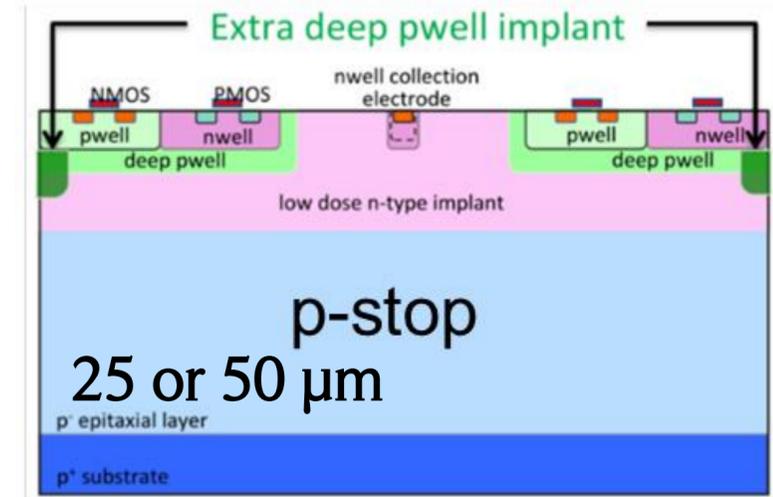
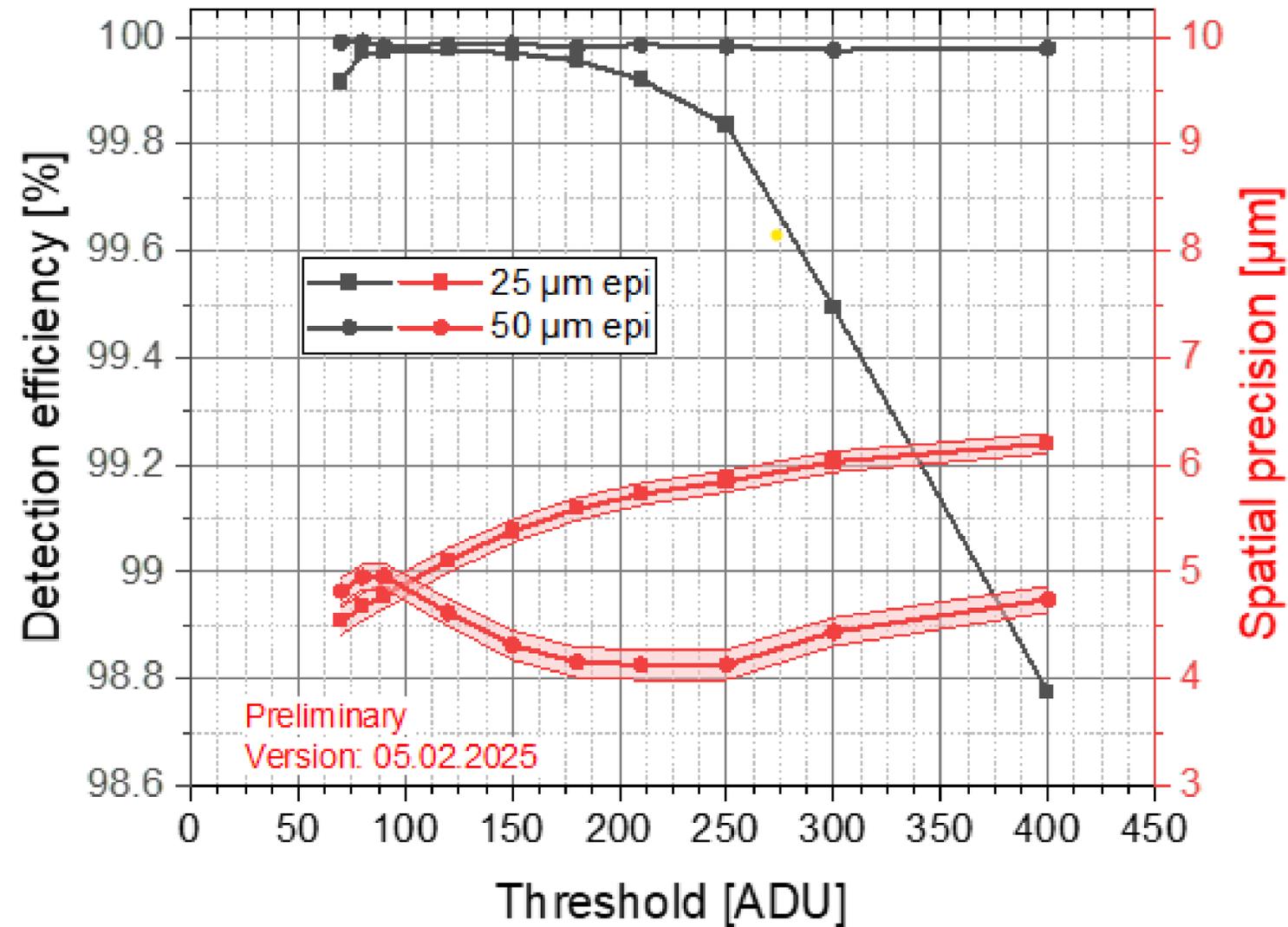


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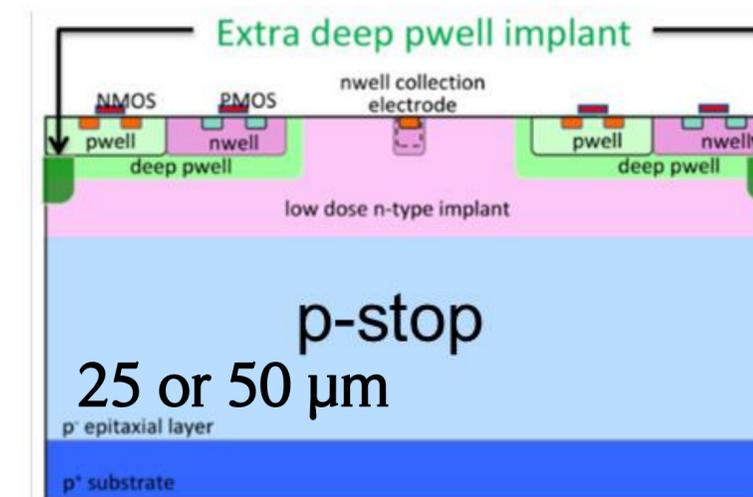
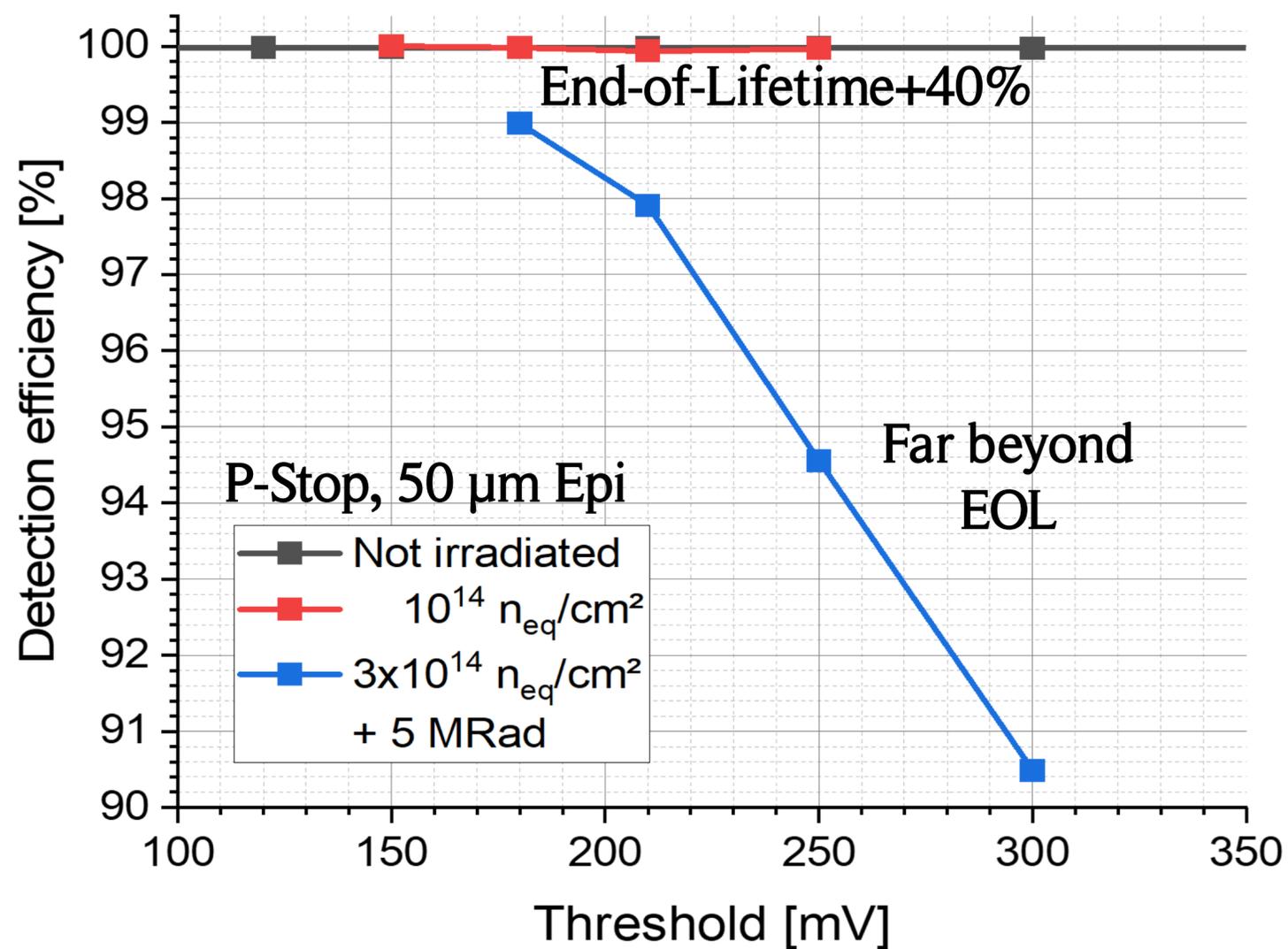
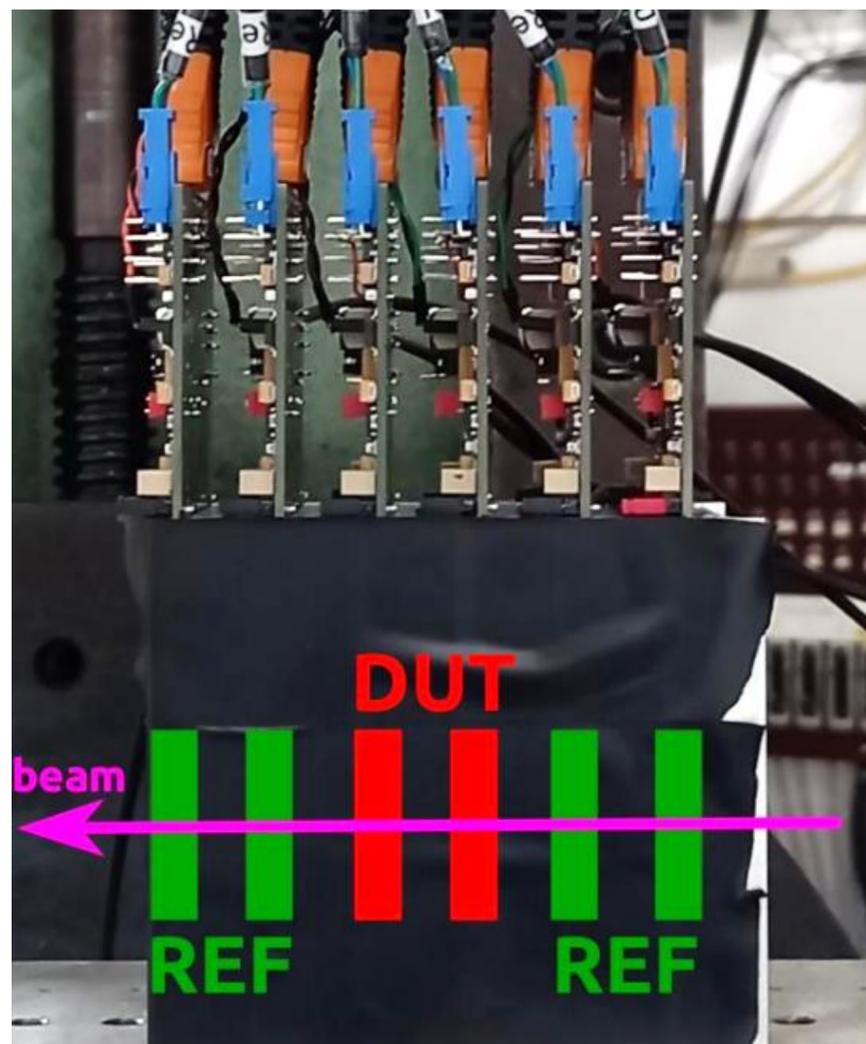
MIMOSIS-2.1 performance (in beam)



# ... after Irradiation

## Induced radiation damage

- Reactor neutrons, 60 keV X-rays
- EOL dose + safety margins
- Dark rate  $< 10^{-6}$ /pixel/frame



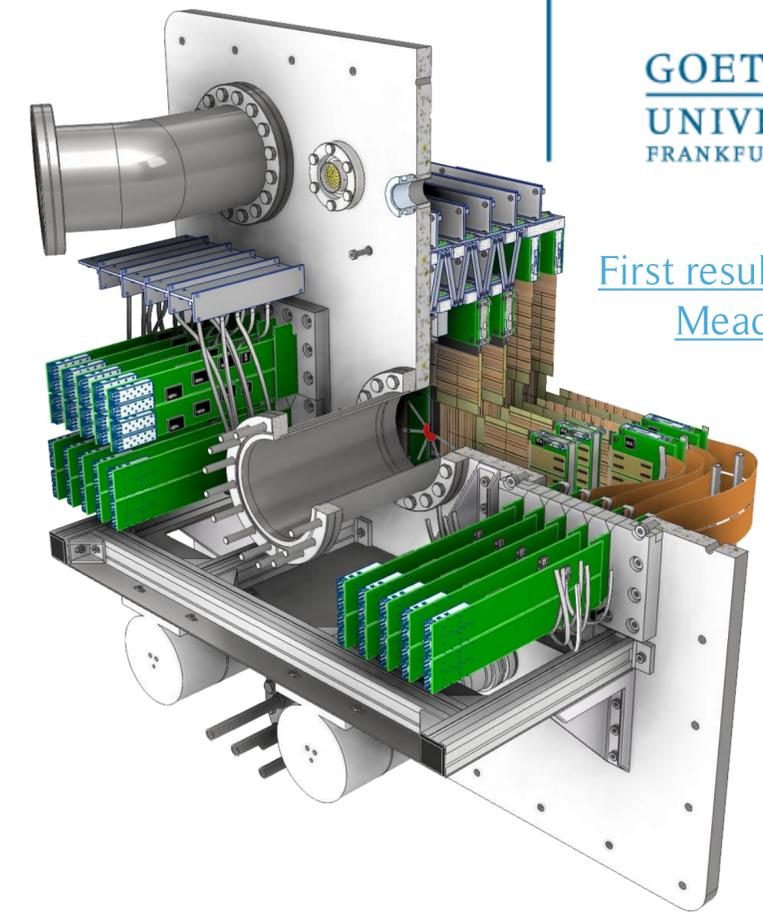
# Challenge: Fixed Target (SEE)

Single Event Effects from beam halo, target fragments, direct beam impact

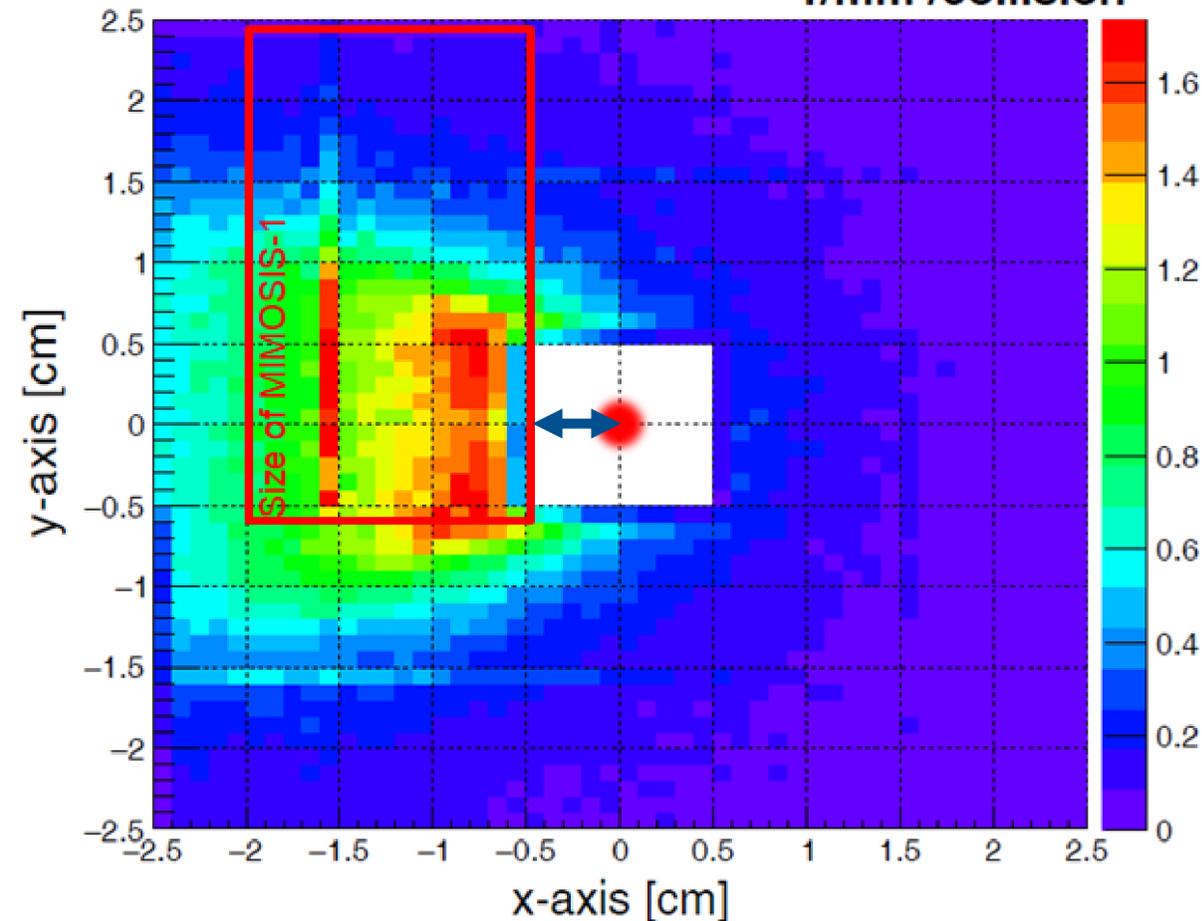
→ 5.4 mm next to the beam!

ALICE: ITS2 23 mm, ITS3: 19 mm, IRIS: 5 mm

→ Validate with ~4 AMeV Au @GSI



Hit gradient 1<sup>st</sup> MVD station  
1/mm<sup>2</sup>/collision



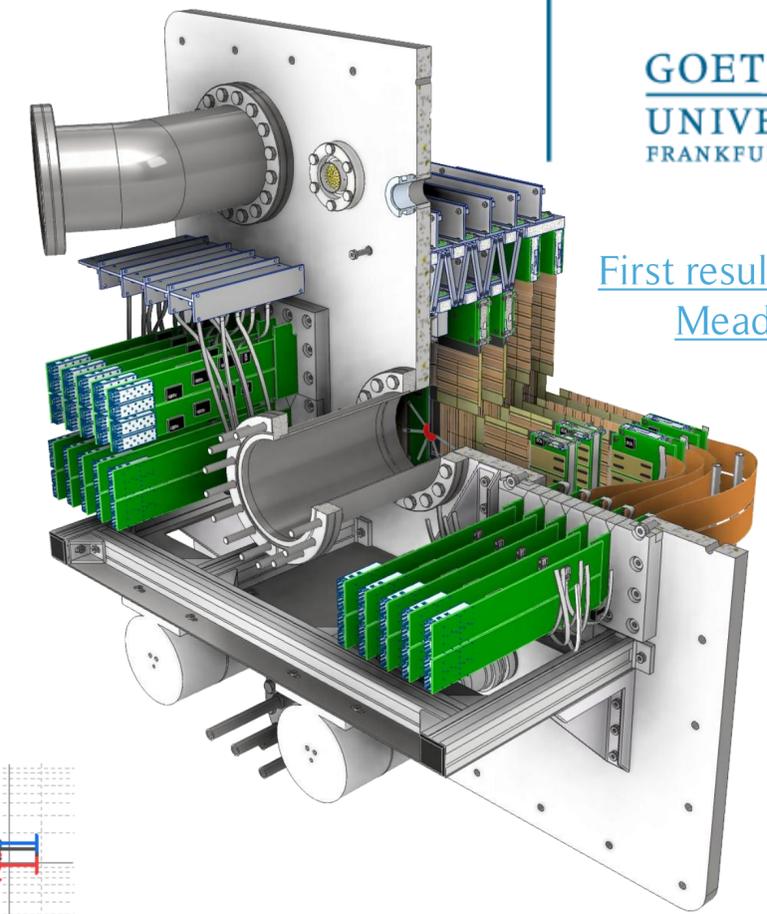
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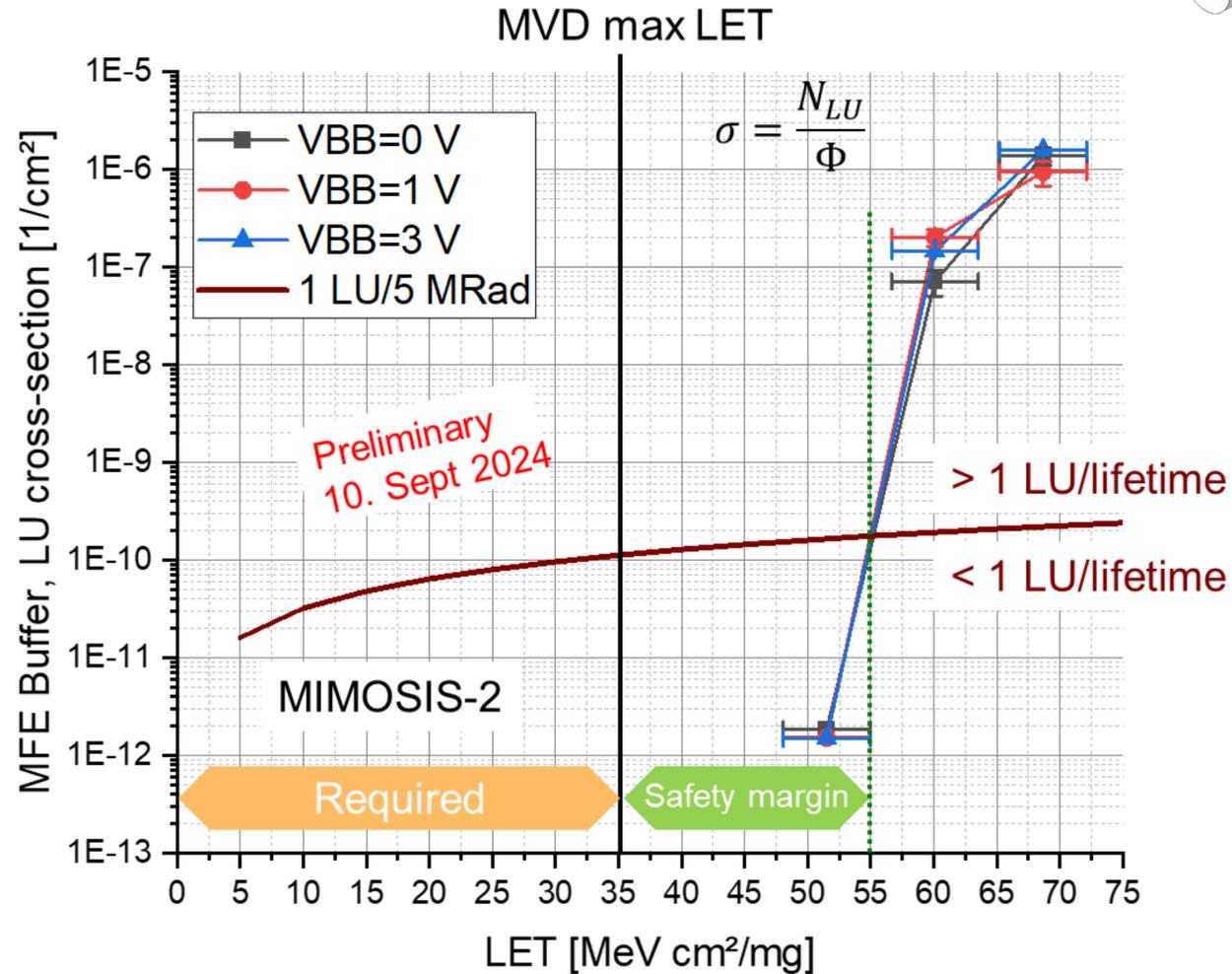
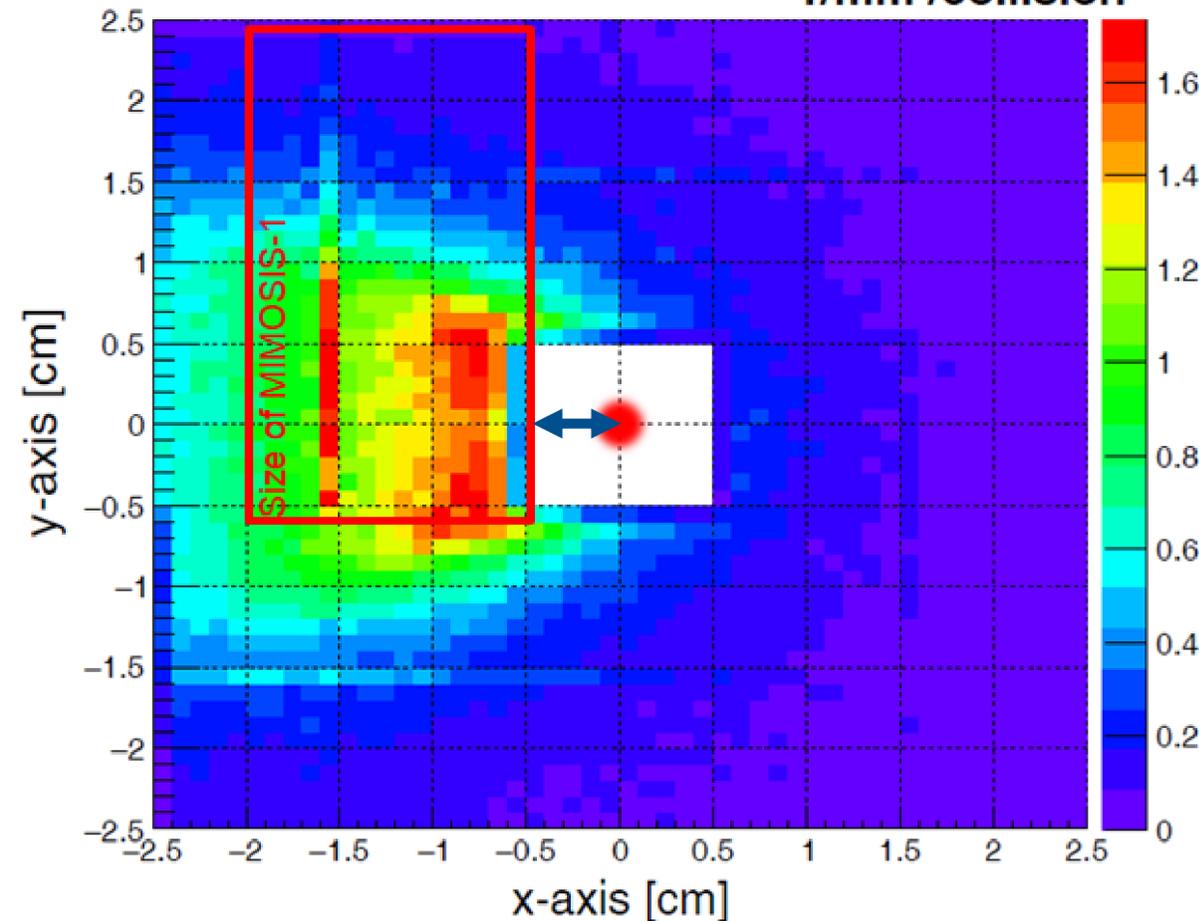
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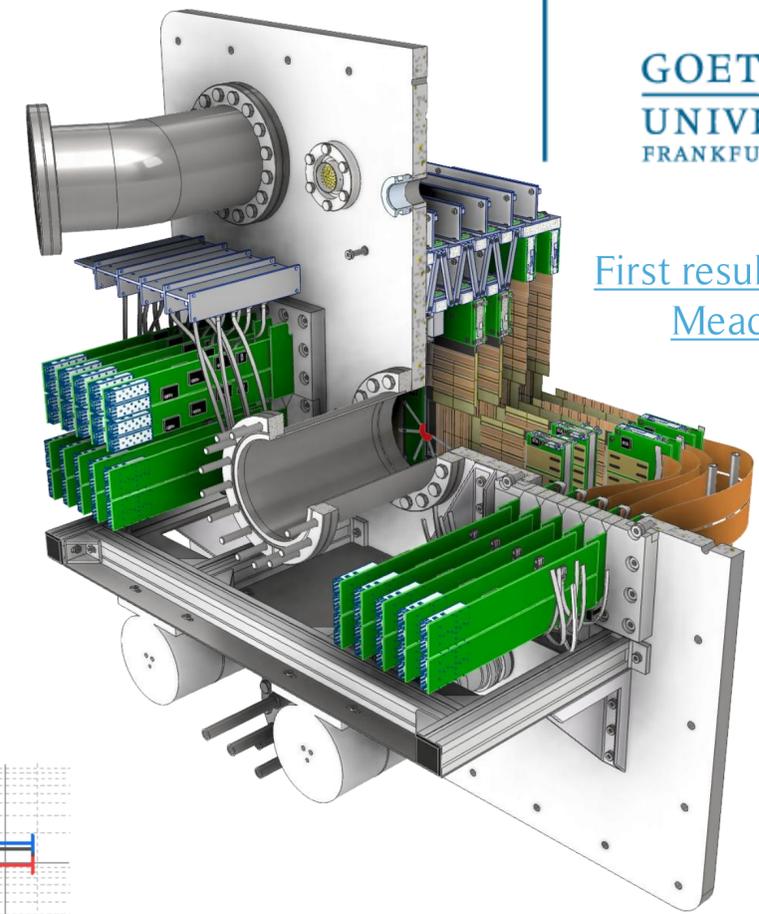
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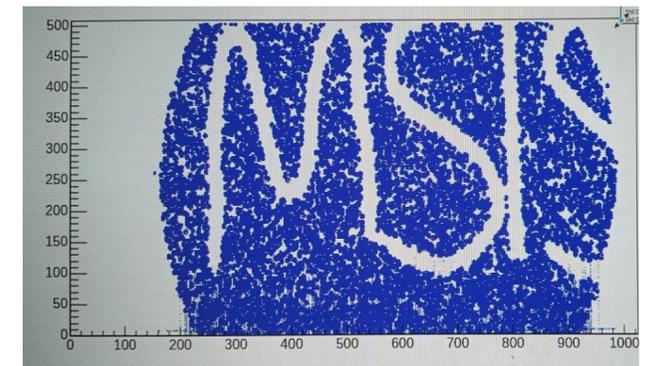
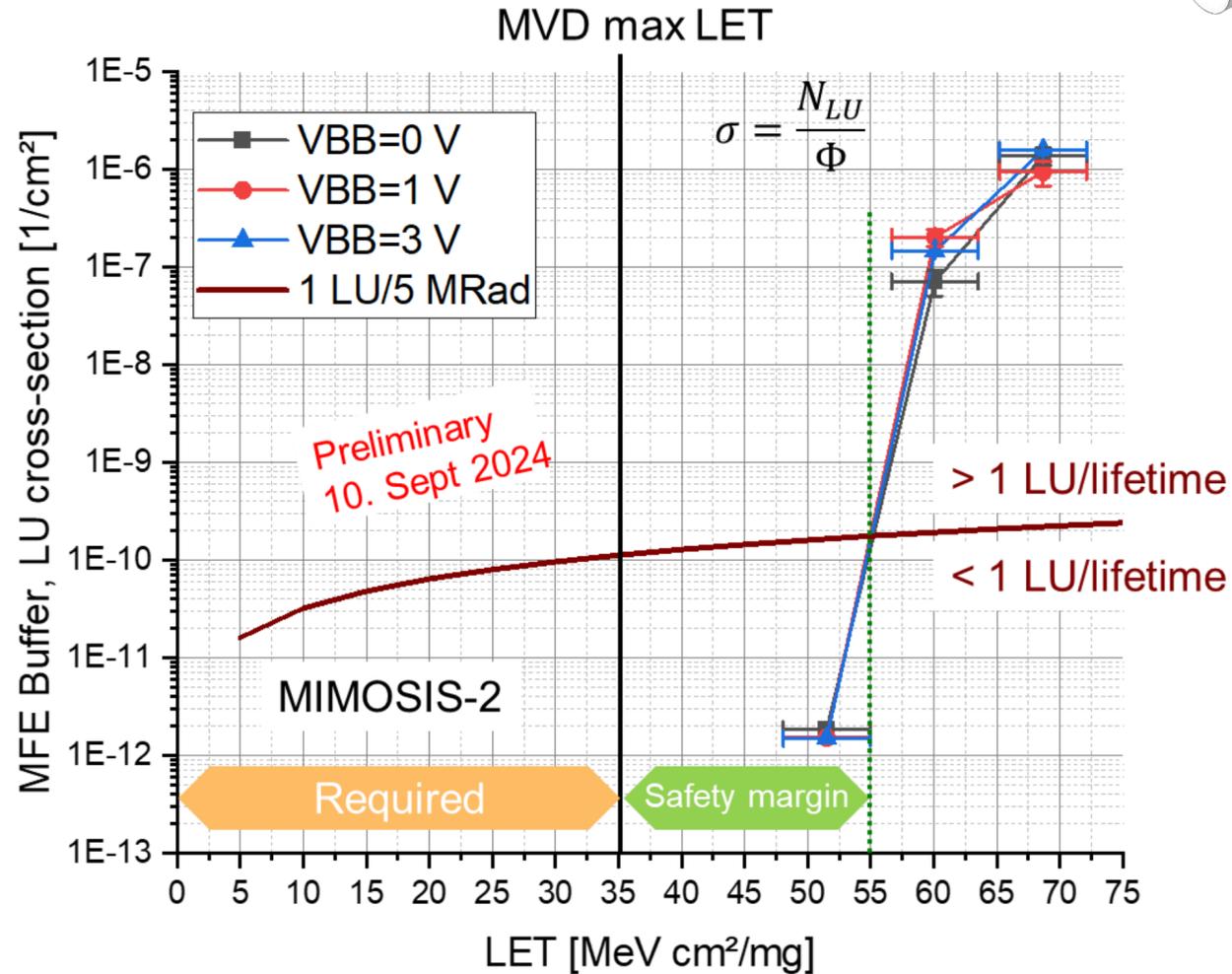
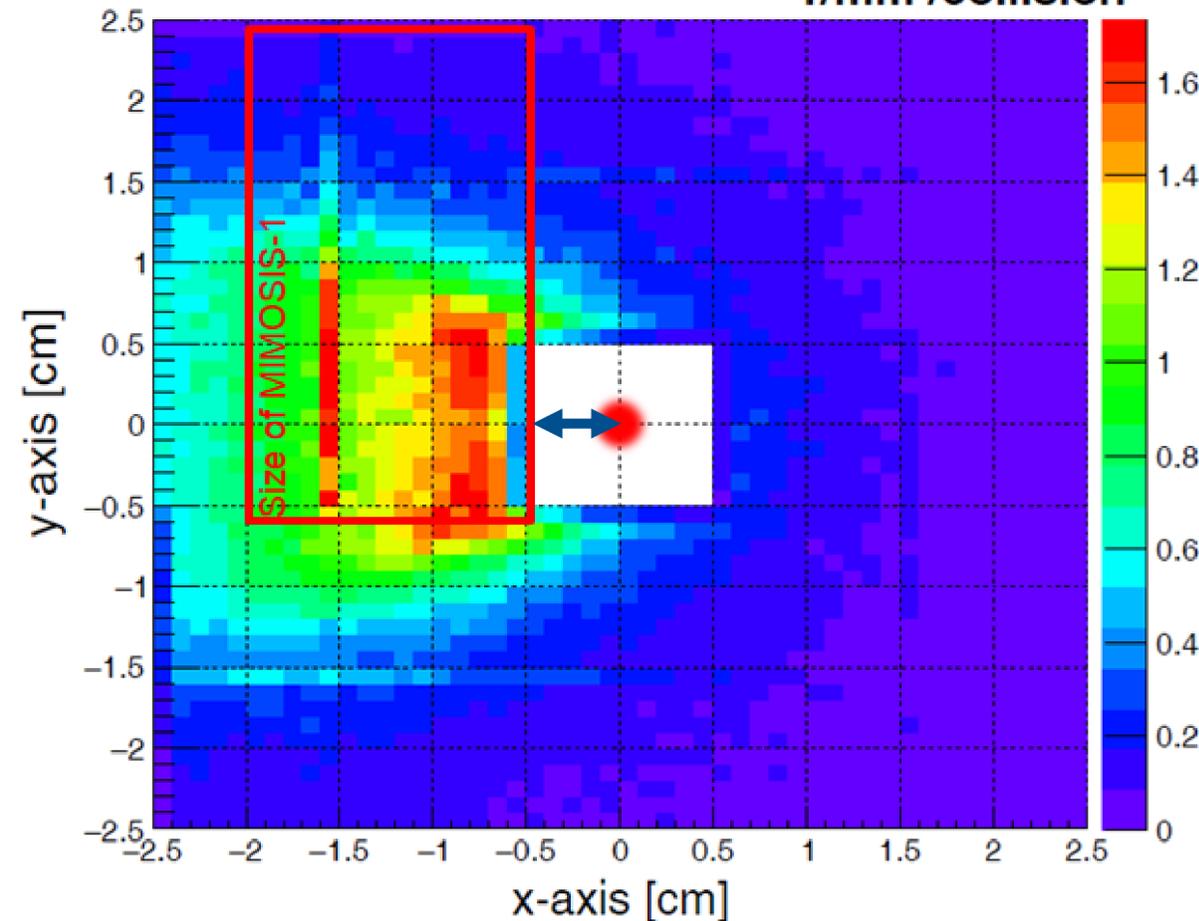
→ Validate with ~4 AMeV Au @GSI

First results: B. Arnoldi  
Meadows et al.



Hit gradient 1<sup>st</sup> MVD station

1/mm<sup>2</sup>/collision



# Challenge: Fixed Target (Deltas)

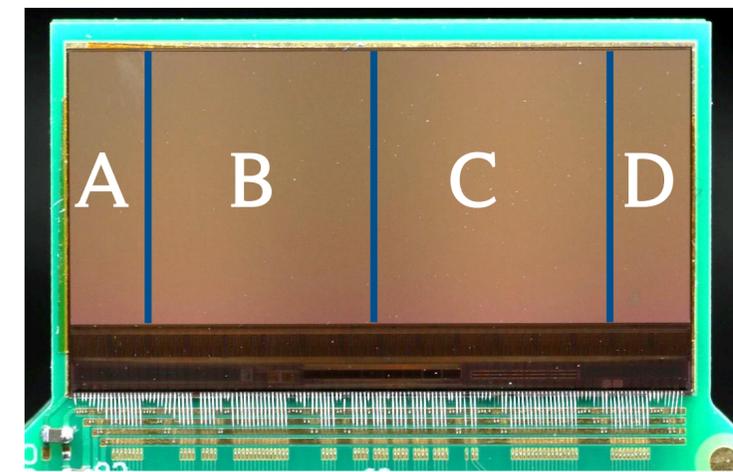
$\delta$ -e<sup>-</sup> (+ dipole field: irradiation gradient)

→ Load uncorrelated to physics events (tracking ambiguity)

**Threshold shift from TID (charge build-up in gate oxide)**

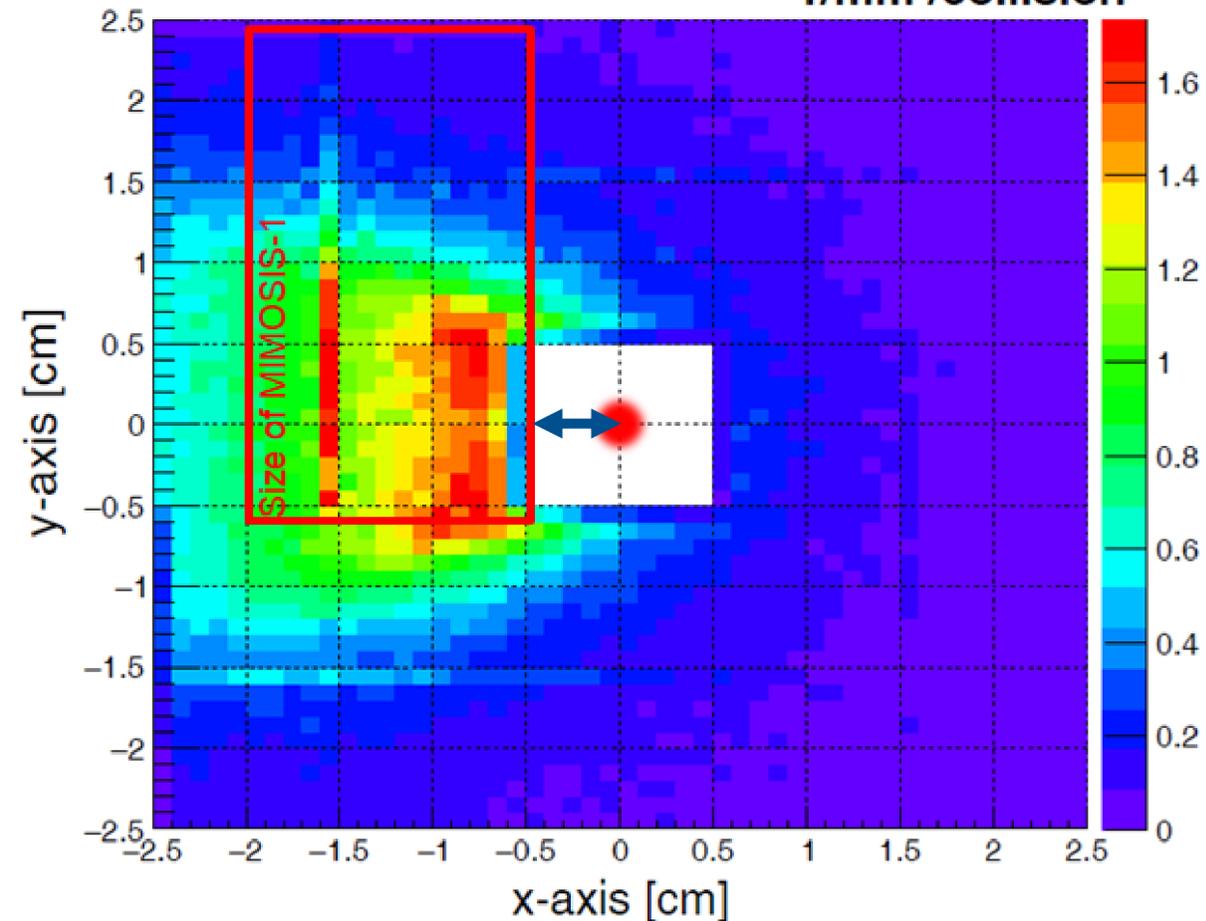
→ Saturates (~1 Mrad if biased, 3 Mrad if unbiased)

→ Pre-irradiation to homogenize pixel response (<sup>60</sup>Co  $\gamma$ )



Hit gradient 1<sup>st</sup> MVD station

1/mm<sup>2</sup>/collision



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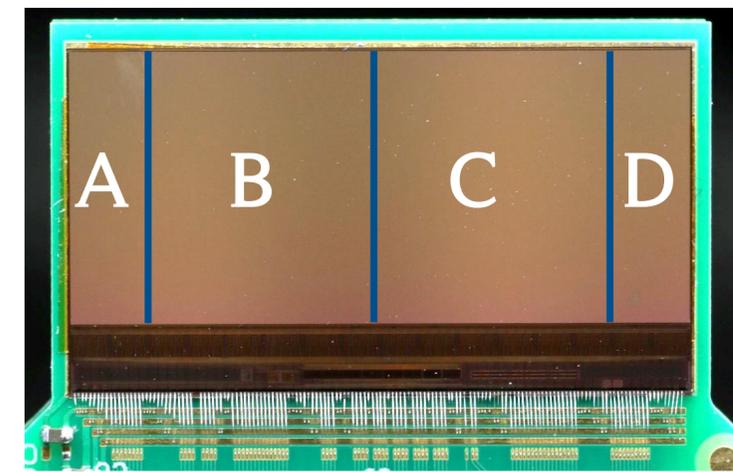
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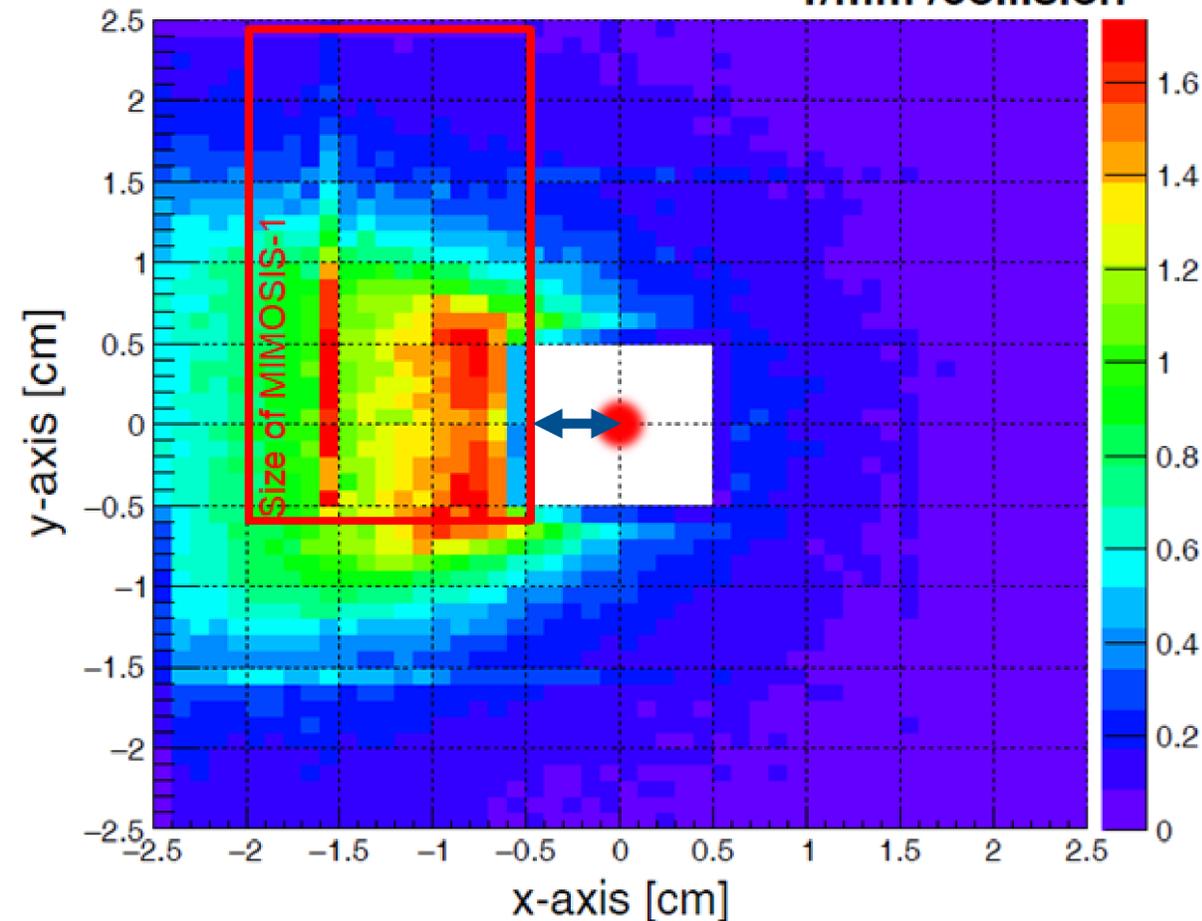
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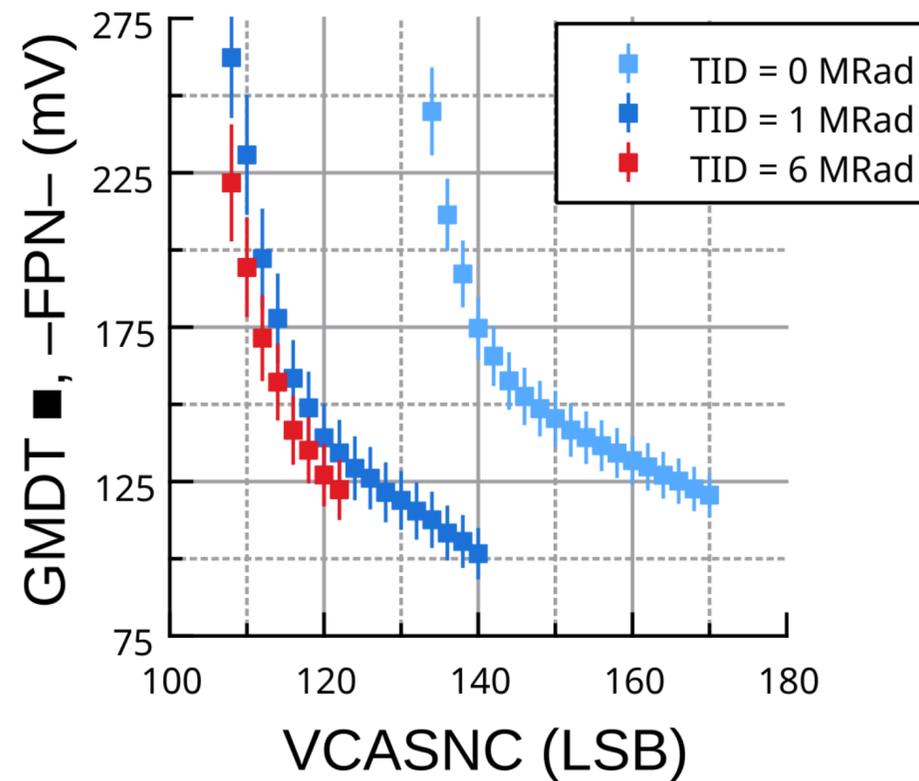
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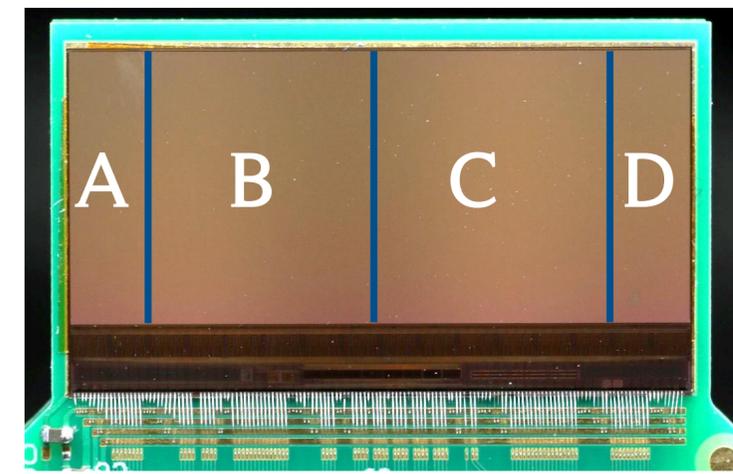
Threshold shift biased MIMOSIS-1

GMDT and FPN, AC cls. design

Various doses, ~ 30 °C



# Challenge: Fixed Target (Deltas)



$\delta$ -e<sup>-</sup> (+ dipole field: irradiation gradient)

→ Load uncorrelated to physics events (tracking ambiguity)

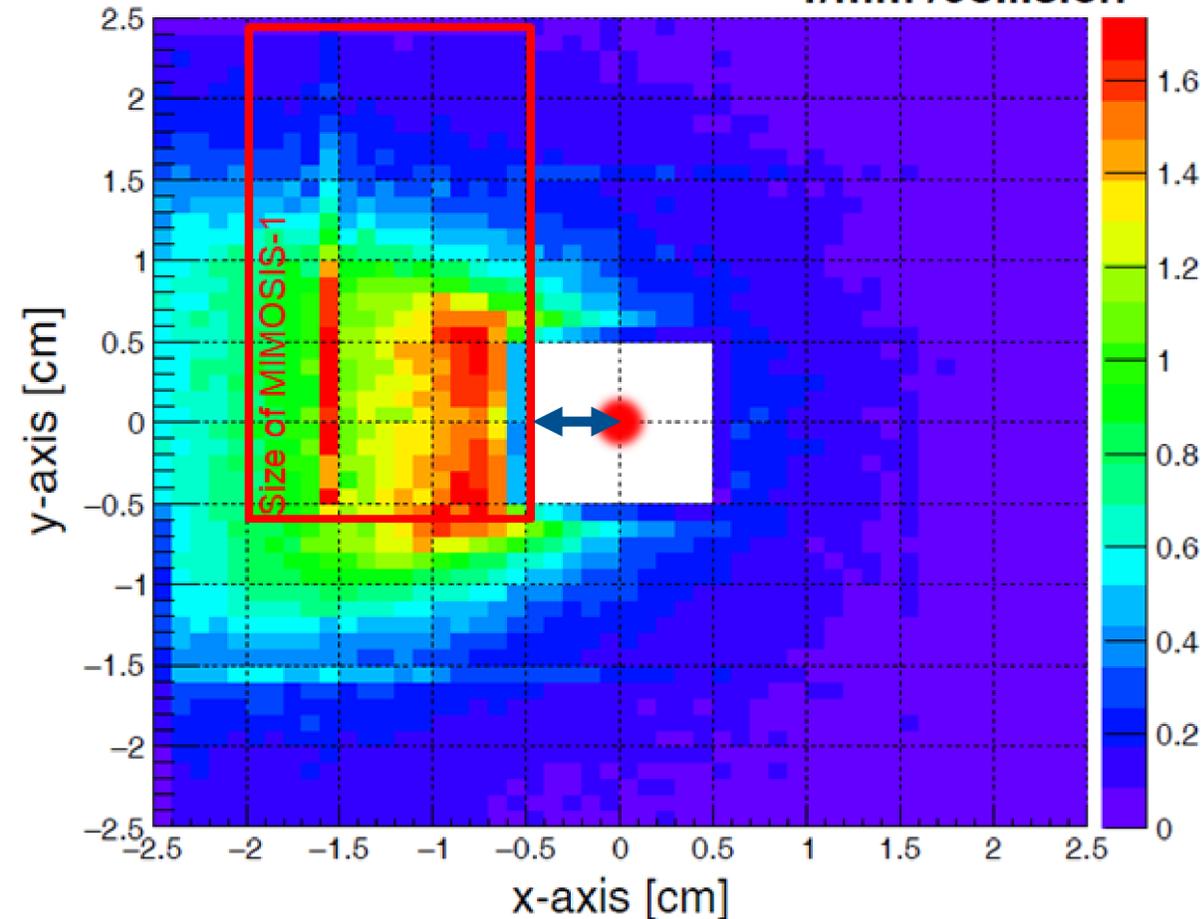
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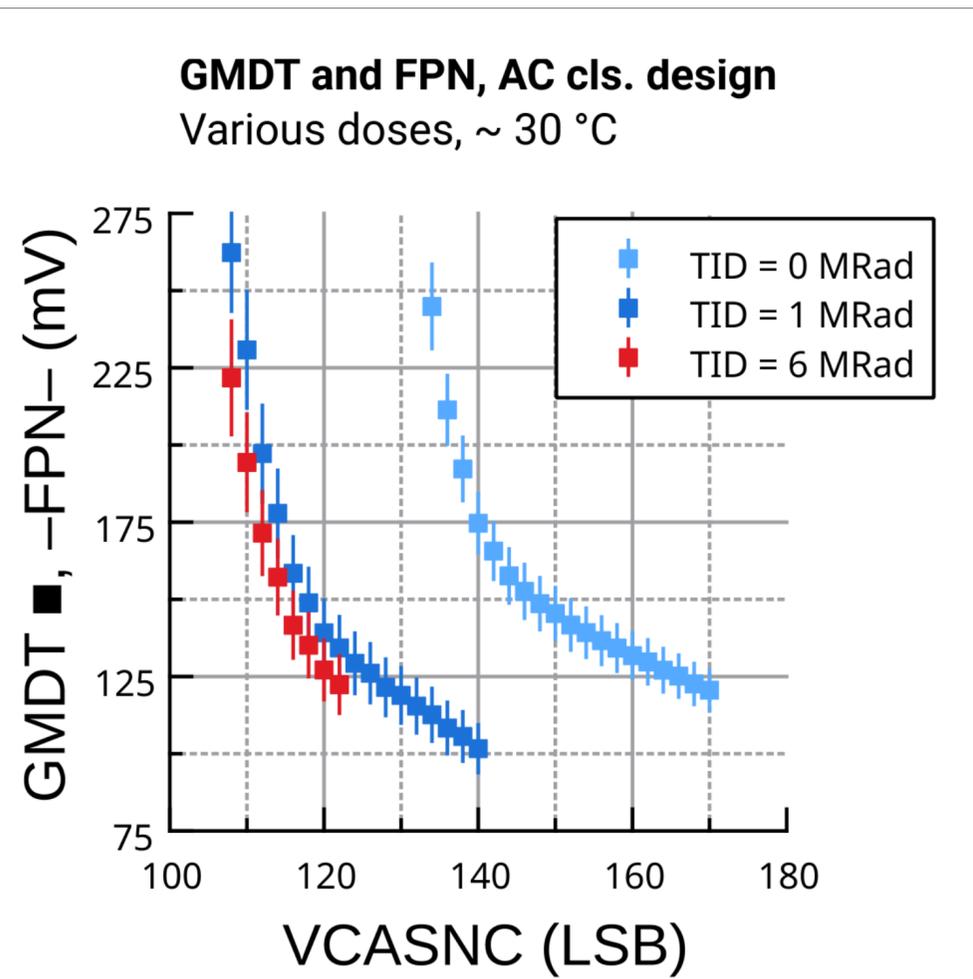
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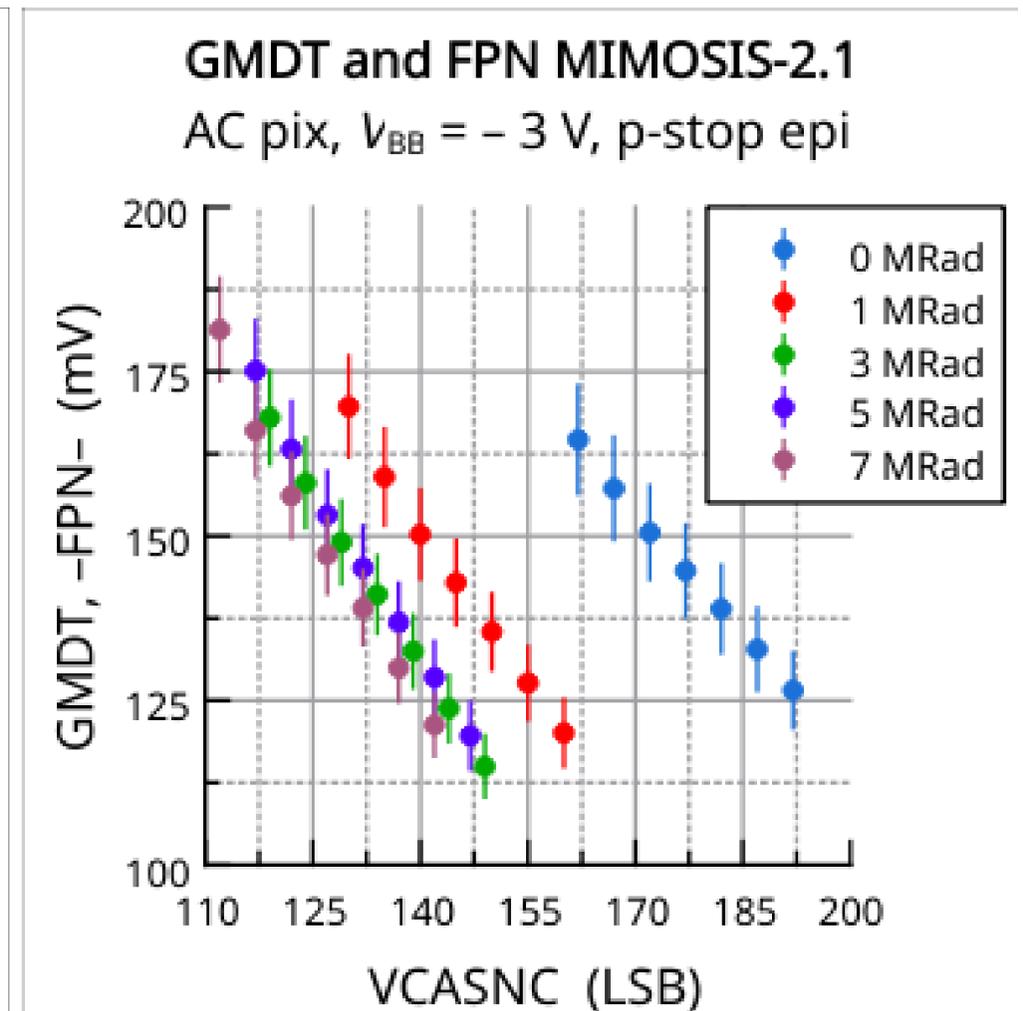
1/mm<sup>2</sup>/collision



Threshold shift biased MIMOSIS-1



Threshold shift unbiased MIMOSIS-2.1

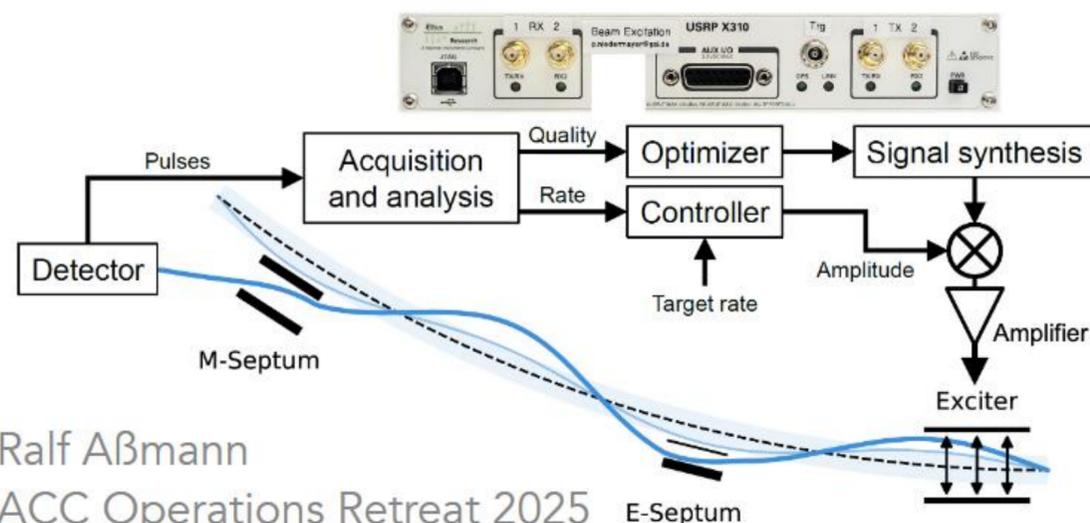


# Challenge: Fixed Target (Intensity Fluctuations)

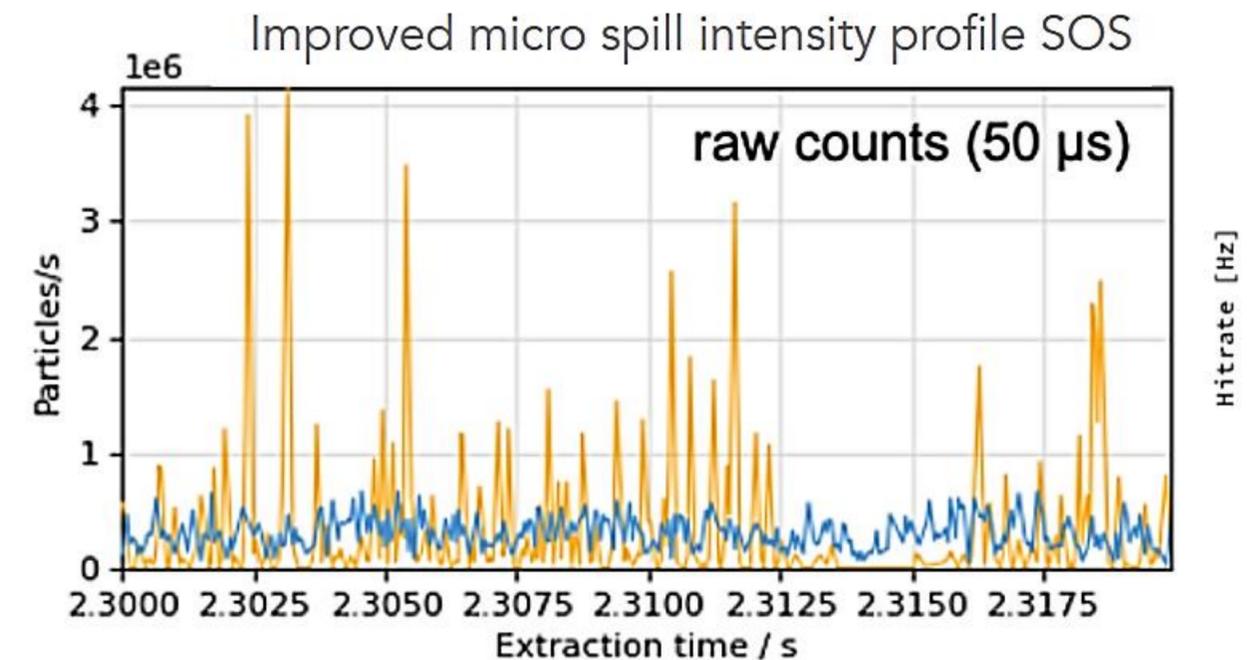
## Non-ideal spills in realistic accelerators (SIS100)

- Global spill: 0.5 s synchrotron refill, 10 s slow extraction
- $\mu$ -spill structure (known from SIS18)
- Substantially improved with Spill Optimization System (SOS)

Spill optimisation system (SOS)



Ralf Aßmann  
ACC Operations Retreat 2025



# Challenge: Fixed Target (Intensity Fluctuations)

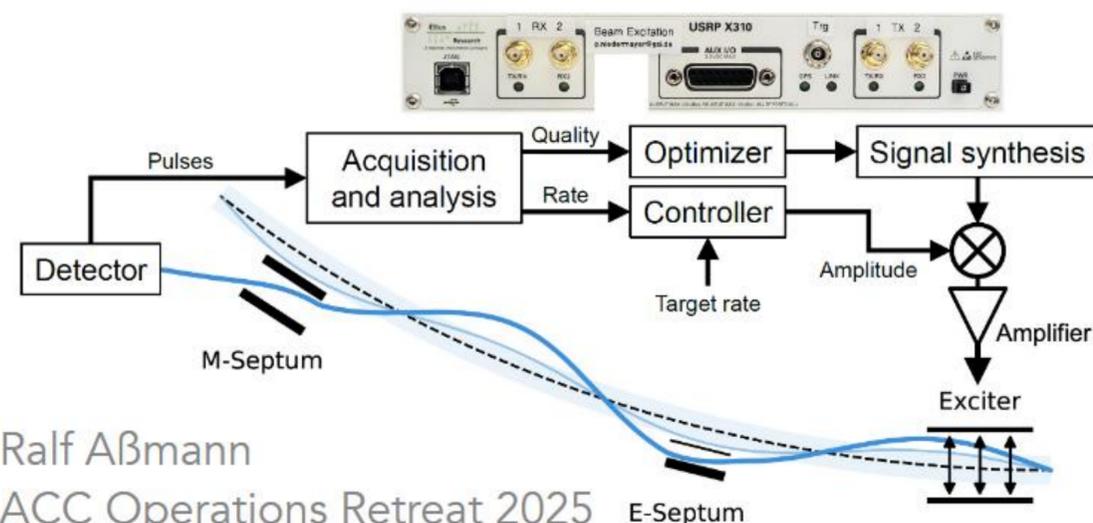
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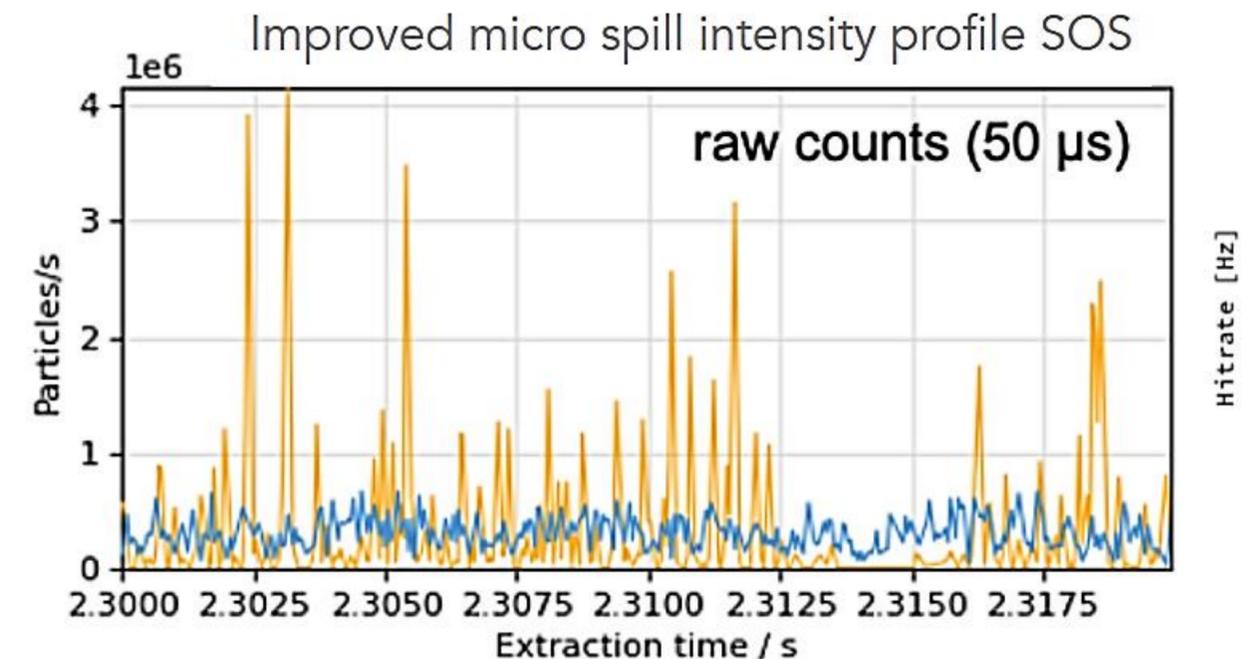
## Elastic buffer in MIMOSIS

- Peak/average  $>3$  for 50  $\mu$ s
- Write speed 10.24 Gb/s  $>$  Read speed 2.56 Gb/s (for 8 links)

Spill optimisation system (SOS)



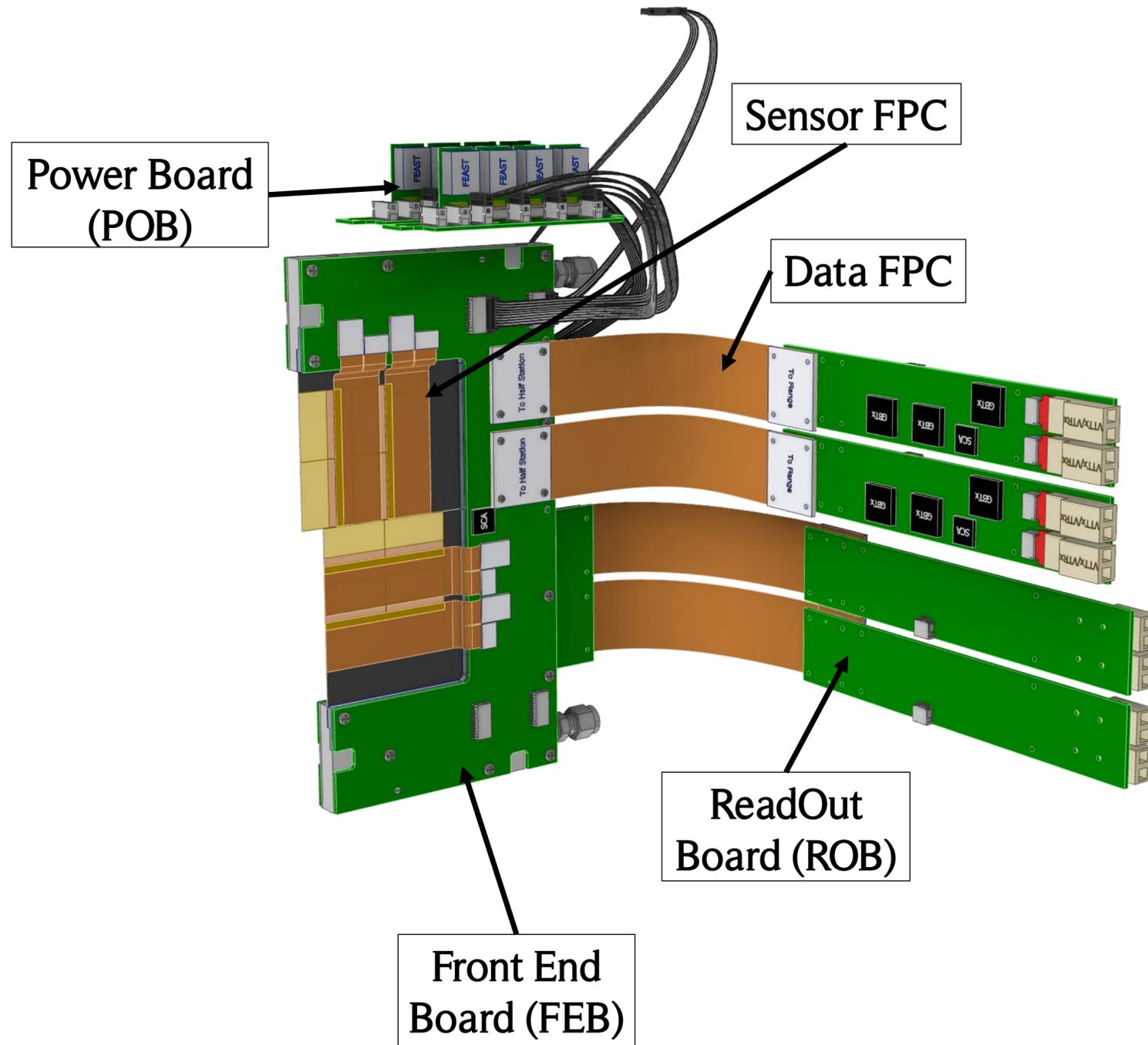
Ralf Aßmann  
ACC Operations Retreat 2025



Chapter 2

# Integration

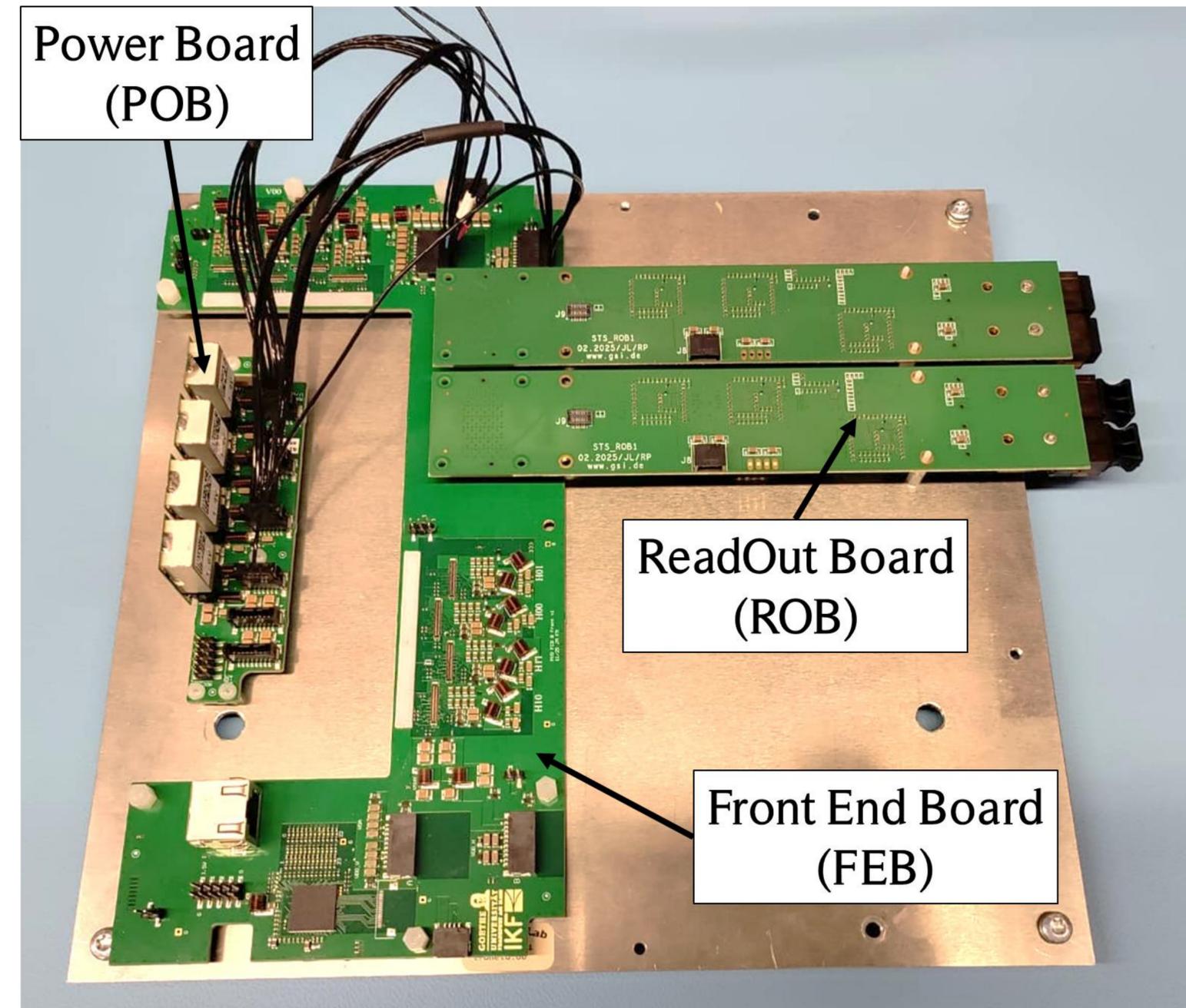
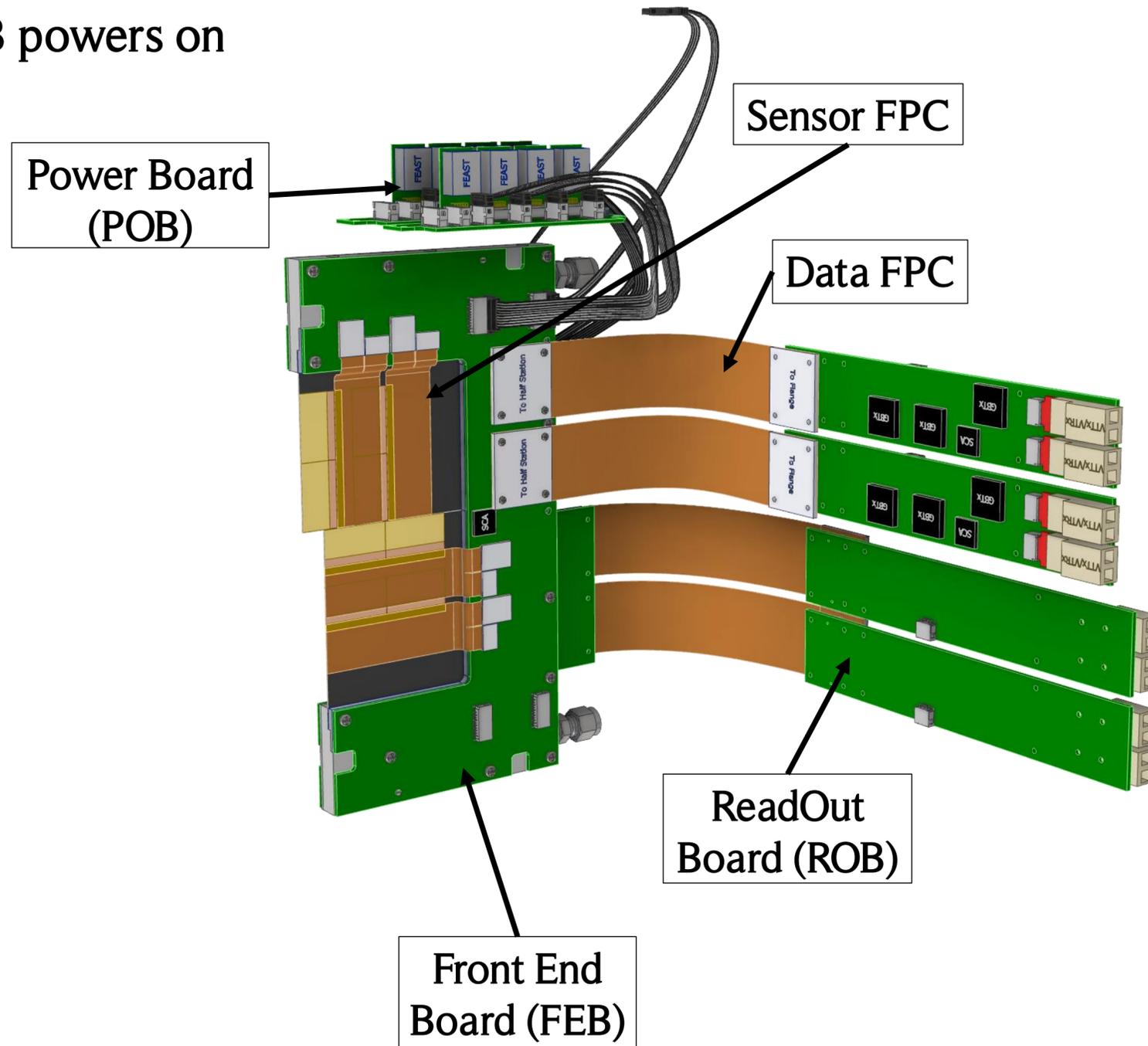
# Front-End Electronics



# Front-End Electronics

ROB and POB fully functional

FEB powers on

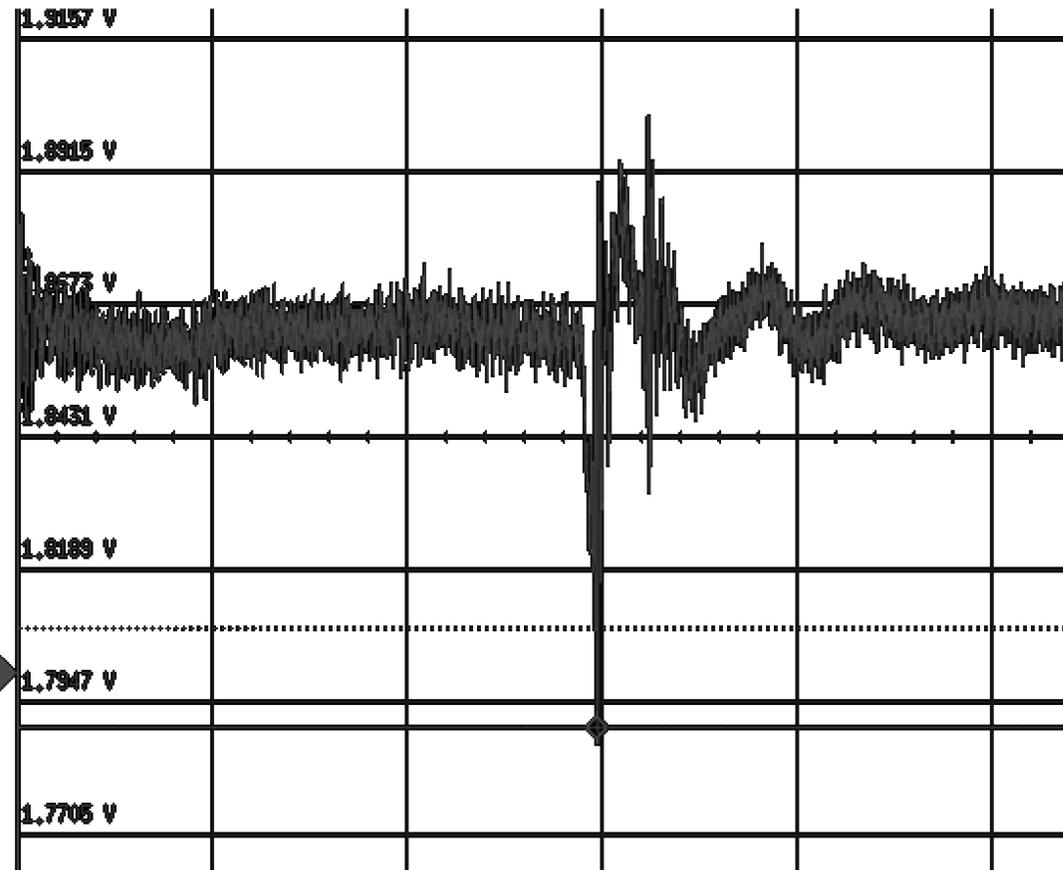


# Challenge: Powering

Optimize power distribution network (on-chip and in-detector)

→ Static and dynamic voltage drops on all time scales

≈ 100 mV voltage fluctuations on  
VDD every frame (5 μs)

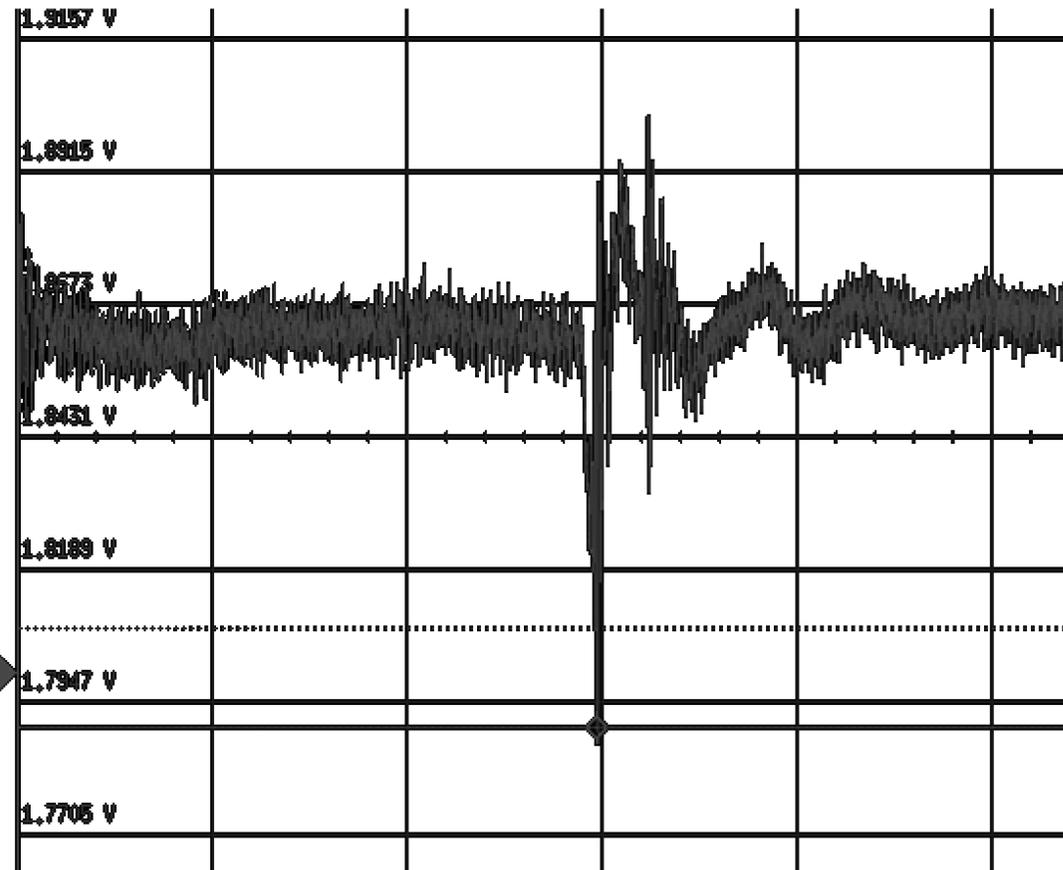


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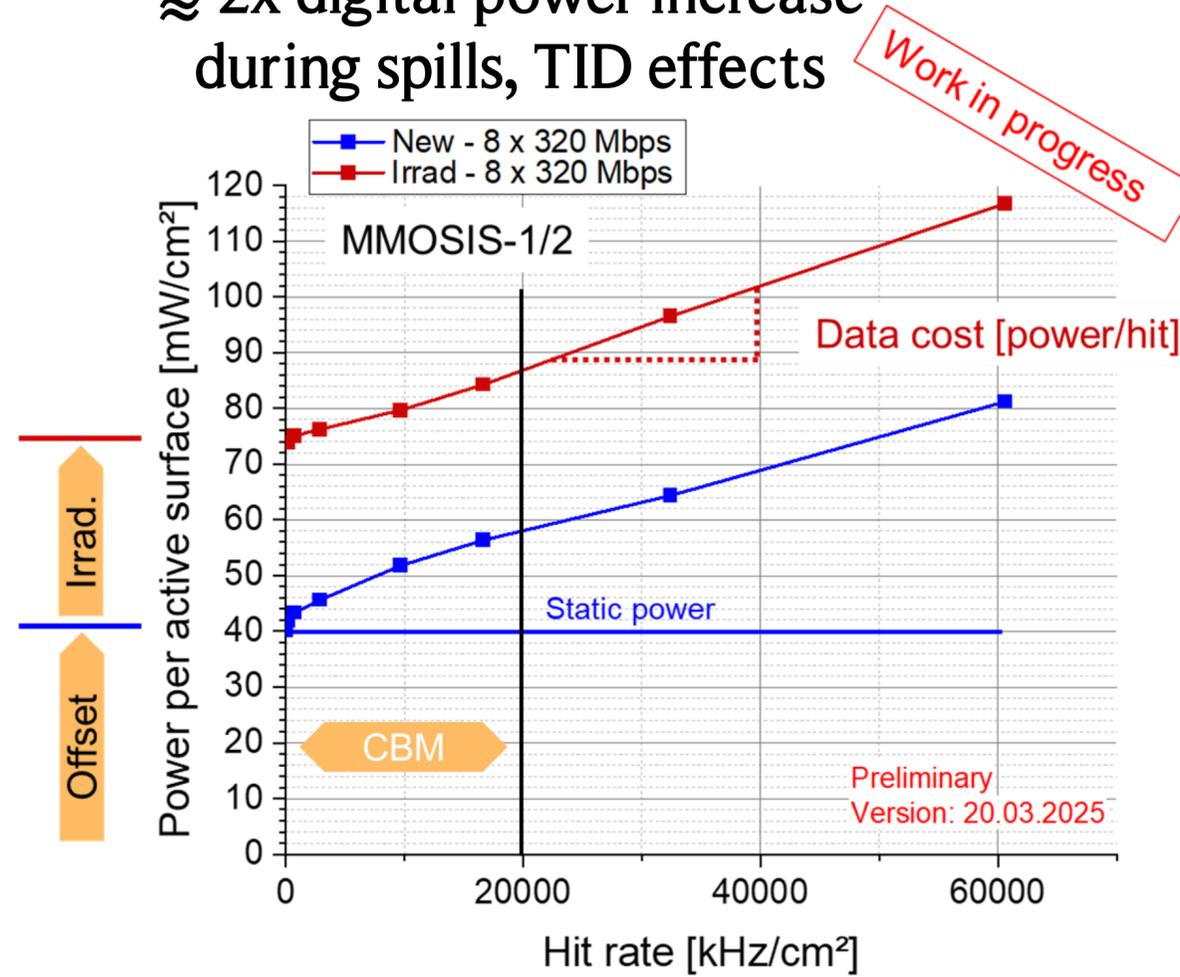
Optimize power distribution network (on-chip and in-detector)

→ Static and dynamic voltage drops on all time scales

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≈ 2x digital power increase during spills, TID effects

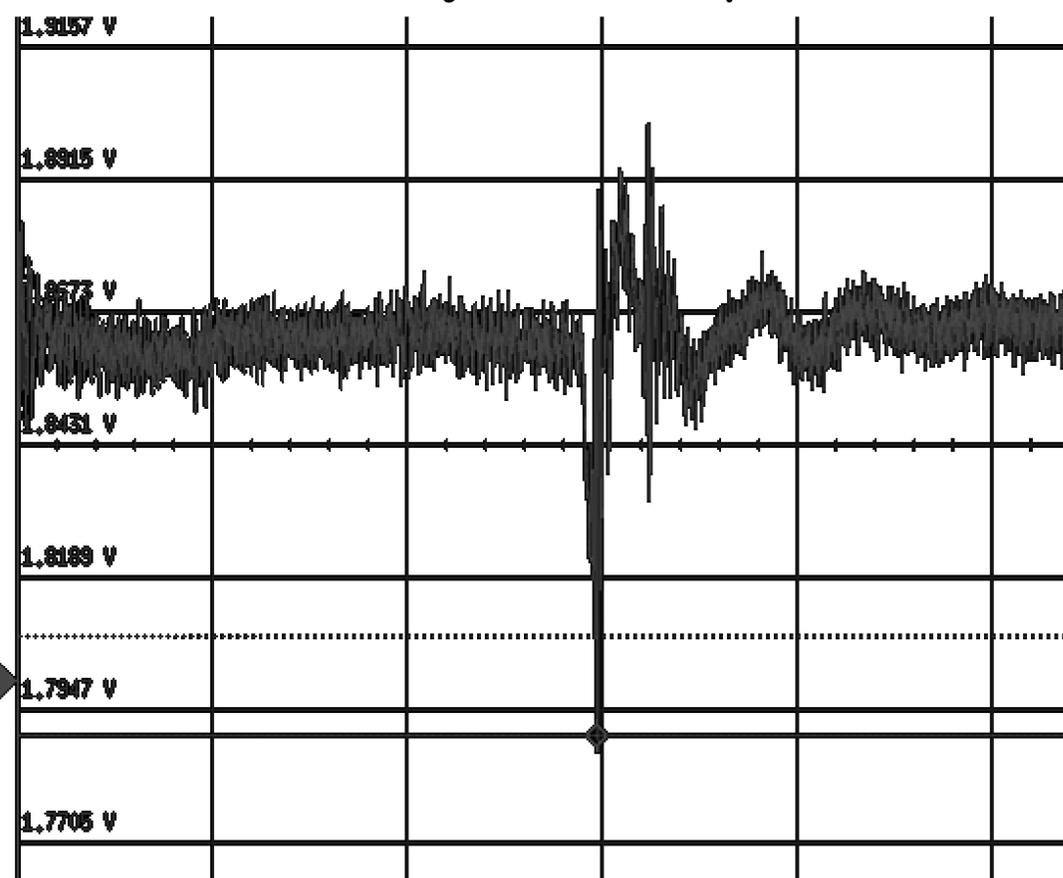


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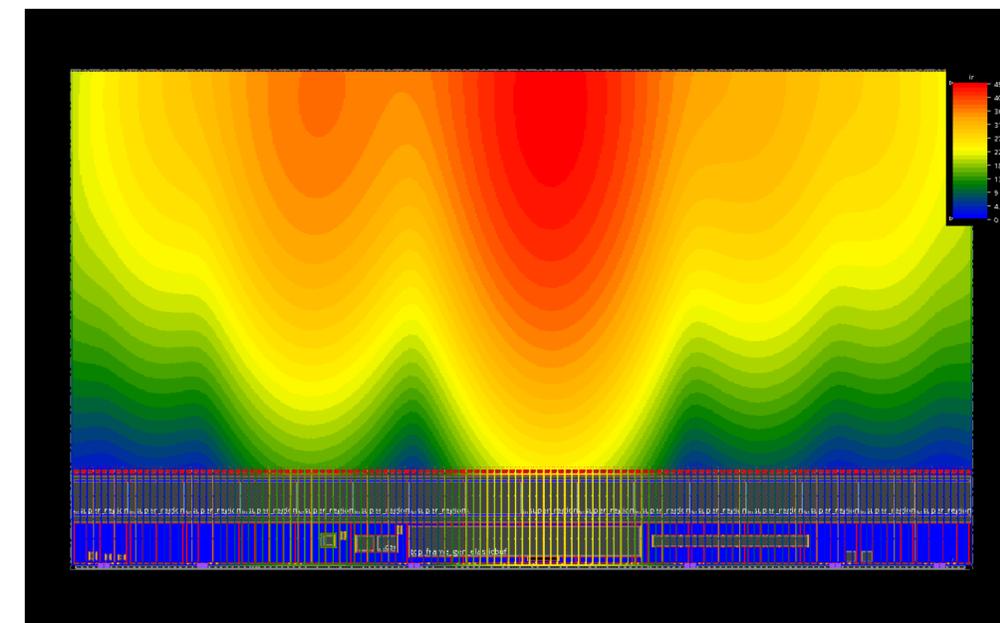
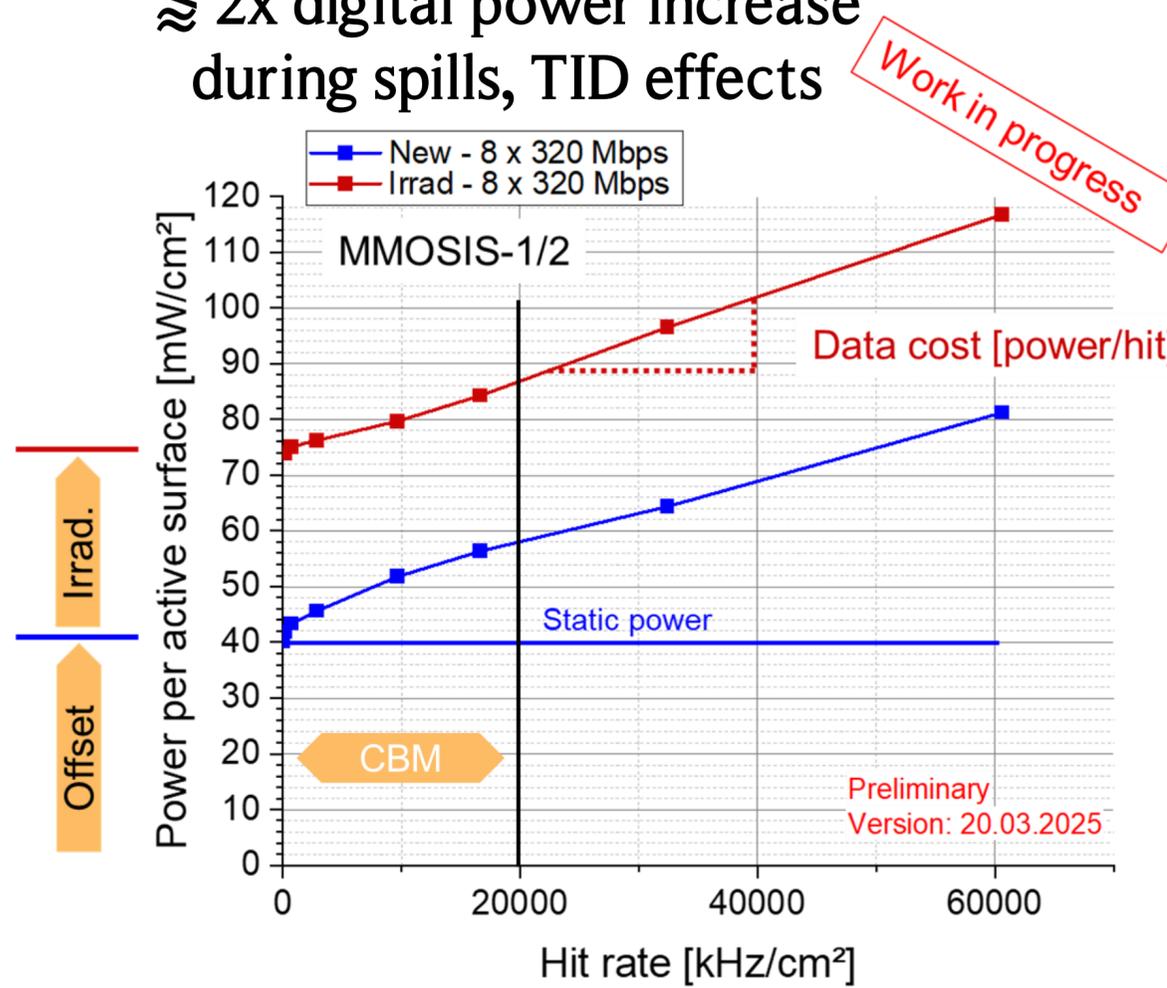
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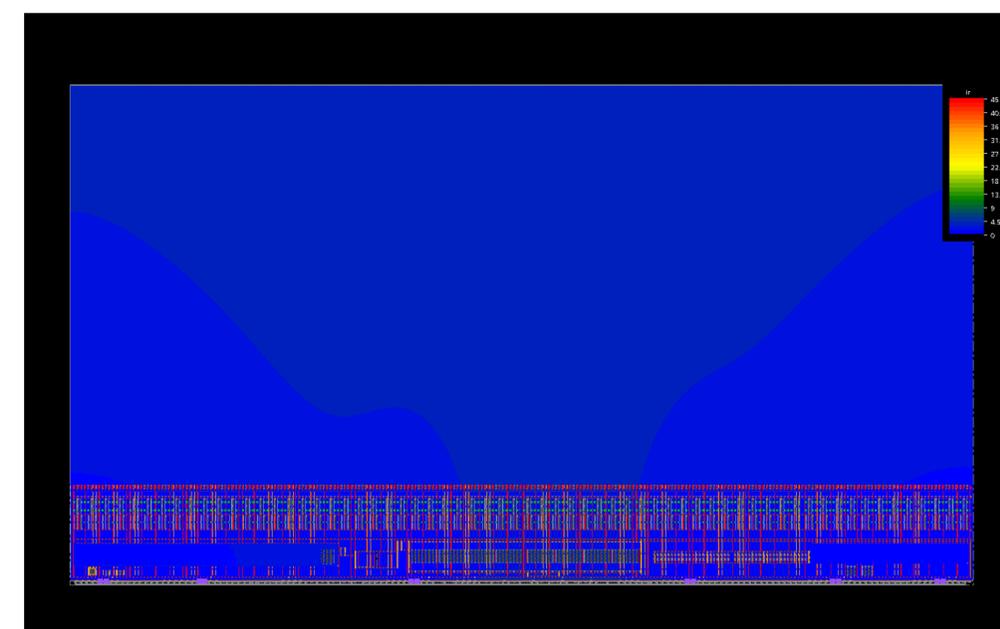
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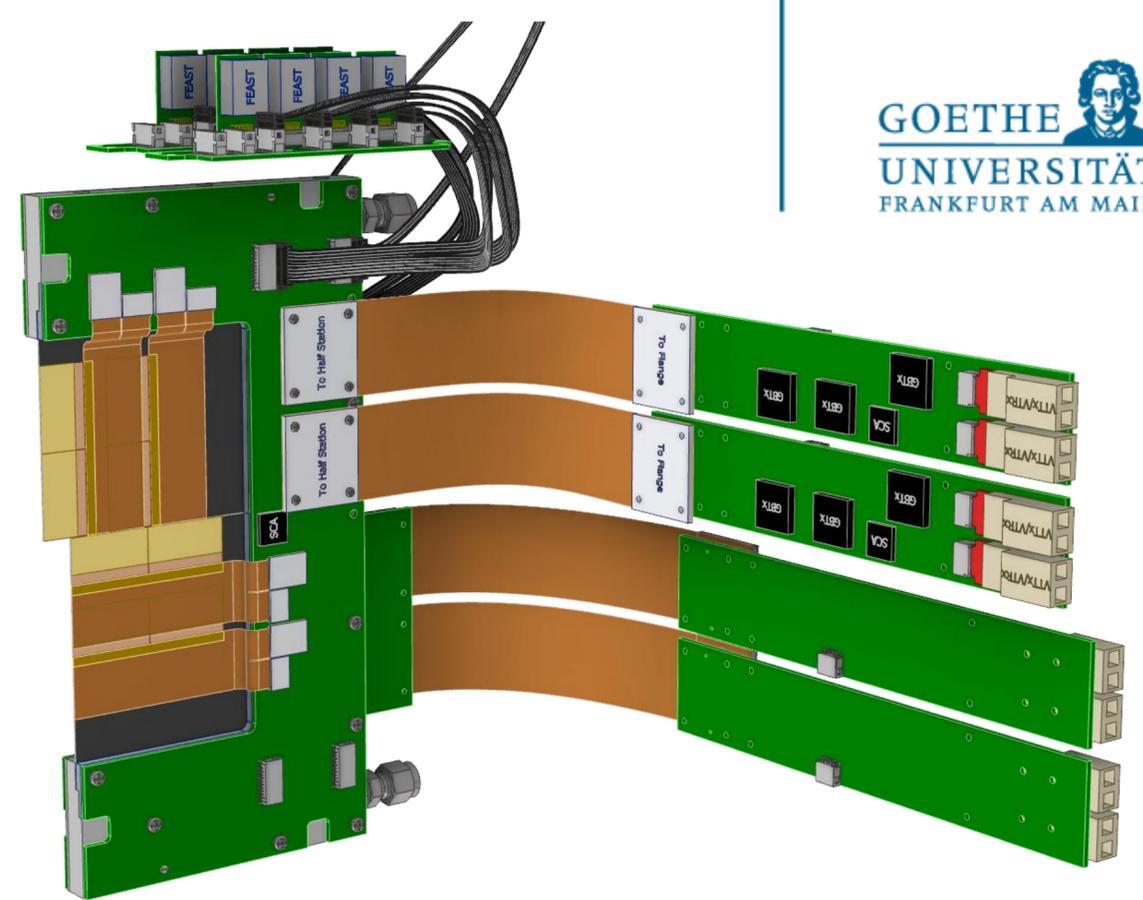
~4x improvements in analog power grid from M1 to M2



# Challenge: Powering

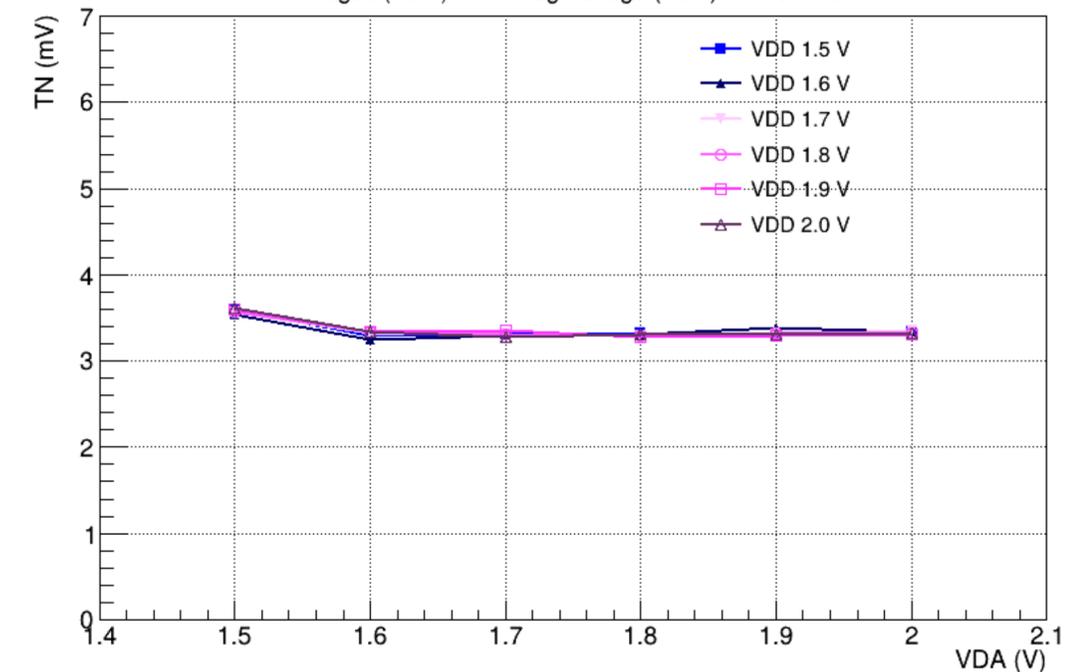
Note: This is an “easy” system

- Parallel powering
- Cross-powering and latch-ups not observed
- Sufficient stable operation voltage range



## Stable operation voltage range

Thermal Noise (TN) for different Digital Voltages (VDD) vs Analog Voltage (VDA) for AC Pixels



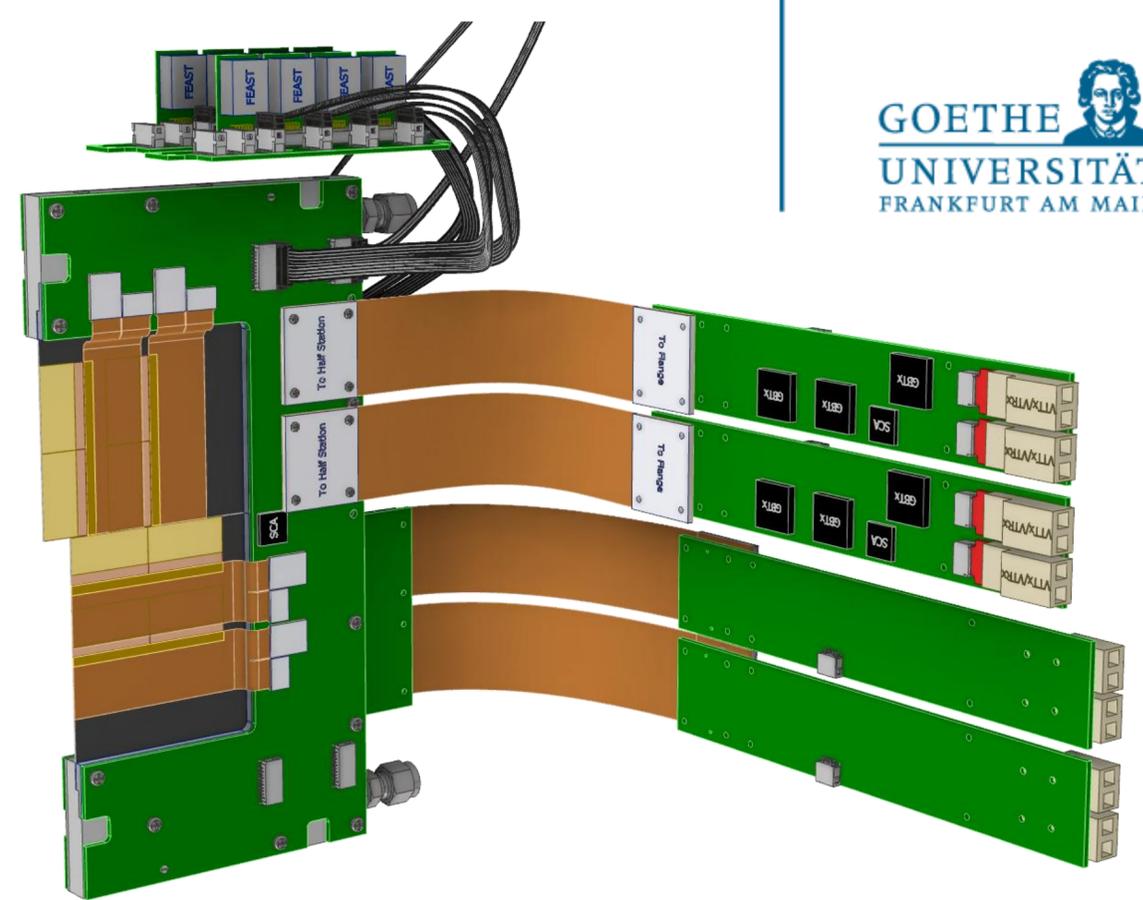
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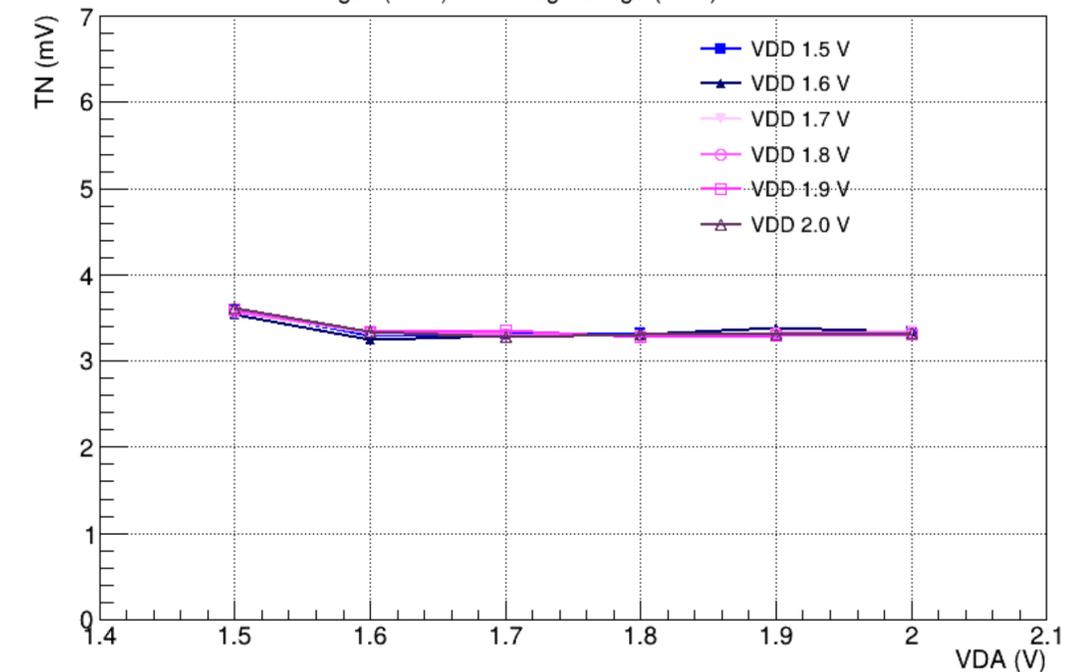
## Detector PDN

- LV distribution in vacuum (FEAST DC/DC)
- Low R cabling
- >50% of FPC area for powering
- Separated power domains



## Stable operation voltage range

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# Challenge: Powering

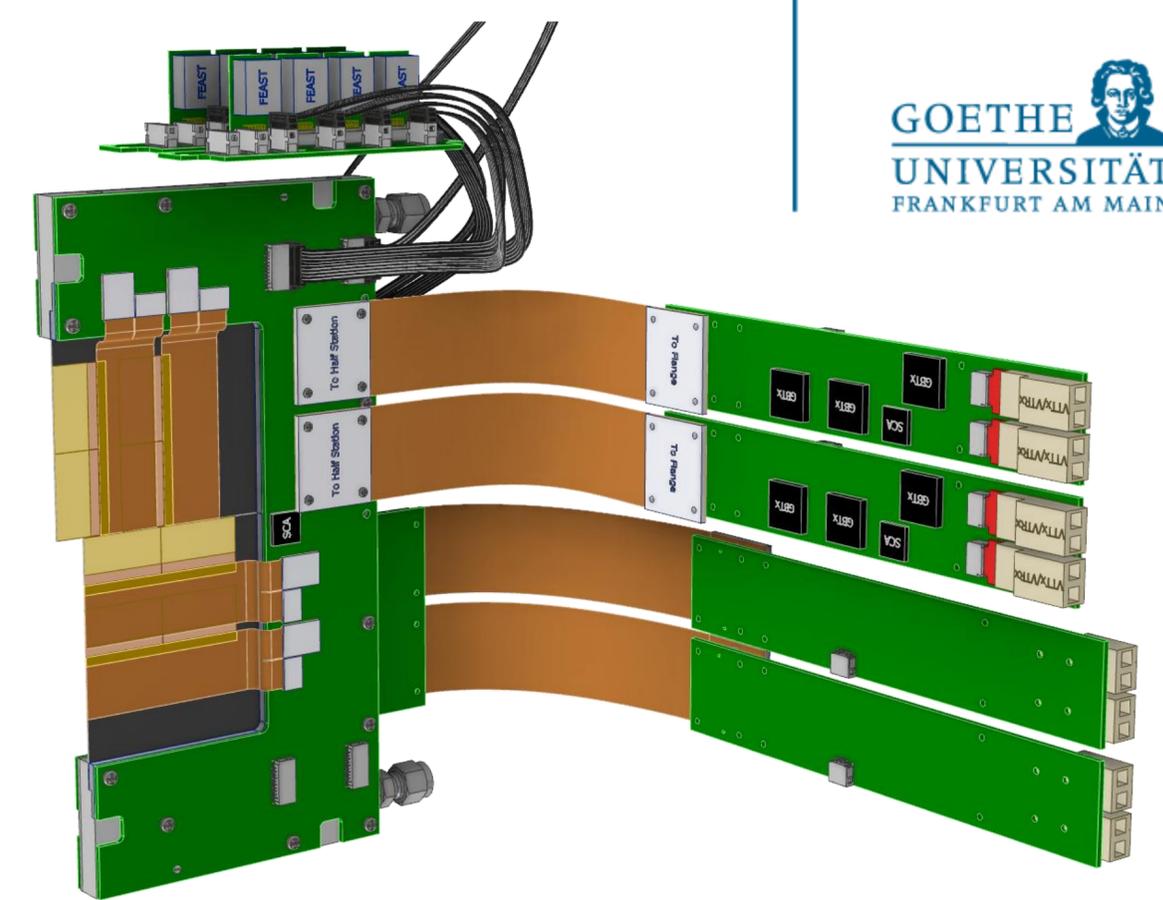
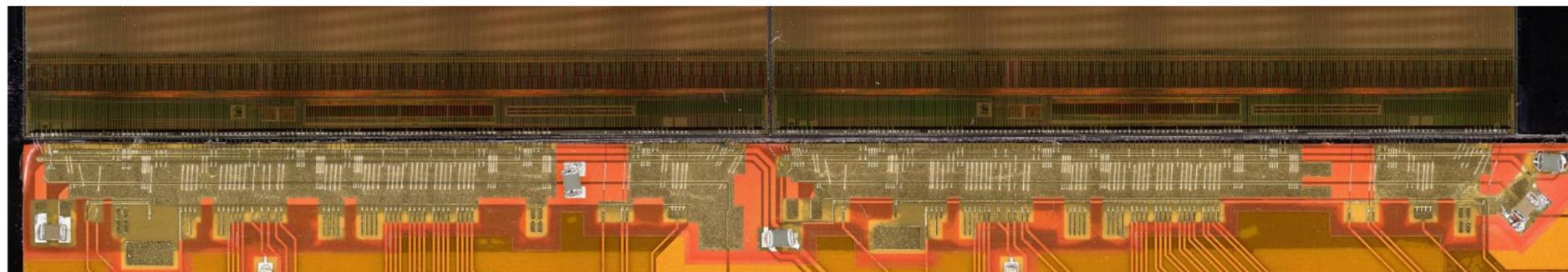
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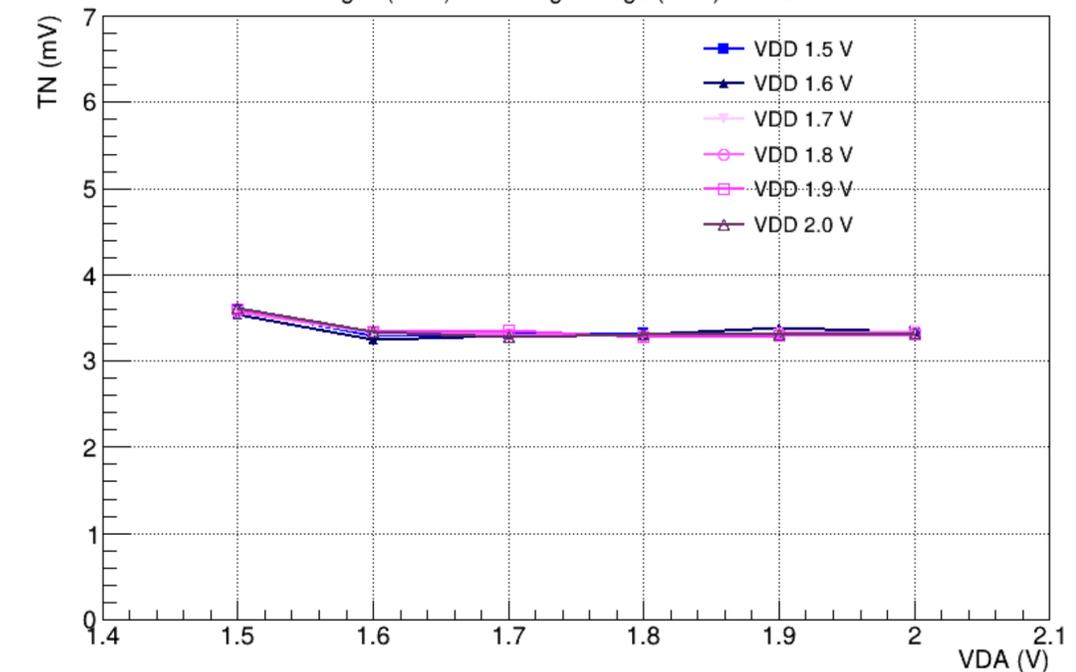
- LV distribution in vacuum (FEAST DC/DC)
- Low R cabling
- >50% of FPC area for powering
- Separated power domains

- But: Capacitors in acceptance
- But: Grouping of components
- But: External biasing (20 m)
- But: ~40 mV GND shift (biasing, SLVS)



## Stable operation voltage range

Thermal Noise (TN) for different Digital Voltages (VDD) vs Analog Voltage (VDA) for AC Pixels

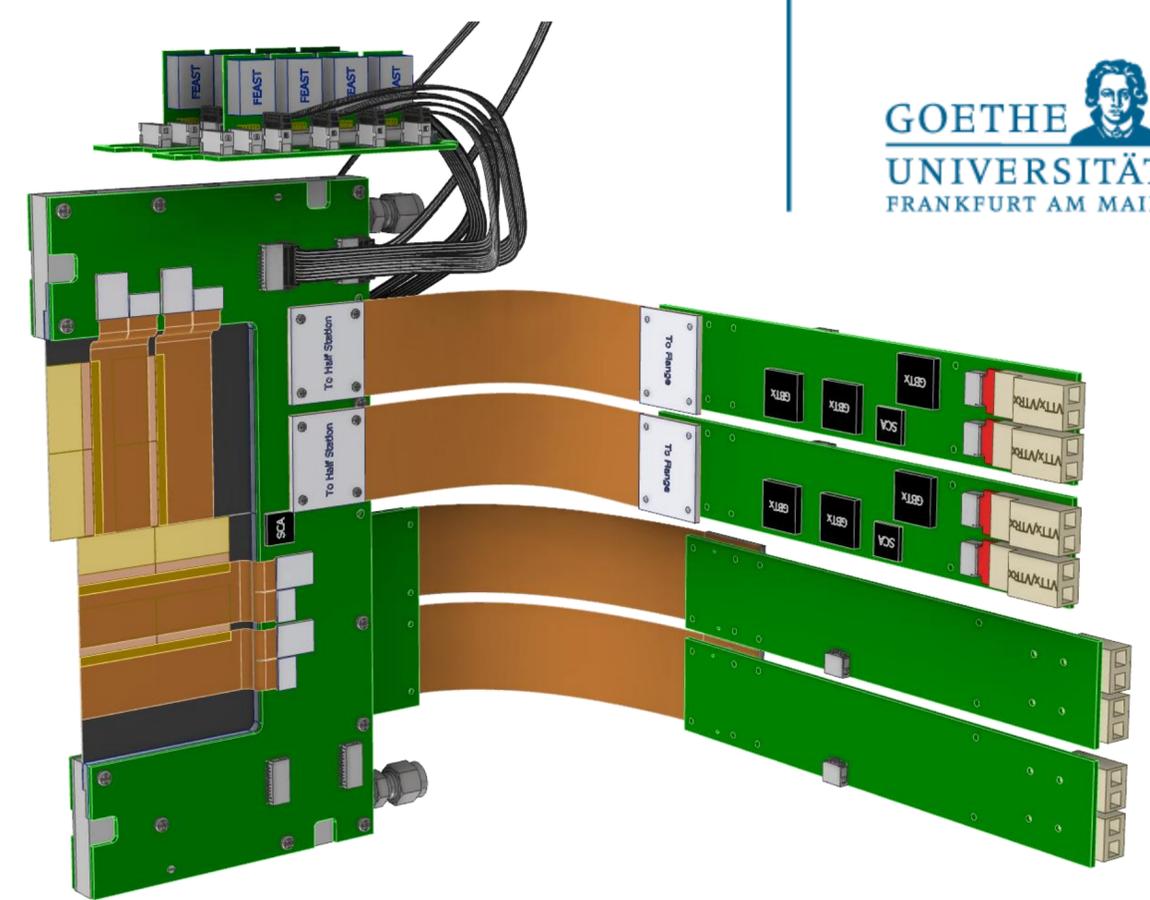


# Challenge: Data Integrity

High-speed signals over imperfect transmission path

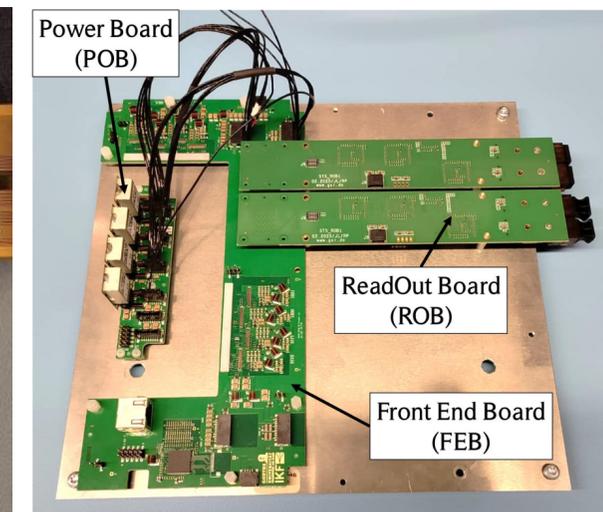
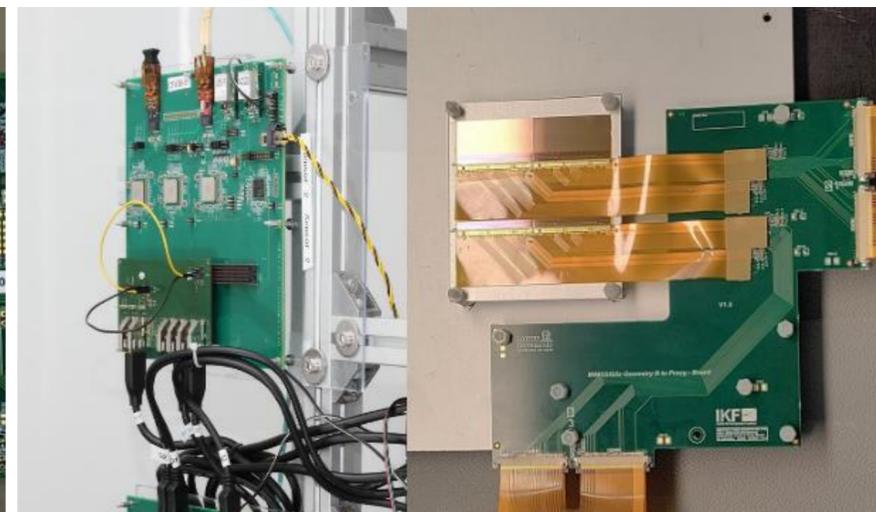
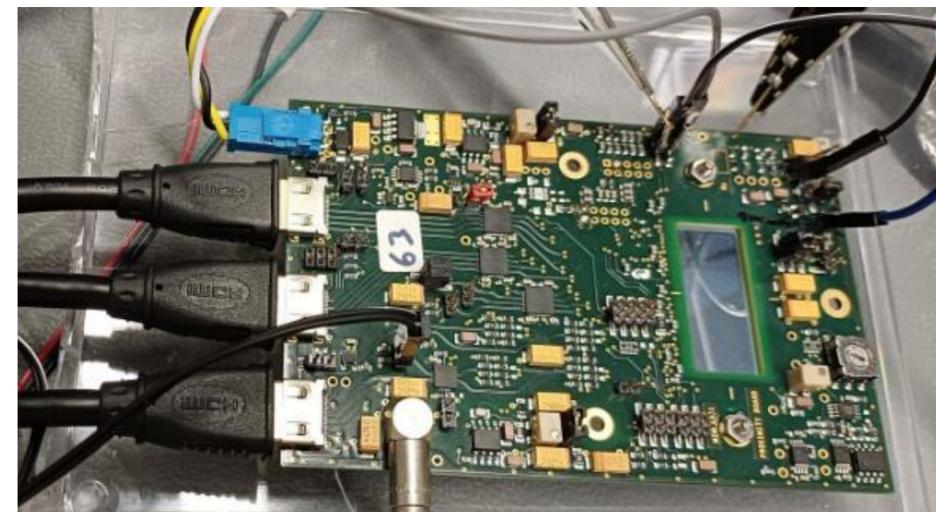
- 320 Mb/s SLVS, up to 90 cm FPCs + PCBs
- Three connectors (discontinuities) in data path
- Single-layer, unshielded FPCs
- SLVS CM (200 mV) shifts due to GND shift (40 mV)
- Dynamic phase shifts due to power fluctuations

Various aspects validated, full system test in preparation



Ideal operating conditions

MVD operating conditions



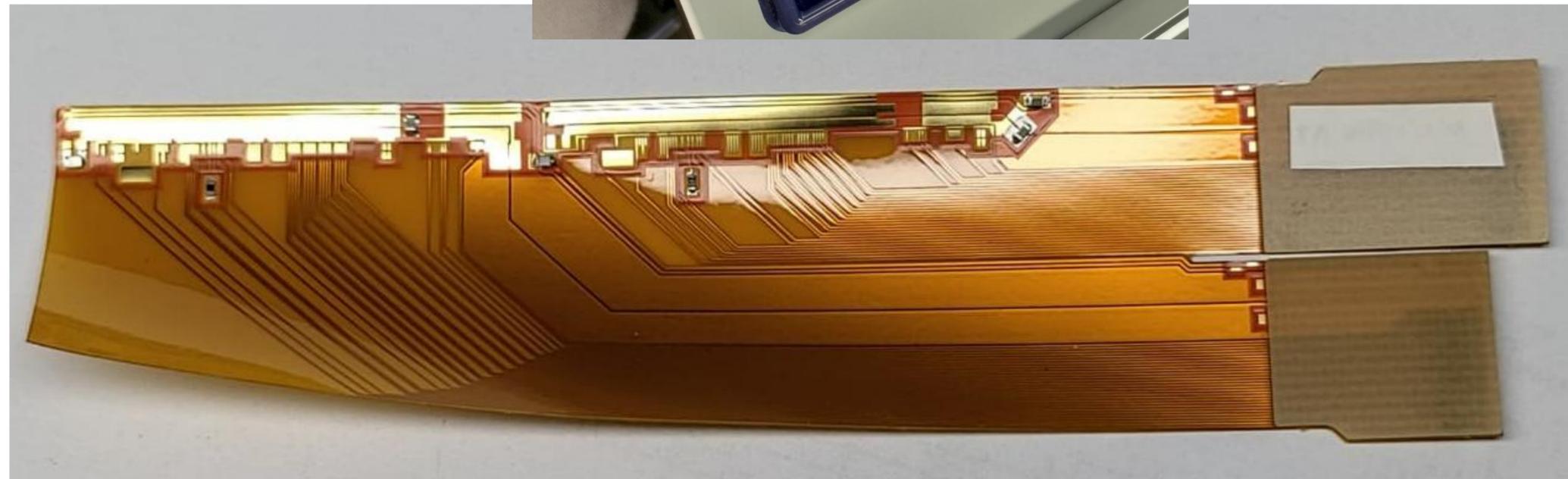
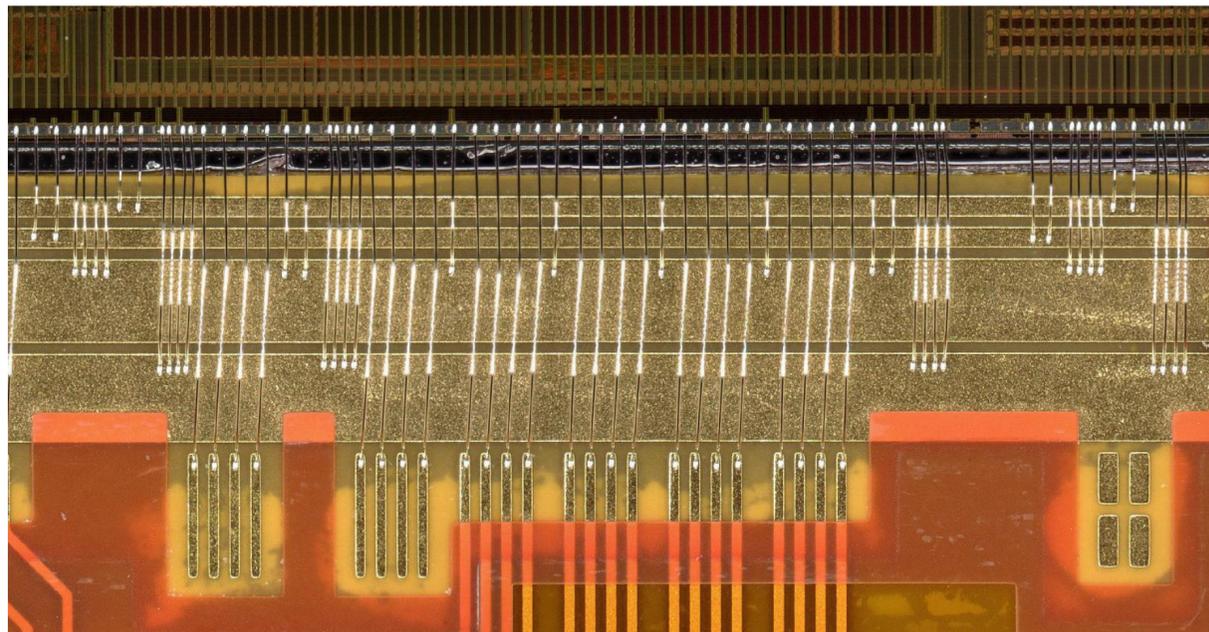
# FEE Validation: Next Steps

## Control functionality and Data Integrity

- Sensor FPCs, wire-bonded MIMOSIS 2.1
- Full-system tests w/ final powering, cable lengths, ...

## Sensor FPC

- Not final ultra-thin design
- Now 18  $\mu\text{m}$ , later 12  $\mu\text{m}$  copper
- Validate FEB, next iteration



# Wire Bonding

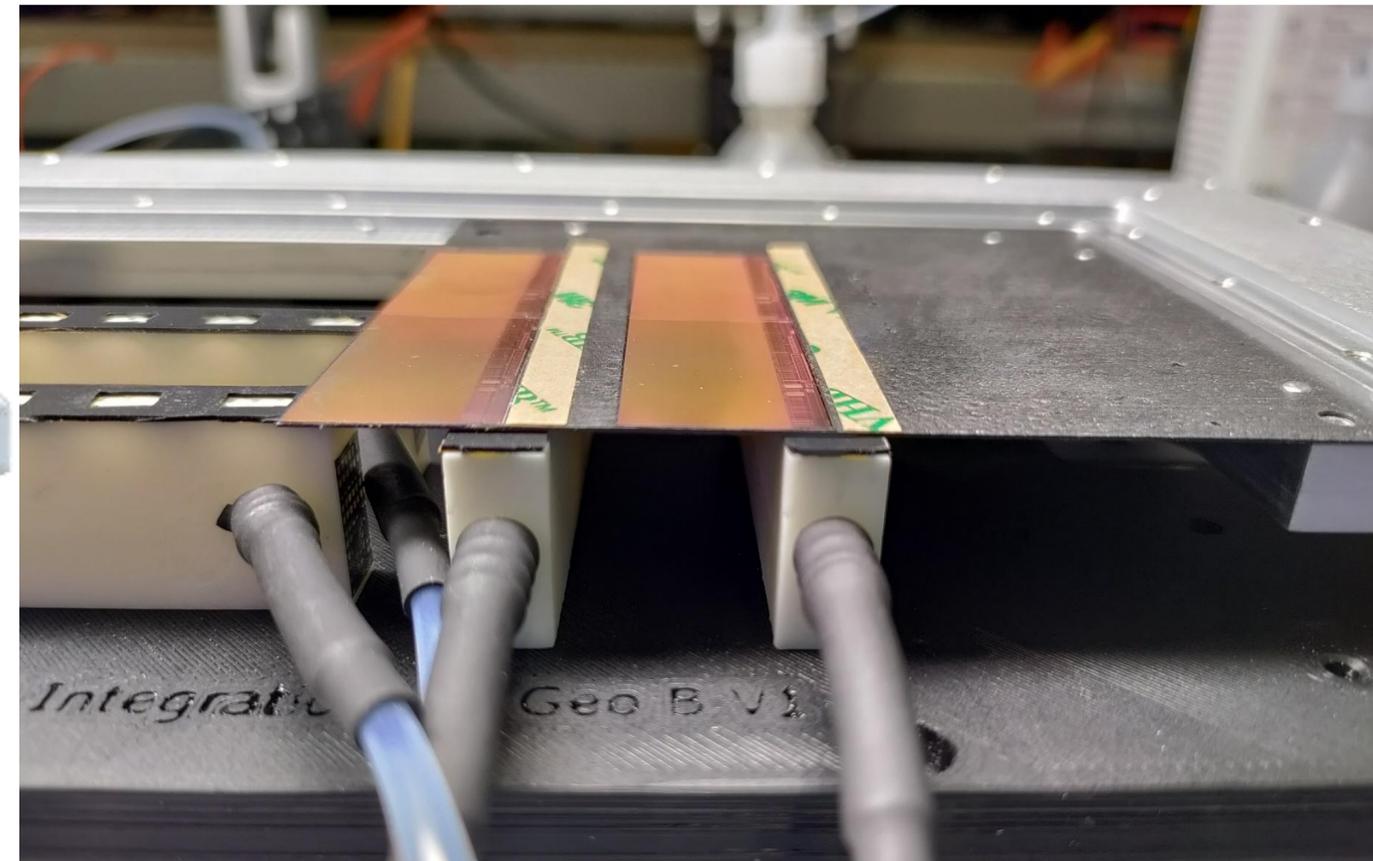
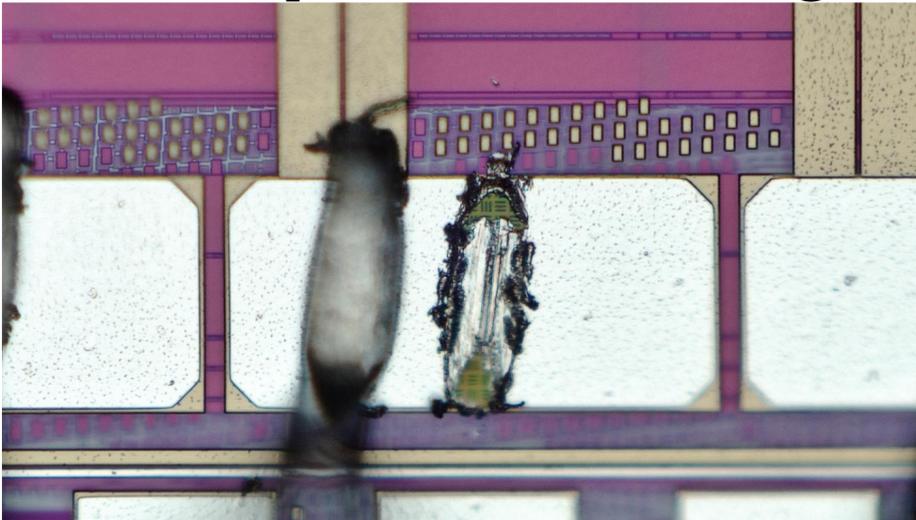
## Double-sided integration

- Wire-bonding: Challenging integration step
- Dedicated vacuum jig (Under validation)

## Full-automatic bonding @GSI Detector lab



## Pad rupture after bonding



## Chapter 3

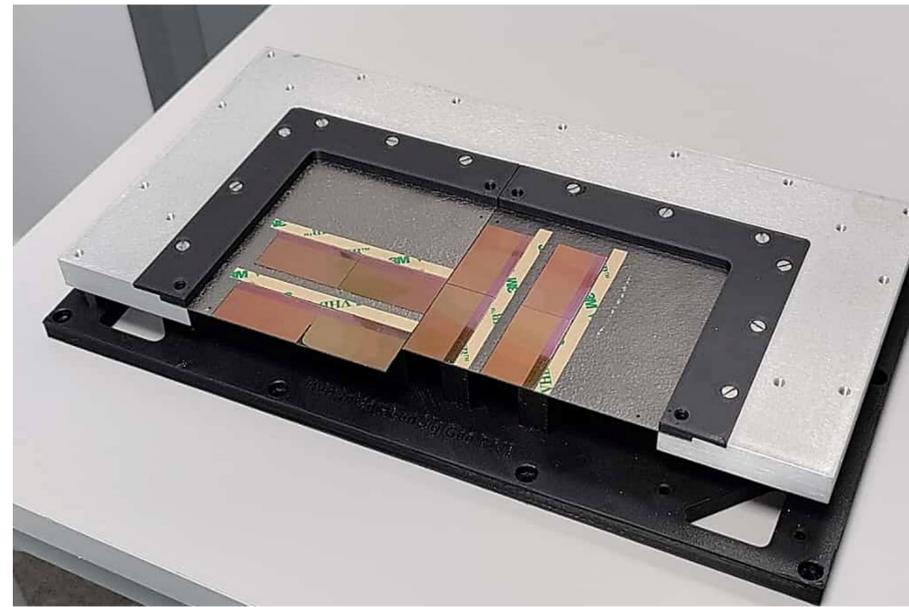
# Upgrades

# Pixel Upgrade

MVD is CBM rate bottleneck

→ 0.1 MHz Au+Au w/ MVD, up to 10 MHz w/o

→ Annual exchange of MVD planned



# Pixel Upgrade

## MVD is CBM rate bottleneck

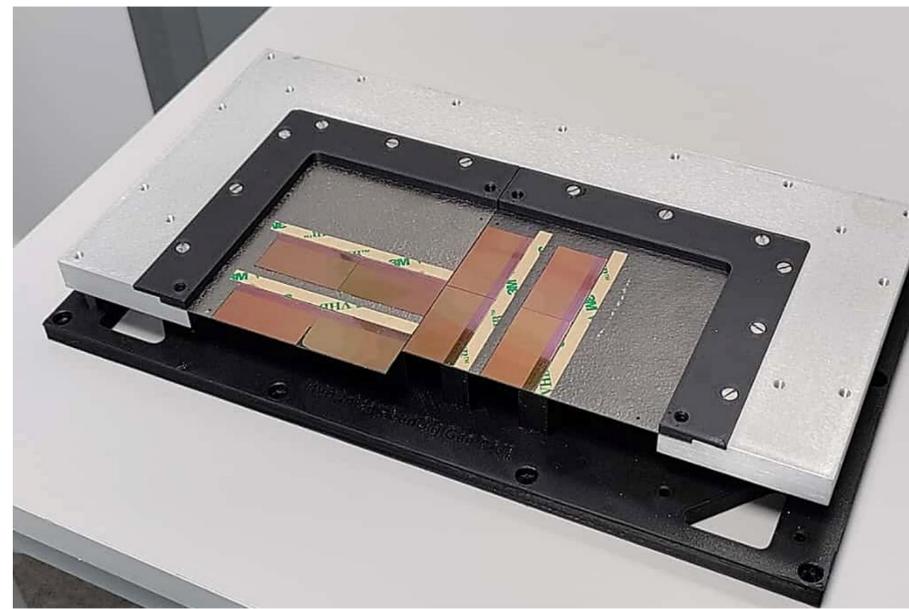
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## Material budget improvement

- MVD concept with early MAPS: limited by cooling
- Now: Limited by mechanics

## Rate improvement

- 1 MHz Au+Au w/ next-gen MAPS



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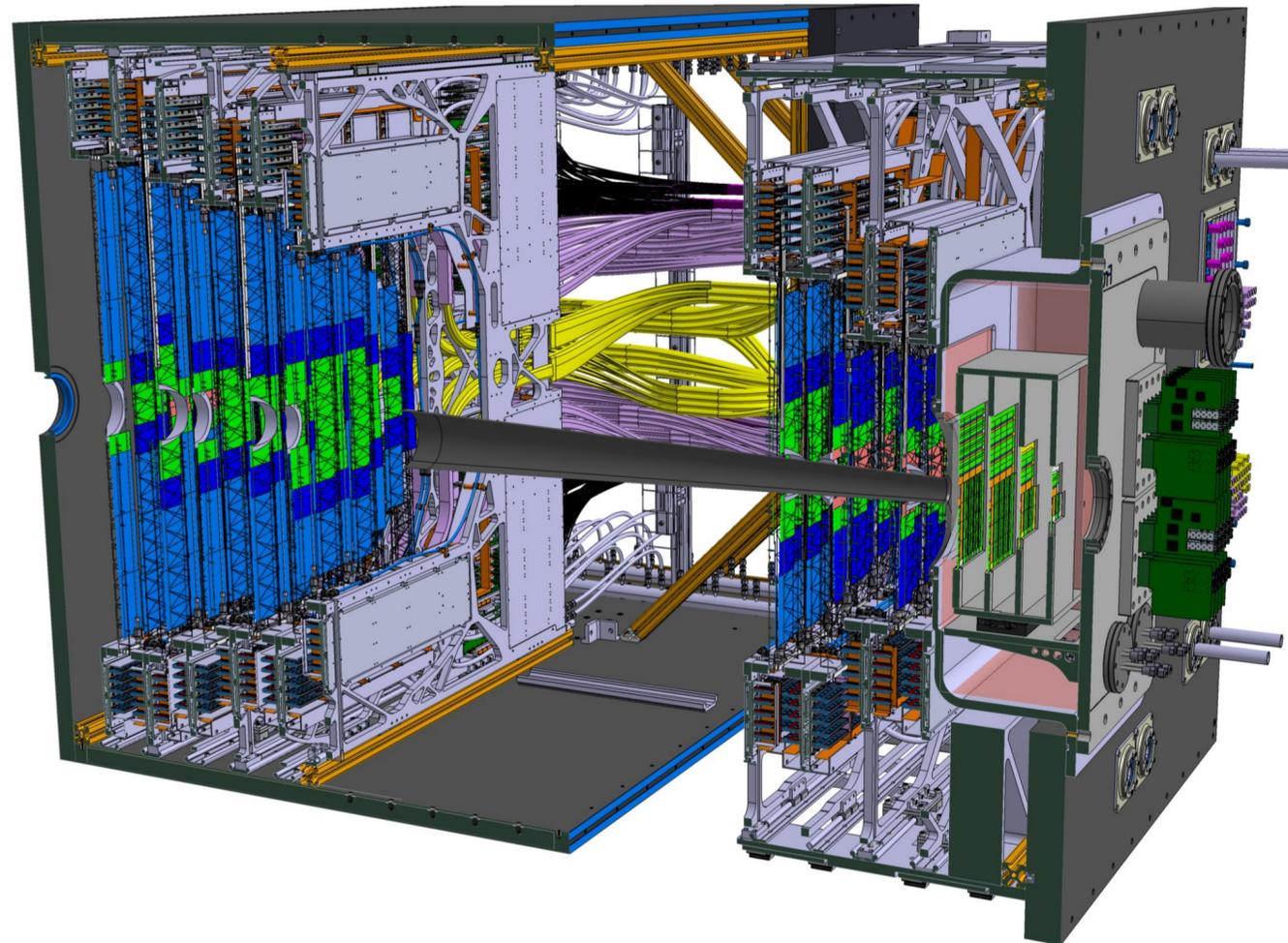
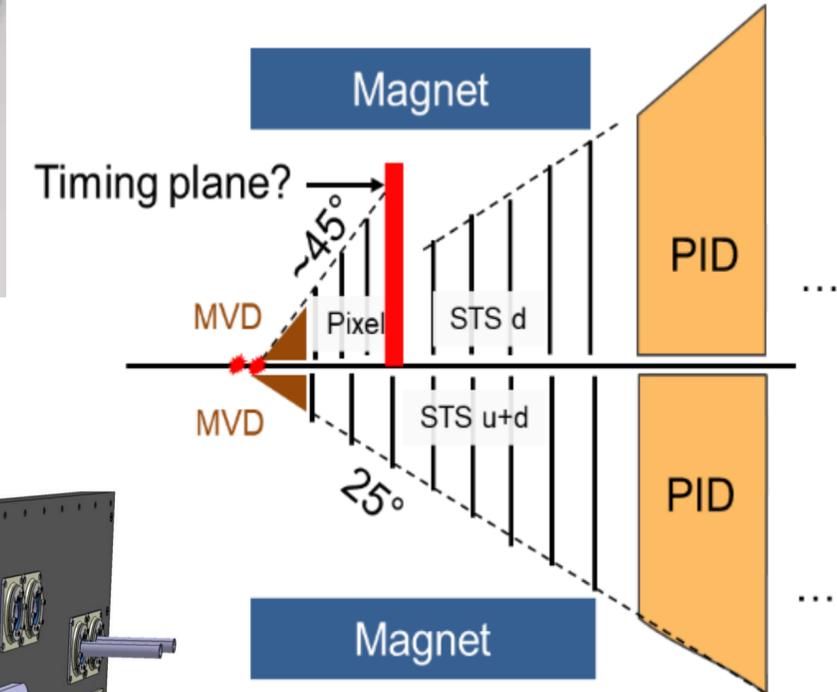
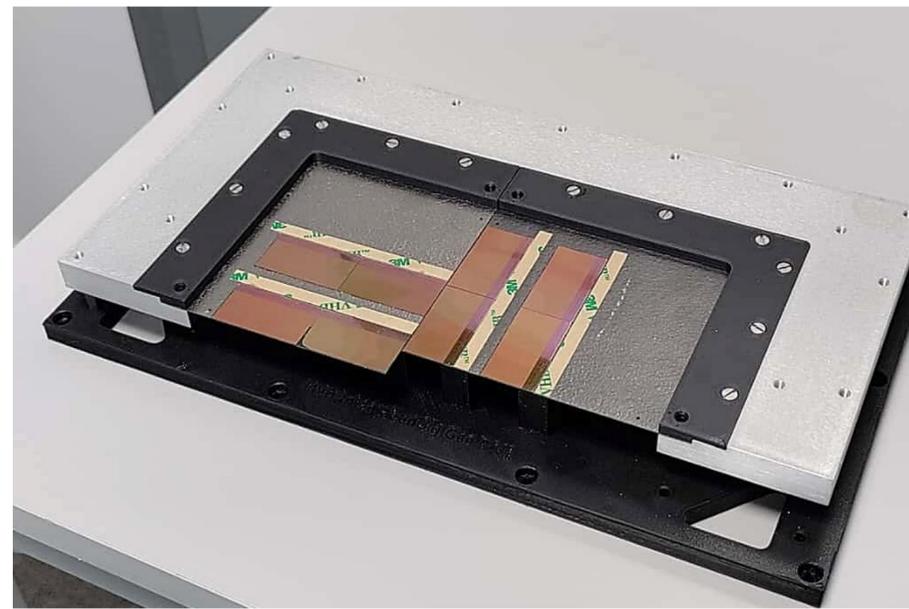
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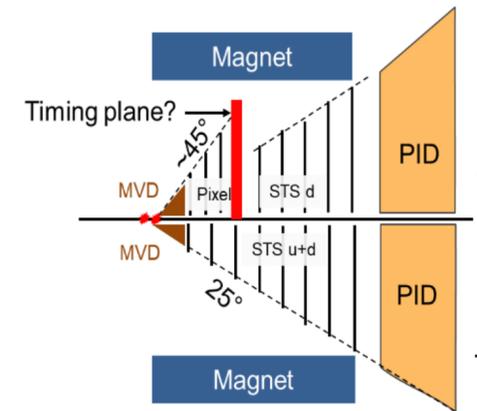
- 1 MHz Au+Au w/ next-gen MAPS

Full Inner Tracker Upgrade

- Next-gen MAPS MVD, Pixelized STS-U
- Extend acceptance from 25° to 45°?
- Material budget reduction?
- Added timing plane?
  - In-beam T0 limited to 0.1 MHz Au+Au



# Requirements Next-Gen MAPS



Back-of-the-envelope, to be scrutinized

Requirement	MIMOSIS	CBM STS Upgrade	CBM MVD Upgrade
Spatial precision ( $\mu\text{m}$ )	$\sim 5$	$\sim 10$	$\sim 5$
Time binning (ns)	5000	$\rightarrow$ $\sim 10$	$\sim 10$
Power dissipation ( $\text{mW}/\text{cm}^2$ )	$\sim 70$	$\sim 50$	$\sim 100$
Annual NIEL dose ( $n_{\text{eq}}/\text{cm}^2$ )	$\sim 3 \times 10^{14}$	$\rightarrow$ $\sim 2 \times 10^{14}$	$\sim 10^{15}$
Annual TID (Mrad)	$\sim 5$	$\sim 17$	$\sim 50$
Rate capability ( $\text{MHz}/\text{cm}^2$ )	20 (80) mean (peak)	$\rightarrow$ $\sim 10 + \text{margin}$	$\sim 90 + \text{margin}$

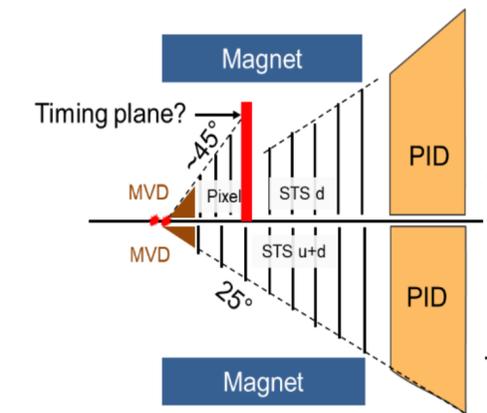
# Requirements Next-Gen MAPS

Move from TJ180 nm to TPSCo 65 nm

## New readout philosophy

- Abandon frame-based readout
- Time walk correction mandatory for timing

## Serial powering



Back-of-the-envelope, to be scrutinized

Requirement	MIMOSIS	CBM STS Upgrade	CBM MVD Upgrade
Spatial precision ( $\mu\text{m}$ )	~5	~10	~5
Time binning (ns)	5000	→ ~10	~ 10
Power dissipation ( $\text{mW}/\text{cm}^2$ )	~70	~ 50	~100
Annual NIEL dose ( $n_{\text{eq}}/\text{cm}^2$ )	~ $3 \times 10^{14}$	→ ~ $2 \times 10^{14}$	~ $10^{15}$
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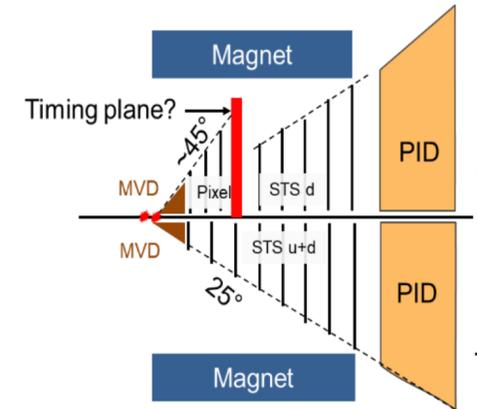
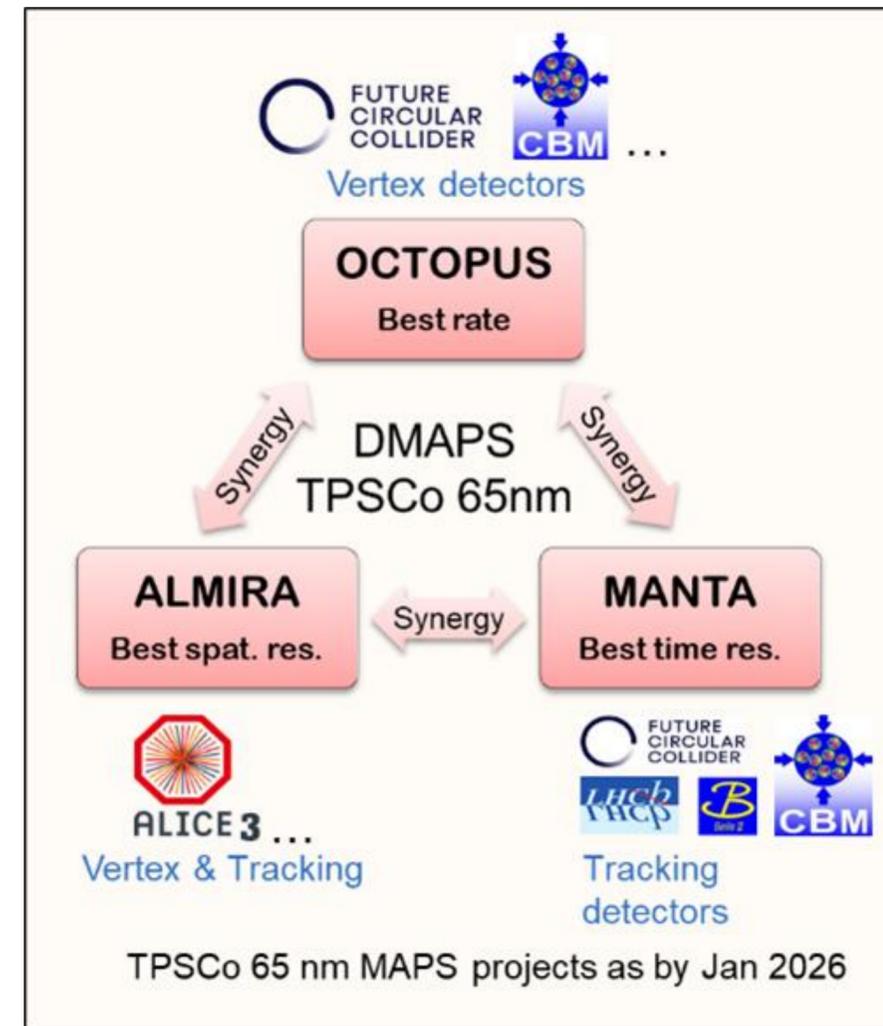
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Annual TID (Mrad)	~ 5	~ 17	~ 50
Rate capability (MHz/cm <sup>2</sup> )	20 (80) mean (peak)	→ ~10 + margin	~ 90 + margin

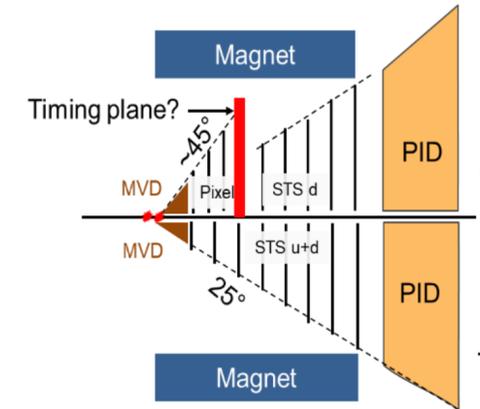
# OCTOPUS and MANTA

## OCTOPUS

- DRD3 recognized functional collaboration
- Sensor R&D ongoing

## MANTA

- Collaboration under preparation
- Sensor R&D started, regular design meetings



# OCTOPUS and MANTA

## OCTOPUS

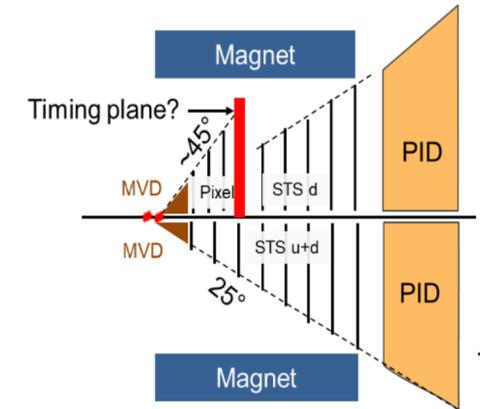
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- Collaboration under preparation
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## SPARC (IPHC) prototype on ALICE/ER2

- 1.5x1.5mm<sup>2</sup>, novel readout, ~6ns time precision expected
- Beam test planned (DESY, 22. May – 05. June)
- Joint OCTOPUS/MANTA team
- Mini-structure on ALICE/ER3 planned



SPARC → Prototype of 32x28 pixels with 24,1µm x 16 µm pitch, in technology TPSCo 65nm, for testing the feasibility of an asynchronous readout architecture in MAPS-type pixel matrix, ~6,3 ns time resolution (4-5ns jitter due to readout), ER2 run

**SPARC Layout**

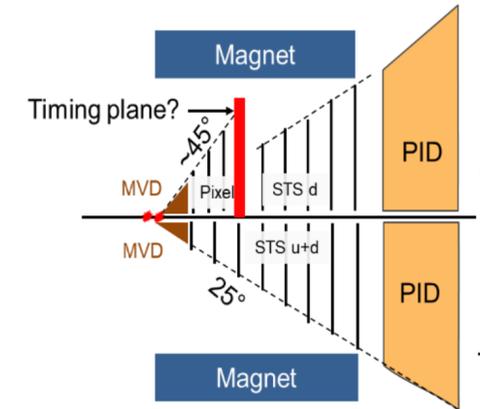
- FIFO with double asynchronous entry, no needs for additional circuitry
- Front-end from the DPTS chip
- TDC for an outside matrix 2ns timestamping

**Readout Architecture**

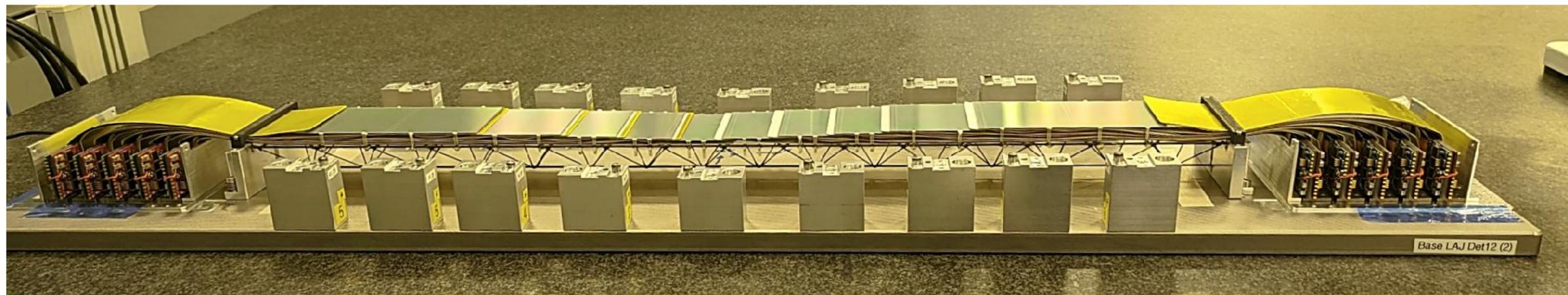
The readout architecture diagram shows a 1.5 mm wide chip. It includes a 'MATRIX' (blue) and 'PADs' (grey). The readout system consists of a 'LINE readout' (blue), a 'FIFO + serializer' (orange), and a 'Biasing' block (yellow). The 'FIFO + serializer' is connected to a 'Slow-Control' block (yellow) and a 'TDC' block (green). The 'TDC' is connected to a 'VCO' block (green). The 'FIFO + serializer' is connected to an 'Address bus' and an 'Output bus'. The 'Biasing' block is connected to an 'Output bus'. The 'LINE readout' is connected to an 'Address bus' and an 'Output bus'. The 'PADs' are connected to an 'SEU info' block (yellow) and an 'Output bus'.

J. Soudier, "A versatile and fast pixel matrix read-out architecture for MAPS", PISA 2024

# First Draft of STS Upgrade Ladder



CBM-STS Ladder  
→ Silicon Strips



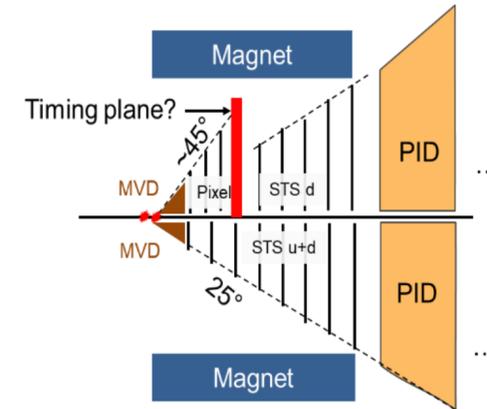
# First Draft of STS Upgrade Ladder



## STAR-HFT

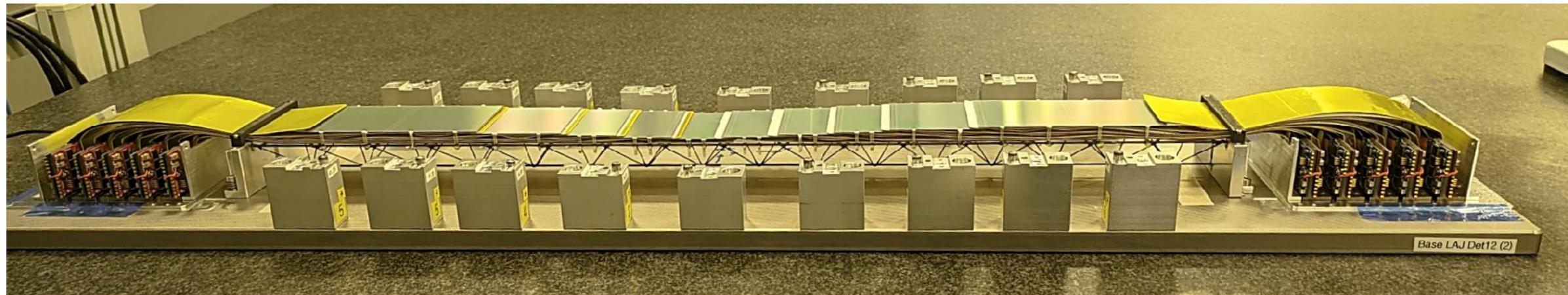
→  $\sim 150\text{mW}/\text{cm}^2$

→ Air-guide



## CBM-STS Ladder

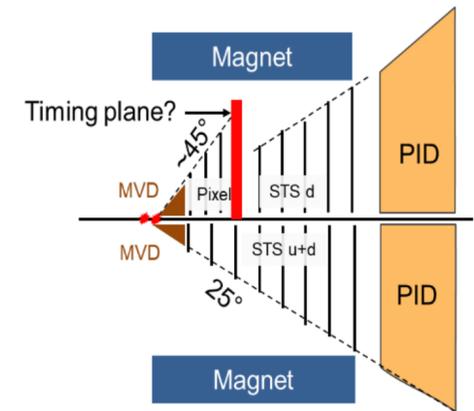
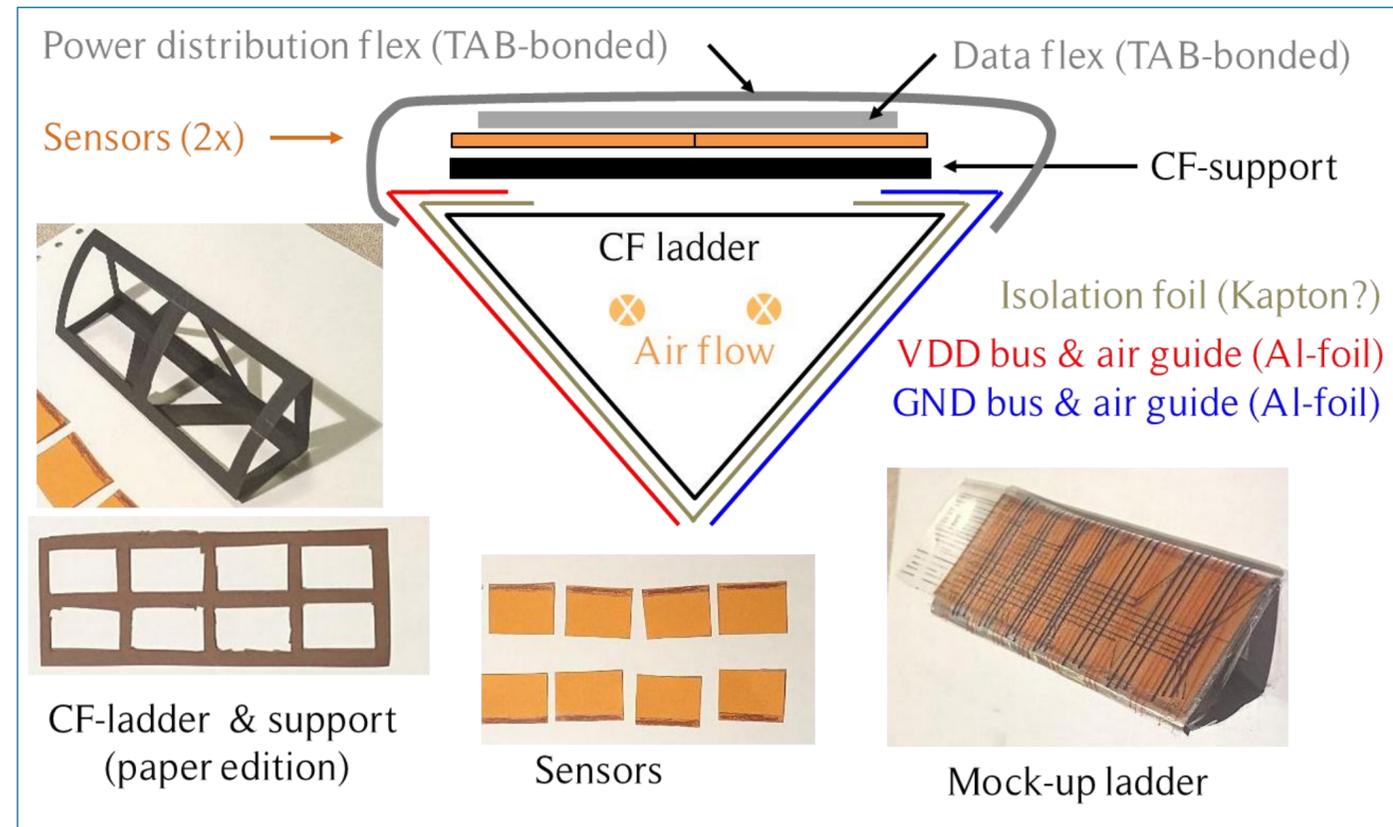
→ Silicon Strips



# First Draft of STS Upgrade Ladder

Air cooling concept similar to STAR-HFT

- Power distribution flex as part of air guide
- CF modules + PGS, assembled on STS ladder

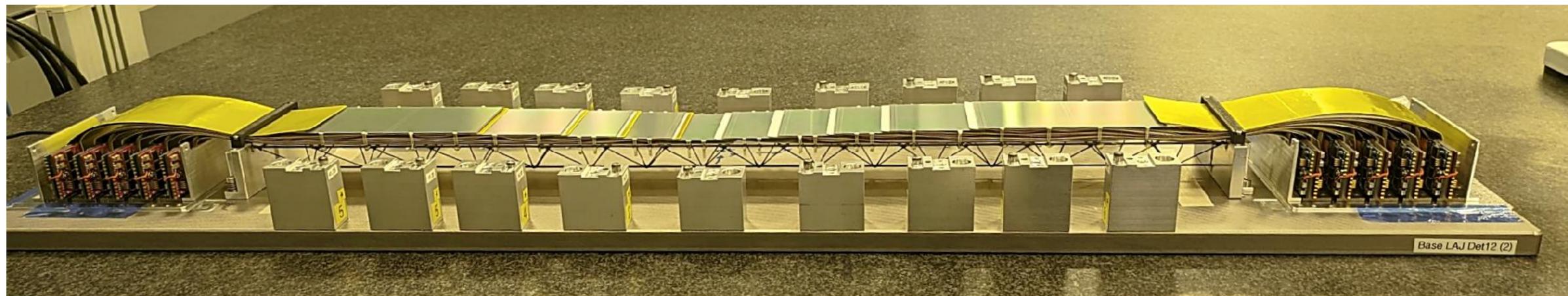


## STAR-HFT

- ~150mW/cm<sup>2</sup>
- Air-guide

## CBM-STs Ladder

- Silicon Strips



# Summary

## MIMOSIS CMOS MAPS R&D concluded

- Performance validated
- M3 submission now, FOS Q4/26

## MVD full-system tests in preparation

- Pre-requisites done
- Pre-production module(s) Q2/26

## Upgrade project started

- Common resources, ideas, ...
- GSI pixel platform



Silicon@GSI: Kick-off event 31 January 2025

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... exciting times for CBM, GSI, and the MAPS community!