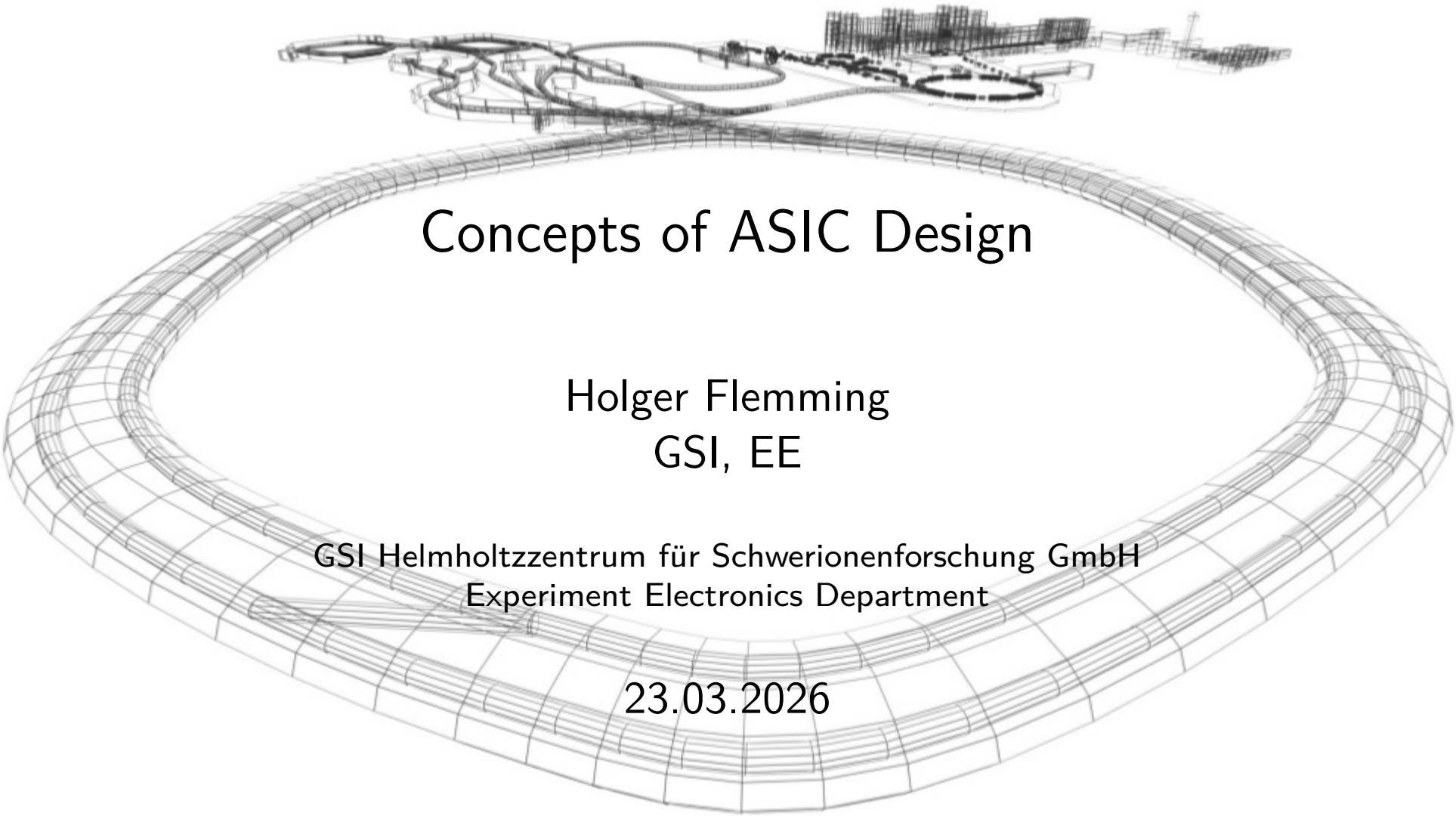

Concepts of ASIC Design

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Contents

Outline

Why ASICs???

Some Preconceptions

- ASICs are expensive
- Needs decades for development
- Inflexible
- Very special knowledge required
- You can do everything with FPGAs

So why concerning oneself with ASIC design?

Some Good Reasons

- Pixel Sensors!
- Readout of detectors with high granularity
- Radiation hardness
- Costs
- It's fun!

Outline

ASIC Characteristics

What is an ASIC

ASIC = **A**pplication **S**pecific **I**ntegrated **C**ircuit

- ⇒ It's specific for your application
- ⇒ Electronic circuit integrated on a single substrate (mostly silicon)

Circuit Integration

Integration on single substrate has several implications
But: physics of an electronics circuit same as on PCB!

Integrated Circuit Technologies

Technologies

- **C**omplementary **M**etal **O**xid **S**emiconductor
  Mainstream technology: CPUs, GPUs, ...
  - Bulk CMOS
  - **S**ilicon **O**n **I**nsolator
- BiCMOS / SiGe-BiCMOS
  - CMOS with additional process steps for bipolar transistors
  - Often usage of silicon - germanium
  - High-Speed applications
- Gallium arsenide (GaAS)
  - RF applications (LNA, power amplifier)
  - Photonics
- Silicon carbide
  - Power electronics

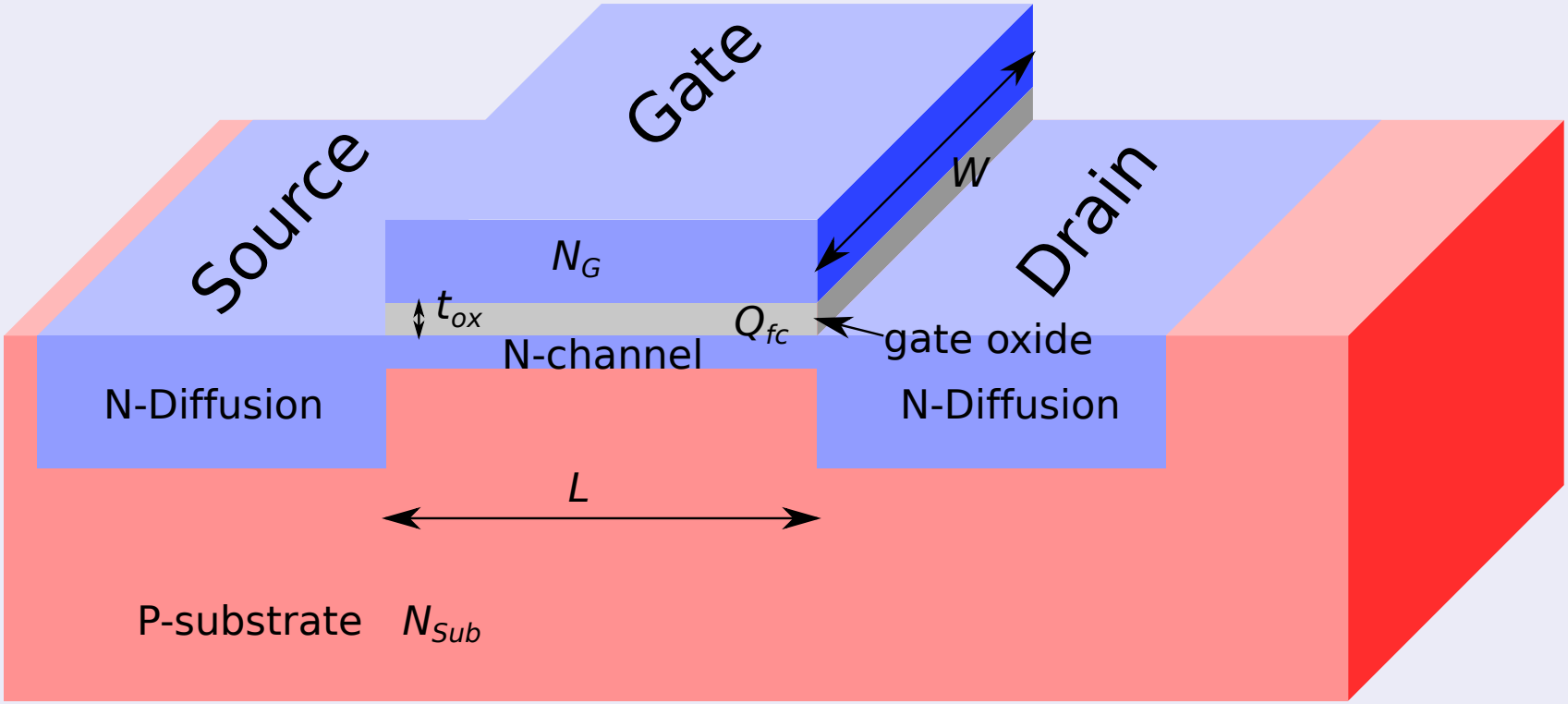
Characteristics of an Integrated Circuit

Challenges of an CMOS Integrated Circuit Design

- Limited types of components
  - N- and PMOS transistors
  - Diodes
  - PNP bipolar transistors
  - Resistors
  - Capacitors
  - Spiral inductors
- Sole degree of freedom in design: component size
- All components are placed in the same substrate
- Limited core voltage
- large spread of component parameter, but good control of parameter ratio of adjacent components
- Resistors, capacitors and inductors require large chip area

Components

MOS-FETs

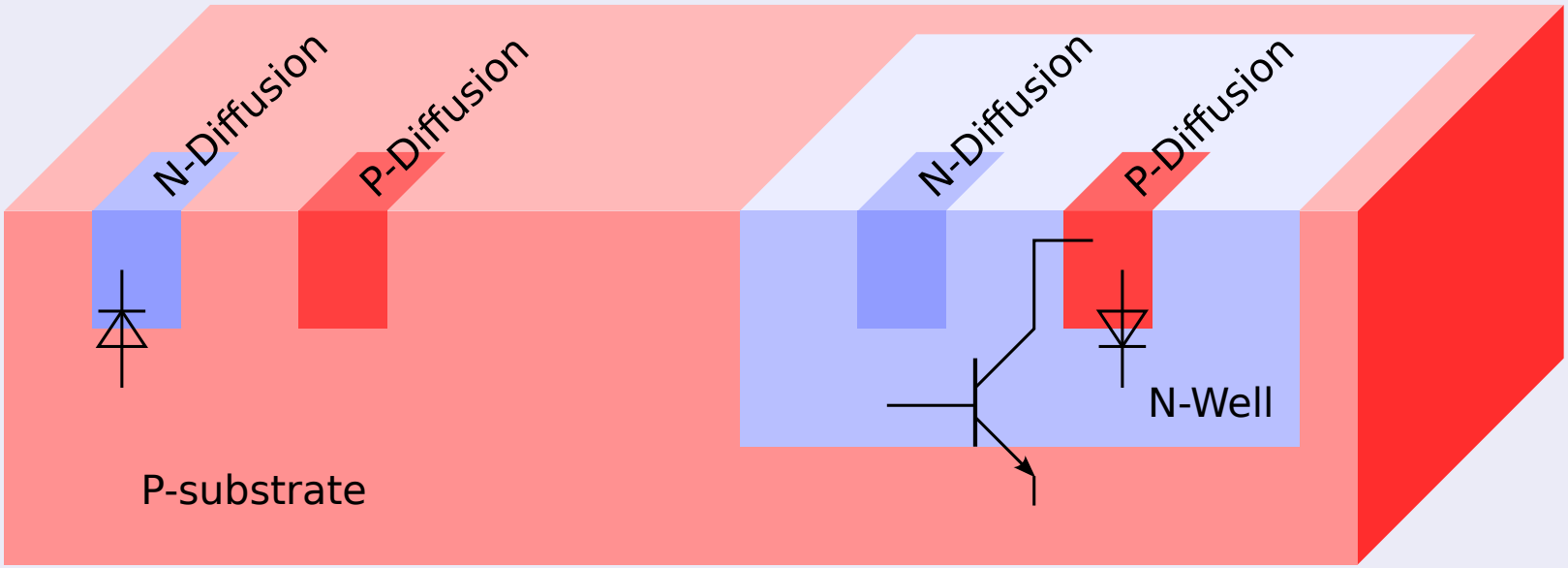


NMOS transistor in p substrate

PMOS transistor with inverted doping placed in N-well

Components

Diodes



- Parasitic diodes and pnp transistors at diffusion zones
- Usage as protection and in some analogue circuits e.g. bandgap
- Varicap

Components

Resistors

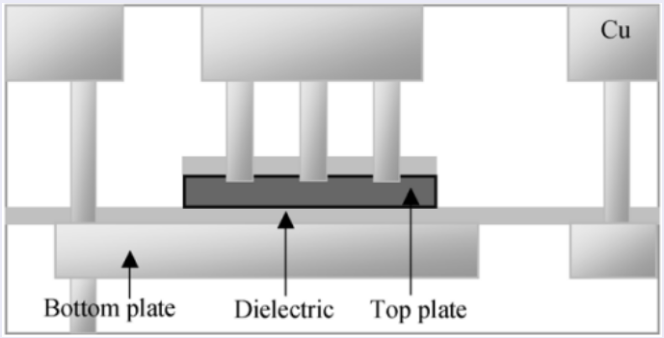
- Any material with high sheet resistance $R_\square$ can be used.
  Resistance R given by $R = R_\square \times l/w$
- Required area $\approx 1/R_\square$
- Metal lines
  Only small resistances feasible
- Weakly doped silicon e.g. N-well
  Surrounded by depletion zone of N-well - p-substrate diode
  $\Rightarrow$ cross-section depends on voltage
  $\Rightarrow$ Non-linearities
- High-resistive poly silicon
  Better linearity
  Additional process step, only available in analogue technologies

Components

Capacitors

- Gate capacitance of MOS-FETs
  + In all CMOS technologies available
  - highly non-linear
- Interdigital capacitors
  + In all CMOS technologies available
  - low capacitance per area
- Poly-poly capacitors
  Need a second poly-silicon layer
- **M**etal **I**nsulator **M**etal capacitor
  Needs additional process step

MIM Capacitor



Cross section of a MIM capacitor[N+05]

Circuit Design

Circuit Design

- Avoid large area components
  - Replace resistors by current sources / sinks / mirrors
  - No AC coupling
- Low core voltage
  350 nm: 3.3 V, 180 nm: 1.8 V, 65 nm: 1.2 V
  - Required drain-source voltage for saturation: 250 mV - 300 mV
  - Typical circuits require 3 transistors in series

  $\Rightarrow$ Remaining voltage swing in 65 nm: 300 mV - 450 mV

  $\Rightarrow$ Use fully differential architecture!
- Large spread of component properties
  Circuit behaviour should never depend on single component properties but on ratios!

ASIC Production

Wafer Processing

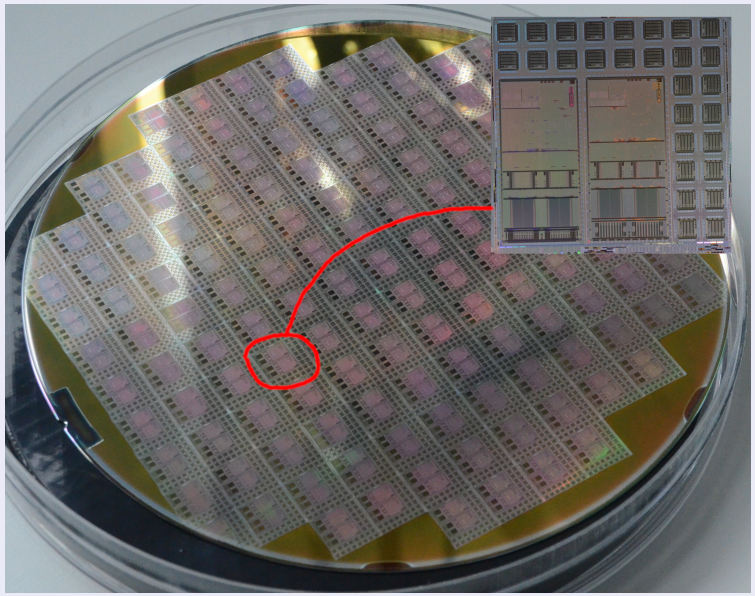
- Wafer produced by a series of doping, etching, oxidation, metallisation etc... steps
- Controlled by lithography

Lithography

- Lithography defines size of chip structures
- Lithography mask production most expensive part of ASIC production
  - 180 nm: €100 k
  - 65 nm: €500 k - €800 k

Lithography

- Masks cover area of typically 20 mm by 20 mm (reticle)
- Reticle stepped over whole wafer

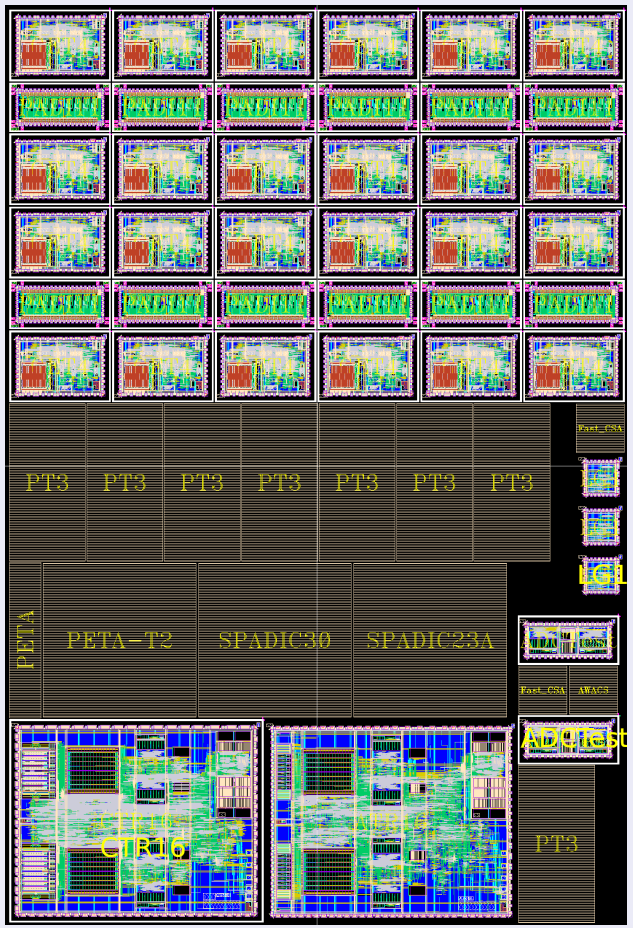


ASIC Production

Multi Project Wafer

- Placing several different chips on a reticle
- Idea: sharing the costs of mask production
- Affordable costs for prototyping
  - 180 nm: 1475 €/mm^2
  - 65 nm: 3691 €/mm^2
- Larger volumes by ordering additional wafer

MPW Reticle



Outline

ASIC-Design

General Remarks

- Prototyping is expensive, long turn-around times
  $\Rightarrow$ First try should be successful!
  $\Rightarrow$ Simulate, simulate, simulate!!!
- It's hard to probe signals on an ASIC
  $\Rightarrow$ Consider debugging in your design from the beginning, especially for early iterations

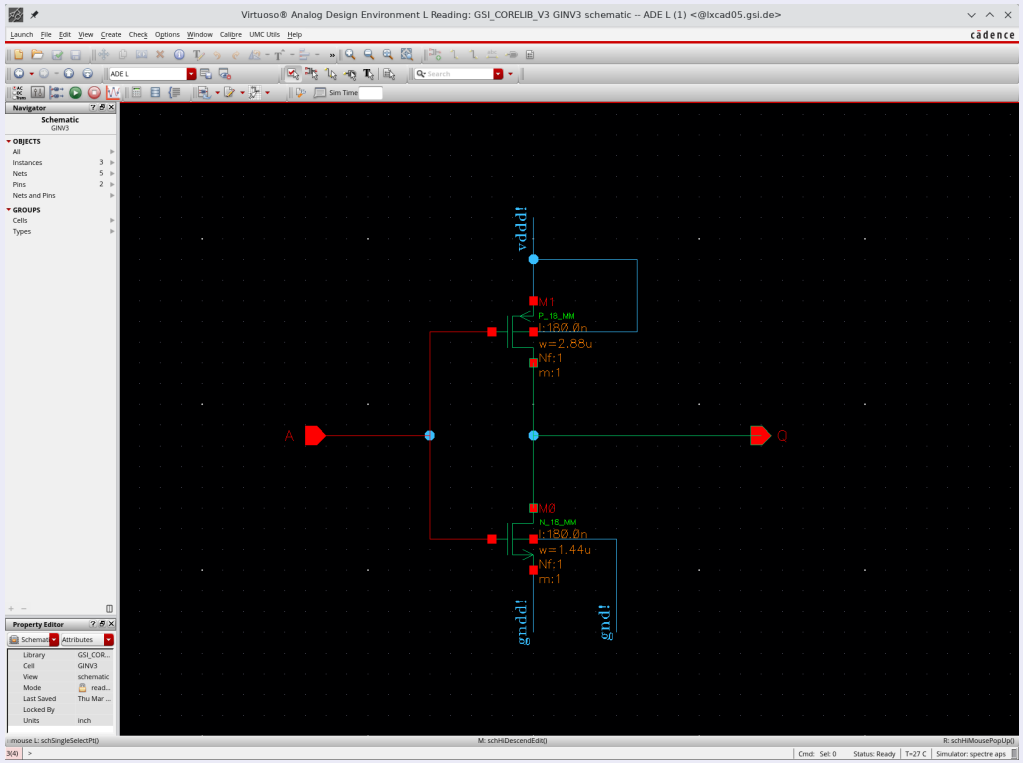
Full Custom Analogue ASIC-Design

Requirements

- ASIC design CAD environment, e.g. Cadence Virtuoso
- Powerful Linux-Server
  - Simulation software has extreme demands on memory
  - Multi-core CPUs might be helpful
- Workstation with large screen is helpful
- **P**rocess **D**esign **K**it
  - Component library for CAD tool
  - Spice models for components
  - Rule files for verification tools
  - Documentation

Full Custom Analogue ASIC-Design

Schematic Entry



Schematic Entry typical for Full Custom Analogue Design

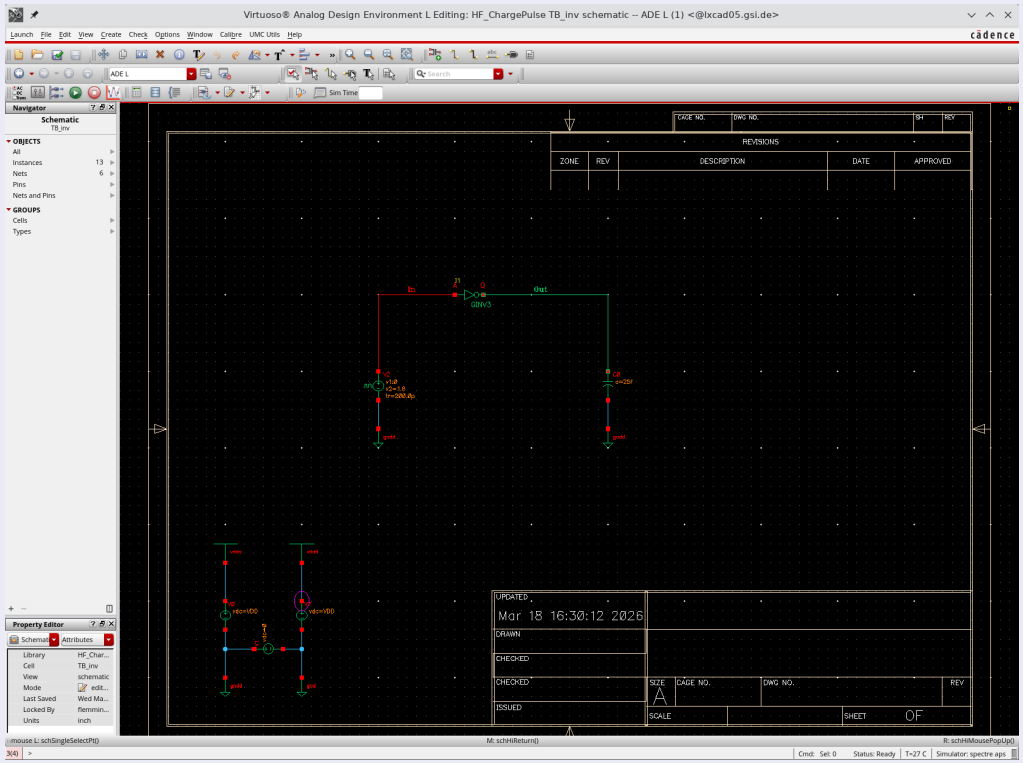
Full Custom Analogue ASIC-Design

Simulation

- Circuit Simulation with spice-like simulators
  - Simulation on analogue component level
  - Solving a network of voltage / current sources and conductivities
- Different types of simulations
  - DC simulation
    - testing dc working point
  - AC simulation
    - Testing open loop gain and phase margin of amplifiers
    - Stability studies
  - Transient simulation
    - Time like behaviour of a circuit
  - Noise simulation

Full Custom Analogue ASIC-Design

Simulation Environment



Simulation Environment for transient simulation

Full Custom Analogue ASIC-Design

Simulation Result

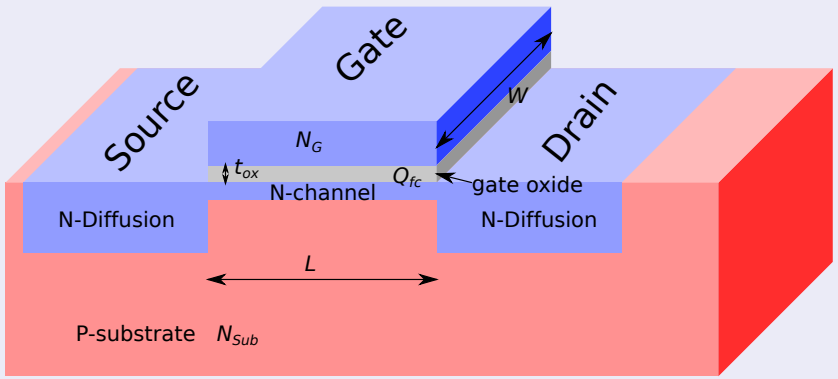
Cadence virtuoso waveform viewer with simulation result

Full Custom Analogue ASIC-Design

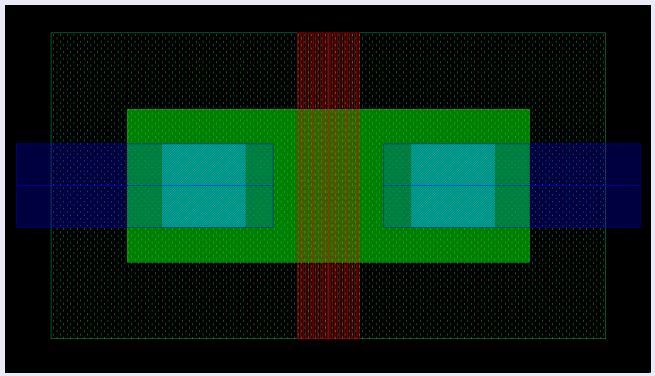
Layout

- Implementing circuit as geometric structure on chip: layouting
- CAD tool provides drawing layer corresponding to technology process steps
- Foundry defines layout design rules which have to be observed

Physical Implementation



Layout

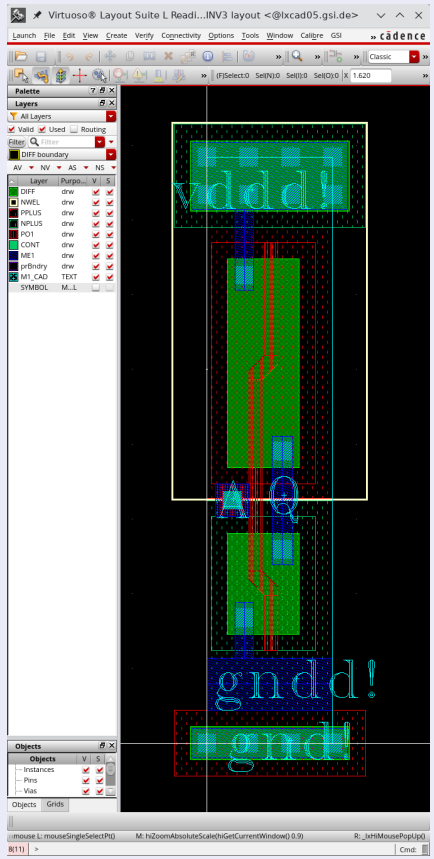


Full Custom Analogue ASIC-Design

Layout

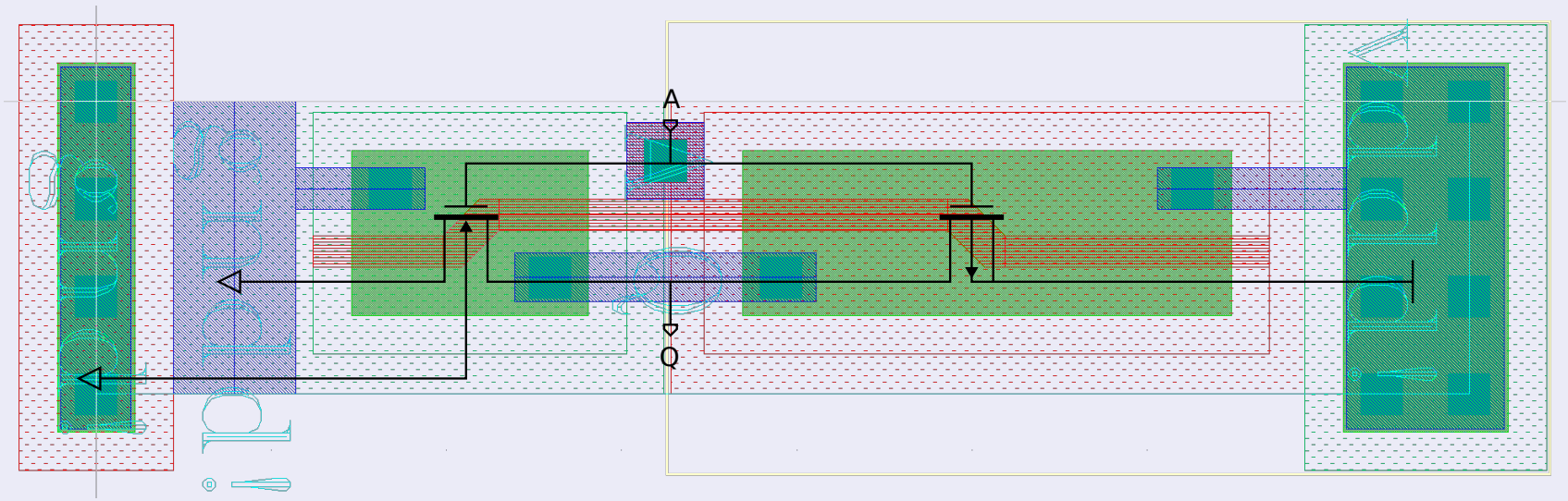
- Components
  - Doping zones
  - Gates
  - Library elements available
  - For very compact design individual layout required
- Substrate and well contacts
- Interconnections
  - Contacts / Vias
  - Metal lines
- Verification
  - **D**esign **R**ule **C**heck
  - **L**ayout **V**ersus **S**chematic check

Inverter Layout



Full Custom Analogue ASIC-Design

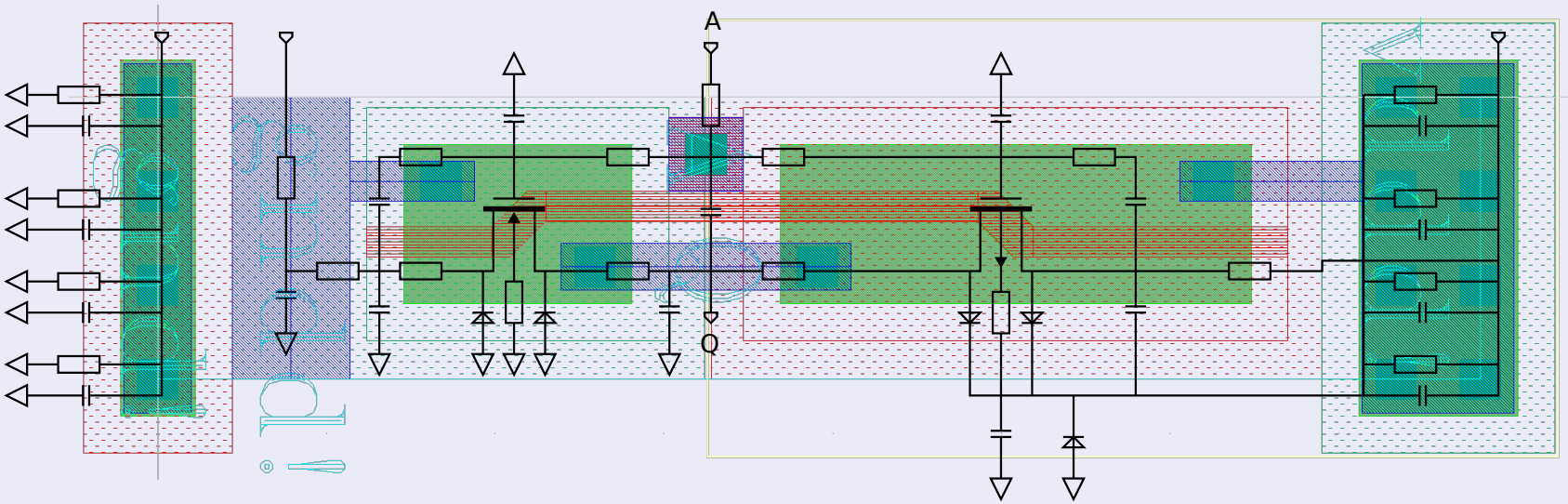
Layout versus Schematic



Schematic extracted from layout

Full Custom Analogue ASIC-Design

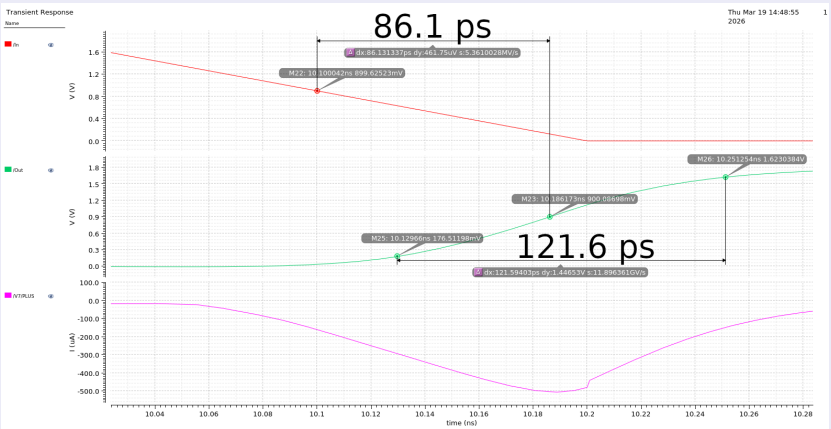
Layout versus Schematic



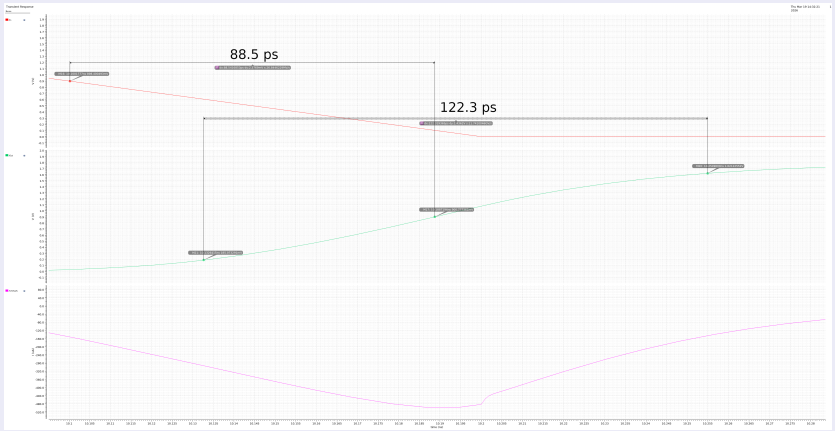
More realistic extraction with parasitic components

Full Custom Analogue ASIC-Design

Schematic Simulation



Parasitic Simulation



Digital ASIC-Design

Requirements

- Digital ASIC design CAD environment, e.g. Synopsys Design Compiler, Cadence Innovus
- Powerful Linux-Server
- Workstation with large screen is helpful
- Standard core cell library
  - Library of simple digital cell: gates flip-flops etc.
  - Behavioral description
  - Timing Models
  - Layout macros
  - In rare cases: Full tape out kit containing schematics and layouts
- IO cell library
- IP cores

Digital ASIC-Design

HDL Entry

- In digital ASIC-design: Design entry with HDL-code (VHDL / Verilog)
- Simulation with HDL simulation tool
- If no special IP cores required: Test on FPGA

Definition of Constraints

- Timing Constraints have to be defined
  - Clock frequency
  - Timing uncertainties e.g. jitter, clock skew
  - input and output delays
  - External drivers for inputs and load on outputs
  - Timing exceptions e.g. false paths, multi-cycle paths

Digital ASIC-Design

Netlist Synthesis

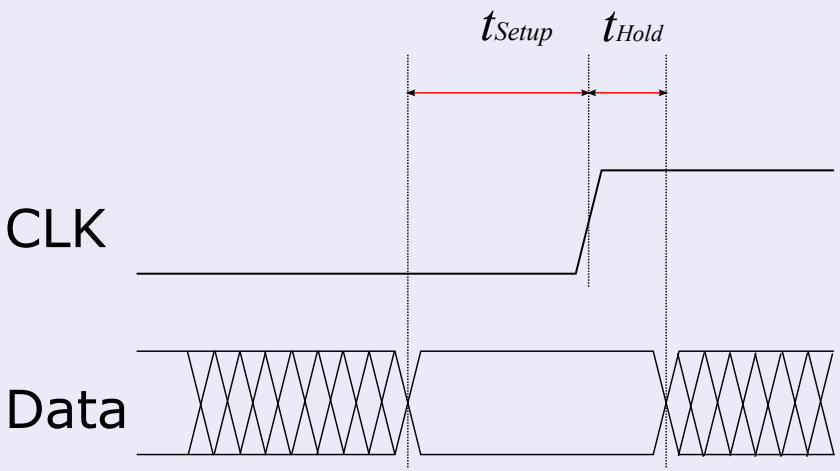
- Compiles netlist of standard library cell from HDL code
- Static Timing Analysis
  - Simplified model of routing delays
- Optimisation
  - Timing
  - Power consumption
  - Area

Formal Verification

- Independent verification tool
- Checks formal equivalence HDL code vs. netlist

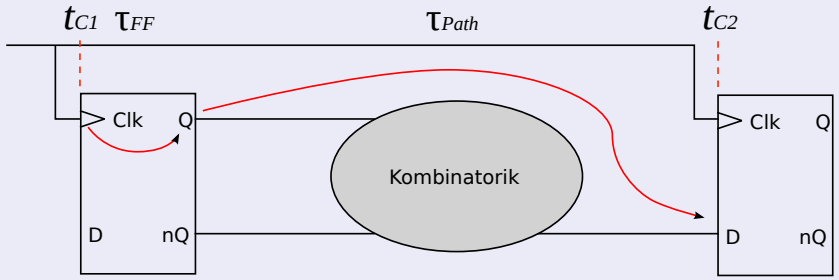
Digital ASIC-Design

Register Timing



- Setup and hold timing has to be fulfilled for each register
- Timing violation might result in meta stability

Static Timing Analysis



- Setup: $T_{SetupSlack} = T_{Clk} - \tau_{uncert} - t_{Setup} - \tau_{FF} - \tau_{Path}$
- Hold: $T_{HoldSlack} = \tau_{FF} + \tau_{Path} - \tau_{uncert} - t_{Hold}$
- $T_{SetupSlack} \overset{!}{\geq} 0$ und $T_{HoldSlack} \overset{!}{\geq} 0$
- For each path!

Digital ASIC-Design

Physical Implementation

- Import of netlist to physical implementation tool
- Floor-planning
- Placement
- Clock tree synthesis
- Routing
- Final verification
- Layout export
  if needed import to full custom tool

Digital ASIC-Design

Floor-planning

- Defining chip size / block size
- Defining position of IO-cells / IO-pins
- Placing IP cores
- Power routing

Placement

- Automatic placement of standard cells from netlist
- Placement is timing, power and congestion driven
- Trial route for first timing analysis

Digital ASIC-Design

Clock Tree Synthesis

- Generation of tree structure to clock each register
- Buffer and Routing
- Low latency, minimum clock skew

Routing

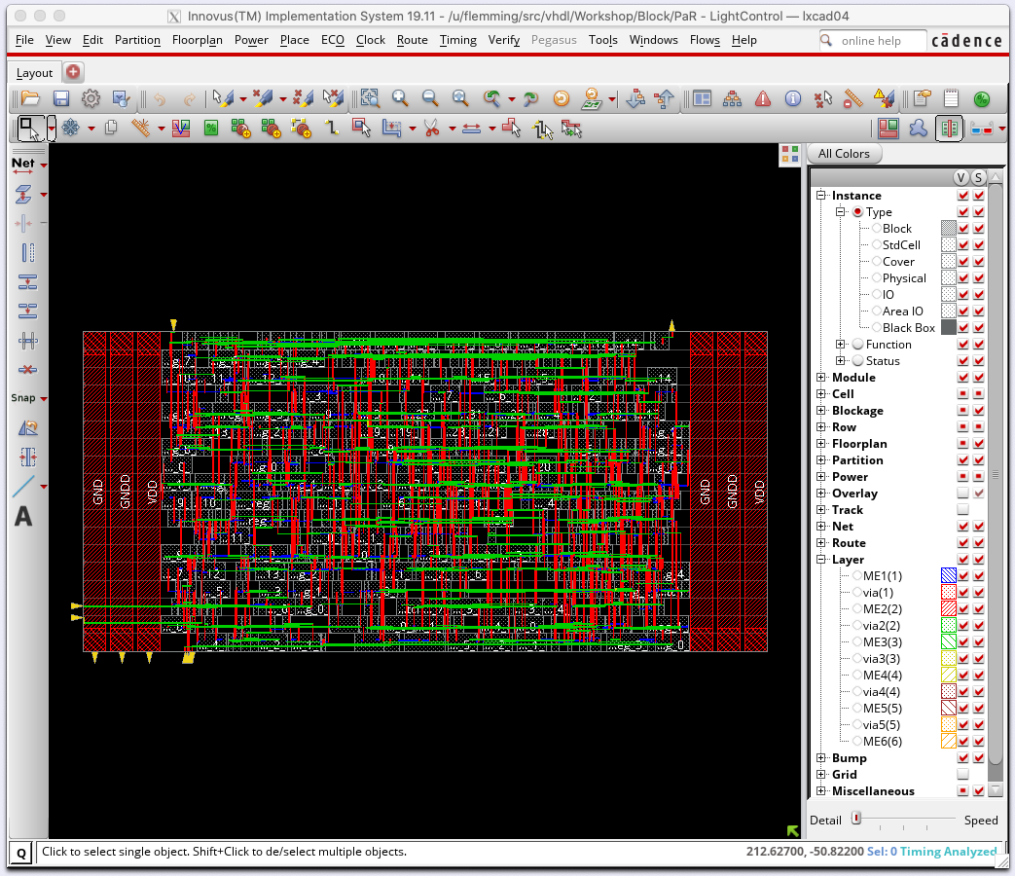
- Final signal routing
- Optimisation for timing, signal integrity, power consumption

Timing Verification

- STA in all phases of physical implementation
- Increasing effort in parasitic extraction from trail route to final layout
- Optimisation by cell movement, buffer insertion, cell resizing

Digital ASIC-Design

Physical Implementation

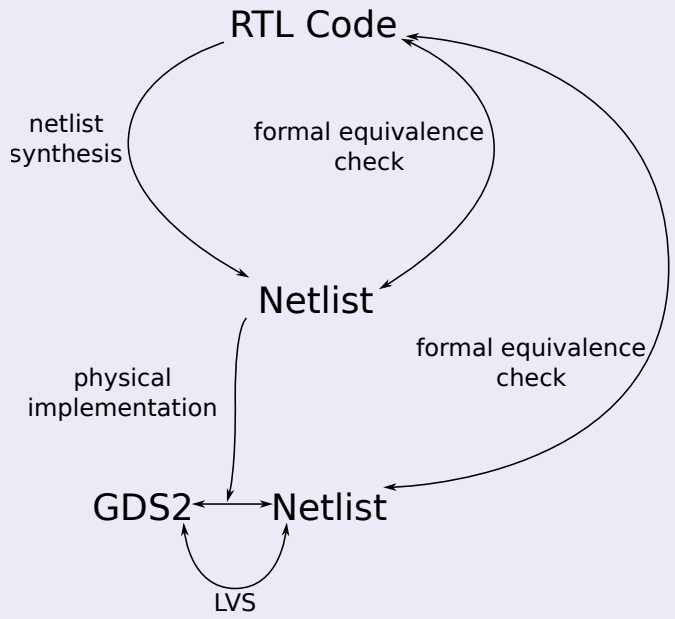


Digital ASIC-Design

Verification

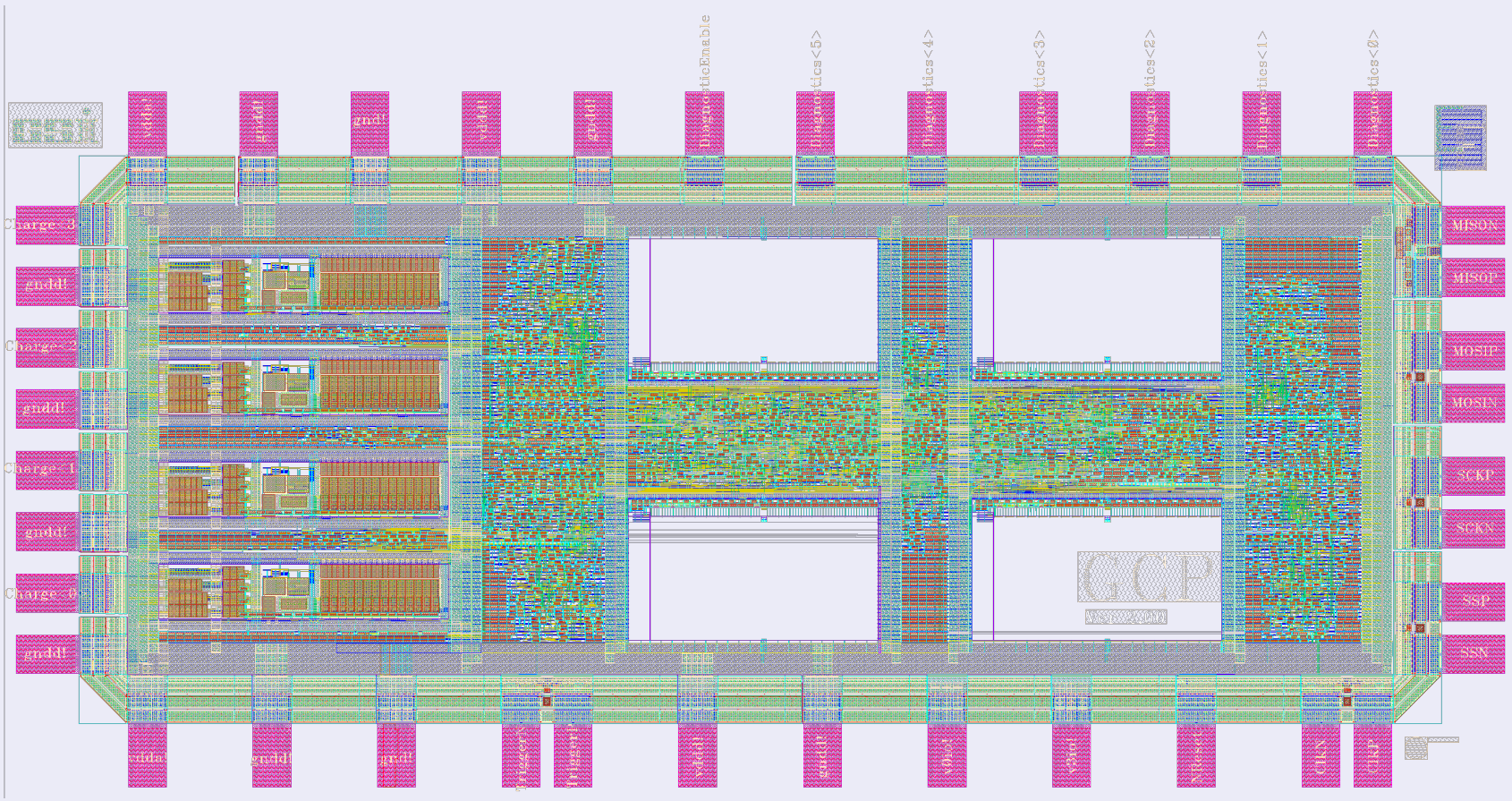
- Checking design correctness
  - Netlist export from physical implementation tool
  - Formal equivalence check between RTL code and netlist
  - LVS check between layout and netlist
- STA on high effort parasitic extraction, e.g. 3D- field solver
- *IR*-voltage drop and electromigration analysis

Verification



Full Custom Analogue ASIC-Design

Final Layout



Thank You

Ng, C.H. et al.: *MIM capacitor integration for mixed-signal/RF applications*. IEEE Trans. Electron Dev., *vol. 52*(2005)(7), pp. 1399