MIMOSIS and Jitter
Feedback from tests and simulations

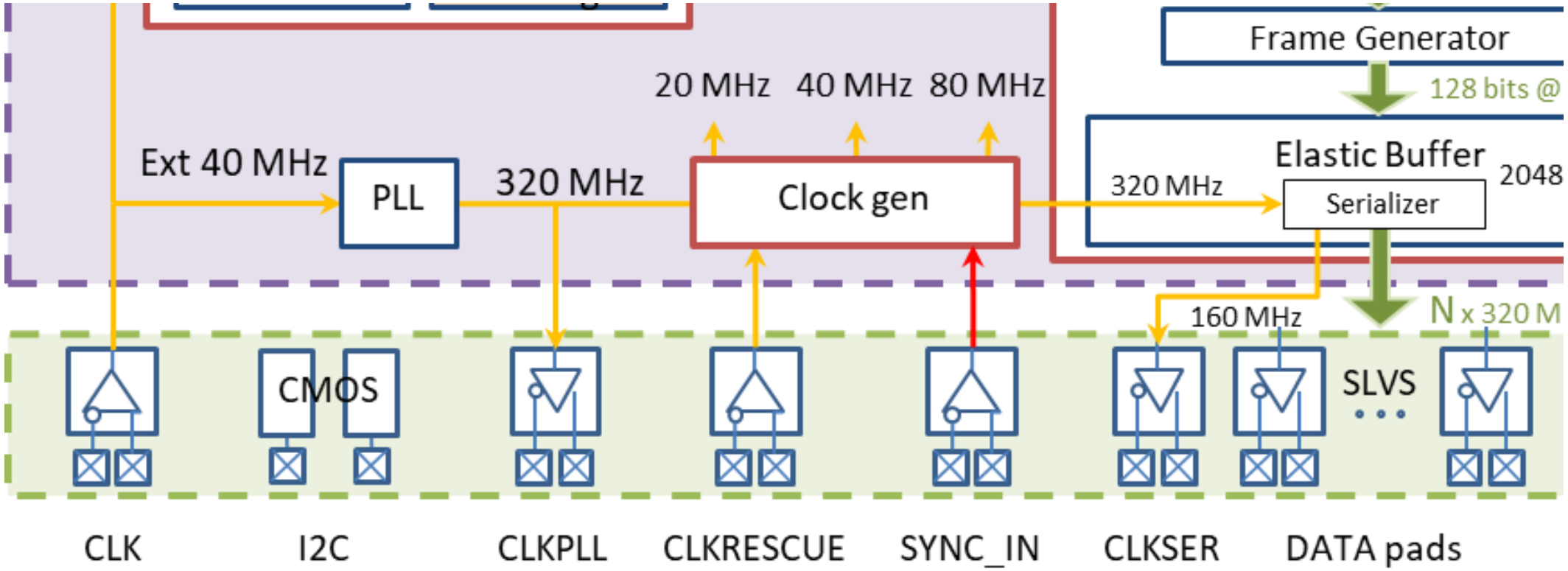
On behalf of the C4PI design team

Outline

- PLL jitter issue (Test vs simulation)
- PLL locking time (Test vs simulation)
- PLL improvements
- Conclusion

Clocks generation

- 320 MHz clock generated by a PLL from 40 MHz output clock (also use for slow control)
  - CLKRESCUE is available to bypass the PLL
- All other clocks are derived from the PLL output



MIMOSIS-PLL

- A Charge-pump PLL
- VCO implementation: Ring oscillator
- Integrated voltage regulator (LDO) for VCO
- Integrated Lock detection circuitry
- Divider with Triple Modular Redundancy (TMR) implementation
- Single power supply: analog power domain (1.8V)

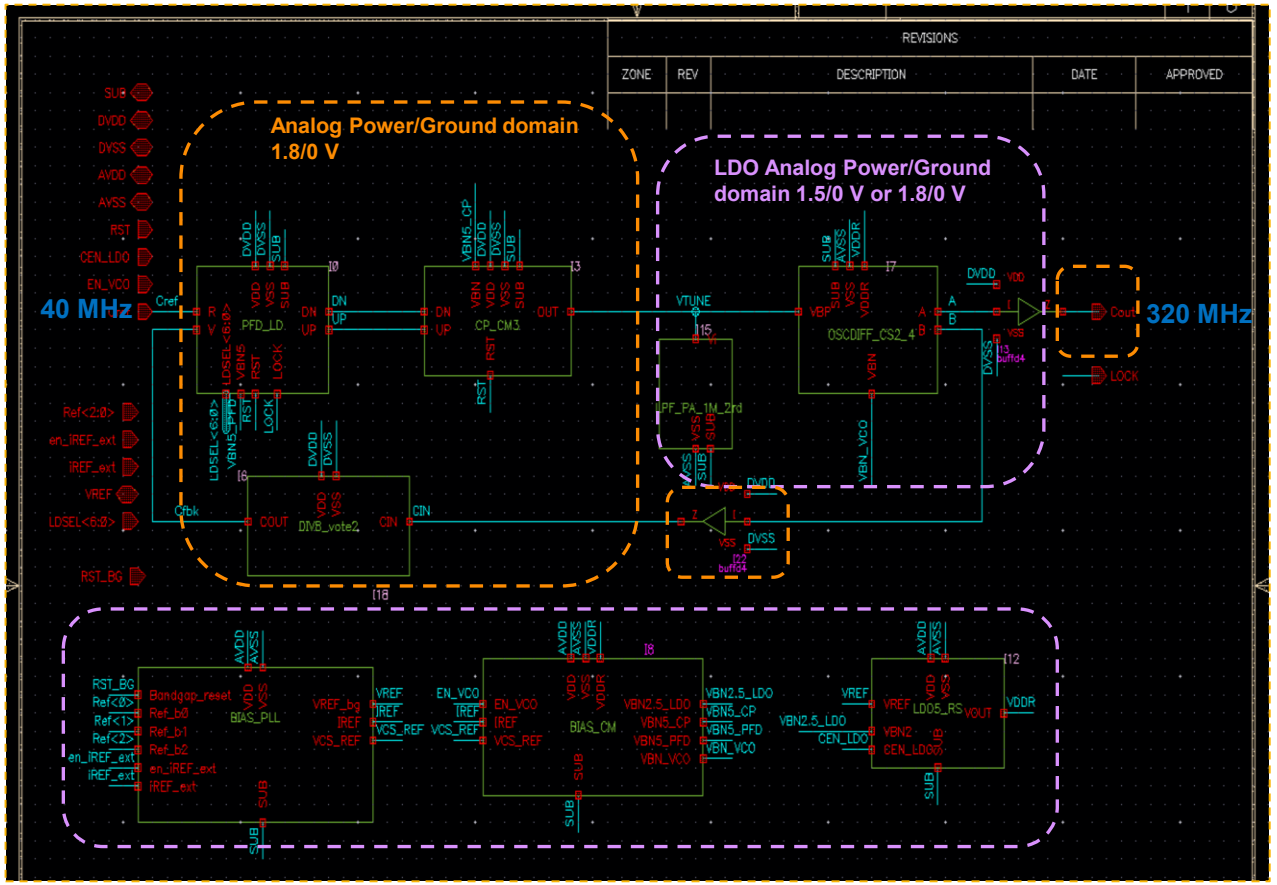
⇒ Post-layout simulation at nominal condition

AVDD = 1.8 V, DVDD = 1.8 V, T = 27°C, Nominal corner

⇒ PLL measurements

(cf MIMOSIS21_PLL_PRELIMINARY_TESTS_251117_1030)

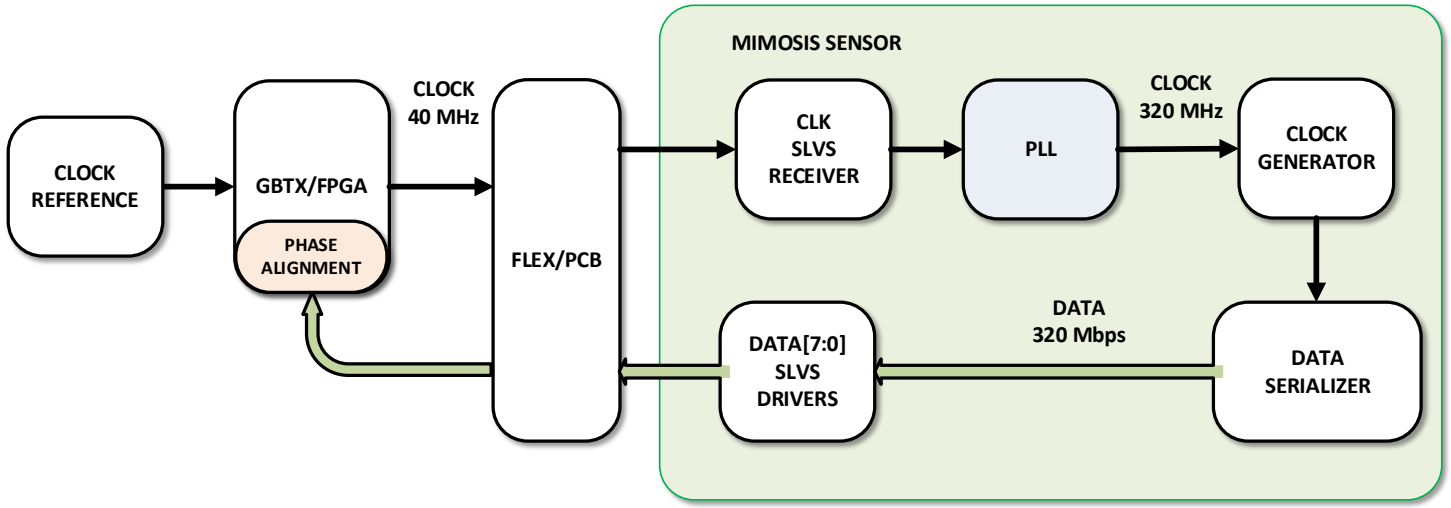
Block diagram



Designed by Yue Zhao
(PhD, 2021)

Detector System clocking scheme

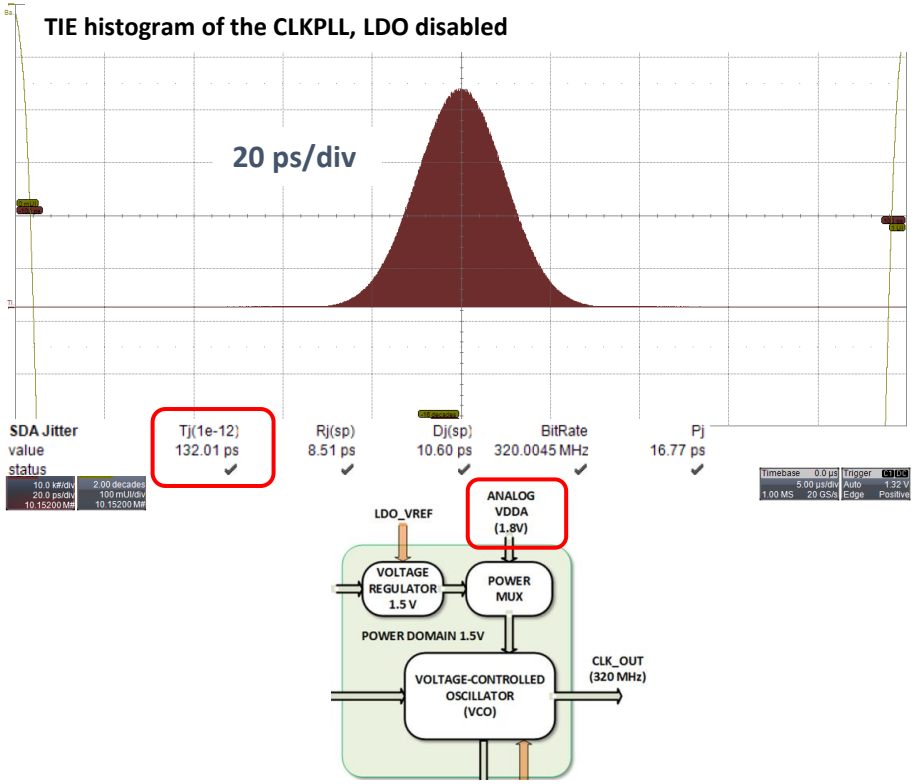
- Common clock scheme:
  - Serial Data from the sensor is synchronized with clock signal provided by the Front-end readout chip (GBTX, FPGA,…)
  - No return clock signal required
  - Phase alignment of Serial Data carried out in Front-end readout chip



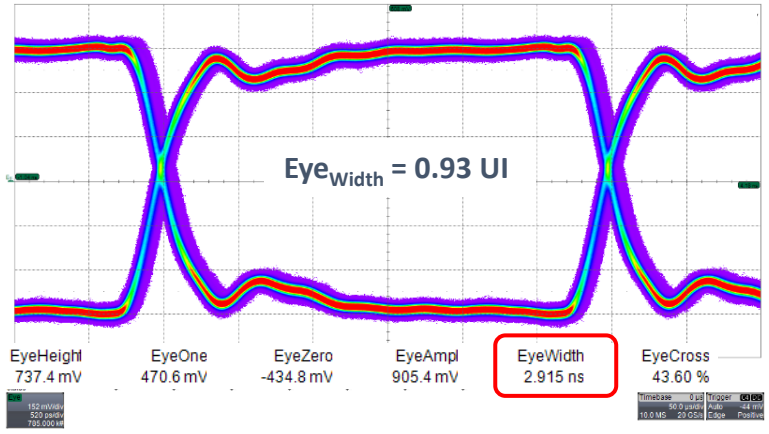
PLL Core Jitter Performance

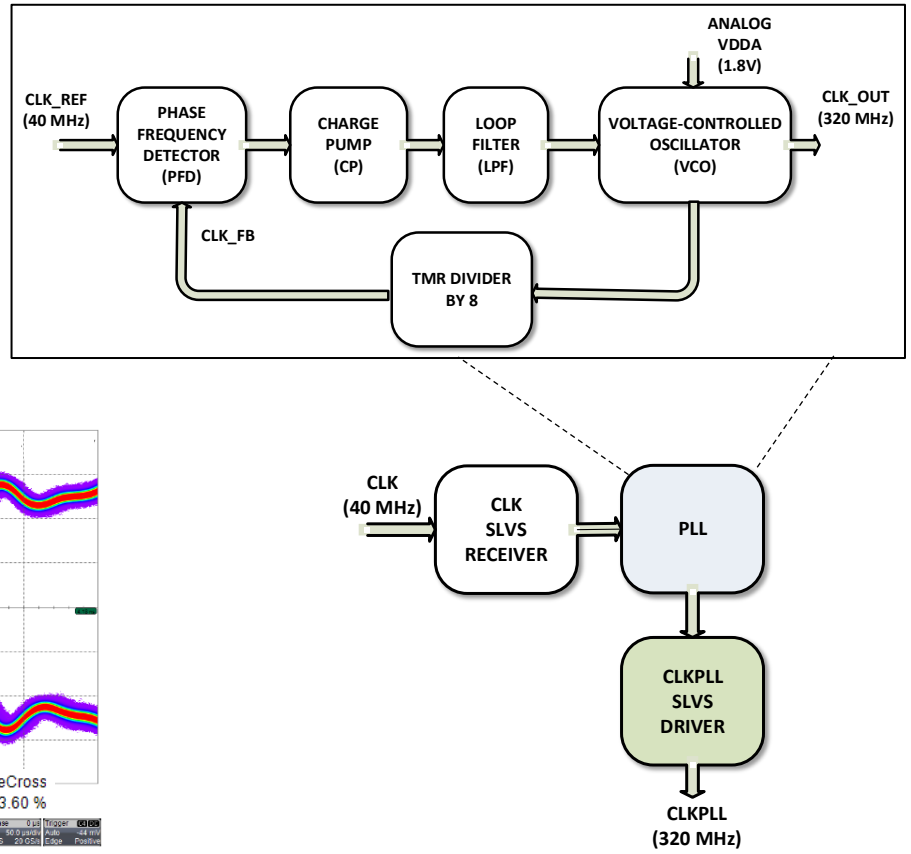
- PLL core consists of five essential building blocks of the PLL: Phase Frequency Detector (PFD), Charge Pump (CP), Loop filter (LPF), Voltage-controller Oscillator (VCO) and Divider
- Jitter Measurement with CLKPLL output
- PLL Core design is operational and fulfills the requirements in low power supply noise conditions
  - LDO disabled, pixel matrix steering and readout not started

TIE histogram of the CLKPLL, LDO disabled



Eye diagram DATA[0] LVDS buffer output,
Data Pattern: ([0xAAAA] x 8),
Clock period: 3.125 ns (320 MHz), LDO disabled

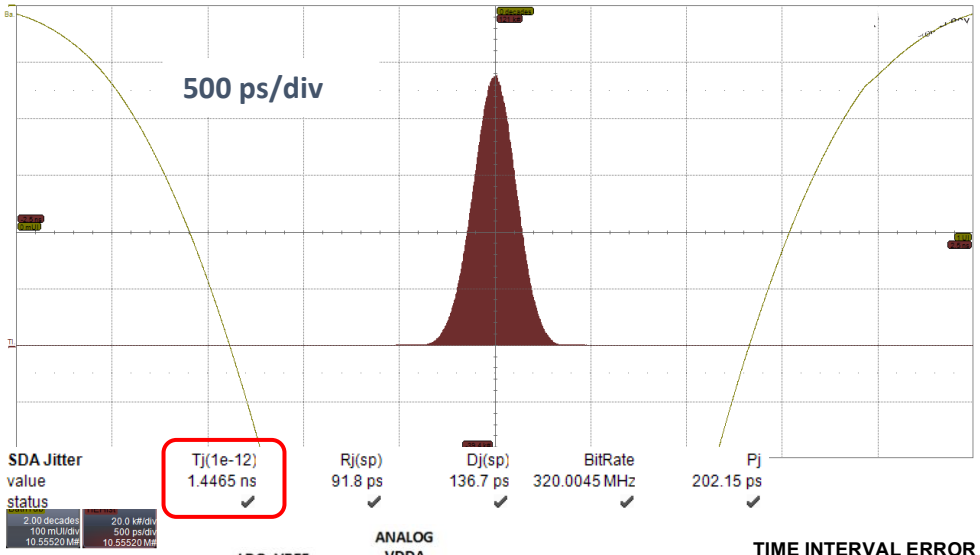




Issue 1: Integrated LDO

- Main task of LDO: To provide a stable and a low-noise power-supply (1.5V) for the VCO
- Problem: Power-supply noise reduction performance of the LDO is inadequate (LDO output unstable)
- LDO cannot be tested directly (no access to LDO output)

TIE histogram of the CLKPLL, LDO enabled



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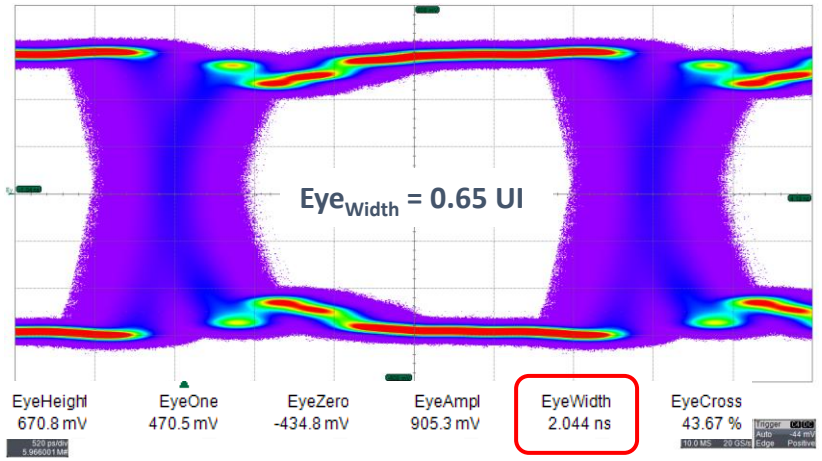
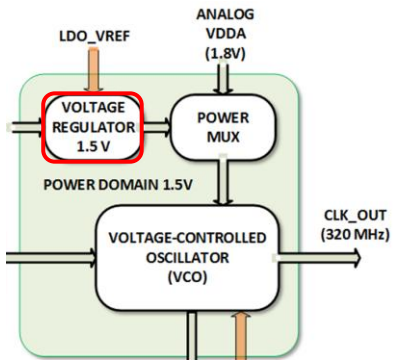
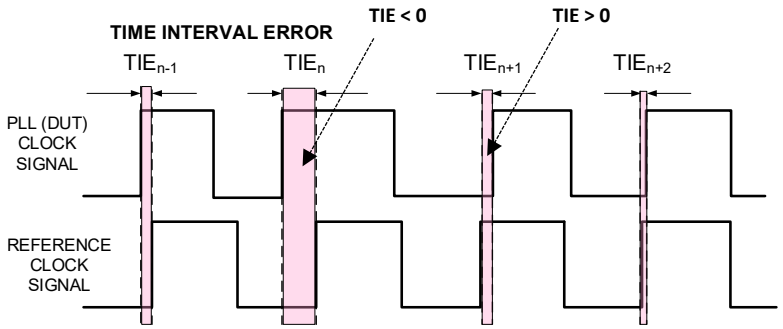
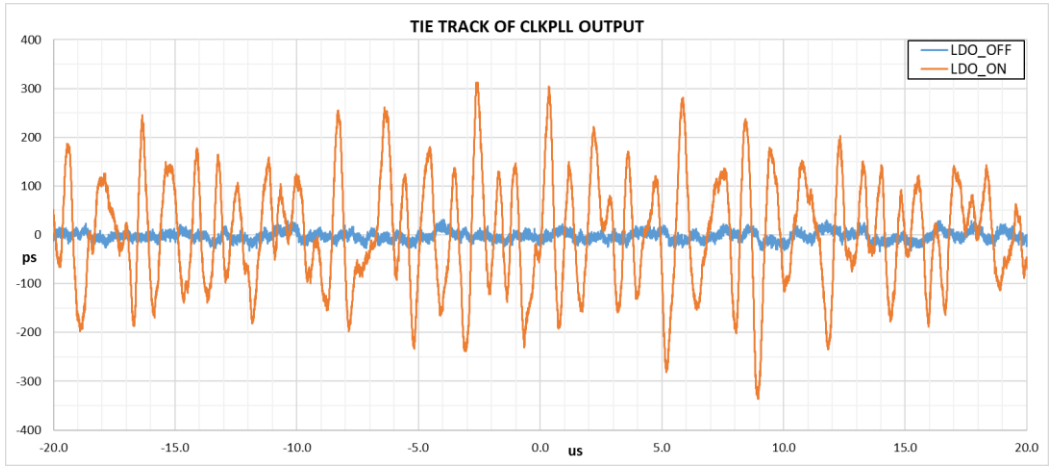






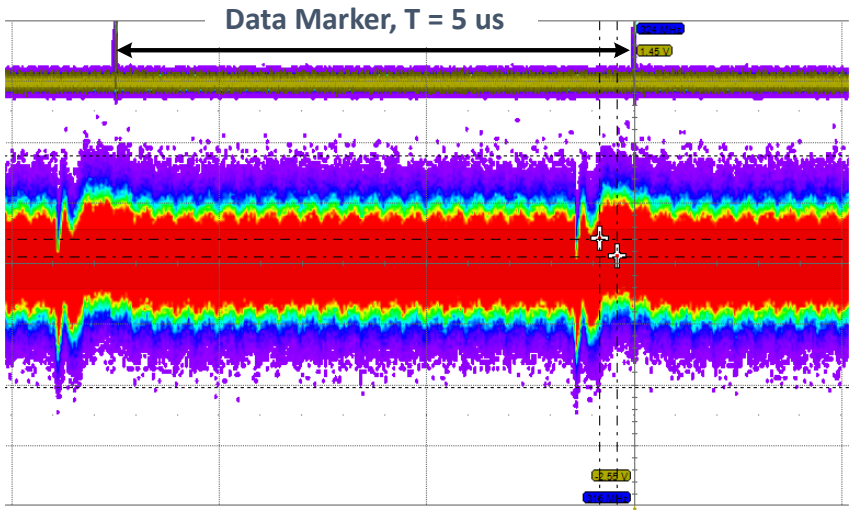
TIE = Measured Arrival Time – Expected Arrival Time



Issue 2: Sequencer block driven digital activity increases jitter in PLL

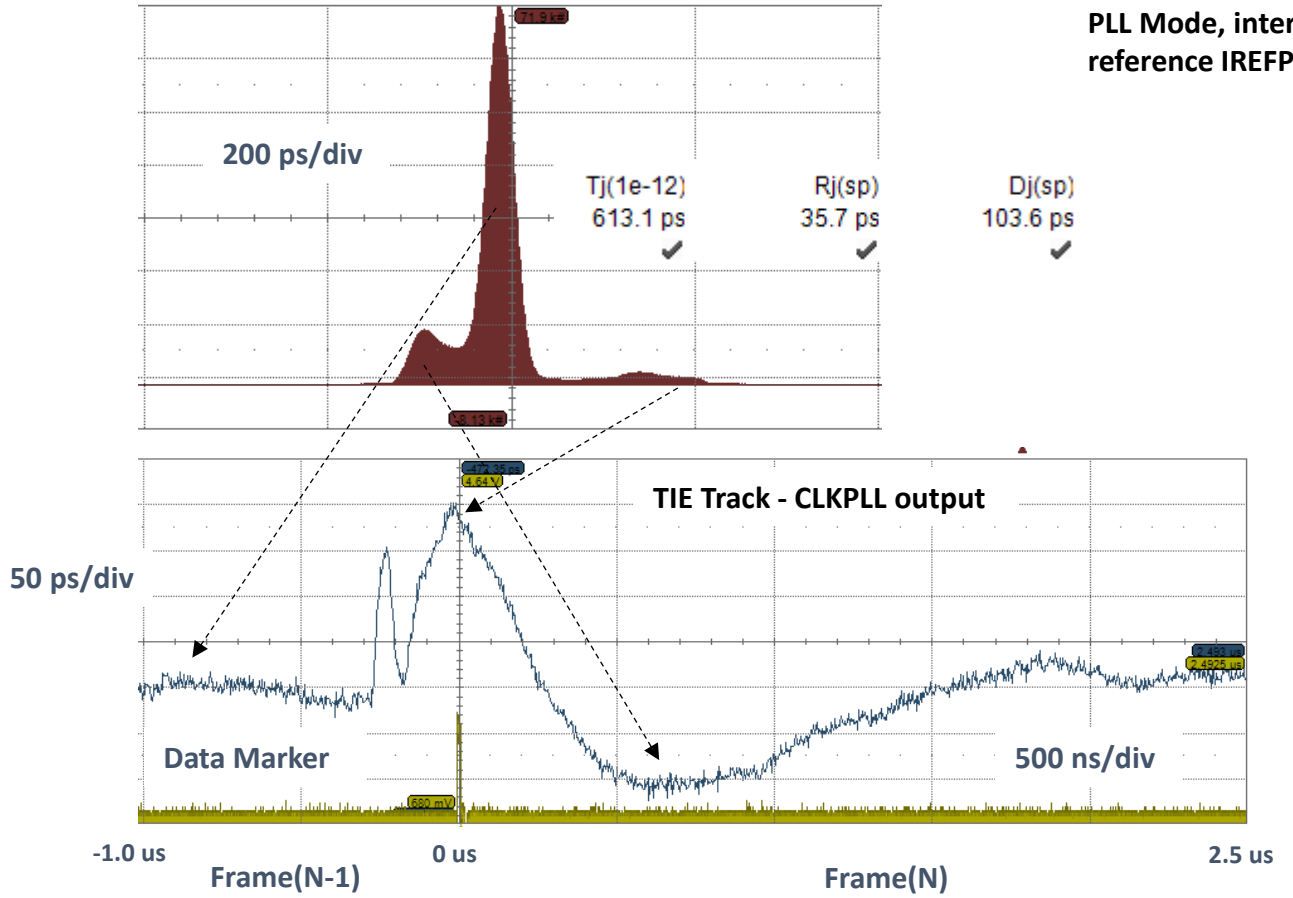
- Without LDO, the Sequencer driven digital activity results in a increase of jitter in PLL block
- The noise injection is concentrated at the end/start phase of the pixel frame readout ($T_{Frame\_Readout}$ = 5 us)

CLKPLL output - Instantaneous clock frequency-tracking plot in persistence mode



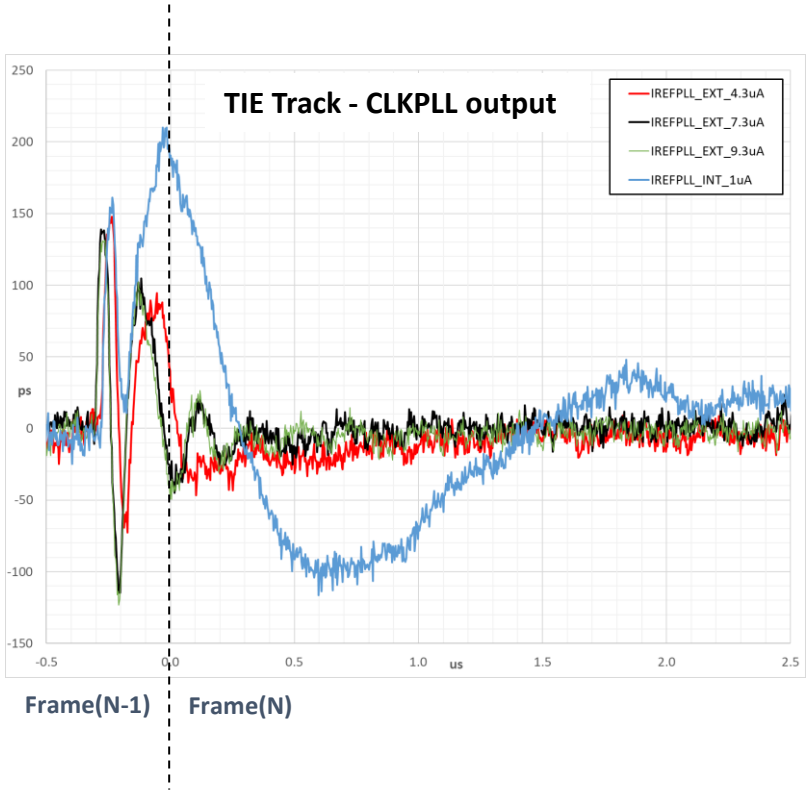
TIE Histogram - CLKPLL output

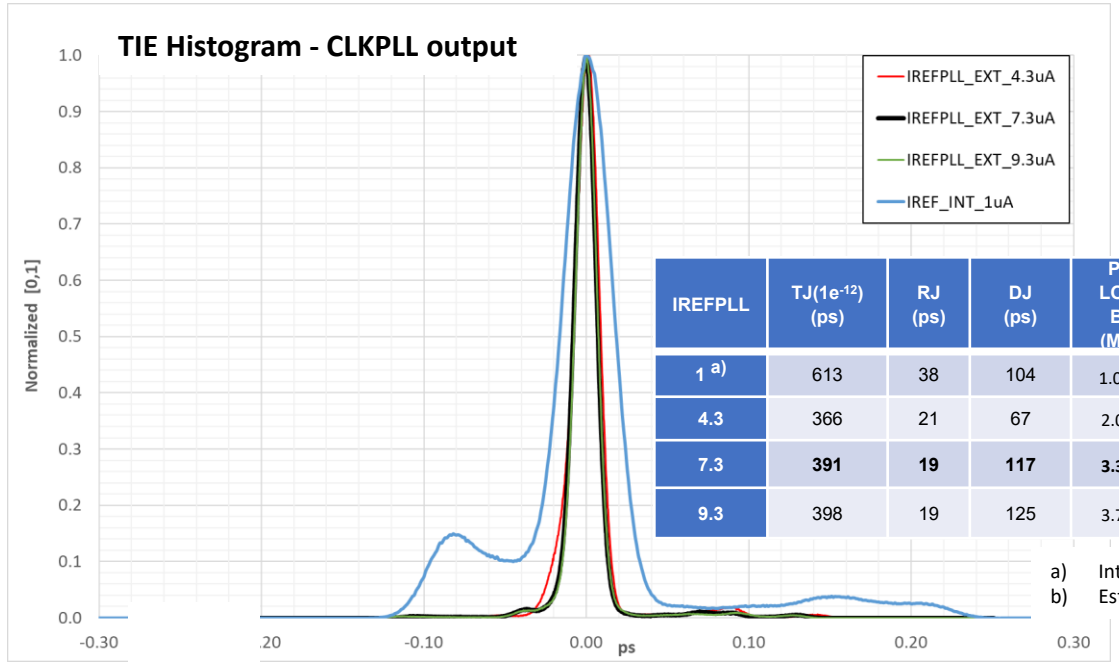
PLL Mode, internal current reference IREFPLL = 1 uA



A Temporary Solution to mitigate the PLL jitter issue

- LDO is disabled!
- Due to use of external reference current (IREFPLL_EXT), the reactivity of the PLL loop (BW) can be adapted
- IREFPLL reference current increased from 1 uA to 7.3 uA to obtain required operation mode
  - Drawback: PLL loop bandwidth increased -> PLL is more sensible for the reference clock jitter





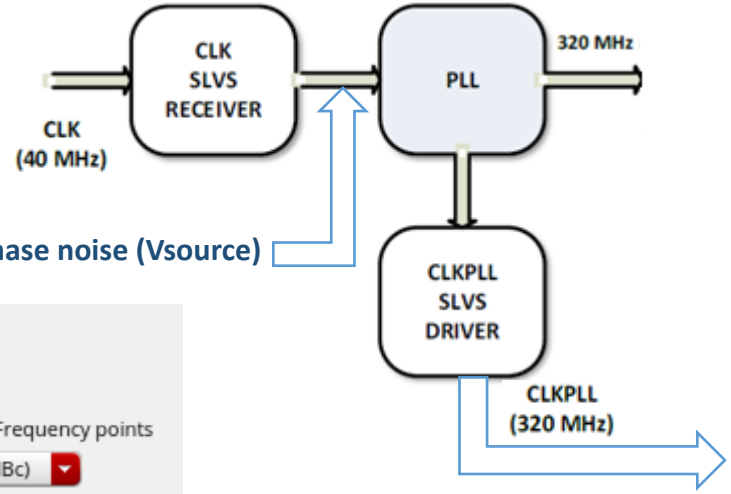
IREFPLL	TJ(1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PLL LOOP BW (MHz)
1 [a]	613	38	104	1.04 [b]
4.3	366	21	67	2.06 [b]
7.3	**391**	**19**	**117**	**3.34** [b]
9.3	398	19	125	3.70 [b]

a) Internal current reference
b) Estimation

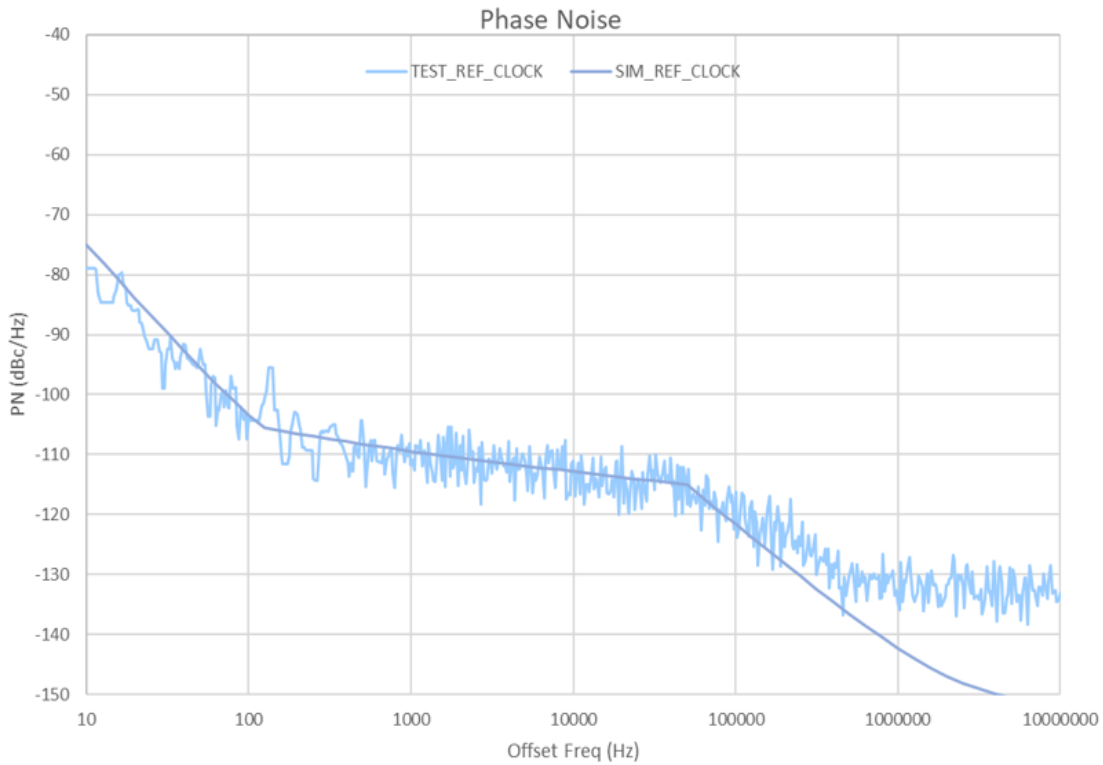
PLL jitter issue

- Test vs simulation: ClkPLL jitter performance versus input clock with additional random jitter

⇒ Noise signal of ($RJ_{rms} = 6.4\ ps$) is added to the input CLK



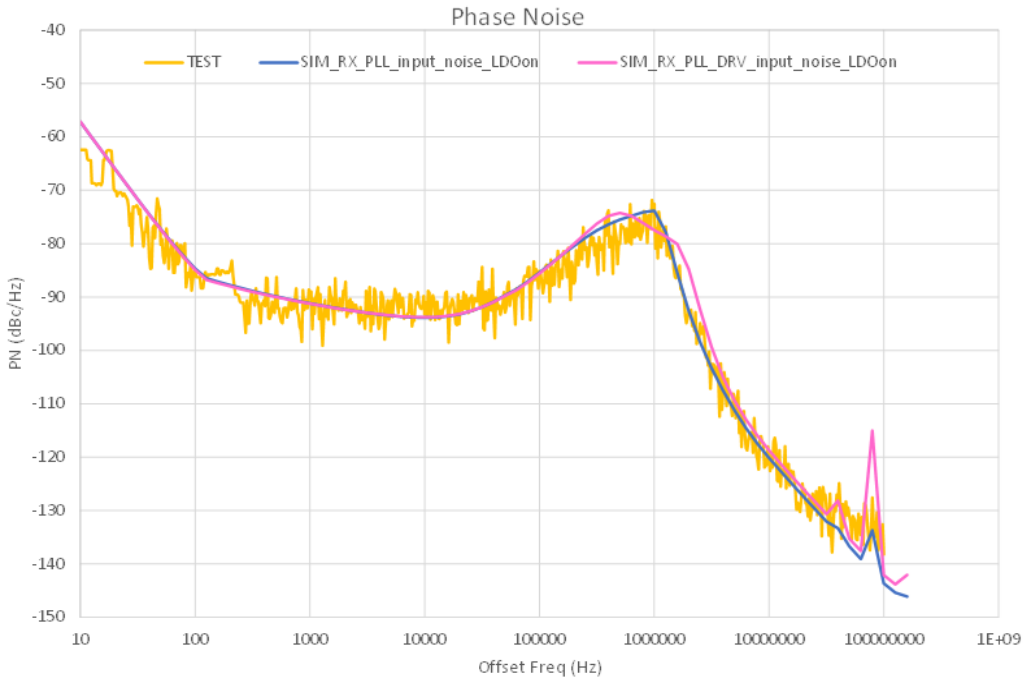
Display noise parameters	☑
Generate noise?	yes
Noise Entry Method	○ File ● Noise/Frequency points
Noise type	Edge Phase Noise(dBc)
Num. of noise/freq pairs	4
Freq 1	10
Noise 1	-75
Freq 2	120
Noise 2	-107
Freq 3	50K
Noise 3	-115
Freq 4	500K
Noise 4	-137



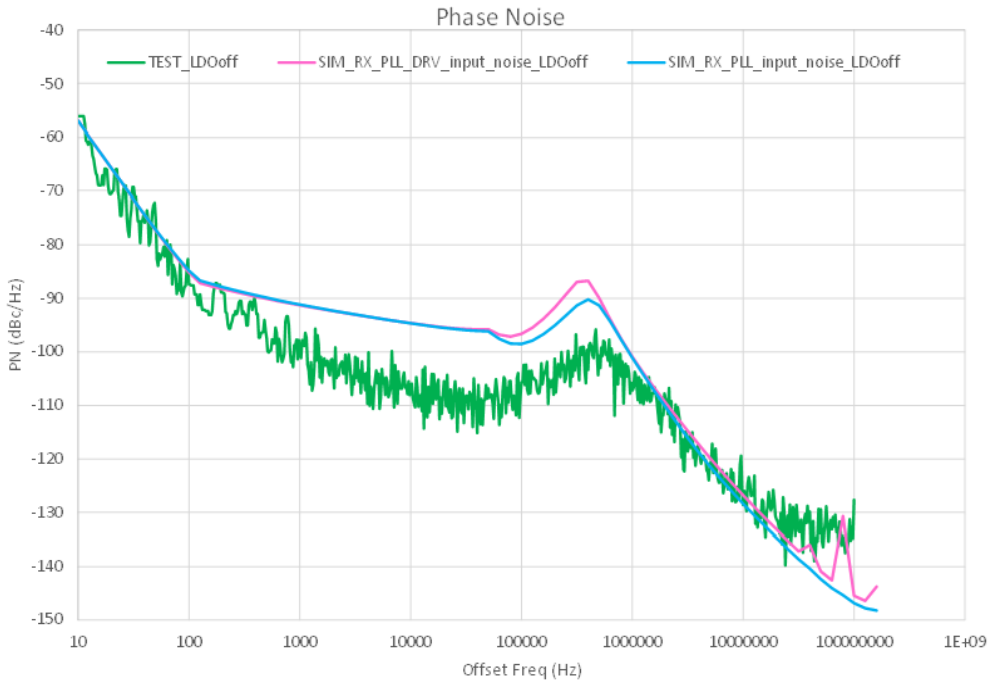
Input Clk noise signal (Test vs simulation)

PLL jitter issue

- Test vs simulation: ClkPLL jitter performance versus input clock with additional random jitter



ClkPLL noise signal (Test vs post-simulation): **LDO_ON**



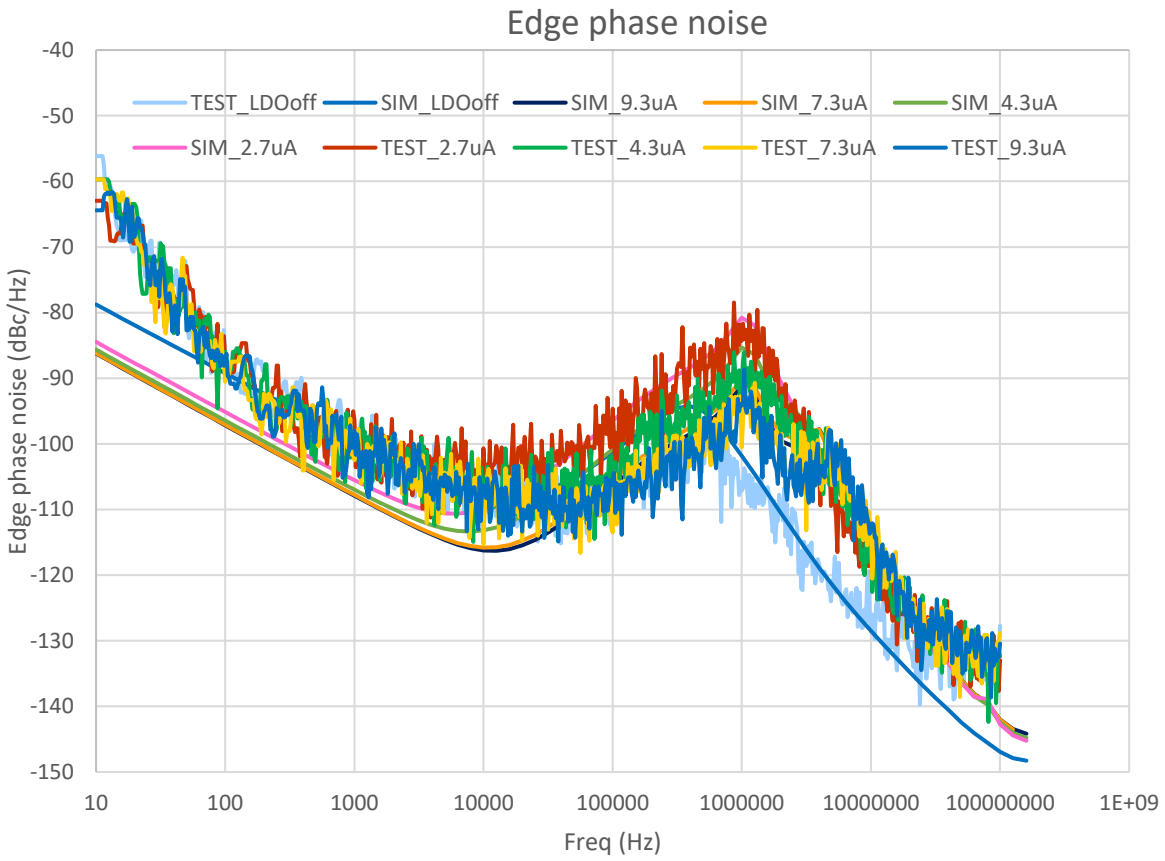
ClkPLL noise signal (Test vs post-simulation): **LDO_OFF**

- LDO_ON => Good correspondence between test and post-simulation results
- LDO_OFF => Low noise level ($100Hz\ to\ 1MHz => \Delta RJ_{max} = 15\ dB$)

Pnoise results RX_PLL_DRV		
Configuration	**RJ_rms (ps)/ Test**	**RJ_rms (ps)/ Post-simulation**
LDO_ON	110.7	130
LDO_OFF	7.2	19.5

PLL jitter issue

- Test vs simulation: ClkPLL jitter performance versus external Iref_ext bias current



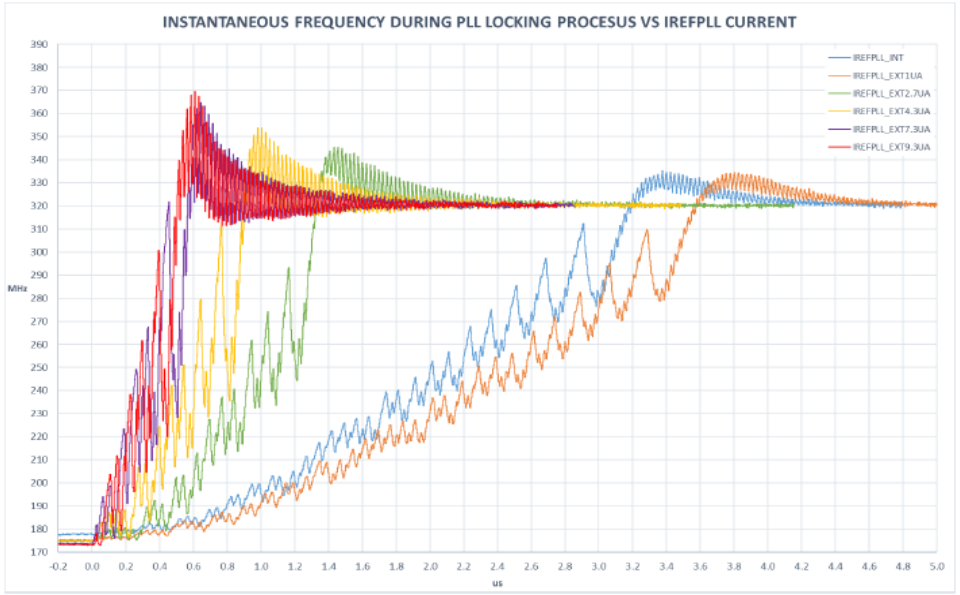
PNoise simulation results / LDO ON / PLL_V3		
Iref_ext (uA)	TEST	SIM
2.7	57	60.09
4.3	33	38.83
7.3	19	25.42
9.2	19	23.43

- Correlation between test & simulation results
- Increasing external bias current => Lower ClkPLL jitter

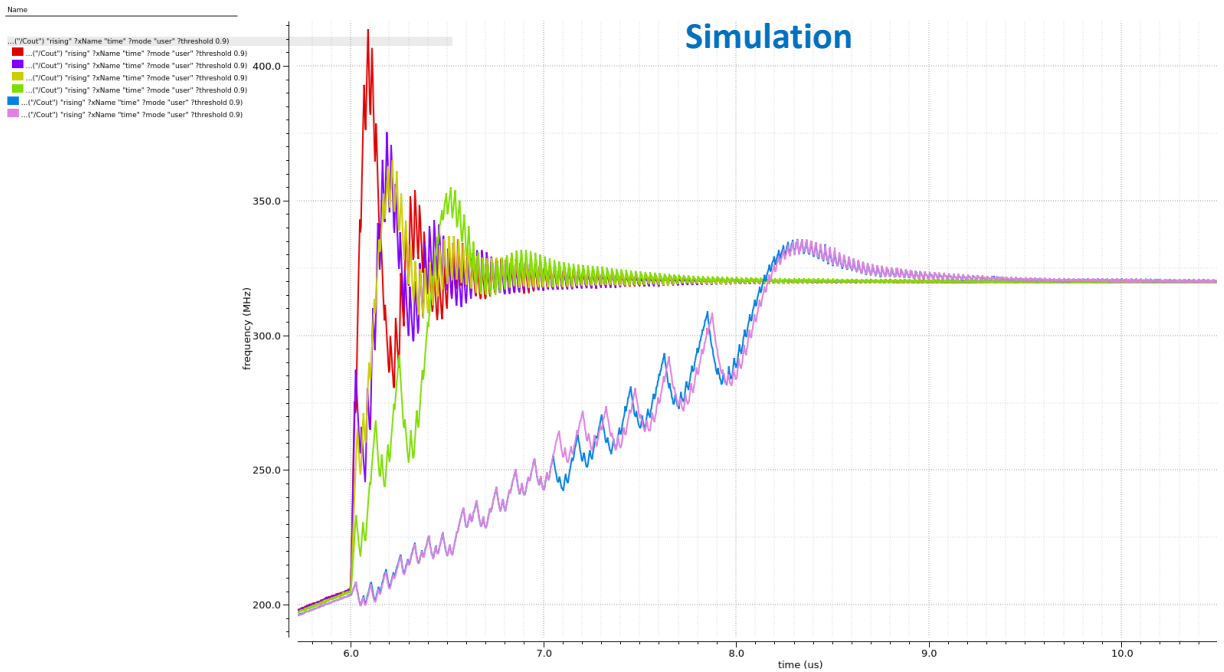
PLL locking time

- Test vs simulation

Test



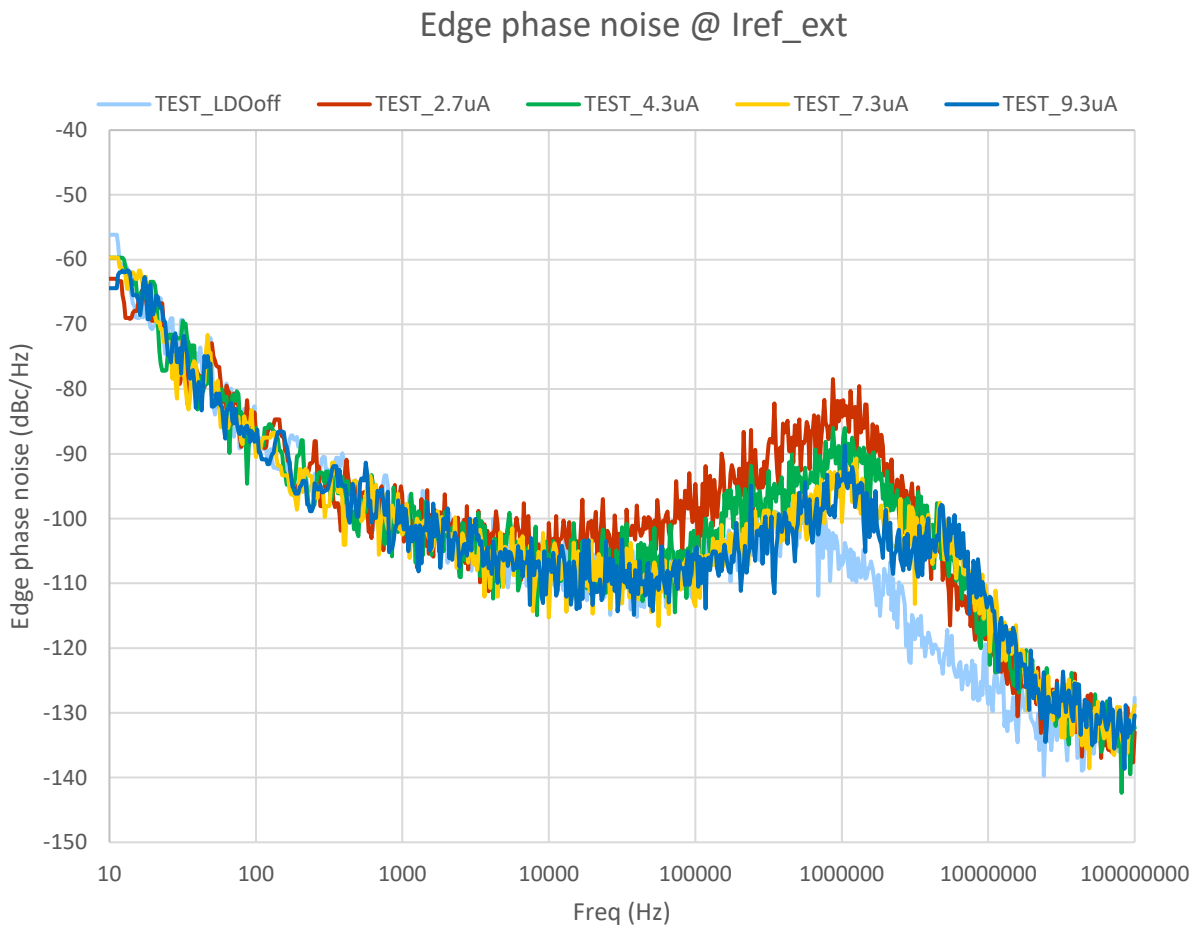
Simulation



Current mode	Iref (uA)	Measured locking time (us)	Simulated locking time (us)
int	-	4.6	5.1
ext	1	4.9	5.2
ext	2.7	3.5	3.25
ext	4.3	2.8	2.83
ext	7.3	2.7	2.5
ext	9.3	2.6	2.4

PLL improvements

- Increase biasing current: IVBAN, ICP?

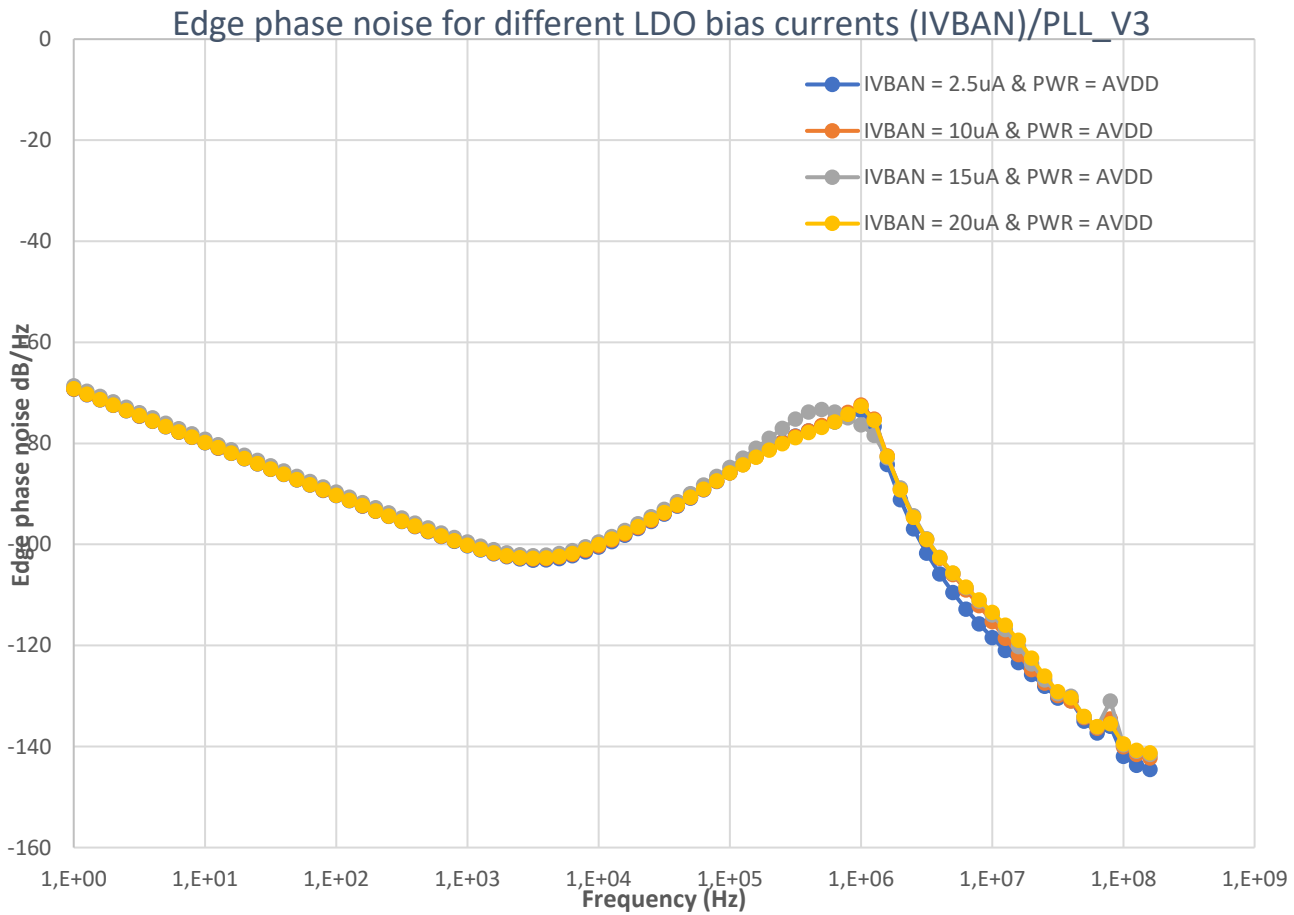


- Increasing external bias current => Lower ClkPLL jitter
  - Increasing Iref_ext = increasing biasing currents in LDO and CP

Iref_ext (uA)	LDO/IVBAN (uA)	CP/ICP (uA)
1	**2.5**	**5**
2.7	6.5	13
4.3	10	20.4
7.3	16	32
9.2	17.75	35.5

PLL improvements

- Increase of LDO bias current (IVBAN)

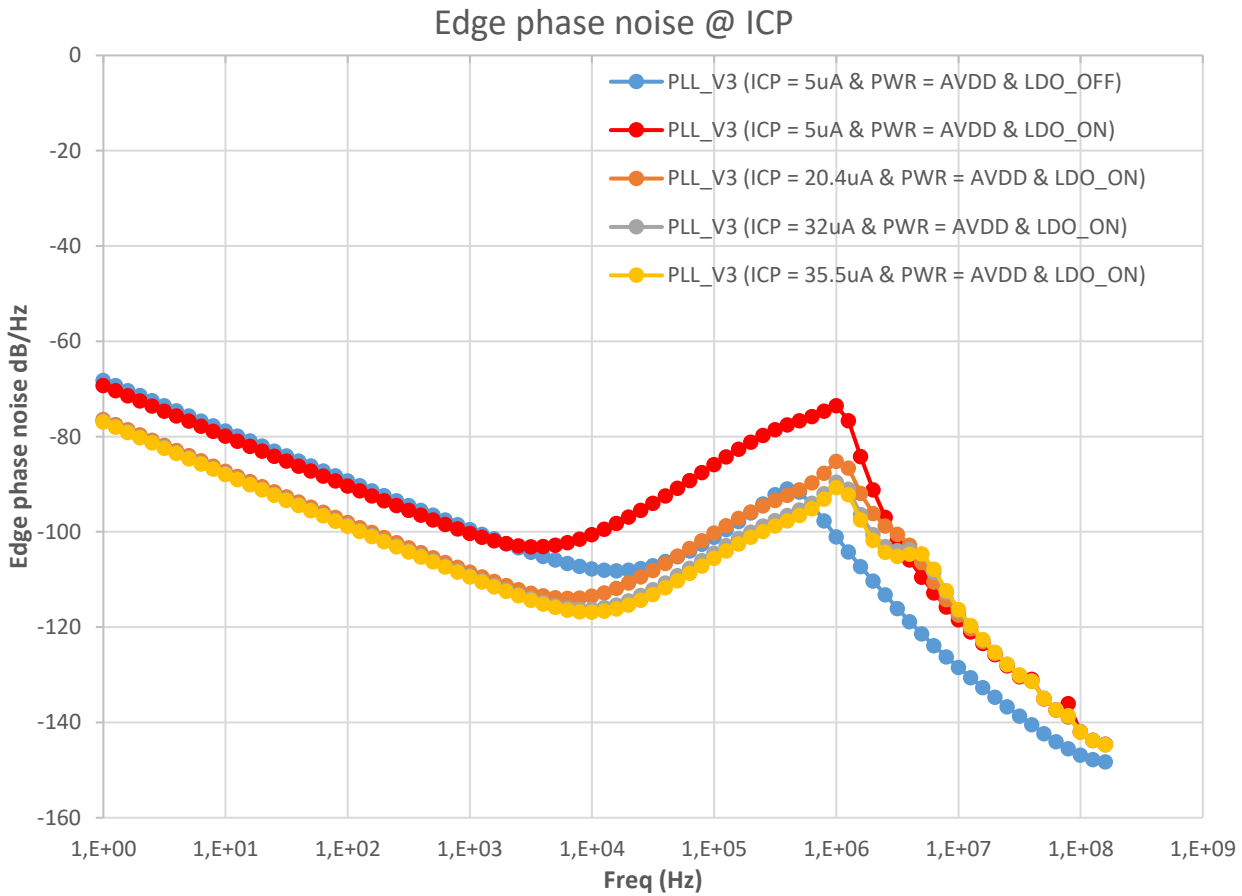


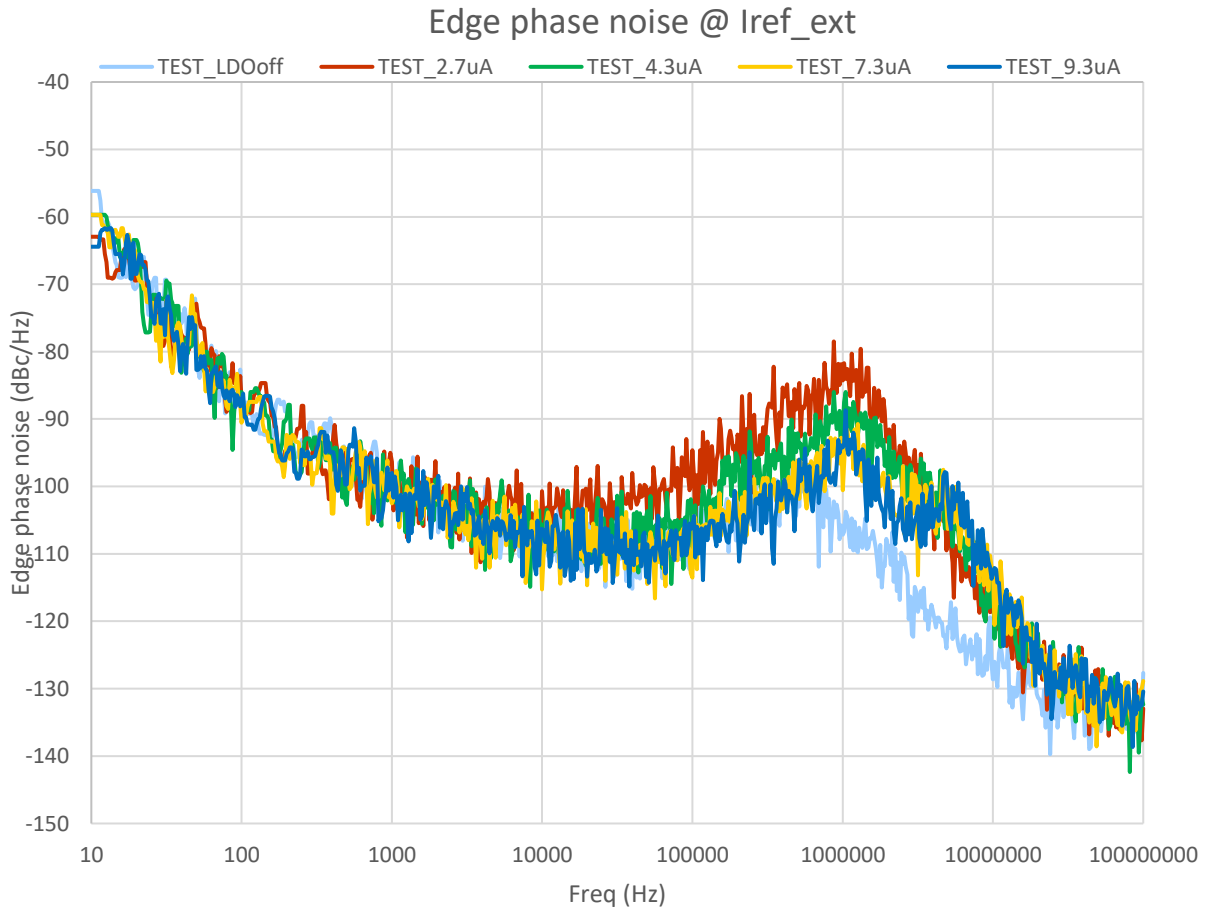
PNoise simulation results / LDO ON / PLL_V3	
IVBAN (uA)	**Random jitter (Jee): RMS (ps)**
2.5	132
10	146
15	138
20	142

LDO bias current increase => ~ No change on PLL noise

PLL improvements

- Increase of CP bias current (ICP)





- Noise in simulation results @ ICP ⇔ Noise in test results @ Iref_ext
- Major contribution of ICP on random jitter

PLL improvements

- PLL noise (Iref_ext vs ICP)

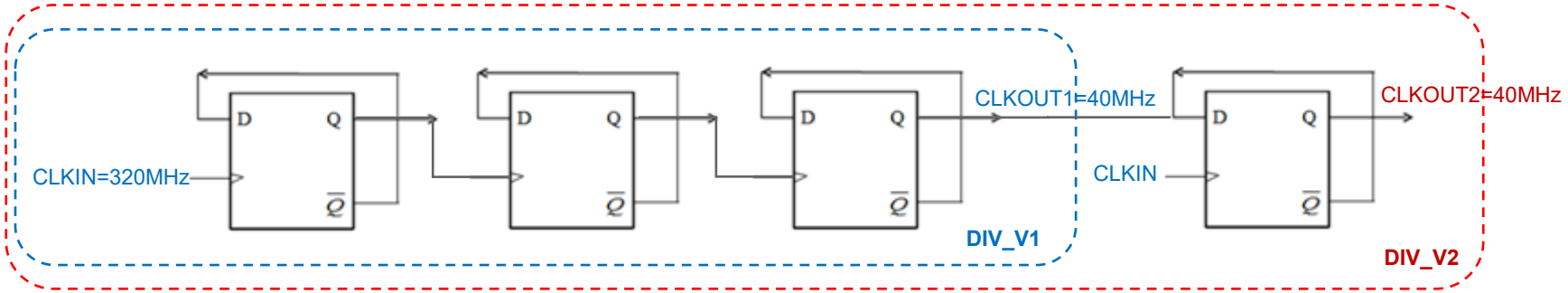
LDO	PLL PNoise test results		PLL PNoise simulation results	
Configuration	**Iref_ext (uA)**	**Random jitter (Jee): RMS (ps)**	**ICP (uA)**	**Random jitter (Jee): RMS (ps)**
OFF	1	8	5	12
ON	1	121	5	132
ON	4.3	33	20.4	36.16
ON	7.3	19	32	22.8
ON	9.2	19	35.5	20.4

- Good correspondence of PLL jitter improvement:
  - Increasing external biasing current
  - Increasing CP biasing current
- Increasing ICP to 20uA => Lower jitter (factor of 3.6)

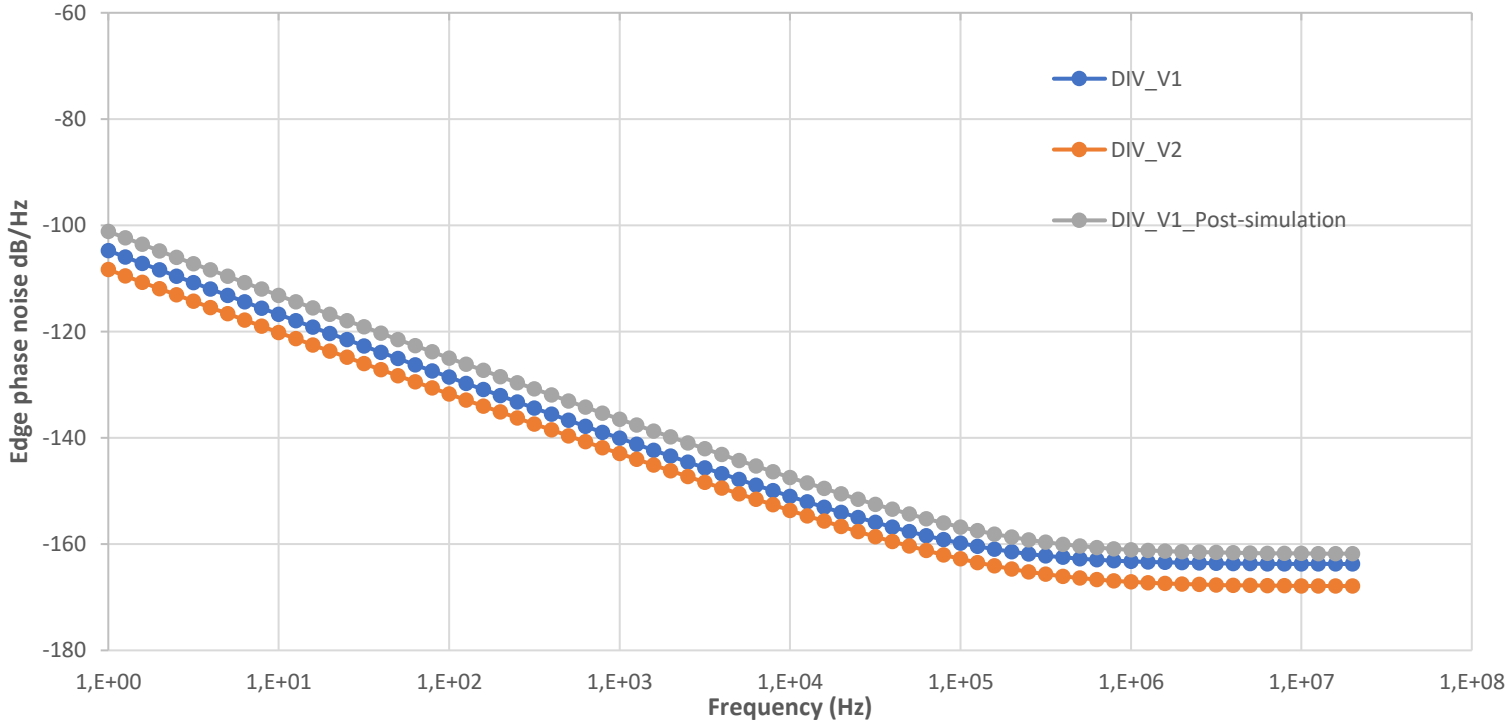
PLL improvements

- Frequency divider (DIV8_vote2)

⇒ Sampling the output stage with the input clock (CLKIN)



Pnoise frequency divider simulation results	
Configuration	**Random jitter: RMS (fs)**
DIV_V1 (Schematic-simu)	22.6
DIV_V1 (Post- simu)	29.84
DIV_V2 (schematic simu)	14.38



- Low jitter of ClkDIV (fs)

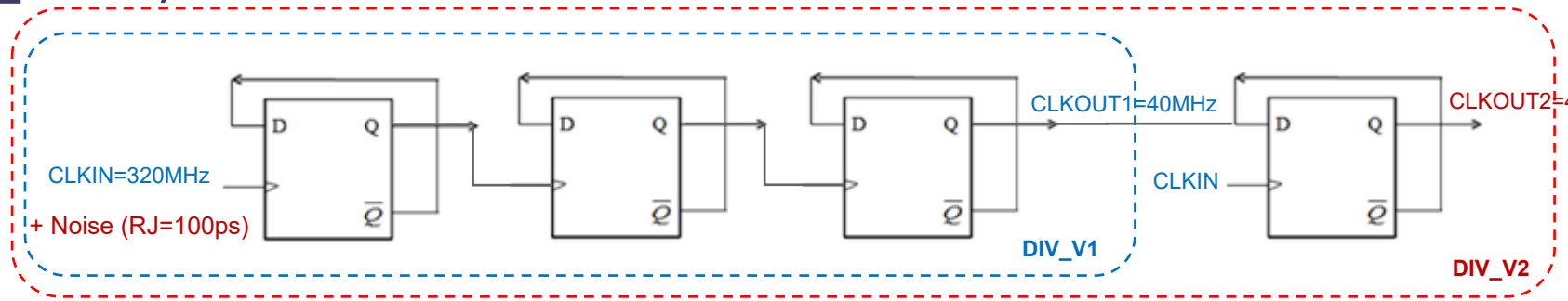
PLL improvements

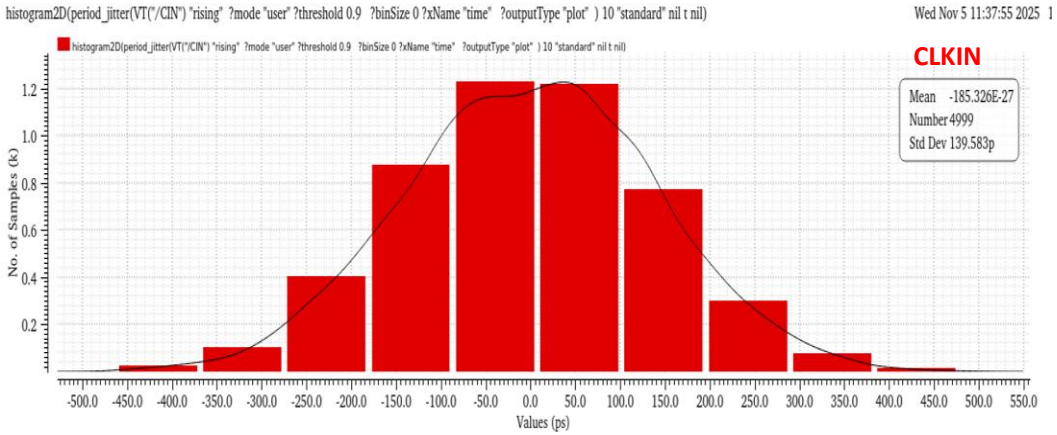
- Frequency divider (DIV8_vote2)

⇒ Sampling the output stage with the input clock (CLKIN)

⇒ **Add a noise on the input CLK** *(vbit with RJ of 100ps)*

⇒ RJ in the time domaine (Std Dev)





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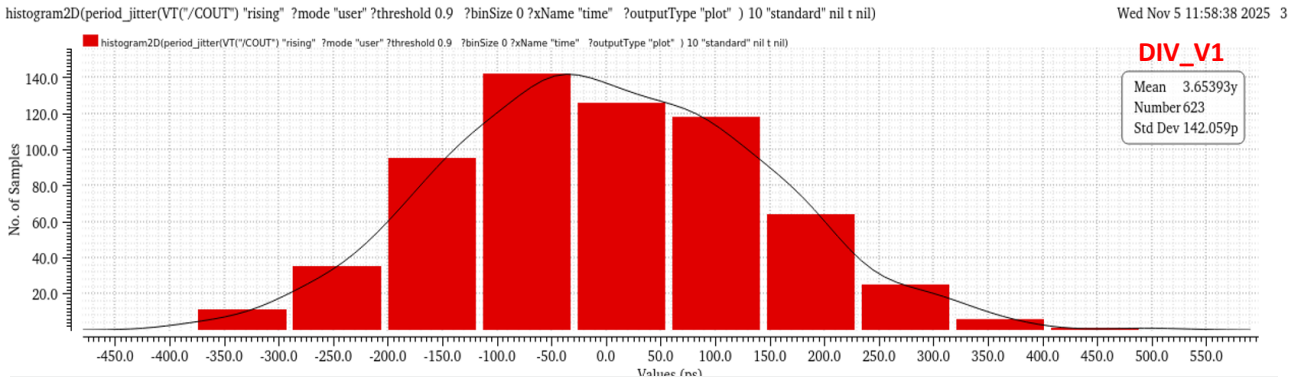
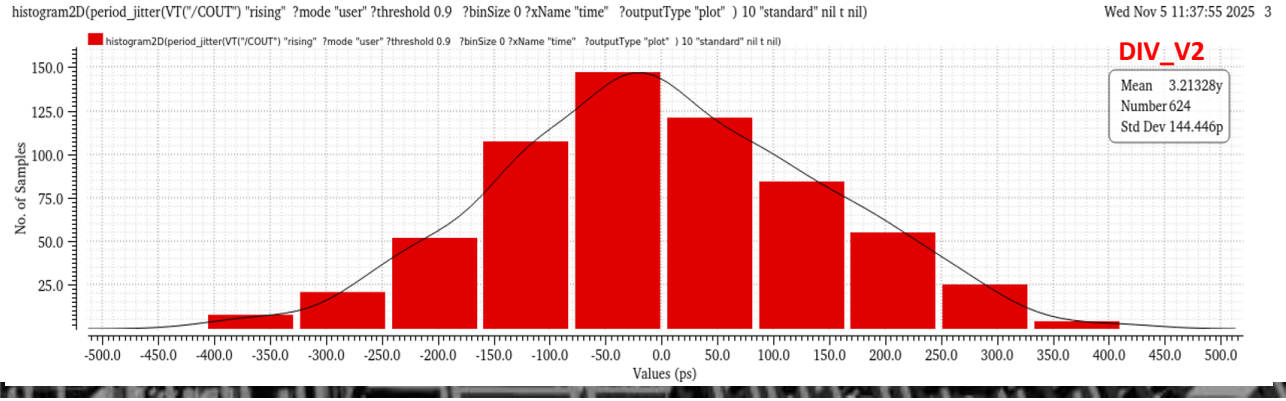
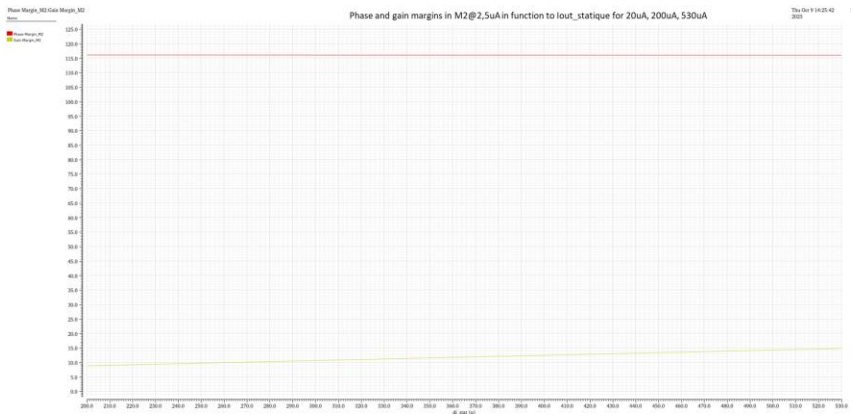


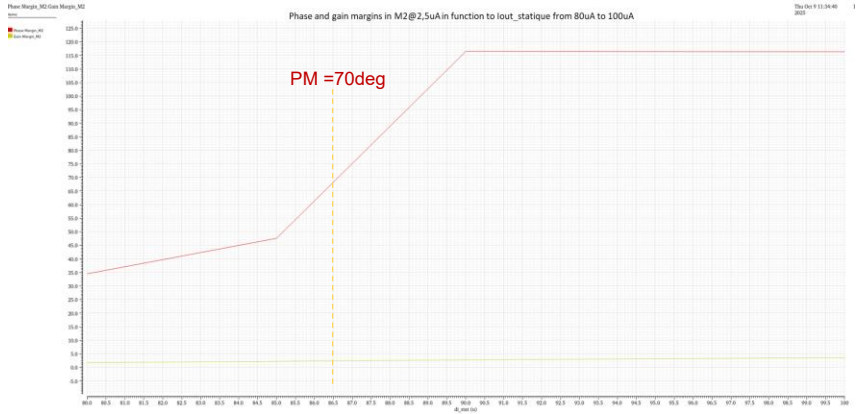


- Low jitter of ClkDIV => Negligable improvement

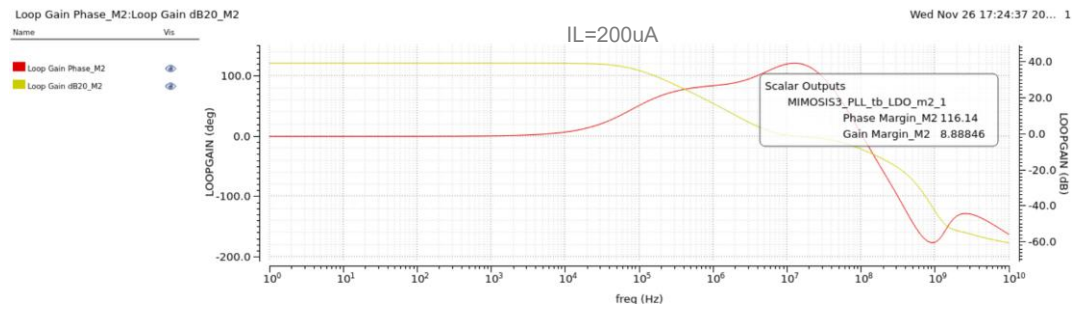
PLL improvements

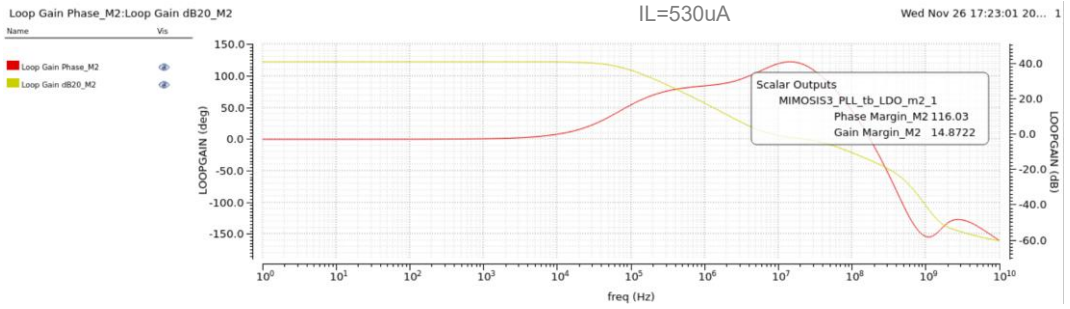
- LDO stability
  - Pre-start: $IL = 20uA$ => system non stable => start to be stable $@IL > 86uA$
  - VCO enabled: $IL = 200uA$ => system stable=> $PM = 116.1deg, GM = 8.8dB$
  - Full load: $IL = 530uA$ => system stable=> $PM = 116deg, GM = 14.8dB$





- Disabled VCO=> Add a load current of 200uA



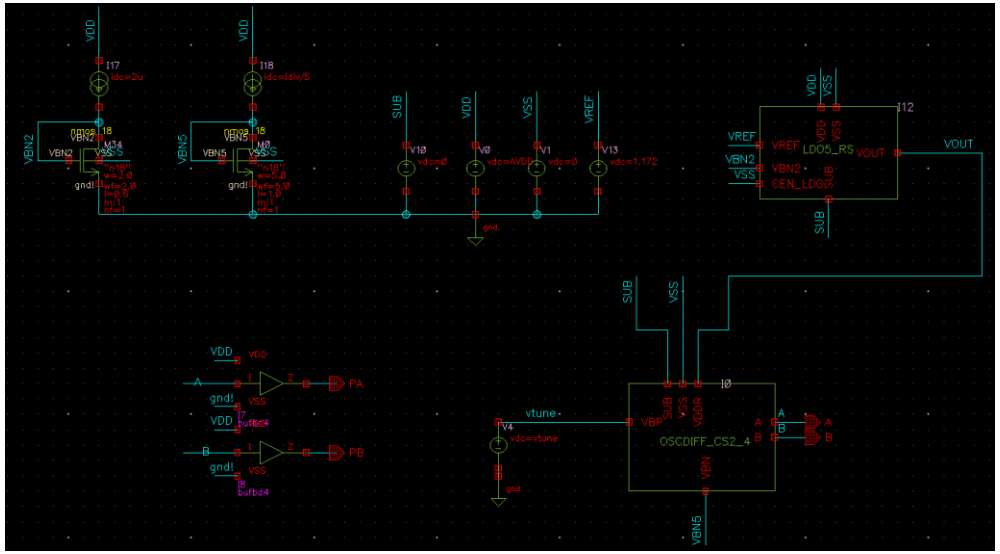


PLL improvements

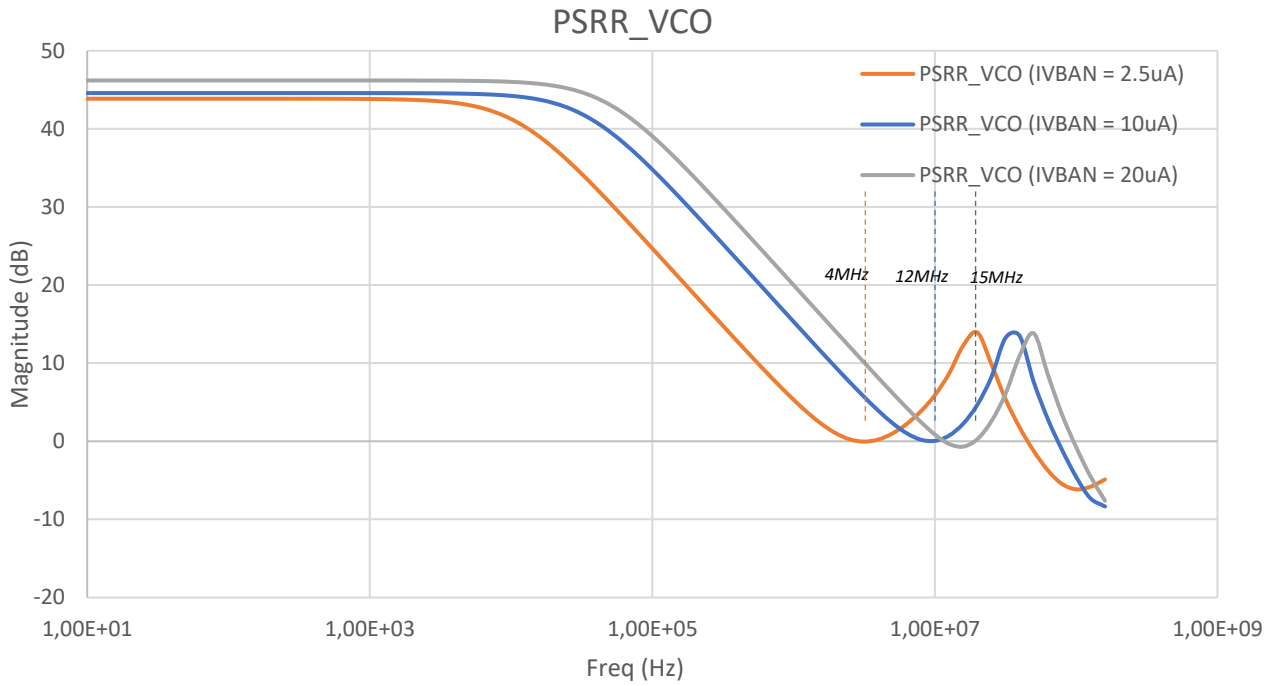
- Power rejection ratio (PSRR) of VCO

⇒ Immunity to noise sources => PSS & PXF analysis

$$PSRR = \frac{V_{tune}\ sensitivity}{V_{DD}\ sensitivity} = \frac{\partial \phi A / \partial V_{tune}}{\partial \phi A / \partial V_{DD}}$$



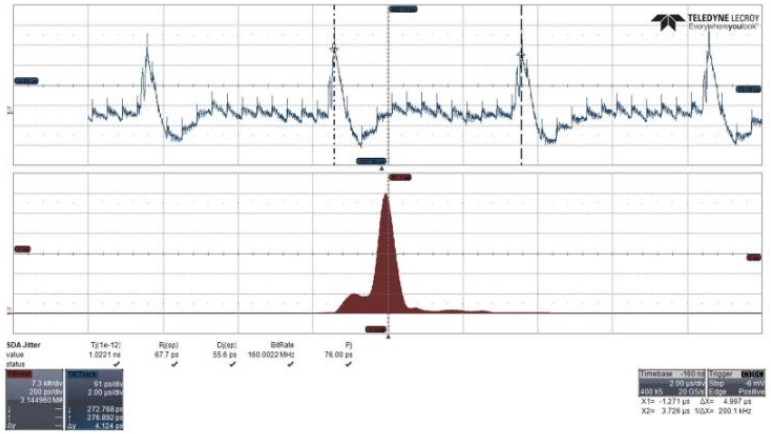
- $V_{tune} = 672\text{mv} \Rightarrow F_{VCO} = 320\text{MHz}$
- $I_{VBAN} = 2{,}5\text{uA}, 10\text{uA}, 20\text{uA}$



- For differents I_{VBAN} : Strong supply noise rejection up to 10KHz (> 40dB)
- Increase I_{VBAN} => increase frequency range of (PSRR > 0dB)

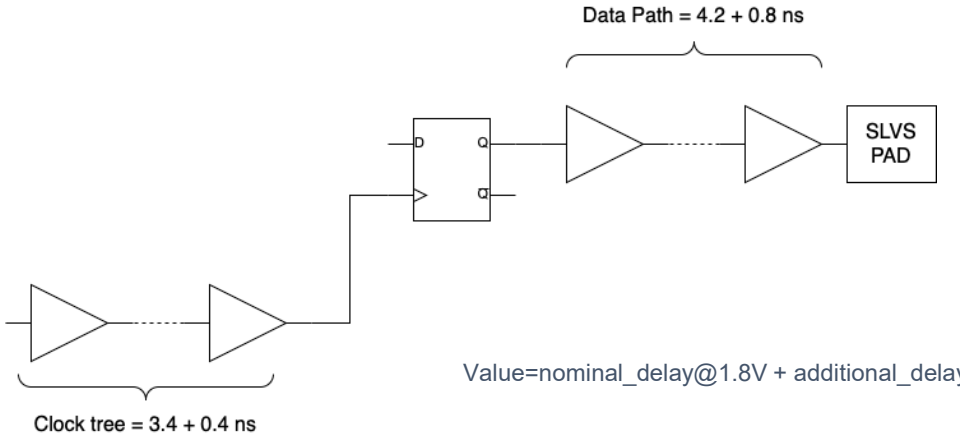
Power supply induced jitter issue

- High dependence between jitter and high-power period (every frame)
  - Around 500 ps / 100 mV (check with power supply variation)
  - Simulations match measurements within 1%
    - 1/3 in clock tree
    - 2/3 in data path
- Variation too significant to be offset by the acquisition
  - A variation around 100 mV on power supply is expected
  - Leads to synchronization lost



msis21n15_clkpll1_dmk1_8ch_clkpat1_clkpatd0_seq_base_nominal_dacs_vco1_not_started_tietrack--00000.png

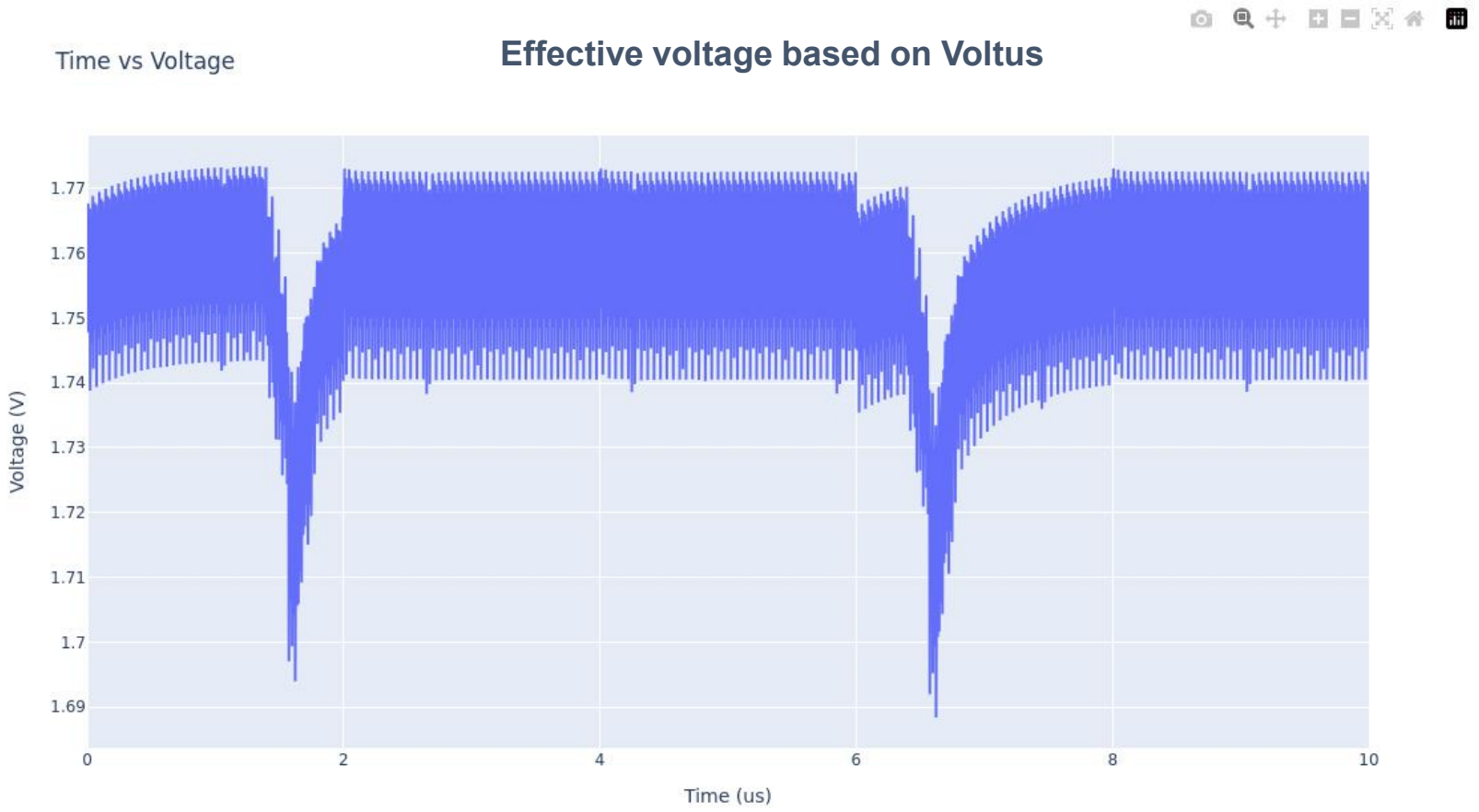
Tj(1e-12) = 1022.1 ps, Rj(sp) = 67.7 ps, Dj(p) = 55.6 ps, Pj = 76.0 ps



Value=nominal_delay@1.8V + additional_delay@1.55V

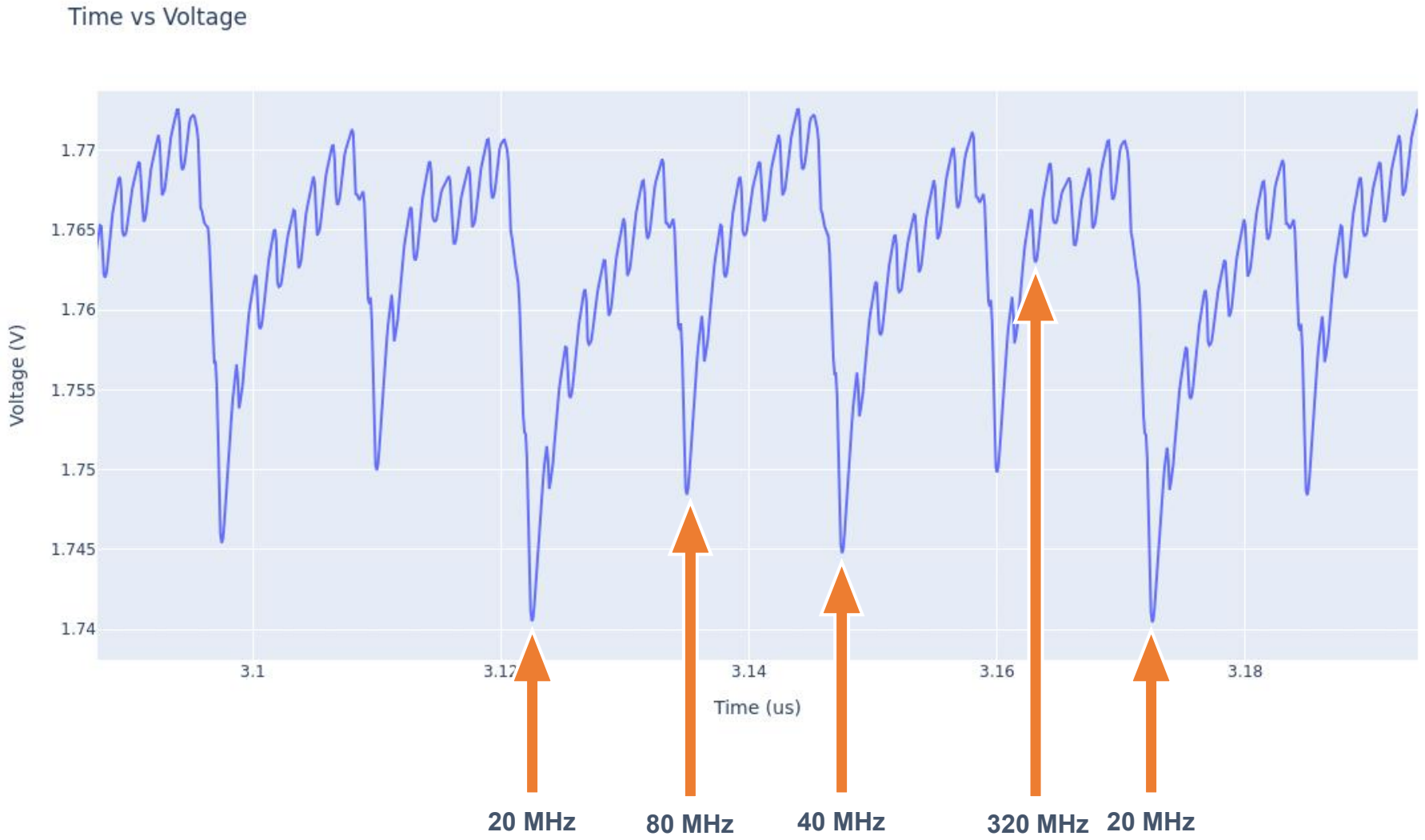
Power supply on MIMOSIS-2.1

- Large IR drop every 5 µs
  - End of frame and Beginning of a new one
  - Comes from header write in region memory



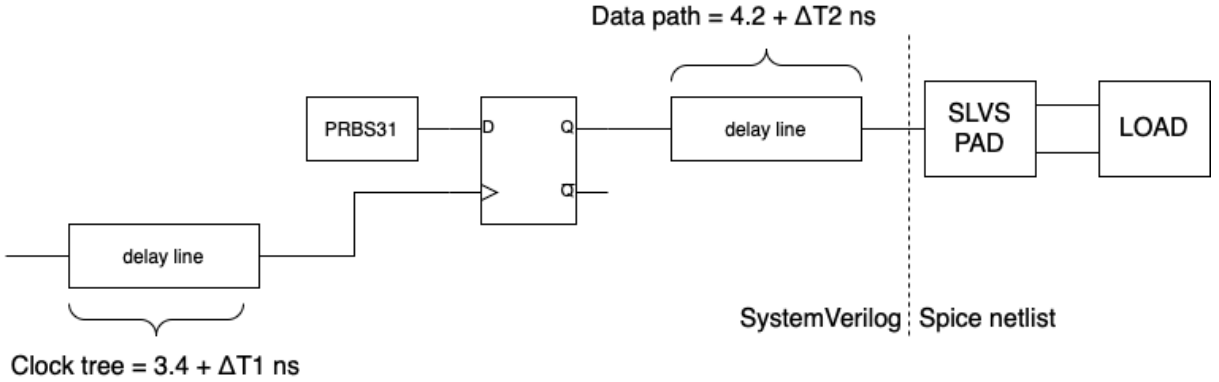
Zoom on effective voltage

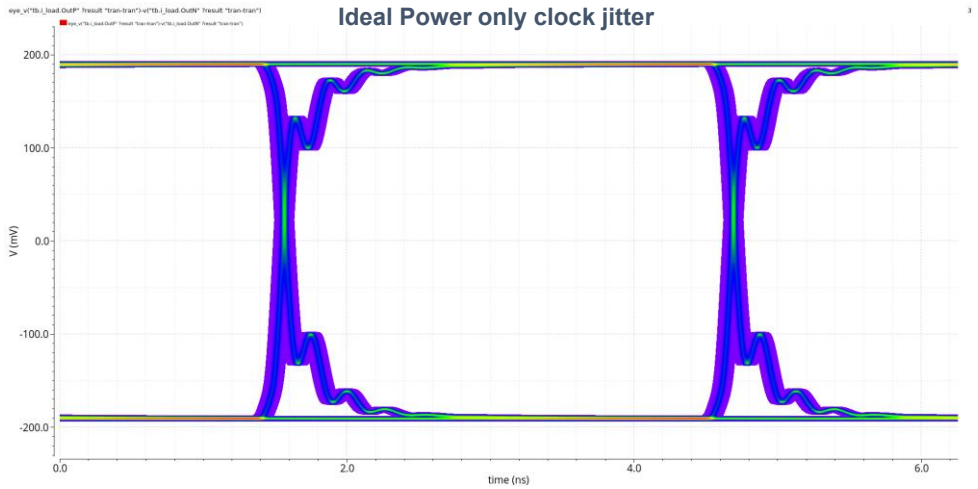
- Each clock edge is seen

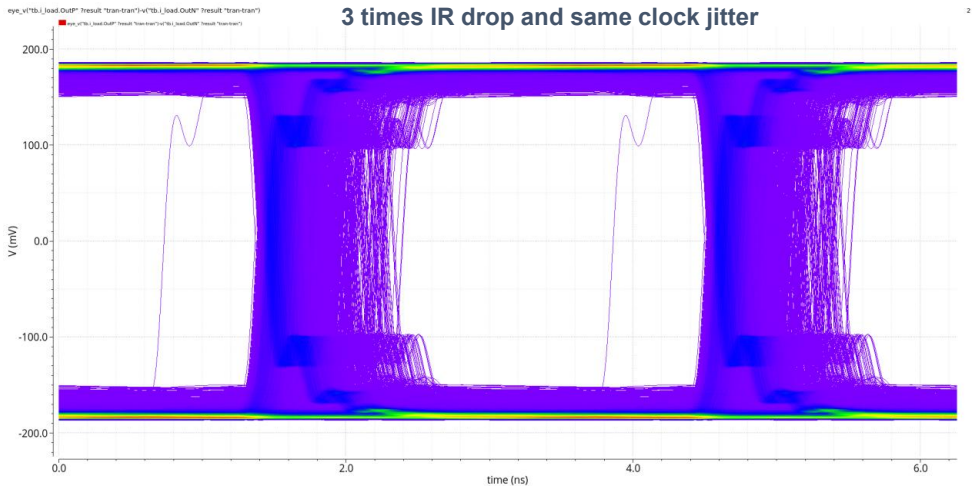


Model of power supply induced jitter

- Based on a SystemVerilog delay line dynamically dependent on power
  - ΔT1 and ΔT2 proportional to IR drop (calibrated with STA)
  - SLVS and LOAD are using dynamic power

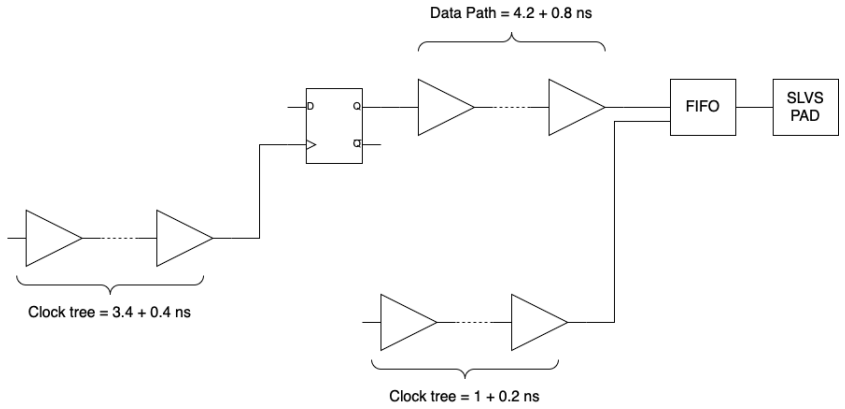




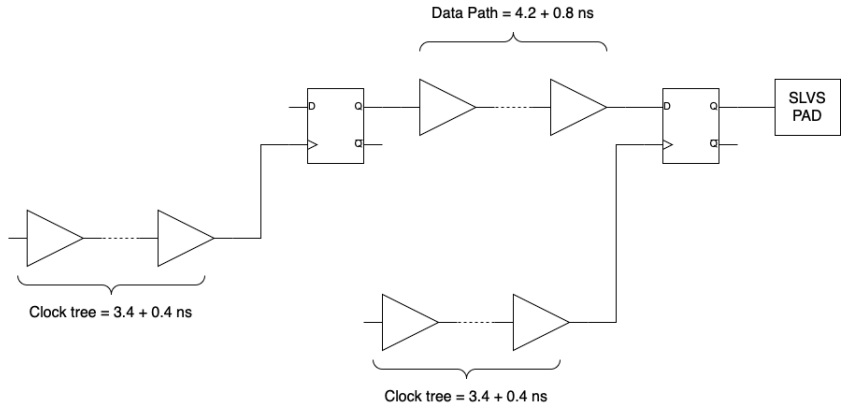


Power supply induced jitter mitigation

- Two solutions:
  - Reduce power variations
    - Need to rethink the readout since the variations is present for ~200 ns (end of frame + restart of new one)
  - Reduce phase shift
    - Increase robustness on external power supply variation
- Mitigation measure for MIMOSIS-3
  - Add a FIFO to resynchronize the output ➔ Reduce Data path and Clock tree variations
  - Backup solution resample with a flip-flop close to the output ➔ Reduce Data path variations



FIFO resynchronization

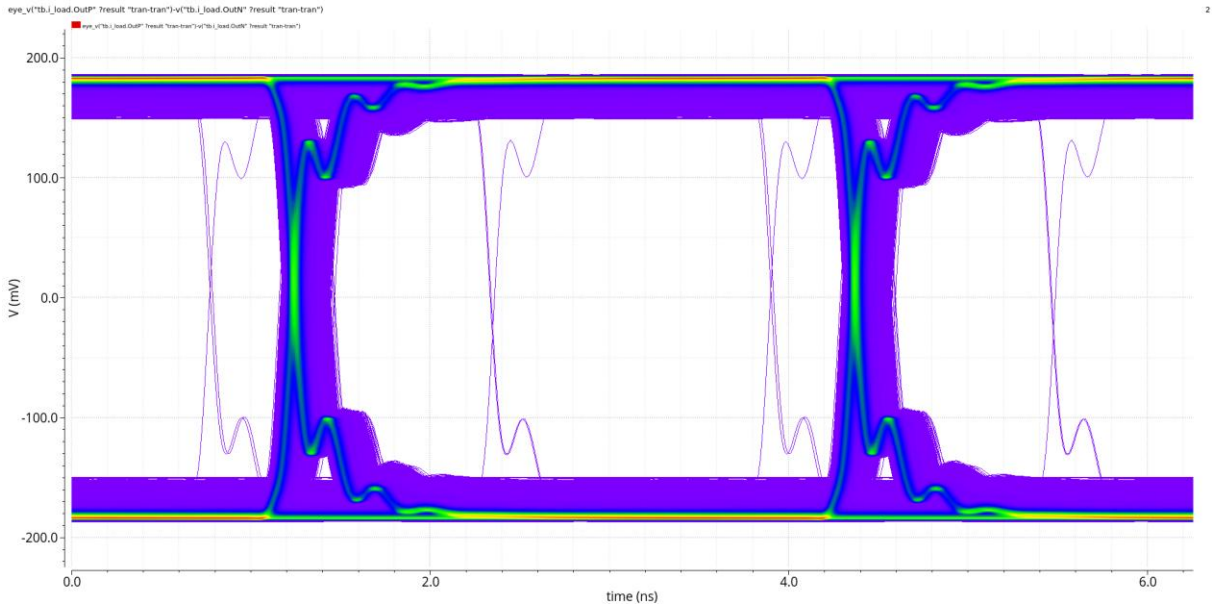


Flip-Flop resynchronization

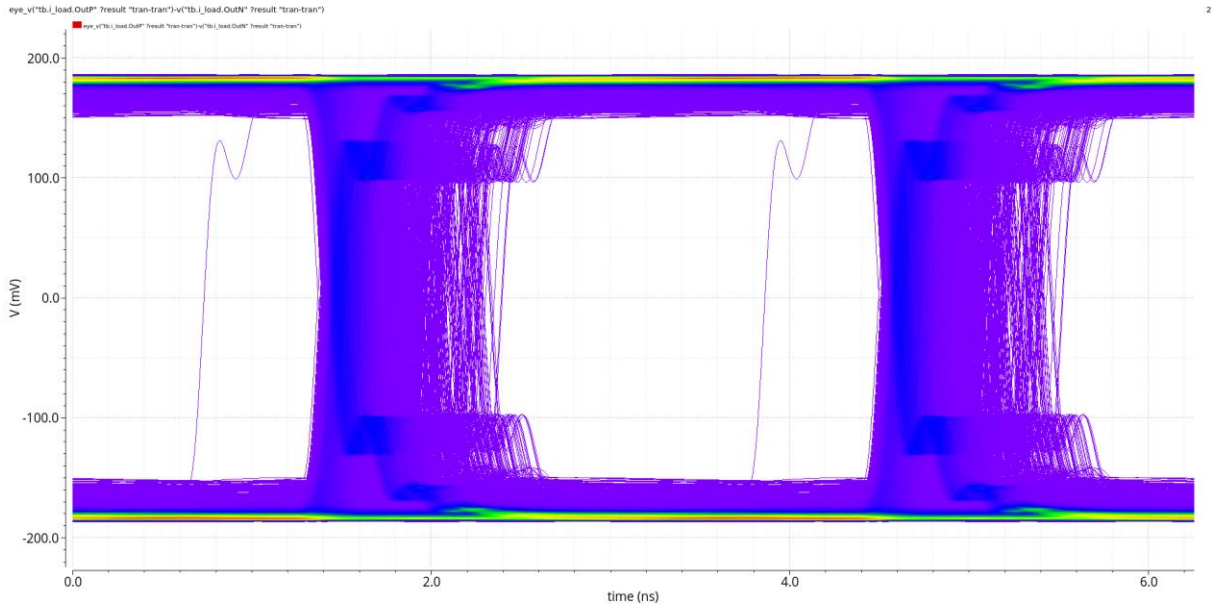
Power supply induced jitter mitigation

- Reduction by a factor of 3.5 the total jitter
  - From 1.1 ns to 300 ps

3 times IR drop with FIFO

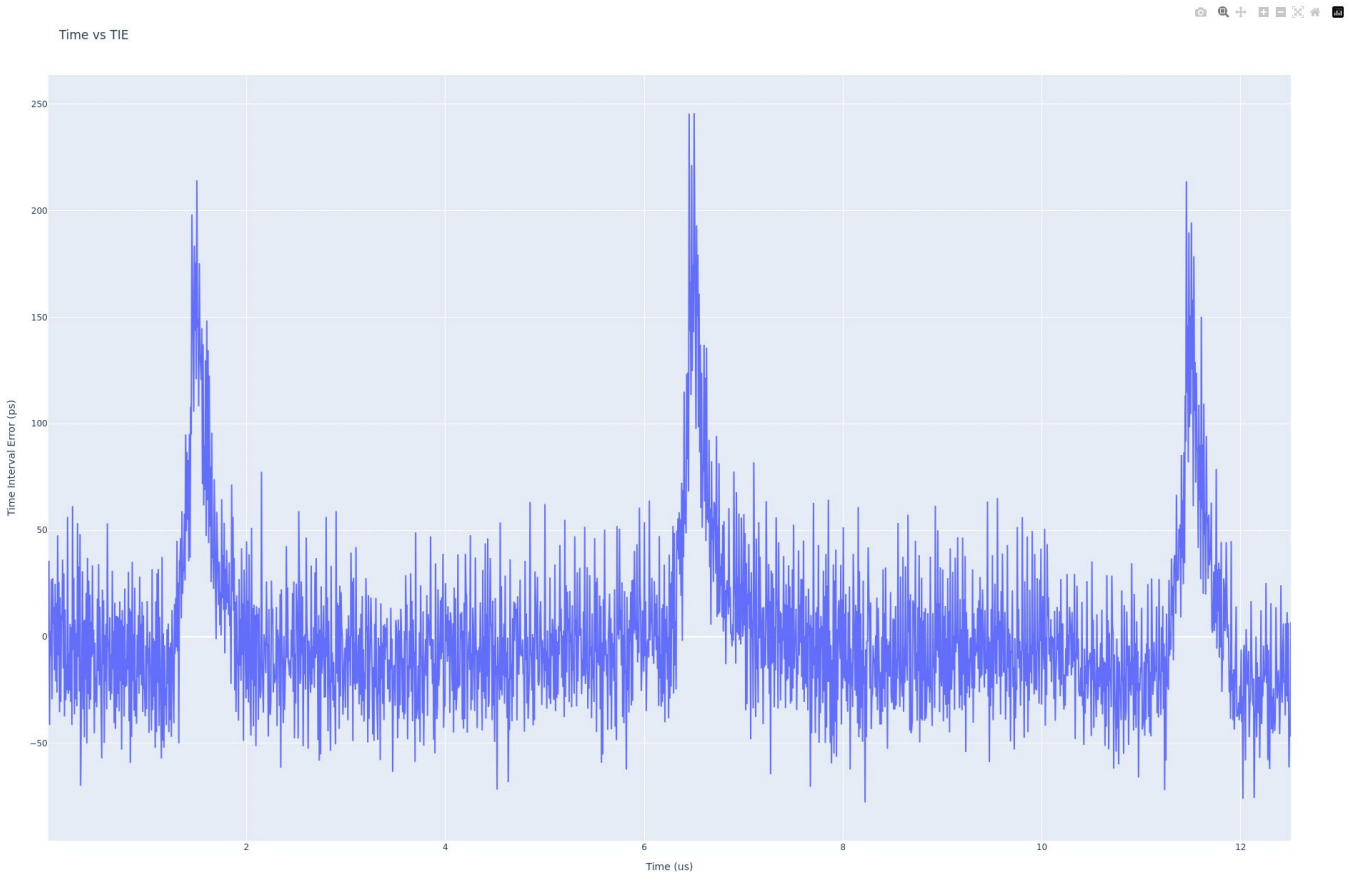


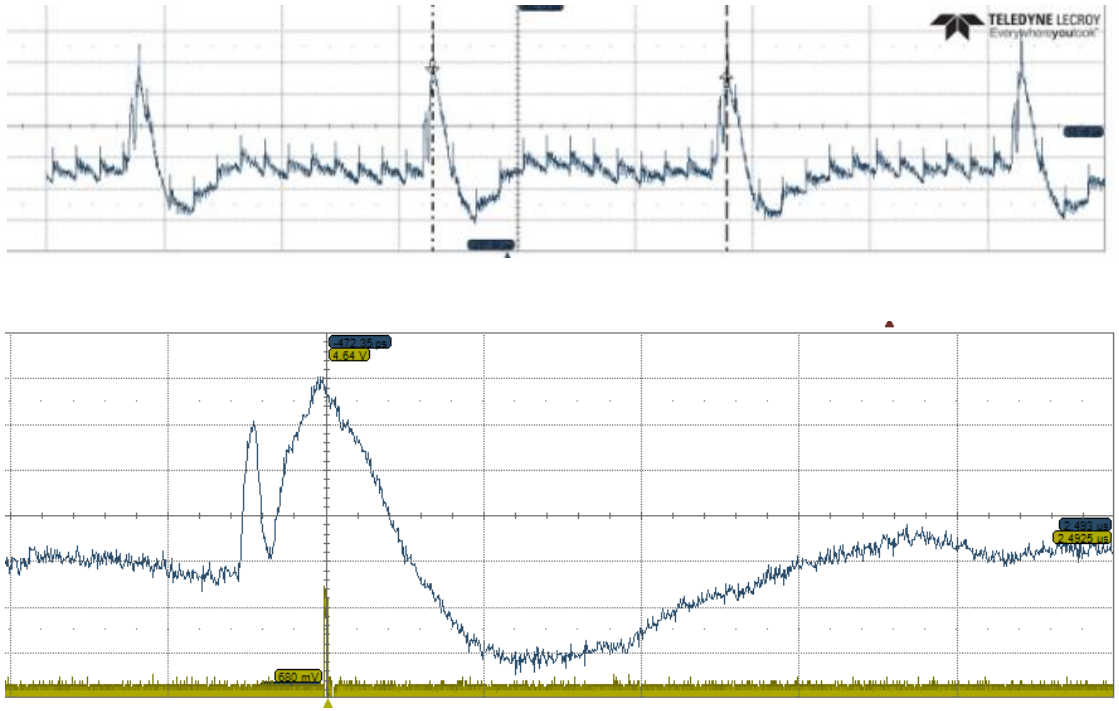
3 times IR drop for MIMOSIS-2.1



TIE track with simulated delay line

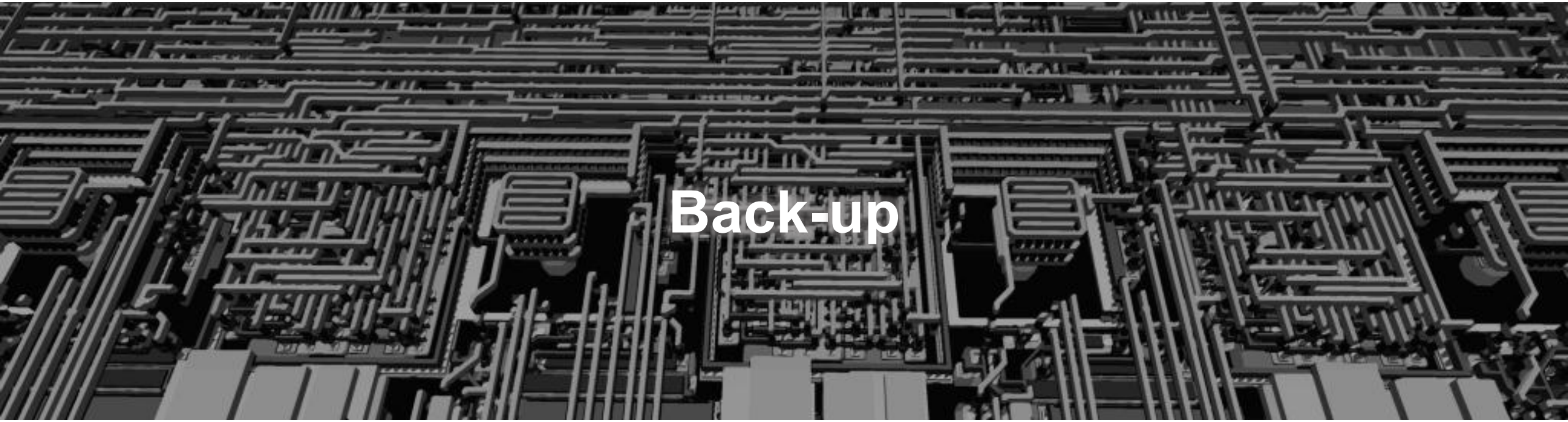
- No model of PLL ➔ No undershoot
  - For nominal IR drop





Conclusion

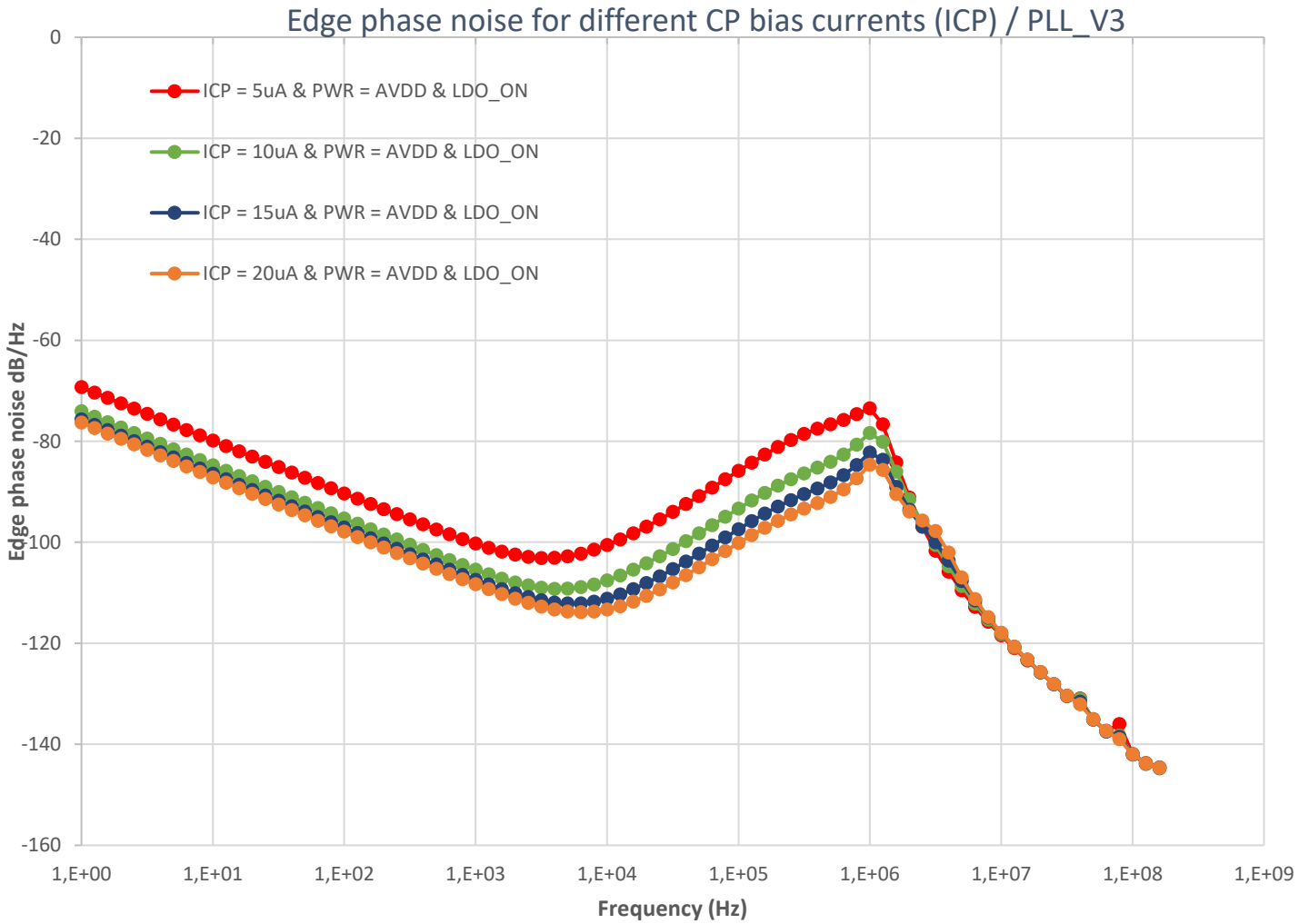
- PLL could be improved but are not the main source of the deterministic jitter
- To improve the PLL
  - Split the current for LDO and Charge Pump
  - Add trimming bits on both currents
  - No modification for the LDO
    - Could be disable if needed
  - No modification for the divider
    - Gain is limited compared to the overall performances
- To improve the clock tree and data path
  - Use a FIFO for resynchronization to reduce clock tree and data path latency
  - If the implementation is difficult use a flip-flop as backup solution
    - Limit the gain by removing only the data path latency



Back-up

PLL improvements

- Increase of the CP bias current (ICP)



PNoise simulation results / LDO ON / PLL_V3	
ICP (uA)	Random jitter (Jee): RMS (ps)
5	132
10	74,57
15	49,55
20	39.93

Increasing CP bias current => Less PLL noise

PLL jitter issue

- Test vs simulation: ClkPLL jitter performance versus input clock with additional random jitter

  ⇒ PSS & Pnoise simulation: LDO ON

PSS

Engine: Shooting / Harmonic Balance

Fundamental Tones

#	Name	Expr	Value	Signal	SrcId
2		1/(per-0)	40M	Large	V7
1		1/(per-0)	40M	Large	V5

Large | Clear/Add | Delete | Update From Hierarchy

Beat Frequency / Beat Period: 40M | Auto Calculate

Output harmonics: Number of harmonics: 40

Accuracy Defaults (errpreset)

Transient-Aided Options

Run transient? Yes / No / Decide automatically

Detect Steady State | Stop Time (tstab): 14u

Run Envelope tstab: yes / no

PNoise

Periodic Noise Analysis

PSS Beat Frequency (Hz): 40M

Multiple pnoise

Sweeptype: default — Sweep is currently absolute

Output Frequency Sweep Range (Hz)

Start-Stop | Start: 1 | Stop: 160M

Stop At Half Fundamental Frequency: no / yes

Sweep Type: Logarithmic

Points Per Decade / Number of Steps: 10

Add Specific Points

Add Points By File

Sidebands

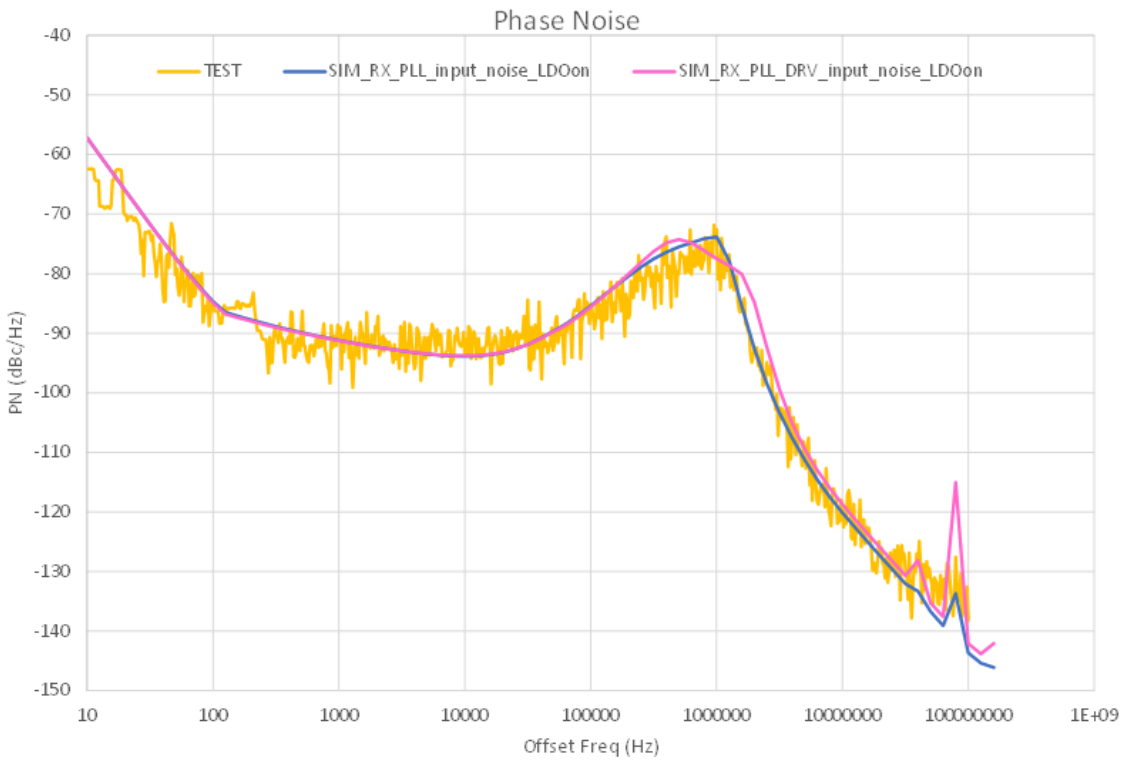
Method: default / fullspectrum

Maximum sideband

Calculates noise contributions up to the frequency determined by PSS time point resolution

Noise Type: sampled(jitter) | Sample Ratio: 8

#	Event Trig	TrigVal	Targ	TargVal	TD
1	cross DRV_OUT-g	0.000e+00	DRV_OUT-g		



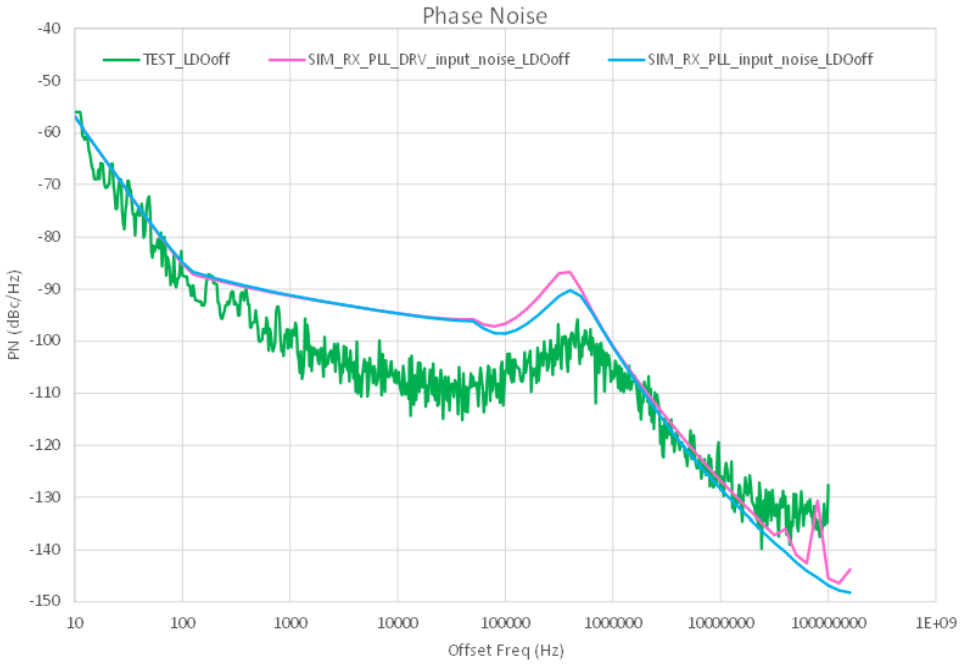
ClkPLL noise signal (Test vs post-simulation): LDO_ON

- LDO_ON => Good correspondance between test and post-simulation results

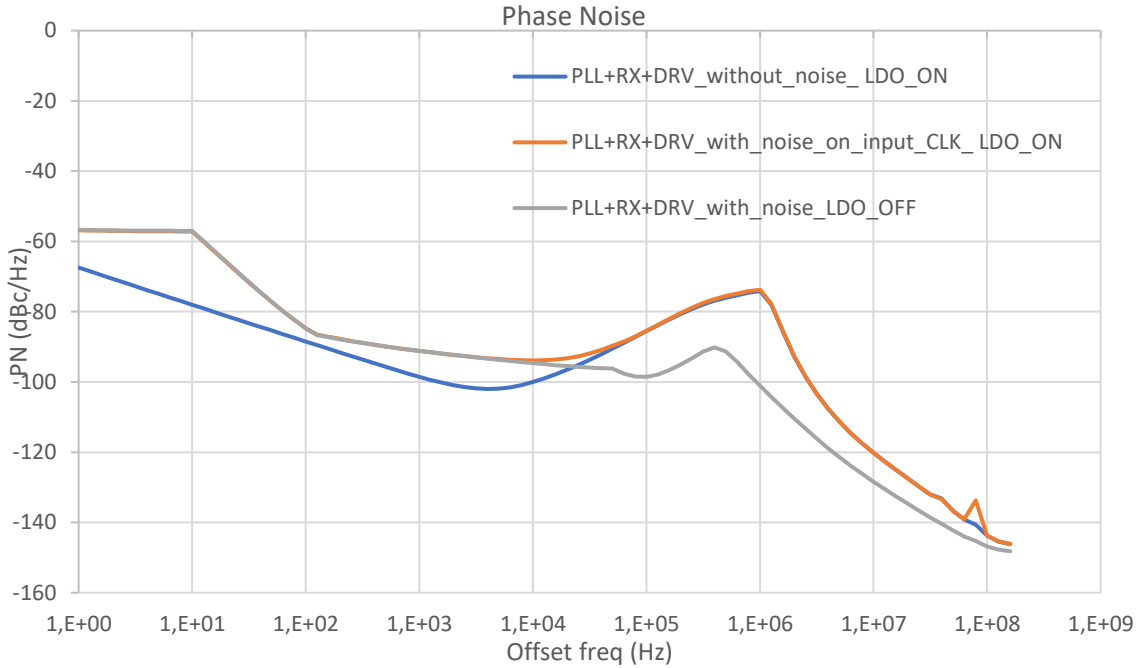
PLL jitter issue

- Test vs simulation: ClkPLL jitter performance versus input clock with additional random jitter

⇒ Noise signal of ($RJ_{rms} = 6.4\ ps$) is added to the input CLK: LDO OFF



ClkPLL noise signal (Test vs post-simulation): LDO_OFF



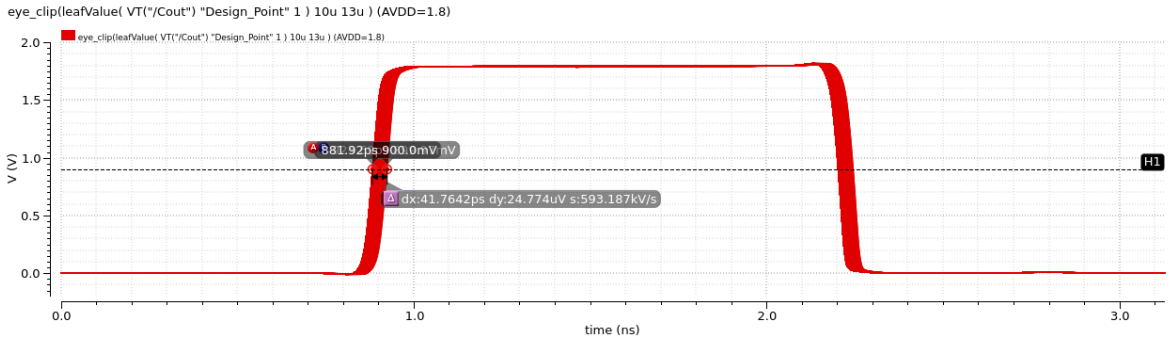
ClkPLL noise signal in post-simulation: LDO_OFF/ON

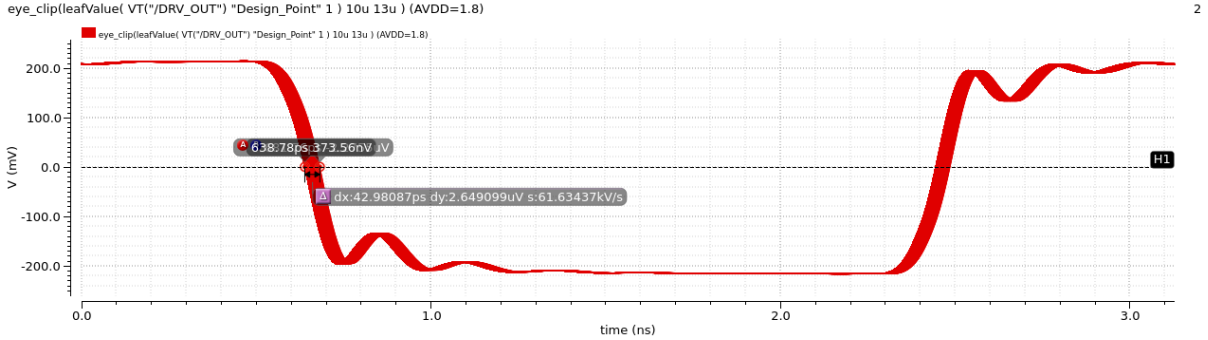
- A light difference between test & simulations when LDO is OFF
- Freq > 80KHz => No effect of CLKin jitter

Pnoise results RX_PLL_DRV		
Configuration	**RJ_rms (ps)/ Test**	**RJ_rms (ps)/ Post-simulation**
LDO_ON	110.7	130
LDO_OFF	7.2	19.5

PLL jitter issue

- Test vs simulation: ClkPLL jitter performance versus AVDD power supply voltage
  - Deterministic jitter => LDO_ON



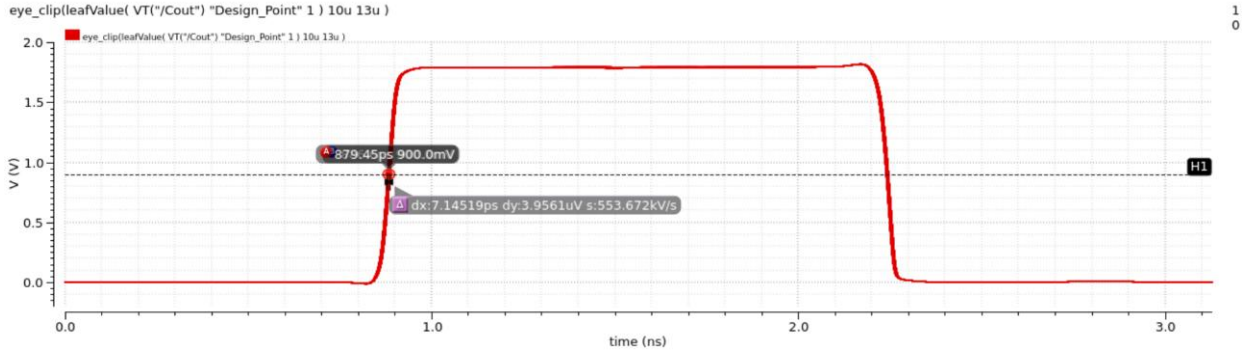


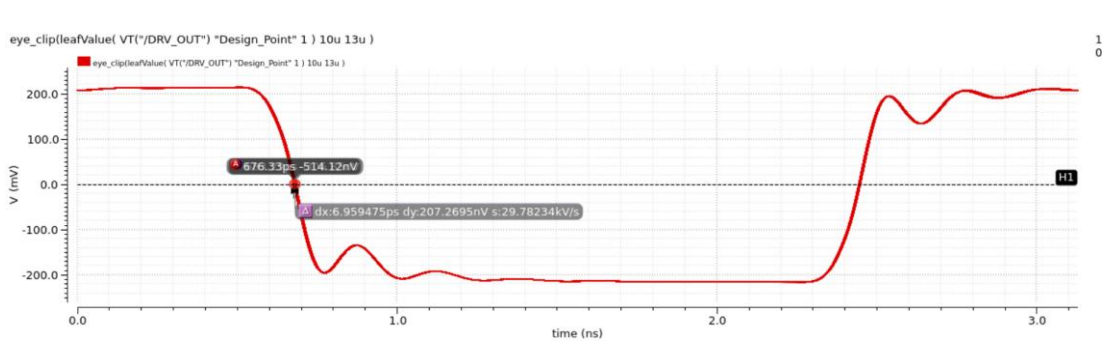
- Low contribution of ClkPLL jitter on total deterministic jitter
- Increasing the AVDD => increase the deterministic noise

Deterministic jitter (DJ) results _LDO ON			
AVDD (V)	Frequency (MHz)	Transient simulation	Test
1.65	320	9.61 *ps*	174.4 *ps*
1.7	320	14.34 *ps*	152,7 *ps*
1.8	320	42.98 *ps*	204,5 *ps*
1.9	320	87.87 *ps*	167,5 *ps*
2	320	120.1,57 *ps*	197,7 *ps*

PLL jitter issue

- Test vs simulation: ClkPLL jitter performance versus AVDD power supply voltage
  - Deterministic jitter => LDO_OFF



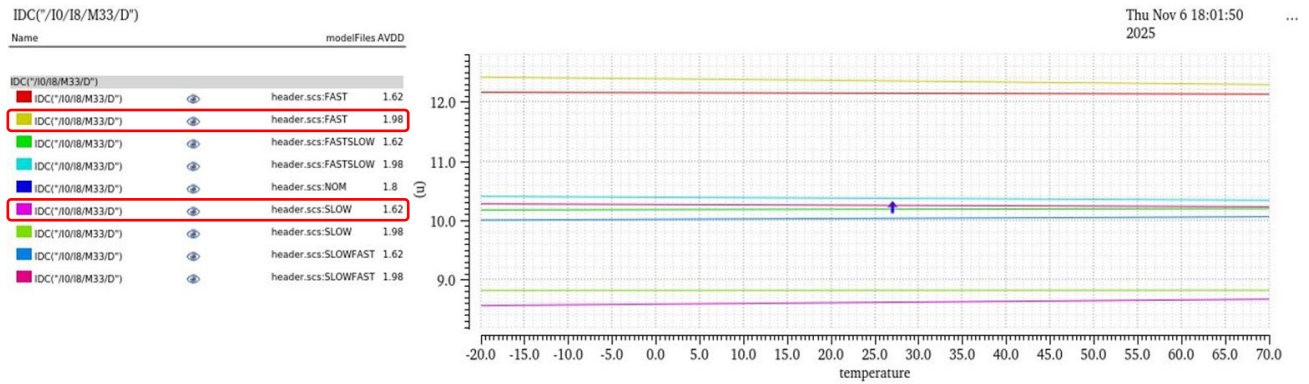


Deterministic jitter (DJ) results _LDO ON			
AVDD (V)	Frequency (MHz)	Transient simulation	Test
1.8 (LDO_ON)	320	42.98 *ps*	204,5 *ps*
1.8 (LDO_OFF)	320	6,95 *ps*	21,2 *ps*

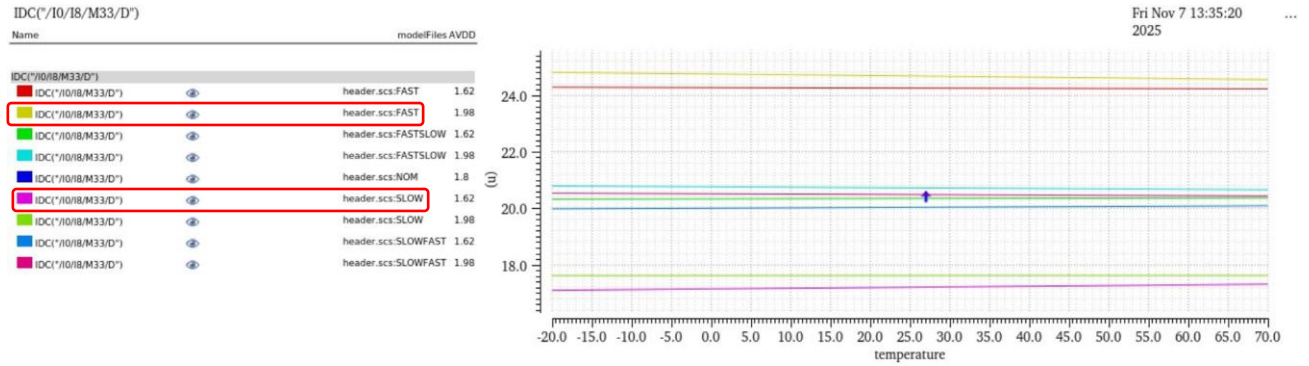
PLL performance

- Corners = f(IVBAN)

⇒ IVBAN (10uA)
- Min: 8,568uA@ SS_LV_LT
- Max: 12,42uA@ FF_HV_LT



⇒ IVBAN (20uA)
- Min: 17,11uA@ SS_LV_LT
- Max: 24,82uA@ FF_HV_LT



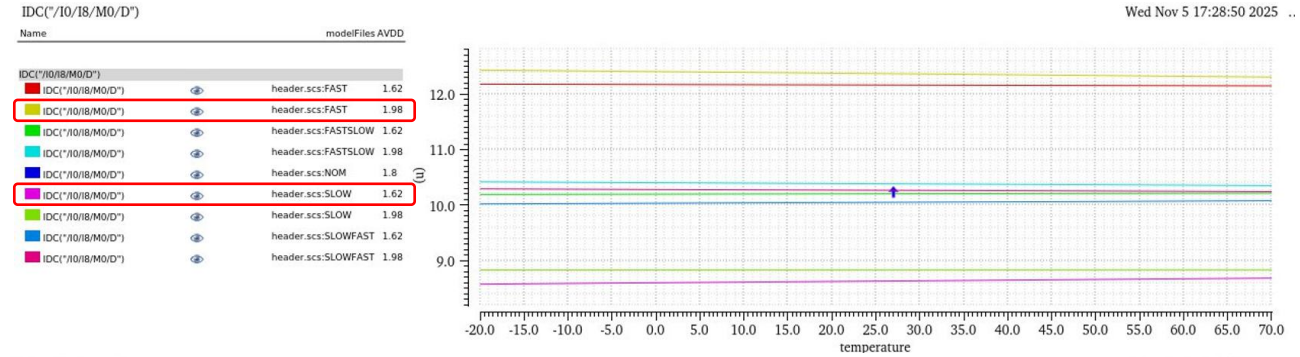
⇒ Deterministic jitter
- Worst case : 0,92% periode => acceptable

Corners of determinstic jitter		
Configuration	**DJ_max (ps)**	**DJ_min (ps)**
IVBAN =10uA	28,87@(320,05MHz&SS_HV_LT)	0,845@(320MHz&FS_LV_LT)
IVBAN =20uA	9,05@(320,1MHz&SS_HV_HT)	0,529@(320MHz&FF_LV_HT)

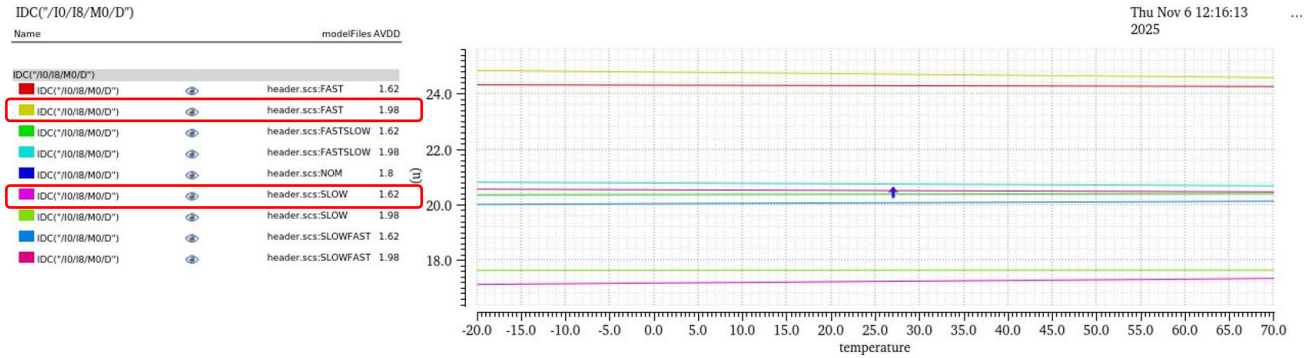
PLL performance

- Corners = f(ICP)

⇒ ICP (10uA)
- Min: 8,577uA@ SS_LV_LT
- Max: 12,43uA@ FF_HV_LT



⇒ ICP (20uA)
- Min: 17,14uA@ SS_LV_LT
- Max: 24,85uA@ FF_HV_LT



⇒ Deterministic jitter
- Worst case : 1,9% periode => acceptable

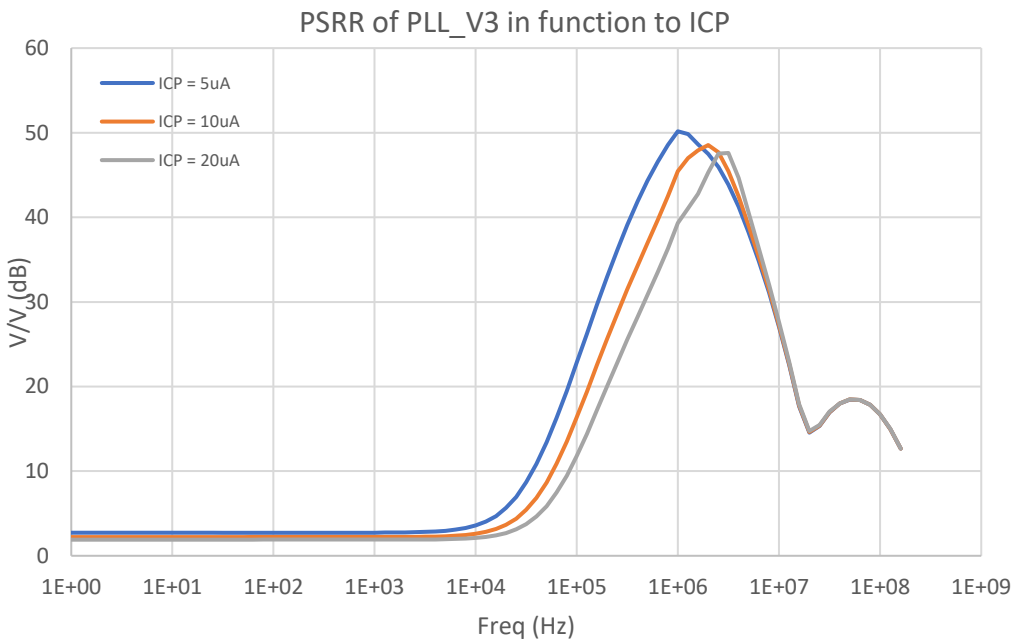
Corners of determinstic jitter		
Configuration	**DJ_max (ps)**	**DJ_min (ps)**
ICP =10uA	59,4@(320,1MHz&SS_HV_HT)	1,8@(320MHz&FS_LV_LT)
ICP =20uA	31,16@(320,1MHz&SS_HV_HT)	1,27@(320MHz&FF_HV_HT)

PLL performance

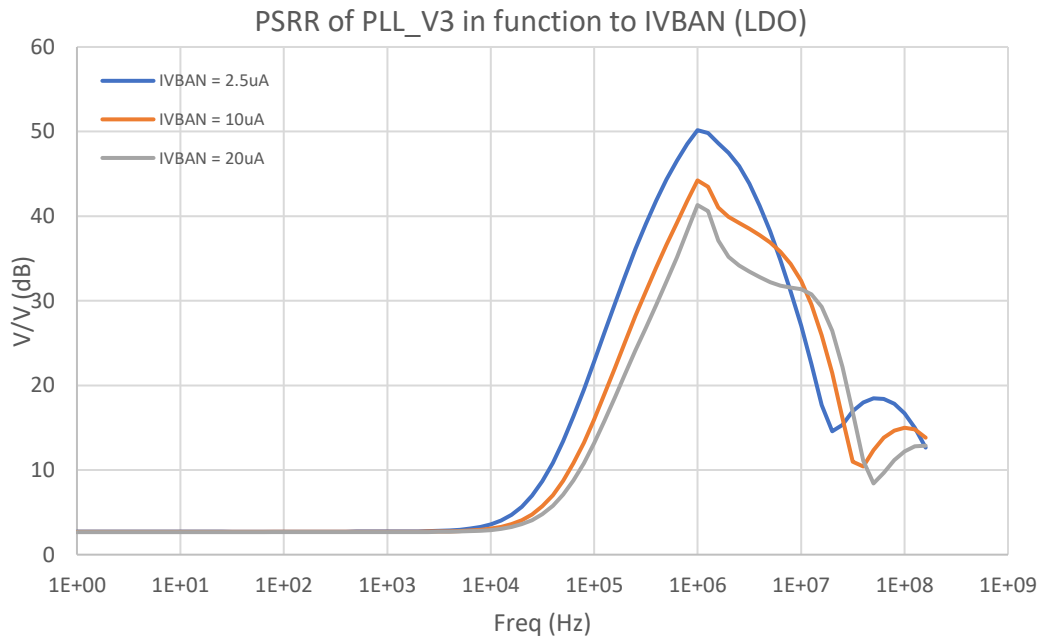
- Power rejection ratio (PSRR) of PLL

⇒ Immunity to noise sources: *VDD sensitivity*

$$PSRR = \frac{\partial \Phi Cout}{\partial V_{DD}}$$



⇒ $Low\ PSRR: (< 100KHz)$
⇒ $PSRR_{max}: (1MHz, 2MHz,\ 3MHz)$
⇒ $\sim same\ PSRR: (> 20MHz)\ for\ all\ ICP$



⇒ $Low\ PSRR: (< 100KHz)$
⇒ $PSRR_{max}: (1MHz)$
⇒ $(> 20MHz):\ Better\ PSRR\ @(I_{VBAN} = 2{,}5uA)$

Jitter issue (Definitions)

- **Random jitter => PSS/Pnoise** (VDD source ripple is turned off) **=> ADE Direct Plot**
  - Produced by **non-precise repeatable perturbations** of the system
  - Practically estimated to be **random Gaussian distribution**=> fully characterized using its Root-Mean-Squared value **(RMS)** or the standard deviation value **(σ)**.
  - **Peak-to-Peak value of RJ ($RJp{-}p$)** : calculated under certain observation conditions => **Bit Error Rate (BER)** targeted by the system under test => $RJp{-}p(t)(BER) \triangleq K \times RJRMS(t)$
- **Deterministic jitter => Transient analysis** (insert a supply ripple into tb) => **Max time – min time at specific crossing point of eye diagram**
  - Produced by **repeatable perturbations of the system** caused by the power supply ripple at discrete frequencies.
  - Typically, the simulation of DJ is performed by adding a sinusoidal perturbation to the supply voltage and running large-signal transient analysis. $DJp{-}p$ **(the peak-to-peak amplitude of DJ) can then be obtained by measuring the opening of the eye diagram.**

BER	Crest factor (K)
10^{-3}	6.18
10^{-4}	7.438
10^{-5}	8.53
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996
10^{-10}	12.723
10^{-11}	13.412
10^{-12}	14.069
10^{-13}	14.698

Table 1: BER and the corresponding RMS multiplier

- **Total jitter =>** net effect of the random jitter and the deterministic ji

  => $TJp{-}p = DJp{-}p + RJp{-}p(BER)$

Jitter issue (Definitions)

- **Pnoise vs transient noise:**
  - **Transient noise => time-domain-based method =>** computes the PSD (Power Spectral Density) of noise by averaging the spectra obtained from consecutive partly overlapped time windows from time 0 to simulation Tstop.
  - **Pnoise => frequency-domain-based method**