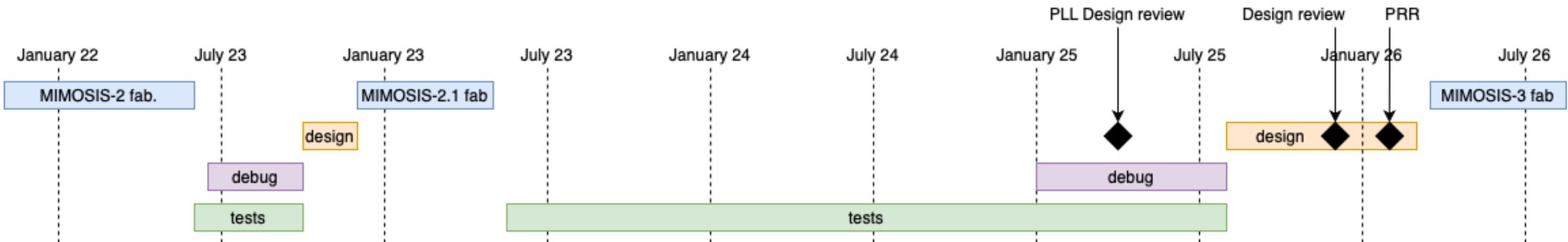# MIMOSIS-3 modifications

Introduction

- Previous correction for MIMOSIS-3 presented at ECE was mainly focus on a jitter issue
  - Mitigation is mandatory to operate the system
- Additional system tests exhibits new mandatory corrections
  - Criticality could be high
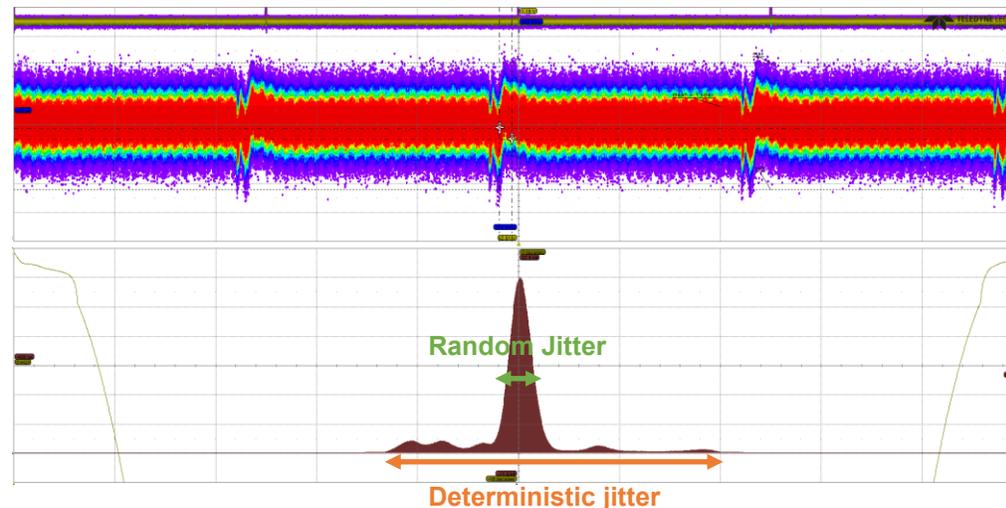
- MIMOSIS timeline starting at MIMOSIS-2 fabrication

- **Issues:**
  - ❑ High random jitter
  - ❑ Power supply induced jitter ➜ Excessive deterministic jitter

- **Previous conclusions:**
  - ❑ Random jitter is mitigated by increasing PLL current
    - From measurement
  - ❑ Mechanism of power supply induced jitter is under investigation
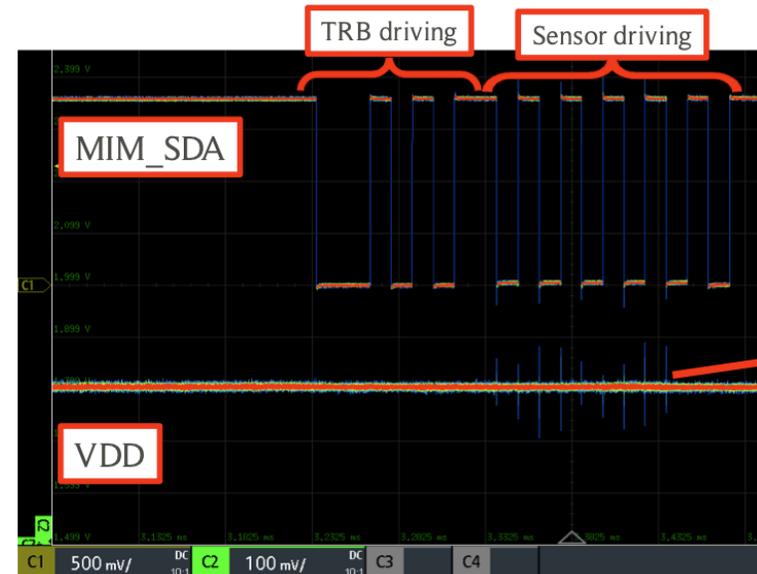   - Looking for an effect of the digital power on the PLL

Pads modifications

- ## I2C pads
  - ❑ Issue:
    - ■ CMOS pads leads to active driving overlap
    - ■ Power supply variations
  - ❑ Corrective action:
    - ■ Create an open drain pad
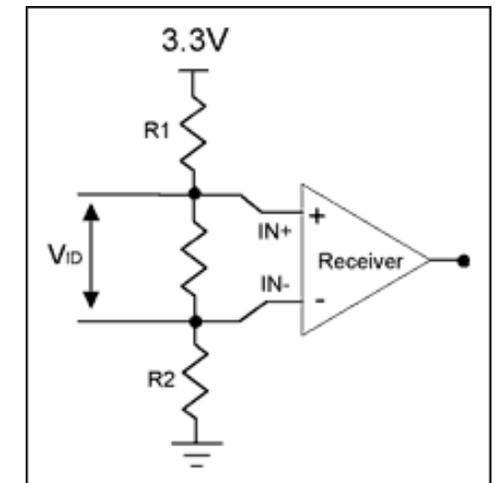

- ## SLVS pads
  - ❑ Issue:
    - ■ Some SLVS pads are let open in the final application (related to reset)
    - ■ Could be trigger by coupling
  - ❑ Corrective actions:
    - ■ Add a disable bit for the pads
    - ■ Add a fail-safe mechanism to existing pads

Remaining modifications

- **Power monitors**
  - Issues:
    - Analogue power monitors are not working
    - High-Z option for power monitors are requested to have a common line for several chips
  - Corrective actions:
    - Fix missing secondary power connection during routing for analogue power monitors
    - Add a configuration bit for High-Z option
- **320 MHz external clock operation for backup**
  - Issue:
    - Since MIMOSIS-1 this operation mode require an additional 40 MHz clock for slowcontrol
  - Corrective actions:
    - Provide the 320 MHz only and generate the 40 MHz for slowcontrol
    - Use an external pad to switch between the two modes (revamp an unused pad)

Remaining modifications

- **Matrix reorganisation**
  - Issue:
    - Sub-matrices for threshold adjustment are based on MIMOSIS-1 cut
    - 2 size of sub-matrices (aggressive and conservative pixel choice)
  - Corrective actions:
    - Make 4 equal sub matrices for threshold adjustment
    - Need to respin the DAC for capacitor compensation adjustment
- **Configuration registers**
  - Issue:
    - Not enough remaining configuration bits to implement fixes
    - PLL, Power monitors, SLVS pads
  - Corrective action:
    - Add 2 configuration registers

Methodology drivers

- **Modifications check by at least two persons or two methods**
  - Risk mitigation

- **Digital update**
  - Use Engineering Change Order (ECO) flow
    - For synthesis and implementation
    - Create a patch to modify functionality of a block
    - Limits modifications w.r.t. netlist, placement, routing, timing
  - Verification plan based on MIMOSIS-2.1
    - Replace manual checks by automatic ones (analogue nets interconnection)

- **Analogue update**
  - Simulations based on realistic system behaviour

Summary

Modification	Blocks	A/D	Risk	Impact
PLL jitter reduction	PLL	A	Medium	Medium
Data path jitter reduction	Top and FIFO (new block)	D	Medium (FIFO)	High (FIFO)
PAD update	SLVS and Open drain (new block)	A	Low	Medium
Matrix reorganisation	Top and DAC	A/D	Low	Low
Fix power monitors	Top	D	Low	Low
Add rescue clock	Top	D	Low	Medium
Add configuration registers	Top and CMU	D	Low	High

- Definitions
  - Risk: Possibility of failure / Impact: Effect of a failure on the operation
- All tasks are independent
  - Except Top implementation which is common
- Manpower
  - 2.5 FTE for analogue design and 2.5 FTE on digital design for a total of 6 engineers

Conclusion

- **Timeline:**
  - ❑ Modifications implementation (Layout and Verification)
    - ▪ Expected to be closed for the design review
    - ▪ 11th December
  - ❑ Submission preparation
    - ▪ Administrative works (Export licences, Purchase order, …) expected to end in December
    - ▪ Needed to start submission procedure
  - ❑ Effective manufacturing start point in mid January

- **Risk management:**
  - ❑ MIMOSIS-3 is a high-risk submission since is not only cosmetic bug correction
  - ❑ Best effort to mitigate the risk of failure

Summary of Requested Modifications

Title	Priority	Motivation	Func	Verif	Layout	A/D
Analog Power Monitor	High	Need power monitoring for detector control	100%	0%	0% (top)	D
High Z power monitor option	Medium	Common ADC to connect several MIMOSIS	100%	0%	0% (top)	D
Protect SLVS floating inputs pads	High	Floating SLVS input pads are triggered by other signals	100%	90%	100%	A
Open drain pad for I2C	High	Shorts between I2C transaction	100%	50%	0%	A
Reduce data outputs phase shift	Critic	High dependence of data output phase with supplies	10%	0%	0%	D
One input clock	High	Use only one pad for 40 or 320 MHz (bypass PLL)	30%	0%	0% (top)	D
PLL jitter reduction	Critic	Reduce intrinsic jitter of the PLL	80%	30%	0%	A
Add configuration registers	Critic	Add new registers for PLL configuration	100%	50%	50%	D
Matrix reorganisation	Optional	Make 4 equal submatrices	0%	0%	0% (top)	D
DAC respin	Optional	For matrix reorganisation	50%	20%	0%	A

Planning explanation

- **Definition**
  - Verification 50%: functional verification done
  - Verification 100%: post layout verification done
- **Goals**
  - Review after double design review (this one and PRR)
  - Close all modifications for PRR (end of January)
  - 1 month after PRR for Tape Out (GDS file send to Tower)
  - 2-4 weeks for Tower to start production
- **Critical Path**
  - Reduce data outputs phase shift
  - FIFO design (based on Chipware like SPARC) ➜ top integration ➜ verification