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MIMOSIS-2.1 TESTS

PHASE-LOCKED LOOP (PLL)

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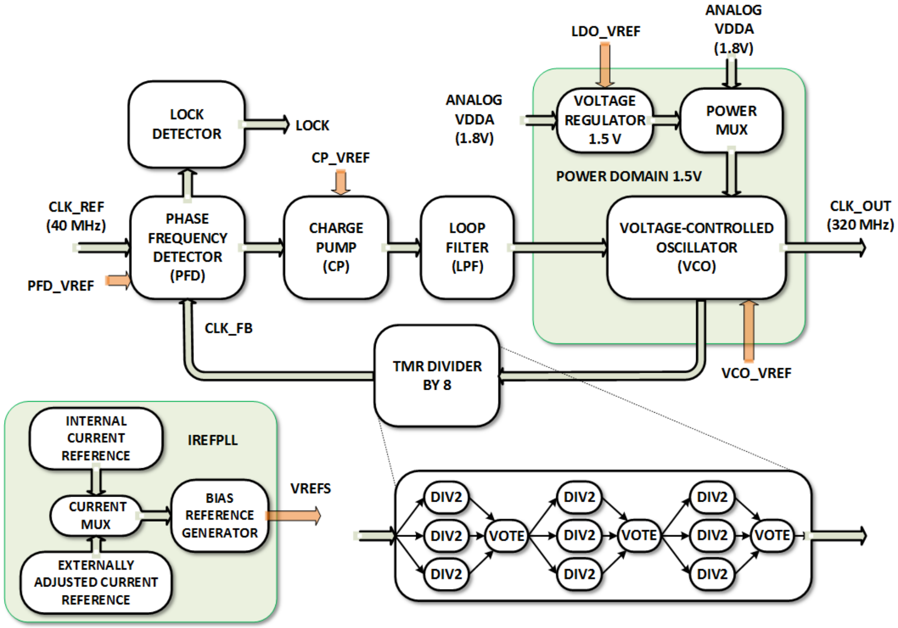
INTRODUCTION

- A Charge-pump PLL
- Additional features
    - Integrated voltage regulator (LDO) for VCO
    - Integrated Lock detection circuitry
    - Divider with Triple Modular Redundancy (TMR) to protect against single-event upset errors (SEU)
- PLL block generates 320 MHz main clock from 40 MHz input clock signal



Design Parameters

Parameter	Value
Fixed multiplication Factor	8
Clock input range	25 MHz to 50 MHz
Clock output range	200 MHz to 400 MHz
Locking time	< 15 µs
Duty cycle ratio	45±5 %
Power supply range	1.5V to 2.0V
Die Area	360 x 320 µm² (0.11 mm²)
Power consumption (Core)	3.6 mW at 320MHz

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MIMOSIS-2.1 PLL CORE

- PLL core consists of essential building blocks of the PLL:

  Phase Frequency Detector (PFD), Charge Pump (CP), Loop filter (LPF),

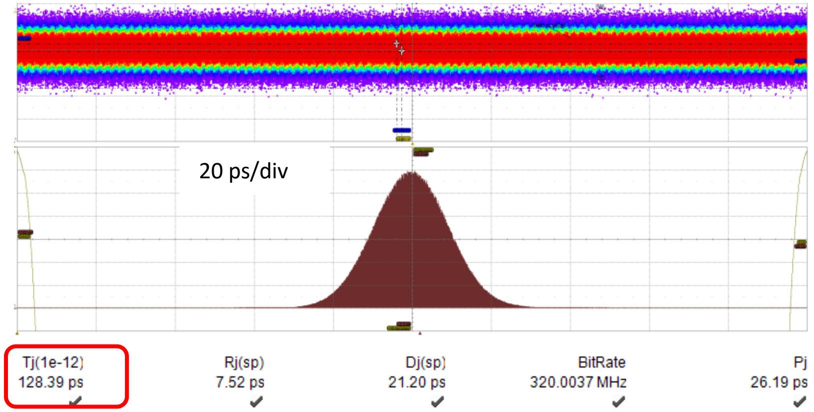
  Voltage-controller Oscillator (VCO) and Divider

- PLL Core design is operational and fullfils the requirements in low power supply noise conditions
  - voltage regulator LDO disabled, pixel matrix steering and readout not started

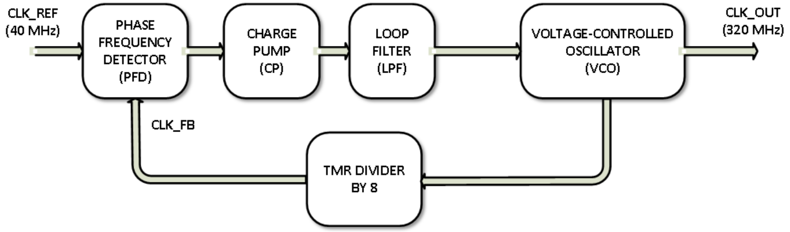
Test Results

Parameter	Value
Clock input range	25 MHz to 80 MHz
Clock output range	200 MHz to 640 MHz
Locking time	4.6 us
Duty cycle ratio	46% at 320 MHz
Total Jitter TJ(BER=1e^{-12})	128 ps (0.04 UI) at 320 MHz

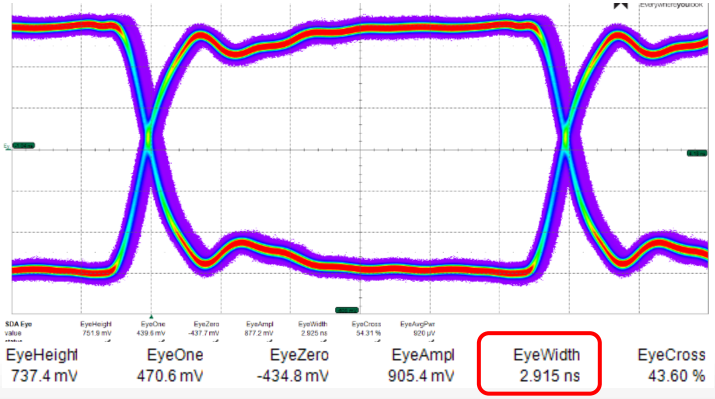
TIE histogram of the CLKPLL and instantaneous clock frequency-tracking plot in persistence mode



Tj(1e-12)	Rj(sp)	Dj(sp)	BitRate	Pj
128.39 ps	7.52 ps	21.20 ps	320.0037 MHz	26.19 ps



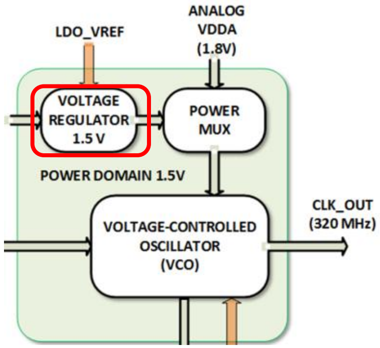
Eye diagram DATA[0] LVDS bufferoutput, Data Pattern: ([0xAAAA] x 16), Clock period: 3.125 ns (320 MHz)



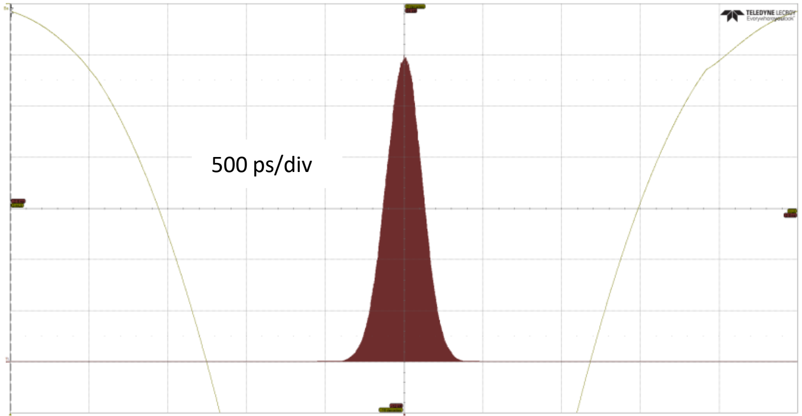
EyeHeight	EyeOne	EyeZero	EyeAmpl	EyeWidth	EyeCross
737.4 mV	470.6 mV	-434.8 mV	905.4 mV	2.915 ns	43.60 %

ISSUE 1: INTEGRATED VOLTAGE REGULATOR (LDO)

- Main task of the LDO:
  - To provide a stable and a low-noise power-supply (1.5V) for the VCO
- Problem: Power-supply noise reduction performance of the LDO is inadequate
  - Improved PLL Jitter performance when the LDO is disabled
- LDO cannot be tested directly (no access to LDO output, a sensitive node for noise injection)
  - PLL output signal is modulated by the output noise of the LDO
- Note: LDO is not a part of the PLL Core blocks (PFD, CP, LPF, VCO and divider)

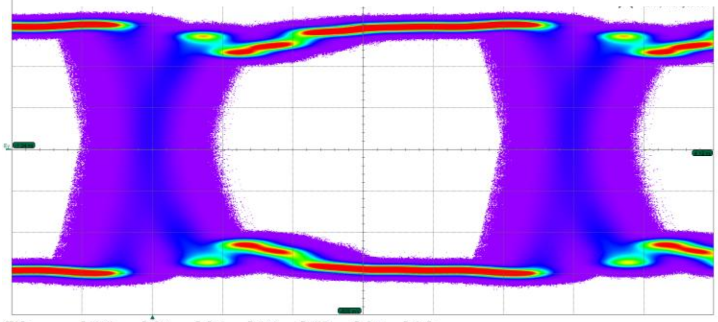


TIE histogram of the CLKPLL – LDO ENABLED



Tj(1e-12)	Rj(sp)	Dj(sp)	BitRate	Pj
1.5069 ns	93.3 ps	176.7 ps	320.0051 MHz	204.58 ps

Eye diagram serializer DATA[0] LVDS buffer output, Data Pattern: ([0xAAAA] x 16), Clock period: 3.125 ns (320 MHz), LDO ENABLED



EyeHeight	EyeOne	EyeZero	EyeAmpl	EyeWidth	EyeCross
670.8 mV	470.5 mV	-434.8 mV	905.3 mV	2.044 ns	43.67 %

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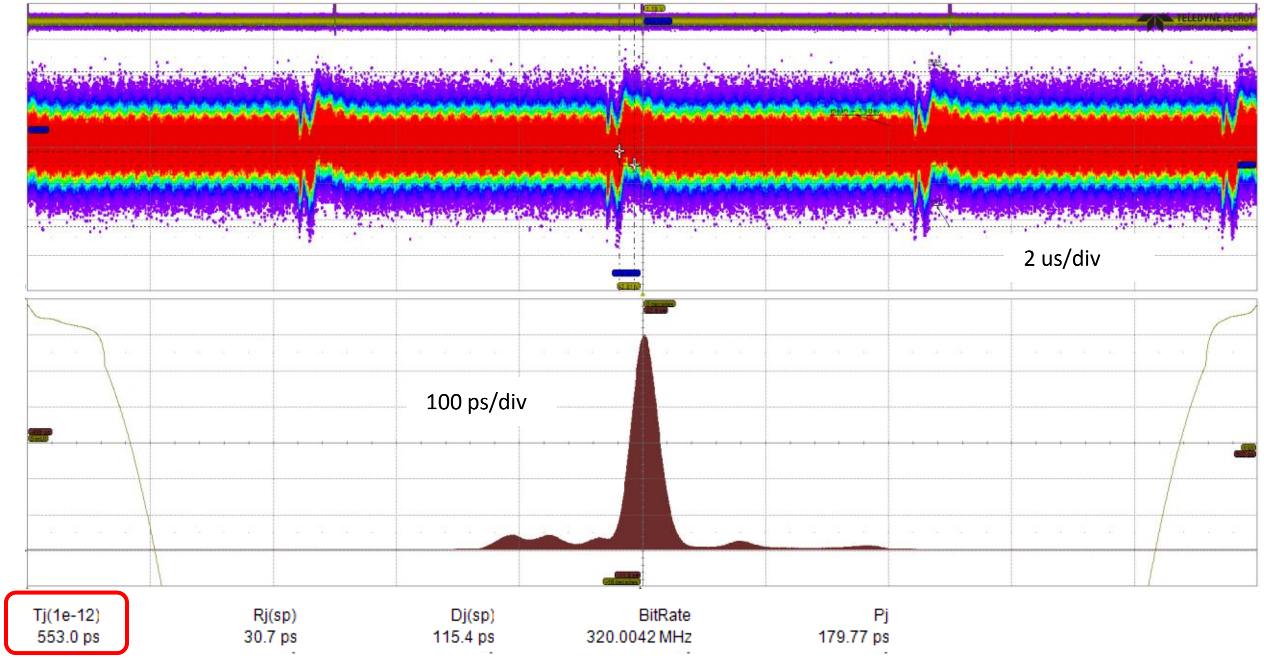
ISSUE 2: NOISE INJECTION FROM DIGITAL POWER SUPPLY TO THE PLL BLOCK

- To disable the LDO is not a solution (Note: using the internal reference current IREFPLL)
  - Good PLL jitter performance at very low activity level of the sensor
  - Problem: Activity of the sequencer block results in noise injection from the digital power supply to the PLL block

TIE histogram of the CLKPLL and instantaneous clock frequency-tracking plot in persistence mode – SEQUENCER BLOCK RUNNING



Tj(1e-12)	Rj(sp)	Dj(sp)	BitRate	Pj
553.0 ps	30.7 ps	115.4 ps	320.0042 MHz	179.77 ps

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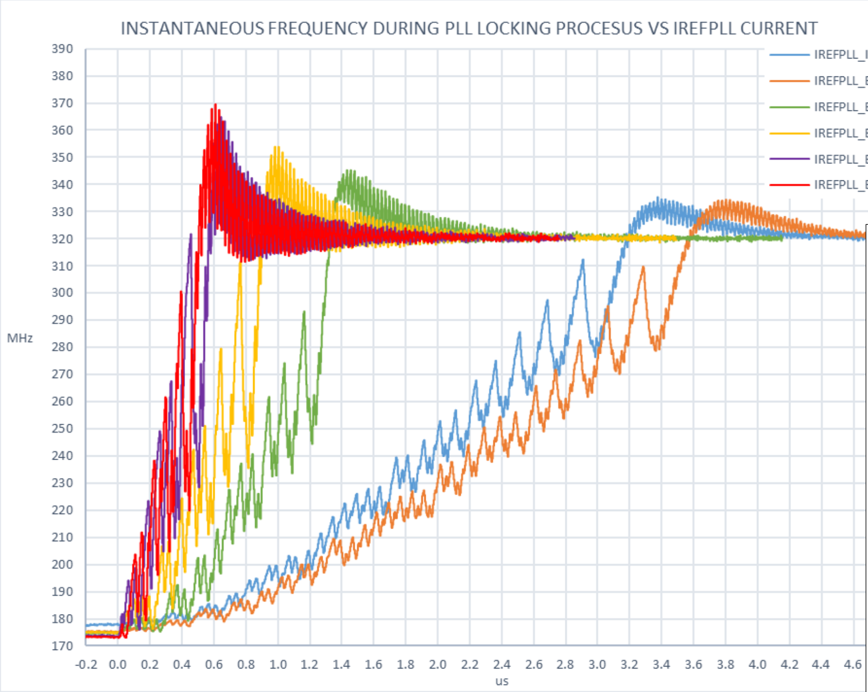
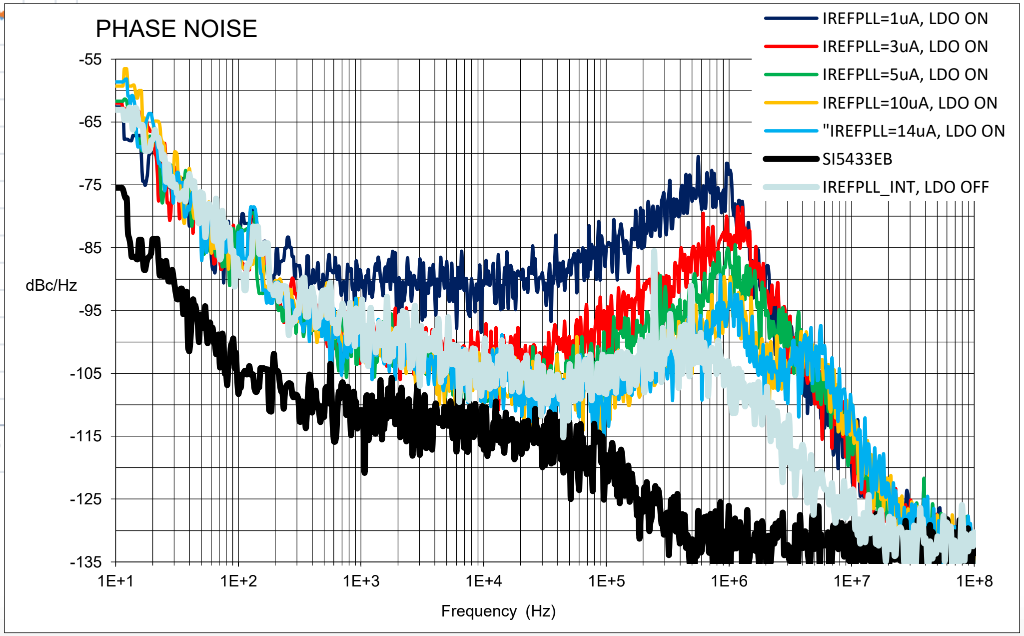
TEMPORARY SOLUTION FOR THE ISSUE OF LDO: EXTERNAL REFERENCE CURRENT (IREFPLL)

- LDO enabled and use of external reference current (IREFPLL) with the higher current (1uA -> 10…14uA)
- Problem: LDO and PLL shares the common reference current circuitry (IREFPLL)
- Increase of the reference current results in:
  - PLL loop bandwidth increase (more reactive, stability?), the PLL is more sensible for the reference clock jitter
  - LDO has improved power-supply noise reduction performance ($TJ_{pk\text{-}pk}$(BER = 10^{-12}) : 1500 ps -> 310 ps)





CONCLUSION

- The PLL Core is operational in low power supply noise conditions (Sequencer block/data readout not started)
- Jitter performance issue of the PLL is related to the LDO block, not to the PLL Core blocks
- Power-supply noise reduction performance of the LDO is inadequate
- In normal operation conditions of MIMOSIS-2.1 , the LDO is required to obtain adequate PLL jitter performance
- Temporary solutions for the LDO issue: use of an external PLL reference current (IREFPLL)

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