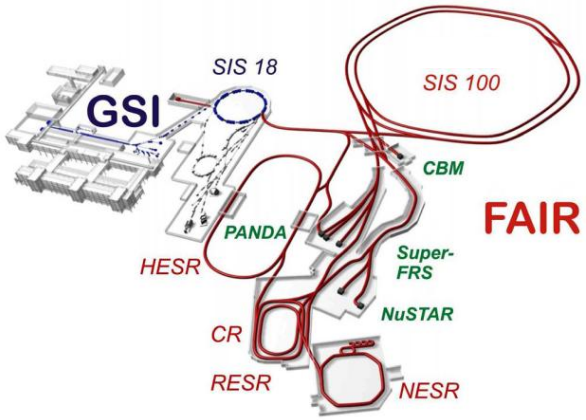
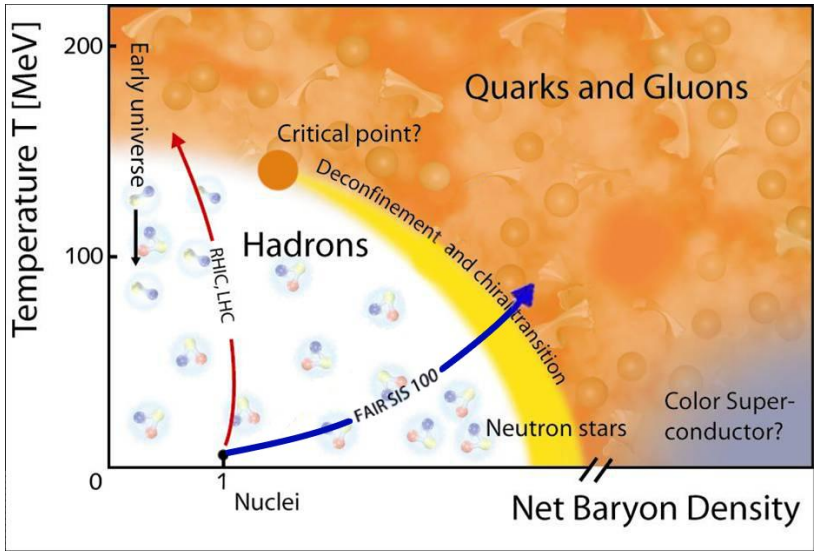
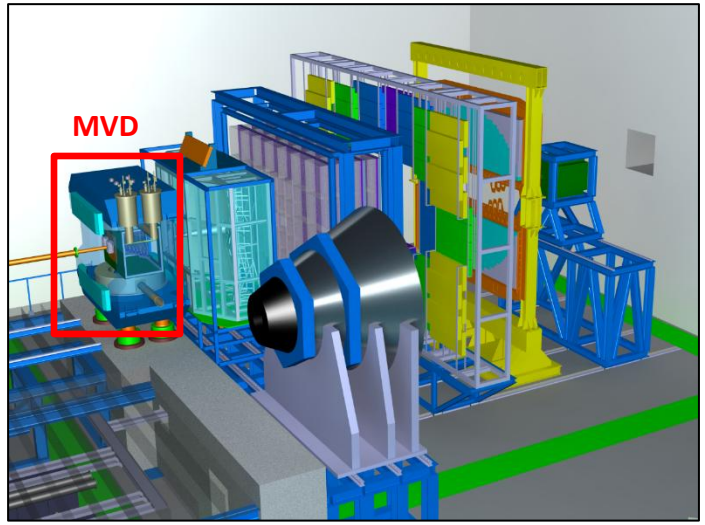
MIMOSIS PLL overview

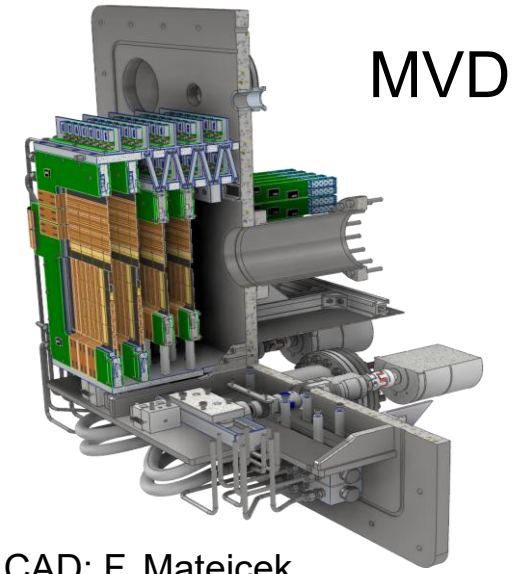
The Compressed Baryonic Matter experiment @ FAIR

- Explore phase diagram at region of highest net-baryon density
- Fix target





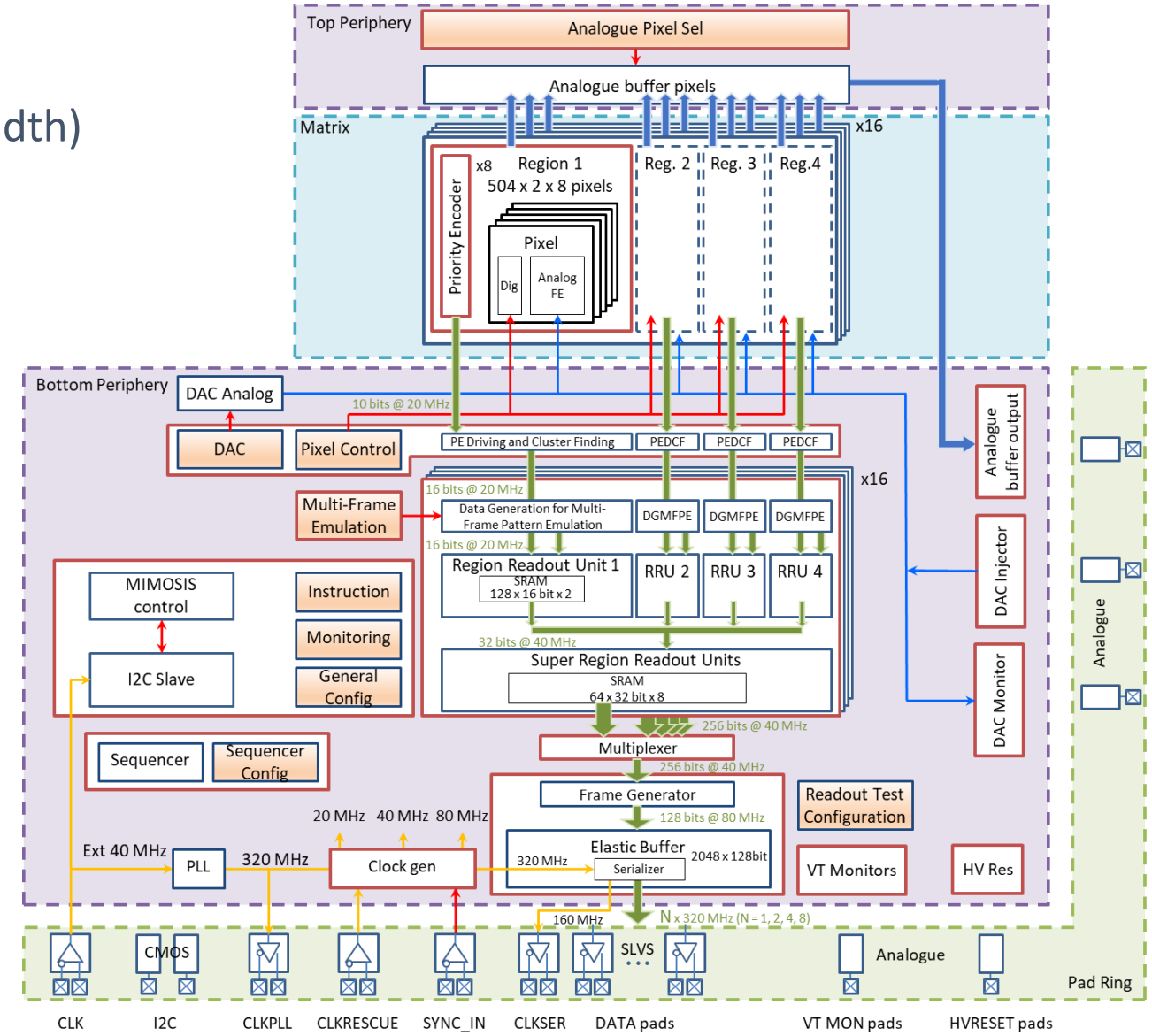




CAD: F. Matejcek

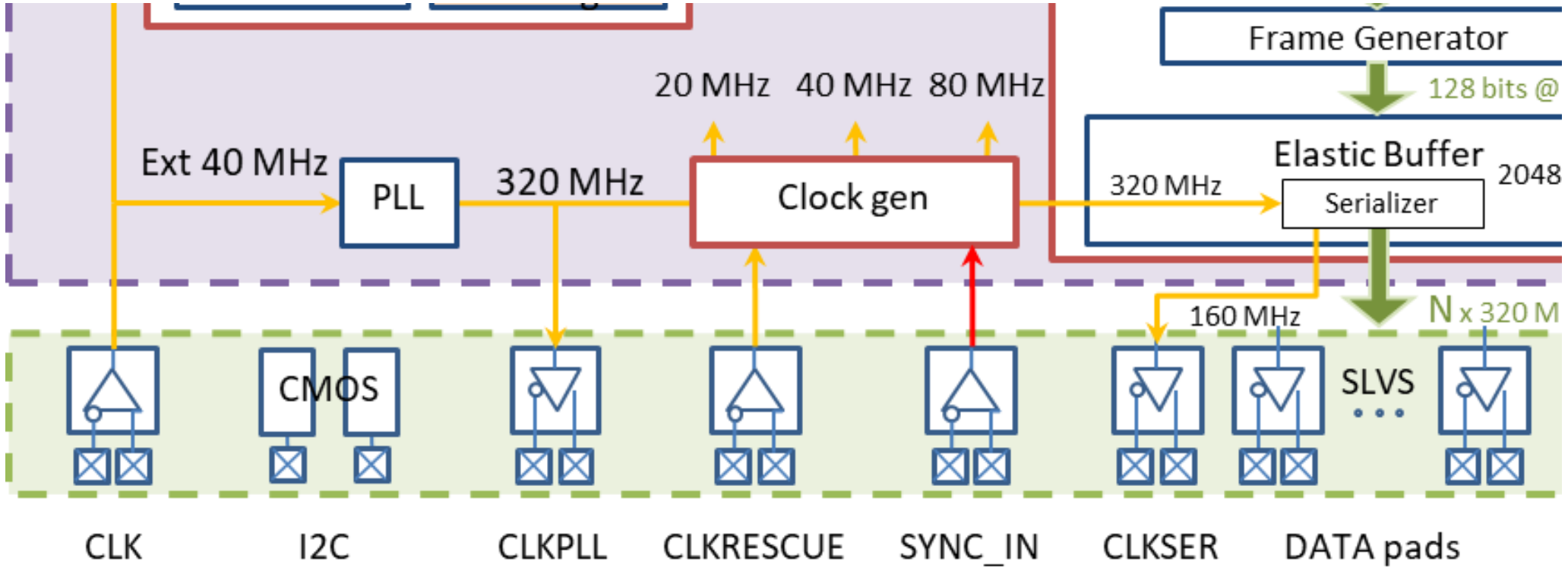
MIMOSIS diagram

- Matrix dimension: 1024 col. X 504 row
- Pixel dimension: 26.88 µm (height) x 30.24 µm (width)
- Integration time: 5 µs
- Tower Semiconductor 180 nm
- 4 sub-arrays for threshold adjustment
- 3 steps prototyping:
  - MIMOSIS0 small scale prototype (2017)
  - MIMOSIS1 first full scale prototype (2020)
  - MIMOSIS2 and 2.1 final prototype (2022-2023)
  - MIMOSIS3 pre-production run (2025)



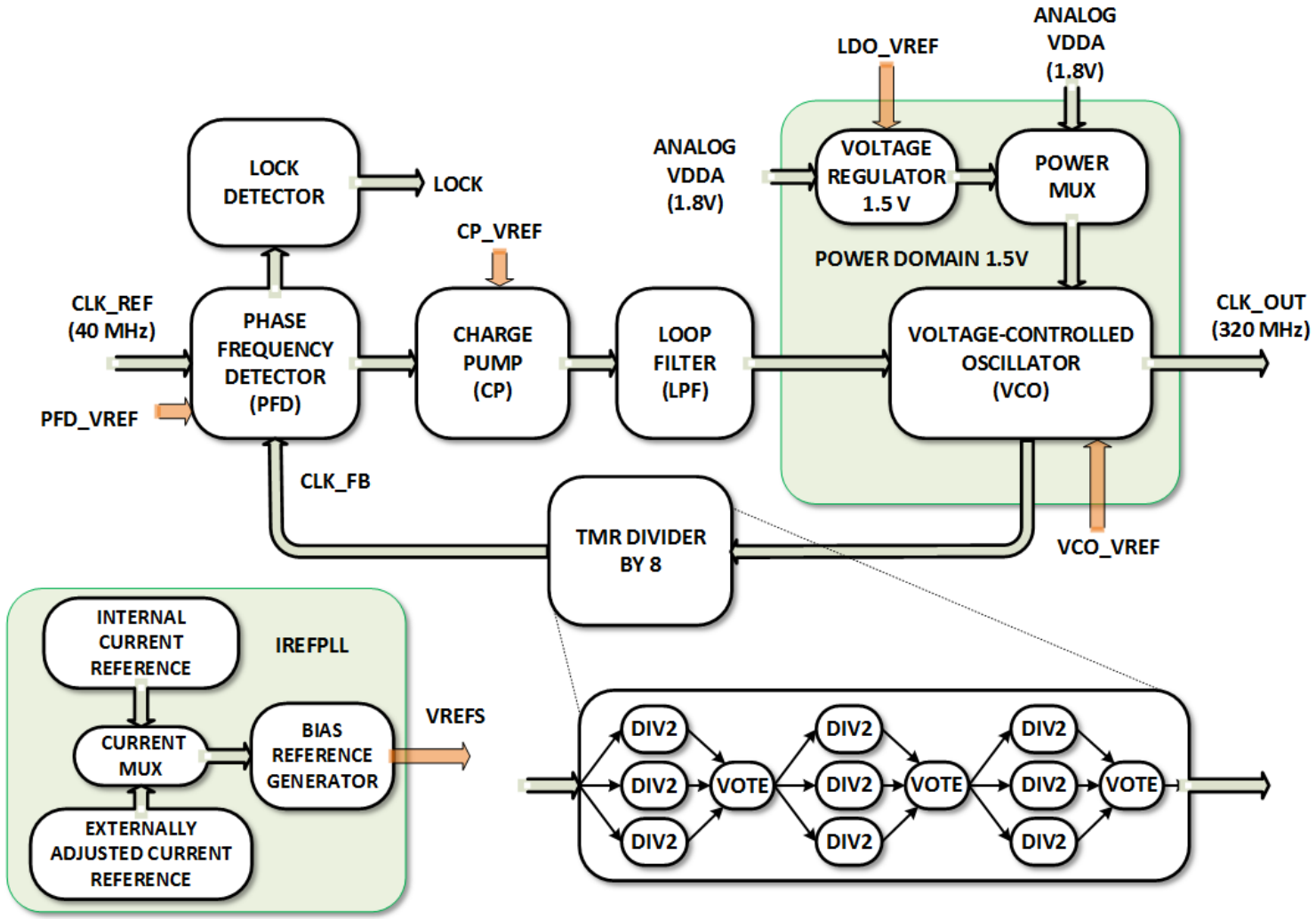
Clocks generation

- 320 MHz clock generated by a PLL from 40 MHz output clock (also use for slowcontrol)
- All other clocks are derived from the PLL output



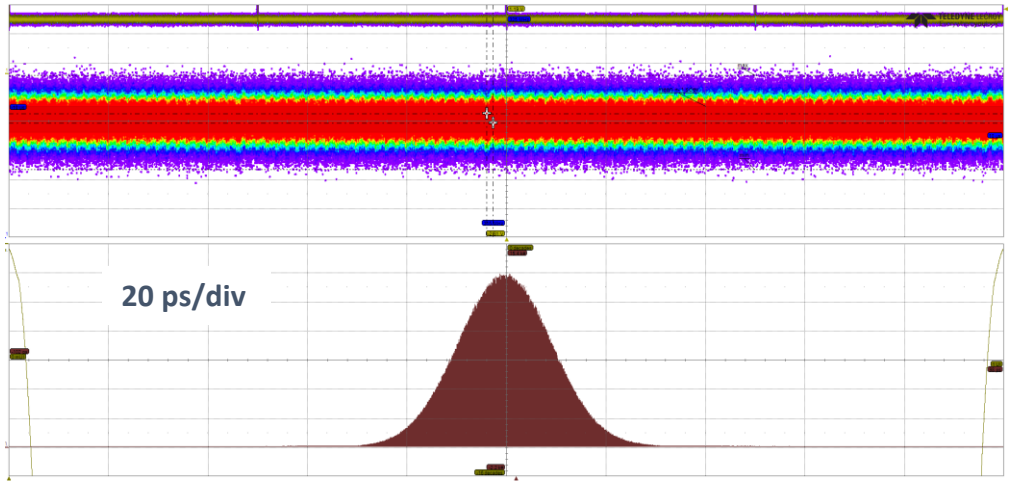
PLL architecture

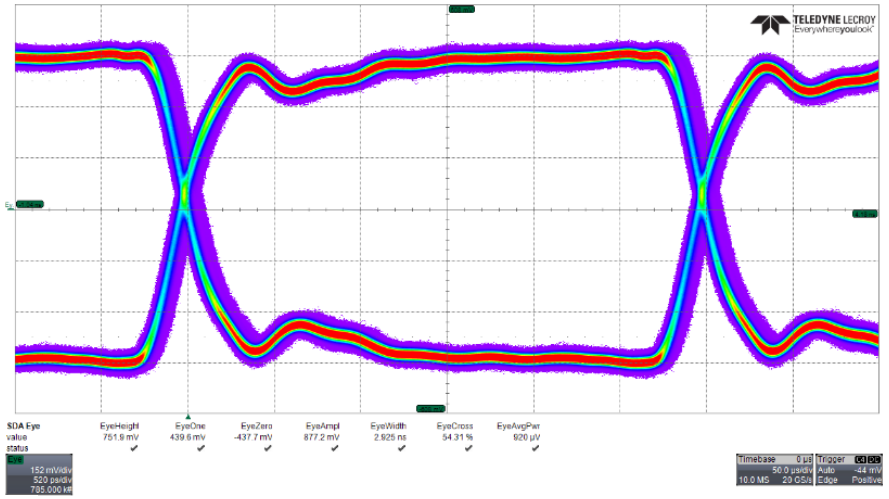
- VCO: Ring oscillator
- Local LDO for VCO
- High jitter observed:
  - LDO performances
  - Digital activity coupling



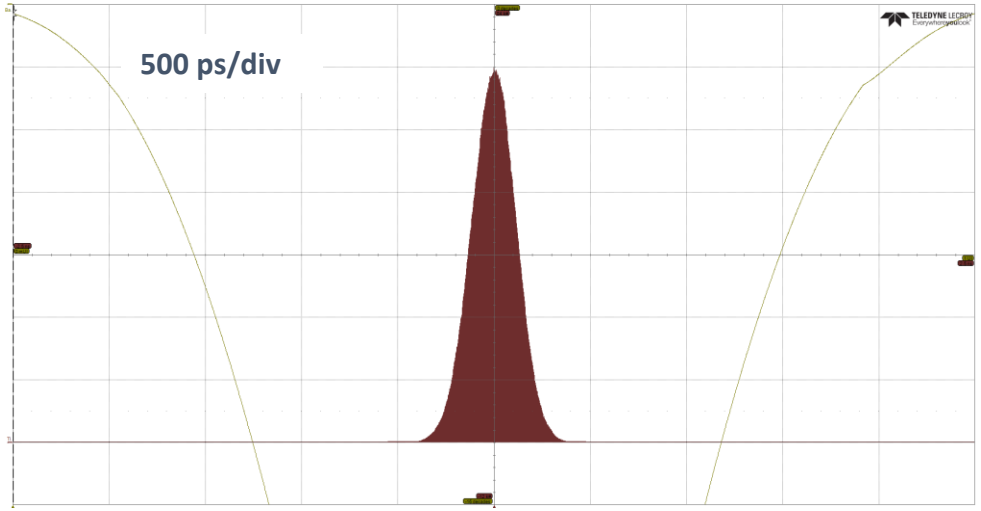
LDO issue

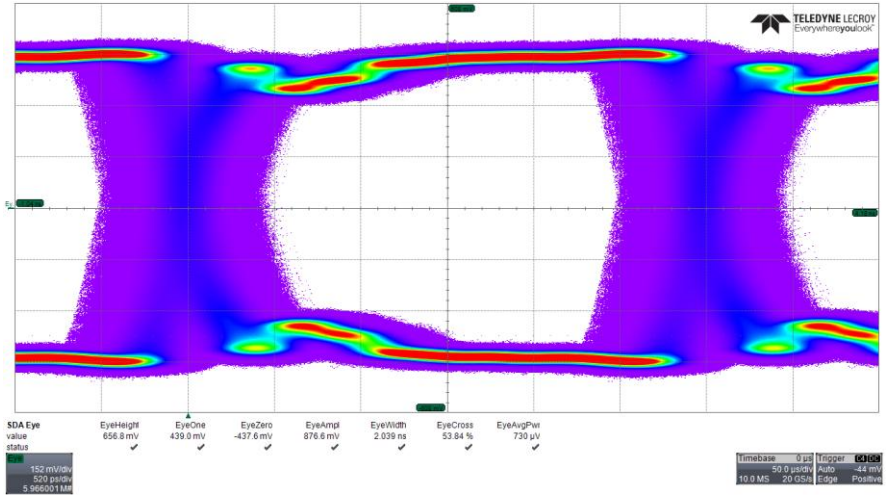
LDO disabled





LDO enabled





Digital activity coupling issue

- Output frequency is coupled with chip activity

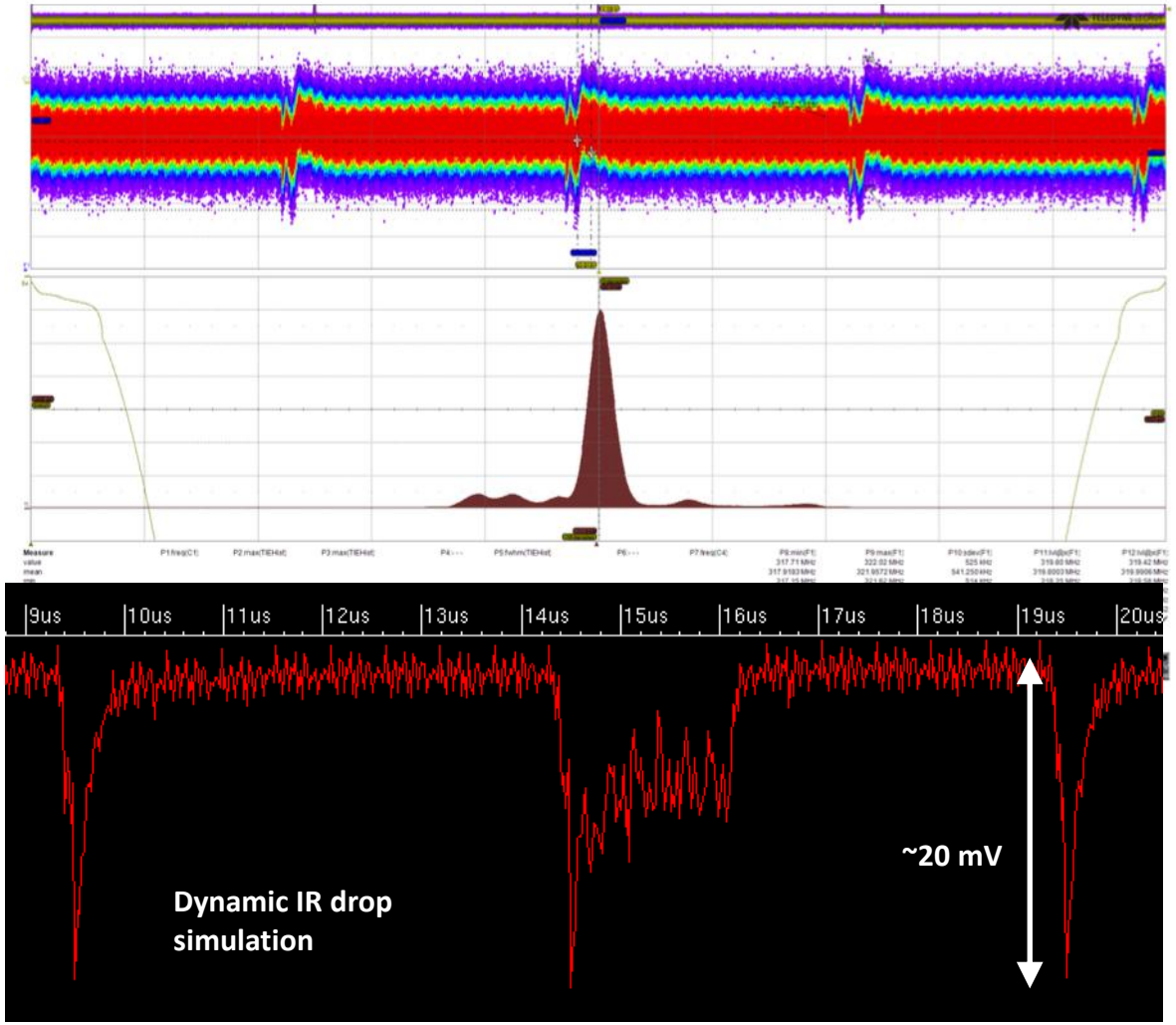


Fig 9. CLKPLL: TIE histogram and instantaneous clock frequency-tracking (default configuration)

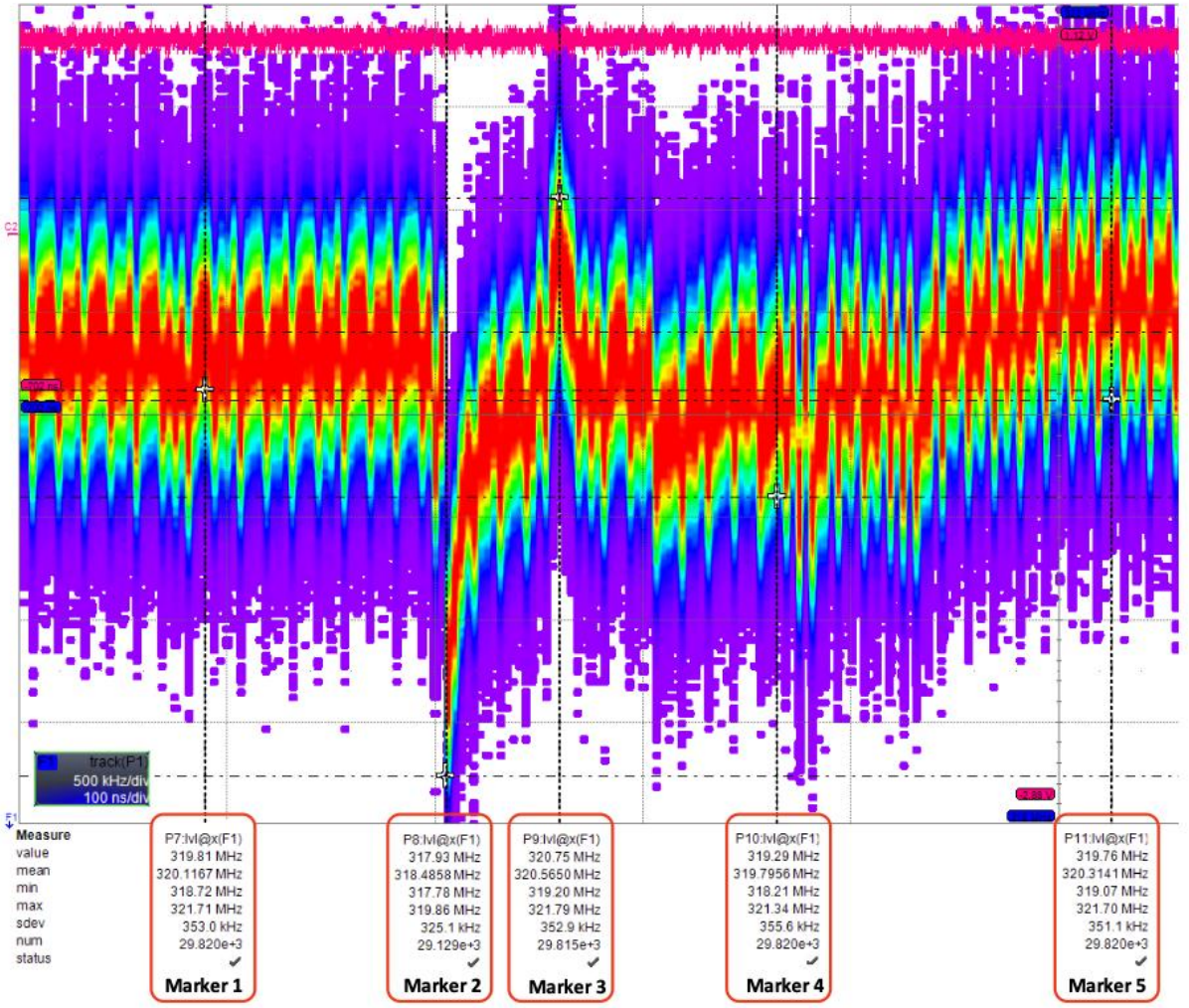


Fig 11.Instantaneous clock frequency-tracking in details (default configuration)

Modifications strategy

- LDO:
  - Increase bias current
  - Decoupled LDO bias and Charge pump currents
  - Add static current to avoid switch-on / switch-off

- Digital activity coupling:
  - Need to identify where it occurs
  - Replace digital power/ground by analogue ones