Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

PLATFORM C4PI - IPHC - IN2P3

MIMOSIS-2.1 PROTOTYPE

PRELIMINARY TESTS OF PLL

Revision Number: 202504141104

IMPORTANT INFORMATION

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C4PI = Centre de compétences de capteurs CMOS à pixels intégrés

Reference: C4PI_MIMOSIS21_PLL_PRE_TESTS (2025-04-14)

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MODIFICATIONS CHRONOLOGY

This is a short report for the preliminary tests of PLL integrated into MIMOSIS-2.1 chip.

Version 240612: Creation of the document.

Version 240703: Corrections.

Version 250414: Corrections.

1. GLOSSARY

Term	Description
DJ	Deterministic Jitter (peak-to-peak), bounded distribution
Duty Cycle	The Duty Cycle is a ratio between the positive pulse duration and the total period of a clock cycle
F_{in}	Input clock frequency
F_{out}	Output clock frequency
Integrated Phase Noise	Single sideband phase noise integrated over a measurement bandwidth from a start/stop offset frequency
IREFPLL	Reference current for biasing circuit
Jitter	In the context of the document, the jitter can be described as a clock jitter. The jitter is the deviation in time from the ideal periodicity of a periodic signal
LDO	A Low-dropout regulator is a linear voltage regulator capable to operate with the output voltage close to the supply voltage level
Locking Time	A time interval required from power-on or a predefined frequency change to obtain a desired phase difference between the input reference clock and the PLL output clock
MIMOSIS-2.1	The second generation proto-type of MIMOSIS sensors, a CMOS Monolithic Active Pixel Sensor for the Micro-Vertex Detector (MVD) of the CBM experiment at FAIR/GSI
Phase Noise	A frequency-domain representation of the noise arising from short-term, random fluctuations in the phase of a signal
PJ	Periodic Jitter (peak-to-peak)
RJ	Random Jitter (rms), unbounded Gaussian distribution
Proximity Board	The Proximity Board is a support PCB board for a MIMOSIS2.1 chip.
TIE	Time Interval Error of a clock signal edge is the time deviation of that edge from its ideal position measured from a reference point.
TJ(BER=$1e^{-12}$)	Peak-to-peak value of the Total Jitter at Bit Error Ratio of 10^{-12}
TMR	Triple Modular Redundancy is a digital design technique to mitigate circuit failures, in which three identical logic circuits are used to process the same input data to produce the output data set (redundant operations). A majority-voting circuit process the output data sets to produce a single output data set by using a majority-voting scheme.

2. INTRODUCTION

This document is primarily intended for circuit design and debugging purposes of MIMOSIS-2.1 sensor.

The PLL measurements presented in this document were carried out with the following sensors: MIMOSIS-2.1 chip mounted on the Proximity Board N° 60 (Standard process, EPI-50 um) or MIMOSIS-2.1 chip mounted on the Proximity Board N° 15 (Standard process, EPI-25 um). By default, the chip N° 60 was used for measurements, if not mentioned otherwise. The characterizations of the PLL were mainly carried out with the CLKPLL output.

If not mentioned otherwise, the following equipment were used for measurements:

- A PLL Evaluation Board Skyworks SI5344-D-EVB4 is used as a clock reference clock: Total Jitter (BER=$1e^{-12}$) = 33 ps, Random Jitter = 2.2 ps, Deterministic Jitter = 1.6 ps and Periodic Jitter = 2.6 ps
- Time Domain measurements with Teledyne LeCroy Serial Data Analyzer (SDA) 760Zi
- Frequency Domain measurement, like Phase Noise measurements with Tektronix RSA3308B Real-Time Spectrum Analyzer
- Power supply units: Agilent E3631A and Agilent E3632A

The PLL implemented in MIMOSIS-21 sensor is a Charge-pump PLL (CPPLL) with a constant multiplication factor of eight. The main goal of the MIMOSIS-21 PLL is to provide a low-jitter 320 MHz clock signal for the readout system of the MIMOSIS-21 sensor. The PLL block includes following additional features:

- An Integrated low-drop voltage regulator (LDO) for VCO
- A Lock detection circuitry
- A Divider with Triple Modular Redundancy (TMR) to protect against single-event upset errors (SEU)

A simplified block diagram of the PLL is presented below.

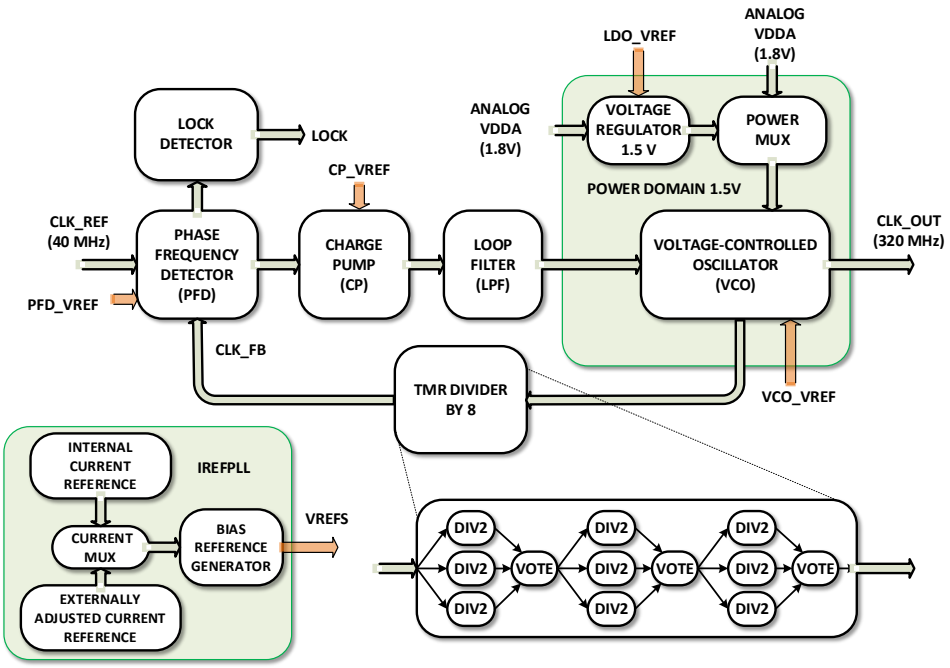

Fig 1. A simplified block diagram of PLL.

Table 1 lists the design parameters of the PLL.

Table 1. Design parameters (nominal values)

Parameter	Value	Description
F_{input}	40 MHz	Input reference clock frequency
F_{out}	320 MHz	PLL Output clock frequency
Clock Divider	8	Divisor value of the feedback divider
K_{VCO}	350 MHz/V	Gain of VCO
I_{CP}	10 uA	Charge pump current
Loop Filter, C1	1.5 pF	Loop filter capacitor C1 value (see the schematic below)
Loop Filter, C2	38.7 pF	Loop filter capacitor C2 value (see the schematic below)
Loop Filter, R1	15 k	Loop filter resistor R1 value (see the schematic below)

Loop Filter schematic (the second-order loop filter)

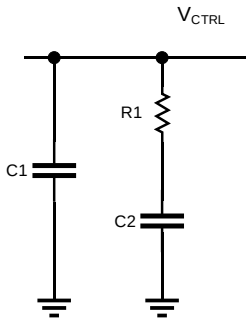

Fig 2. Schematic of the PLL loop filter

The PLL is a part of clock generation functionality of the MIMOSIS-2.1 chip. A simplified block diagram of the MIMOSIS-2.1 clocking scheme is shown in Fig. 3.

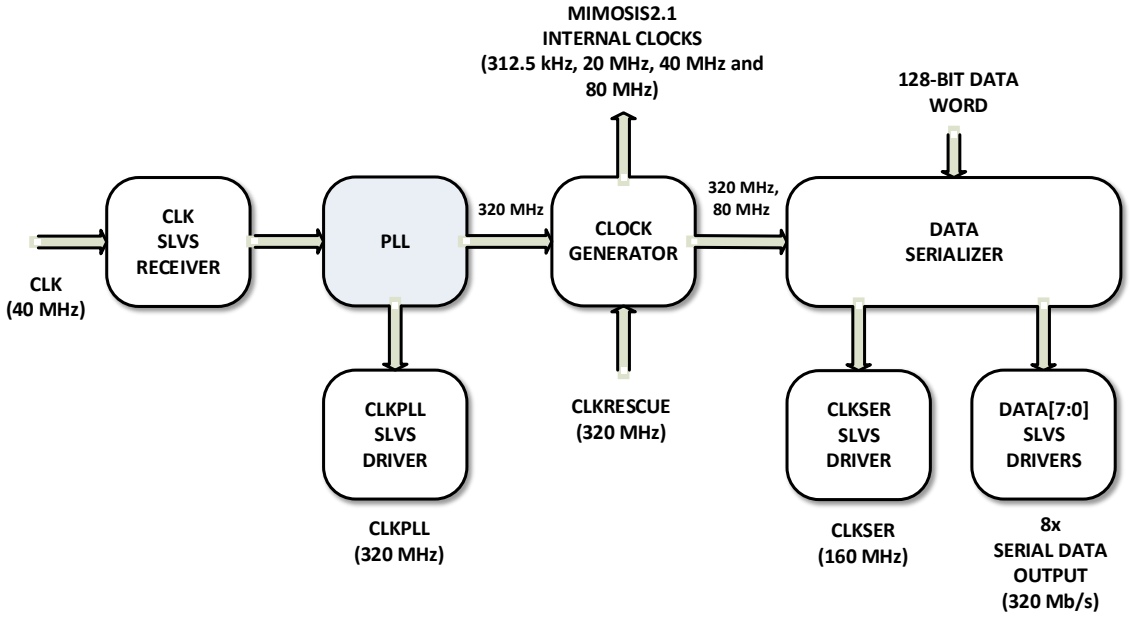

Fig 3.A simplified block diagram of the MIMOSIS-2.1 clocking scheme

According to the default-clocking scheme, the MIMOSIS-2.1 chip is designed to operate with a single clock signal of 40 MHz provided by CLK input. The clocking scheme includes a possibility to replace the PLL's output clock with an external clock via a CLKRESCUE input. The nominal frequency of the CLKRESCUE clock input is 320 MHz.

All the internal clock signals of MIMOSIS-2.1 are generated by a clock generator block. The clock generator block provides also two clock signals for a data serializer block. The data serializer block serializer a 128-bit data word for serial data outputs. The number of the serial data outputs in use can be programmed via the slow control interface. A CLKSER clock signal is provided for synchronization of the serial data outputs and it is a double data rate (DDR) clock signal operating at 160 MHz.

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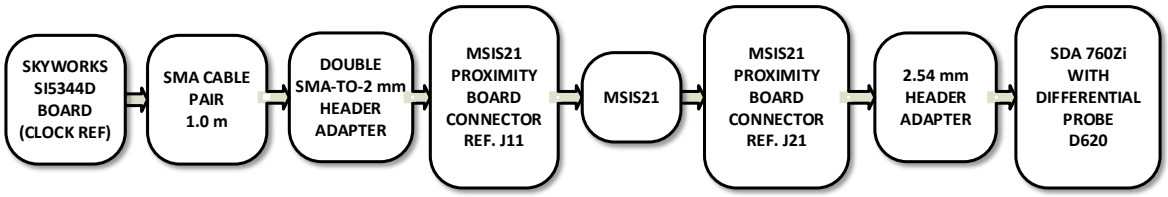
3. CLKPLL JITTER PERFORMANCE VERSUS INPUT CLOCK FREQUENCY

The following summarizes the jitter performance of MIMOSIS-2.1 PLL clock output in different reference clock frequencies (F_{in}). The following operating conditions were used:

- Chip is not started
- MIMOSIS-2.1 main clock input source is “clock rescue” and the source clock signal is disabled
- Internal IREFPLL current source is selected

Signal Path Diagram



3.1.PLL LDO DISABLED (DIS_PLL_LDO = 1)

The internal voltage regulator (LDO) was disabled and the PLL is powered directly by VDDA, the analog power supply (1.8V). The PLL’s operating frequency range is from 192 MHz to 640 MHz.

Table 2. CLKPLL Jitter performance versus input clock frequency (DIS_PLL_LDO=1)

F_{in} (MHz)	F_{out} (MHz)	TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
24	192	178	11.15	19.03	21.99
25	200	164	10.76	10.33	16.04
26	208	153	10.21	7.47	14.73
27	216	146	9.73	7.07	12.35
30	240	129	8.73	3.33	8.58
32	256	120	8.14	4.35	9.28
35	280	115	7.86	2.62	9.21
37	296	108	7.43	2.10	9.07
40	320	105	7.07	3.70	6.51
42	336	105	7.10	3.34	8.41
45	360	97	6.63	2.77	8.11
47	376	99	6.73	3.19	6.24
50	400	96	6.58	1.97	4.95
55	440	91	6.35	0.8	6.37
60	480	90	6.18	1.94	5.27
65	520	85	5.86	1.6	6.76
70	560	74	5.07	1.29	5.78
75	600	89	5.30	13.47	21.63
80	640	86	5.19	12.38	20.69

Total Jitter (peak-to-peak value at Bit Error Ratio = 10-12)

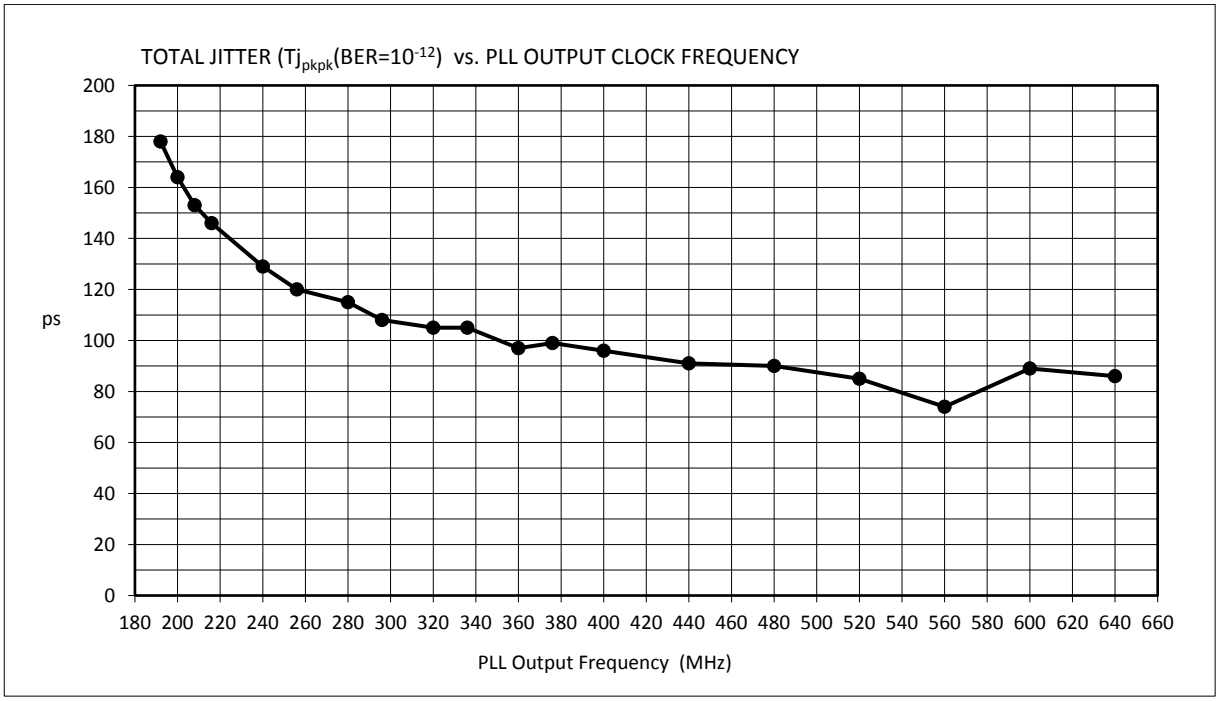


Fig 4. TJ(BER=$1e^{-12}$) versus input clock frequency (DIS_PLL_LDO=1)

3.2.PLL LDO ENABLED (DIS_PLL_LDO = 0)

The internal voltage regulator (LDO) was enabled and the PLL circuitry is powered with the LDO (1.5V). The PLL's operating frequency range is from 200 MHz to 528 MHz when the LDO is active.

Table 3. CLKPLL Jitter performance versus input clock frequency (DIS_PLL_LDO=0)

F_{in} (MHz)	F_{out} (MHz)	TJ(BER=$1e^{-12}$) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
25	200	2555	177.7	26.4	133.0
30	240	2118	140.9	108.9	185.2
40	320	1507	93.3	176.7	204.6
50	400	1209	76.4	120.4	140.3
60	480	686	43.4	67.9	94.3
65	520	728	45.3	82.2	115.8
66	528	794	50.8	69.3	106.5
70	529	-	-	-	-

Total Jitter (peak-to-peak value at Bit Error Ratio = 10-12)

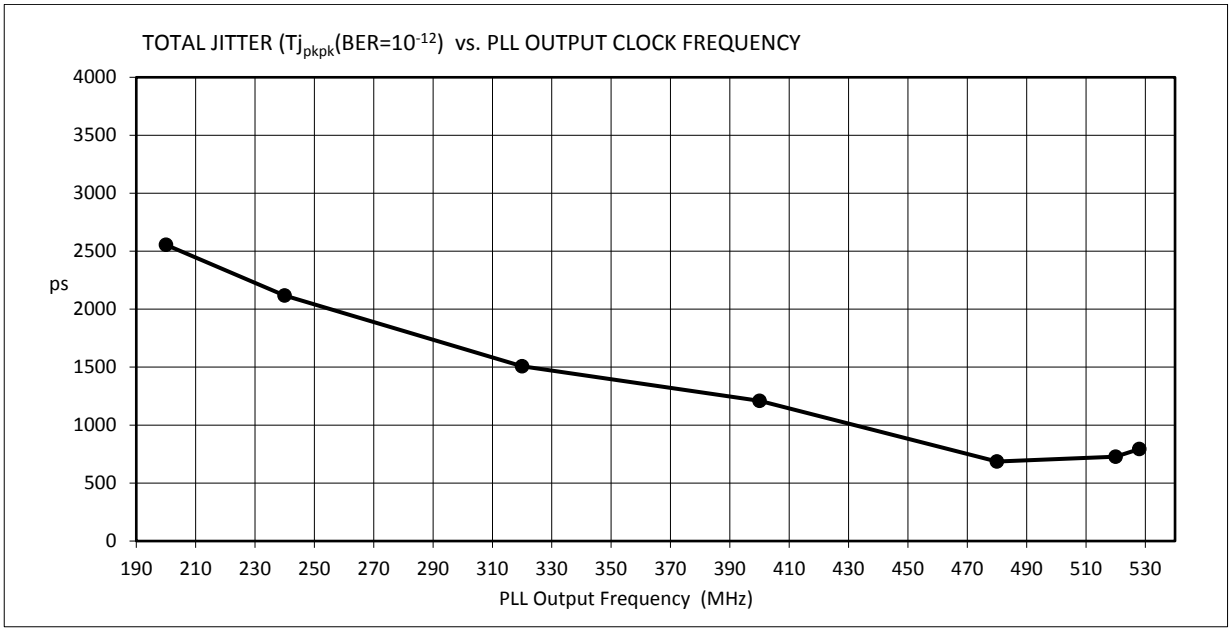


Fig 5. TJ(BER=$1e^{-12}$) versus input clock frequency (DIS_PLL_LDO=0)

4. JITTER PERFORMANCE VERSUS IREFPLL BIAS CURRENT

The following operating conditions were used:

- Chip is started manually (software mode)
- PLL output clock frequency is 320 MHz, the CLK_SER and the Serial Data[0] output each generate a clock signal of 160 MHz
- Pattern mode and Data Marker output are enabled
- Number of serial outputs = 2
- Clock Rescue disabled on S3 Lab board
- Slow control register values of the sequencer block is defined in Table 24 (Appendix A)
- The DACs are set to the values shown in Table 26 (Appendix A)

The jitter measurement were carried out for the PLL output, the serializer output clock (CLKSER) and the serializer data output D0 for reference.

4.1. PLL LDO DISABLED (DIS_PLL_LDO = 1)

Table 4. Jitter performance versus IREFPLL bias current (DIS_PLL_LDO=1)

	CLKPLL				**CLKSER**	**DOUT[0]**
IREFPLL (uA)	TJ(BER=1e^{12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)	TJ(BER=1e^{12}) (ps)	TJ(BER=1e^{12}) (ps)
(internal) 1	523	29.3	105.5	175.01	663	737
1	486	26.61	106.46	168.75	679	751
3	344	21.81	32.83	26.39	592	620
5	266	15.56	44.17	25.62	483	532
10	224	11.59	58.52	43.24	439	496
14	204	11.54	39.69	27.70	427	490

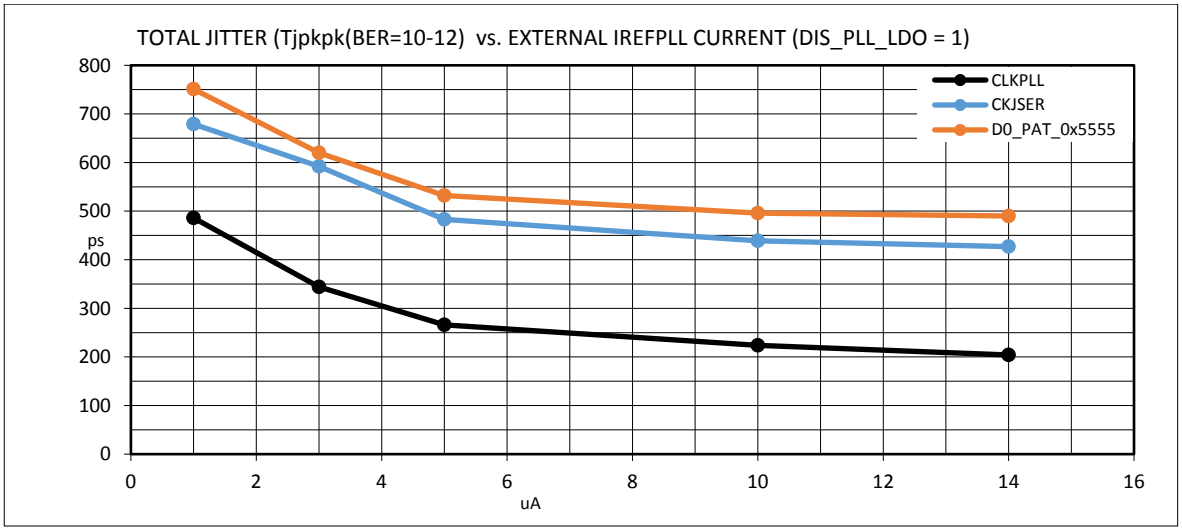


Fig 6.TJ(BER=1e^{-12}) versus IREFPLL bias current (DIS_PLL_LDO=1)

4.2.PLL LDO ENABLED (DIS_PLL_LDO = 0)

Table 5. Jitter performance versus IREFPLL bias current (DIS_PLL_LDO=0)

	CLKPLL				CLKSER	DOUT[0]
IREFPLL (uA)	TJ(BER=1e^{12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)	TJ(BER=1e^{12}) (ps)	TJ(BER=1e^{12}) (ps)
(internal) 1	1530	97.2	143.2	207.6	1678	1716
1	1592	102.1	135.5	201.9	1736	1778
3	781	50.6	58.6	72.42	938	1005
5	499	33.57	20.48	29.81	669	740
10	327	21.67	17.56	19.85	515	581
14	311	20.75	15.55	18.84	505	550

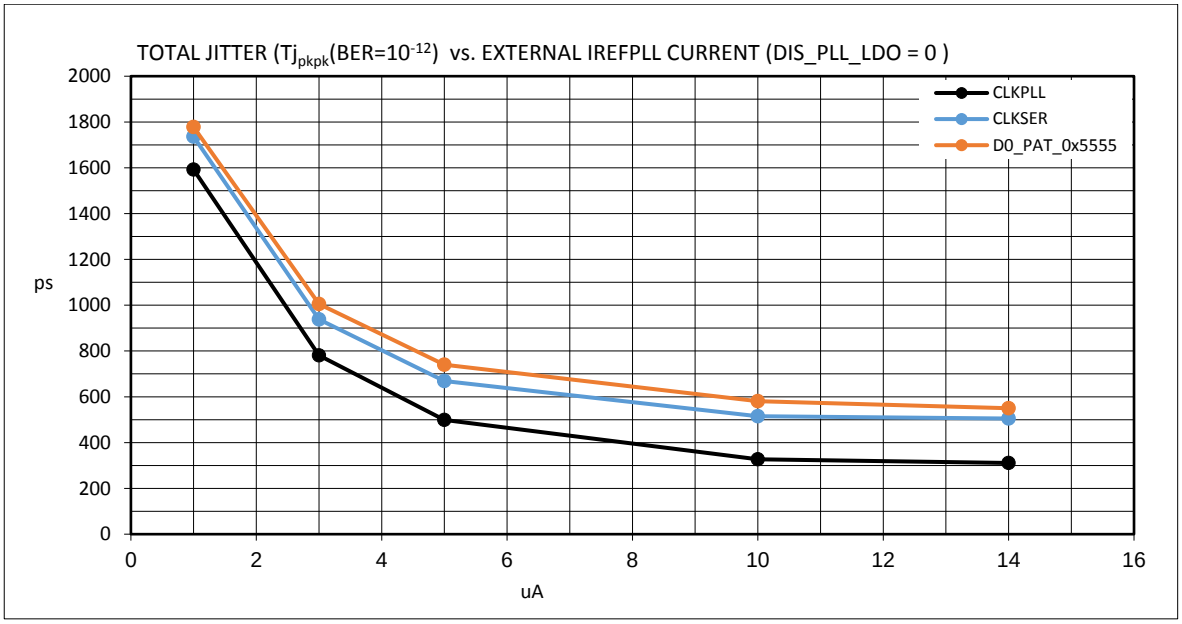


Fig 7. TJ(BER=1e^{-12}) versus IREFPLL bias current (DIS_PLL_LDO=0)

5. JITTER PERFORMANCE VERSUS PLL TRIM VALUE

The operation conditions described in previous Chapter 4 were used in this measurement, except the Internal IREFPLL was selected (1uA). The PLL TRIM results in a fine adjustment compared to the external IREFPLL adjustment with a resistor.

5.1. PLL LDO DISABLED (DIS_PLL_LDO = 1)

The TRIM values from zero to two have a negligible effect on jitter.

Table 6. Jitter performance versus TRIM value (DIS_PLL_LDO=1)

TRIM Value	TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
0	506	26.46	128.39	186.39
1	513	27.09	126.19	186.61
2	512	27.4	121.8	181.17
3	504	26.9	120.1	177.12
4	494	26.67	113.82	167.95
5	488	26.94	103.26	159.60
6	475	26.24	100.96	151.85
7	465	26.05	93.15	144.06

5.2. PLL LDO ENABLED (DIS_PLL_LDO = 0)

The TRIM values from zero to one have a negligible effect on jitter.

Table 7. Jitter performance versus TRIM value (DIS_PLL_LDO=0)

TRIM Value	TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
0	1696	104.9	199.9	211.84
1	1698	104.6	206.7	205.4
2	1615	101.3	169.7	206.69
3	1621	99.4	203.1	204.82
4	1575	97.7	181.6	211.07
5	1530	97.2	143.8	212.19
6	1497	77.1	408.8	197.59
7	1449	87.4	202.3	198.19

6. CLKPLL JITTER PERFORMANCE VERSUS SEQUENCER ACTIVITY

In this measurement, the effect of the individual control signal of the sequencer block to the jitter performance of the PLL was measured. The Jitter measurements were carried out in two steps, firstly by enabling individual sequencer functions one at a time and secondly by disabling functionality one at a time.

The sequencer block generates the clock-synchronized control signals for steering of the pixel matrix. Some of these steering signals control pixel-level functionalities, e.g. PIX_LOAD, powered by an analog power supply, VDDA.

In the PLL block, the VCO and the reference biasing generators are also powered by VDDA if the LDO is disabled. Thus, the voltage fluctuations of the VDDA resulting in the activity of the pixel matrix are propagated to the PLL block

The sequencer control signals are configurable. The block generates rectangular pulse waveforms for control signals with a specified pulse start time and pulse width. The waveform parameters are programmed via slow control interface. This programming feature allows one's disable or enable the sequencer functions one by one.

For operation of the sequencer block, the MIMOSIS-2.1 chip must be started.

The following operating conditions were used (base configuration):

- The LDO is disabled
- Internal IREFPLL selected (1uA)
- The Data Marker is enabled
- Number of serial outputs = 2
- Pattern mode disabled
- Clock Rescue disabled on S3 Lab board
- Slow control register values of the sequencer block is defined in Table 24 APPENDIX A.2.1: NOMINAL SEQUENCER CONFIGURATION and in Table 25 APPENDIX A.2.2: BASE SEQUENCER CONFIGURATION
- The DACs are set to the values shown in Table 28 (Appendix A)

Two following Figures (8 and 9) show multi-plots with a TIE histogram of the CLKPLL, instantaneous clock frequency-tracking plot in persistence mode.

In Fig. 8, the sequencer is set to the base configuration with the minimum activity. The TIE histogram consists of one peak. Total Jitter, TJ(BER=$1e^{-12}$) is 128 ps or 0.04 UI at 320 MHz.

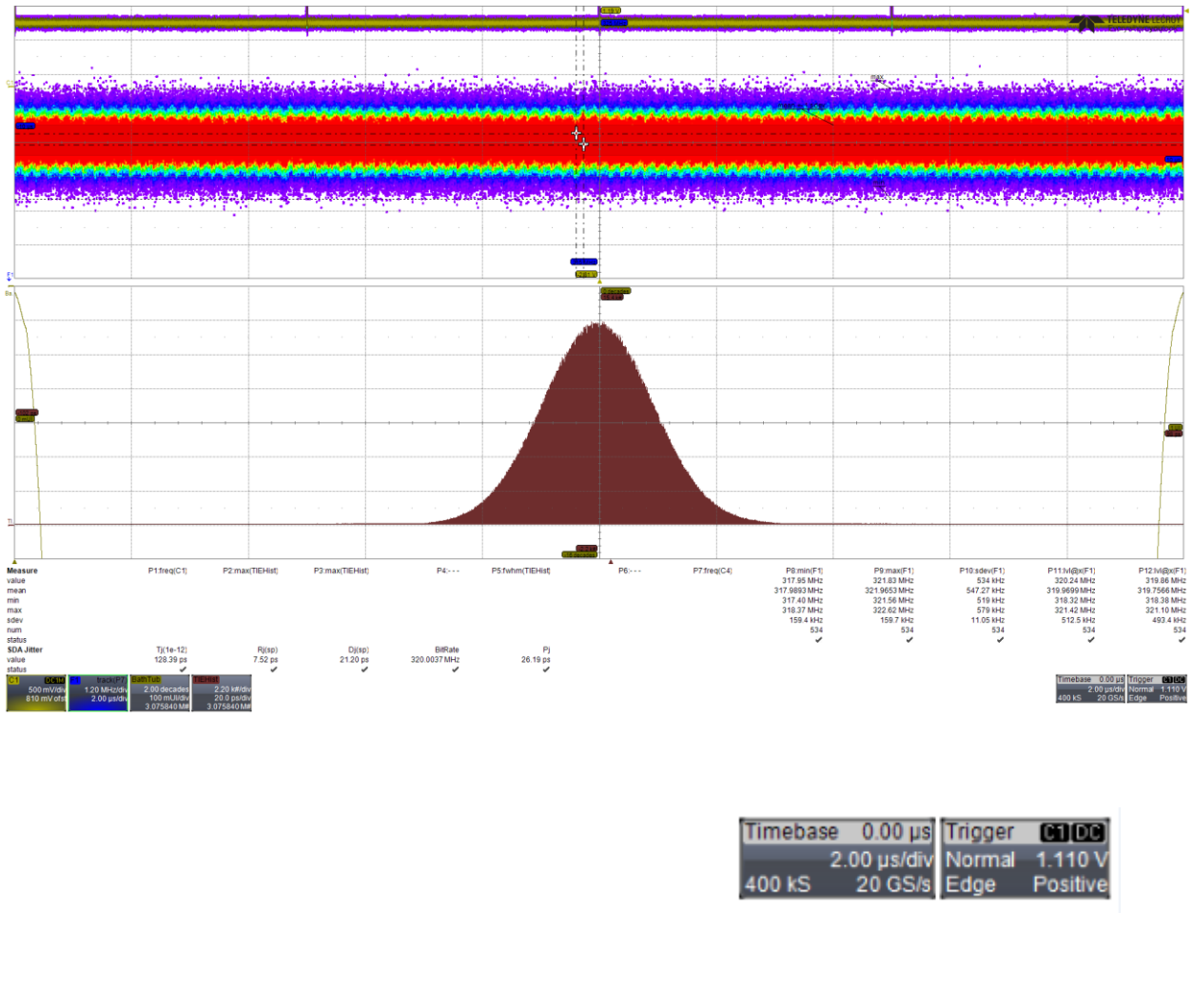


Fig 8. CLKPLL: TIE histogram and instantaneous clock frequency-tracking (base configuration)

In Fig. 9, all the sequencer register are programmed with the nominal configuration values.

The TIE histogram is multimodal with four to five peaks. The instantaneous CLKPLL frequency changes can be observed in frequency-tracking plot in persistence mode. Total Jitter, TJ(BER=1e^{-12}) is 553 ps or 0.18 UI at 320 MHz.

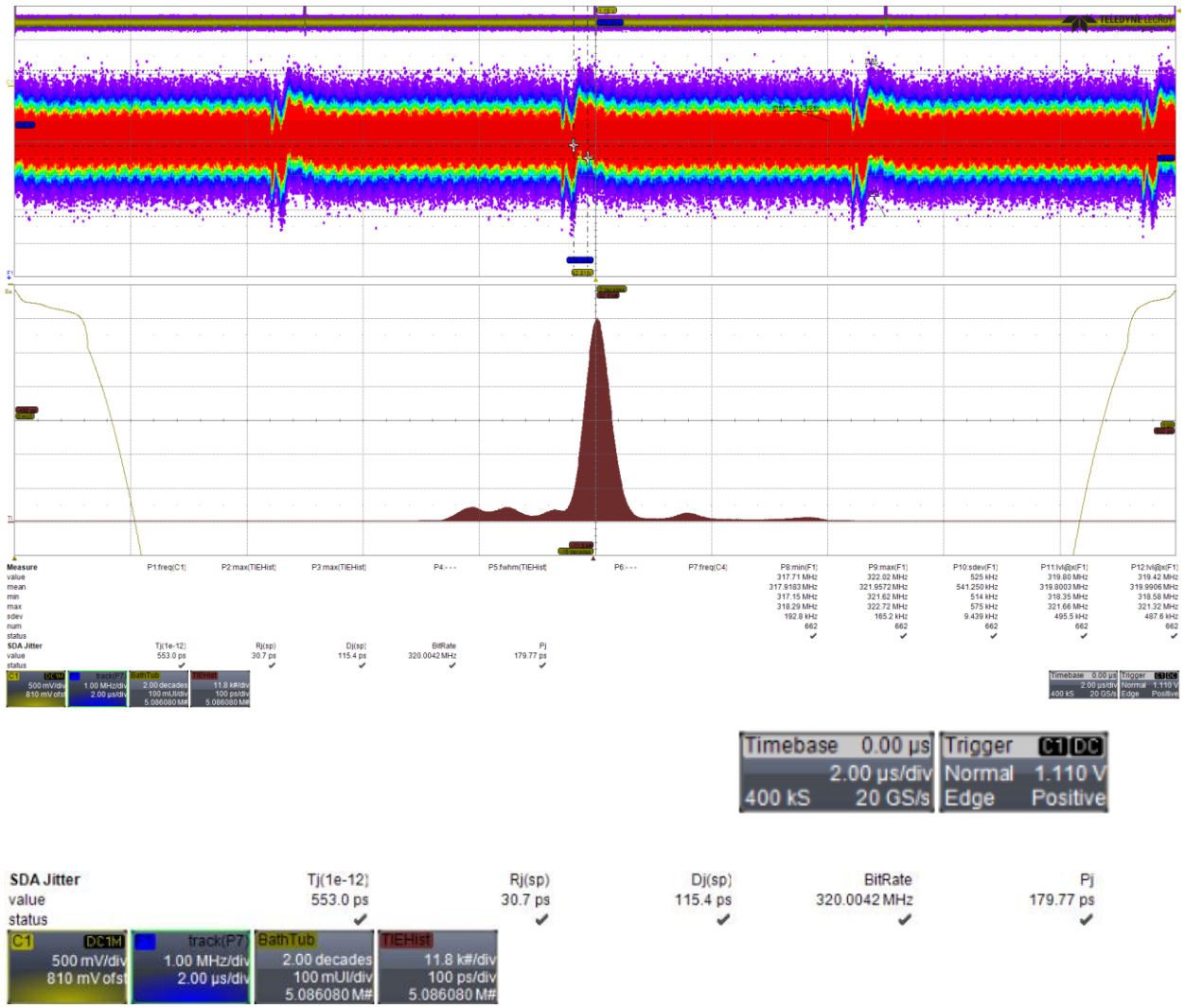


Fig 9. CLKPLL: TIE histogram and instantaneous clock frequency-tracking (default configuration)

More detailed instantaneous clock frequency-tracking plot in persistence mode is shown in Fig. 10 and Fig. 11. The tested chip is MIMOSIS-2.1 N° 15. The data marker output of the MIMOSIS-2.1 is acquired with the channel 2 (shown in red) and it is used as a trigger. The CLKPLL frequency value is presented in clock cycle basis. The frequency measurement markers (5) are positioned into the frequency-tracking plot to shown the instantaneous frequency values. At the position of the Marker 2 in Fig. 11, a frequency shift of the clock signal can be observed. The maximum frequency deviation is approximately 3 MHz and the mean value of the frequency deviation is about 1.6 MHz at the position of the Marker 2. The frequency deviation is mainly resulting of voltage drop in VDDA power supply. The total duration of the process to return to nominal operating frequency is approximately 300 ns.

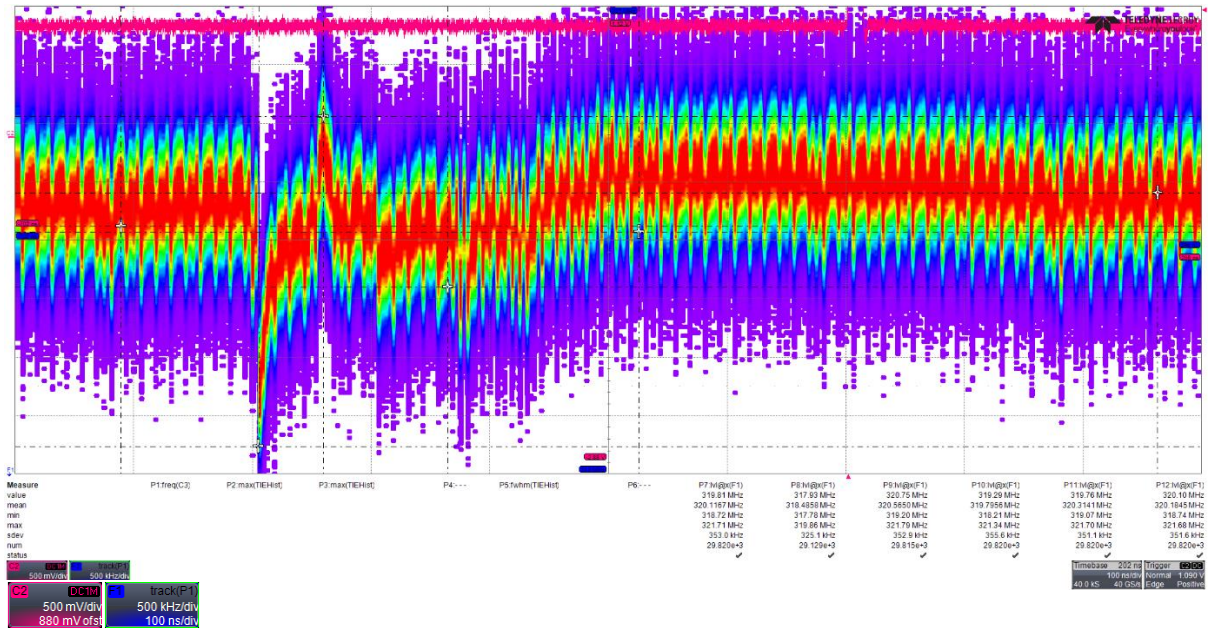


Fig 10. Instantaneous clock frequency-tracking (default configuration)

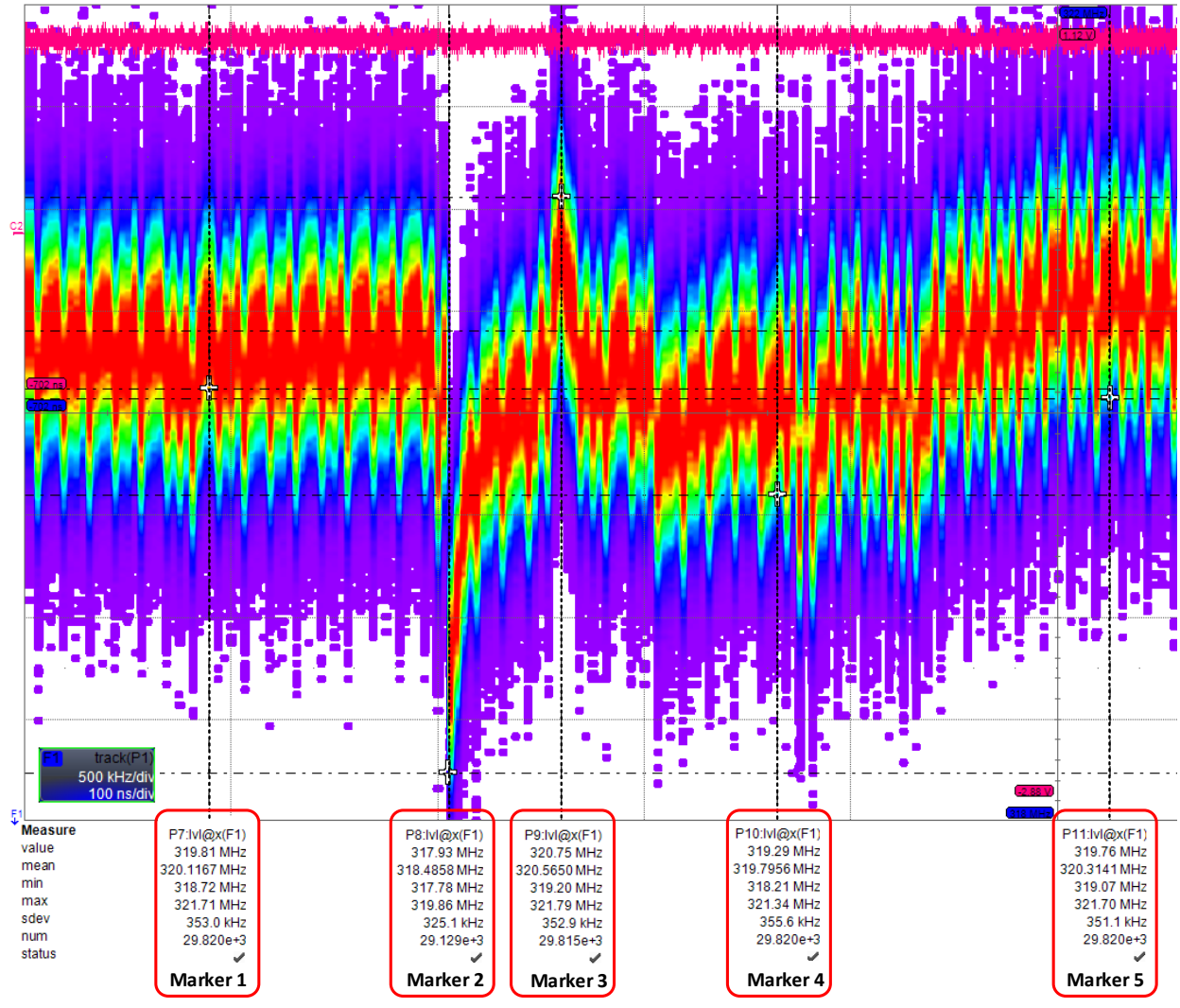


Fig 11.Instantaneous clock frequency-tracking in details (default configuration)

6.1. ADDITIVE EFFECT OF A SINGLE SEQUENCER FUNCTION ON JITTER (1/2)

The table 8. presents measured jitter values when only one sequencer function is enabled at a time. The main jitter source of the sequencer block is the PIX_LOAD function. When the PIX_LOAD function is active the Total Jitter (BER=$1e^{-12}$) is 334 ps (Fig. 9).

Table 8. CLKPLL Jitter performance versus sequencer activity (one function enabled at a time)

Sequencer function enabled	**TJ(BER=$1e^{-12}$) (ps)**	**RJ (ps)**	**DJ (ps)**	**PJ (ps)**
BASE CONFIGURATION	128	7.52	21.2	26.19
PIX_LOAD_A =0x0, PIX_LOAD_B = 0x1	334	20.44	42.75	53.39
DP_TOKEN_A=0x2, DP_TOKEN_A=0x3	183	10.76	29.45	35.07
PIXREAD_A=0x0, PIXREAD_B=0x61	127	7.19	24.24	27.02
DPEND_A=0x63, DPEND_B=0x64	222	12.72	40.59	31.31
PIXRSTB_A=0x62, PIXRSTB_B=0x63	283	17	40.57	51.04
MKSEQ1_A=0x0, MKSEQ1_B=0X2	127	7.11	25.04	27.53
MKSEQ2_A=0x0, MKSEQ2_B=0X2	128	7.13	26.30	27.70
DEFAULT CONFIGURATION	553	30.7	115.4	179.77

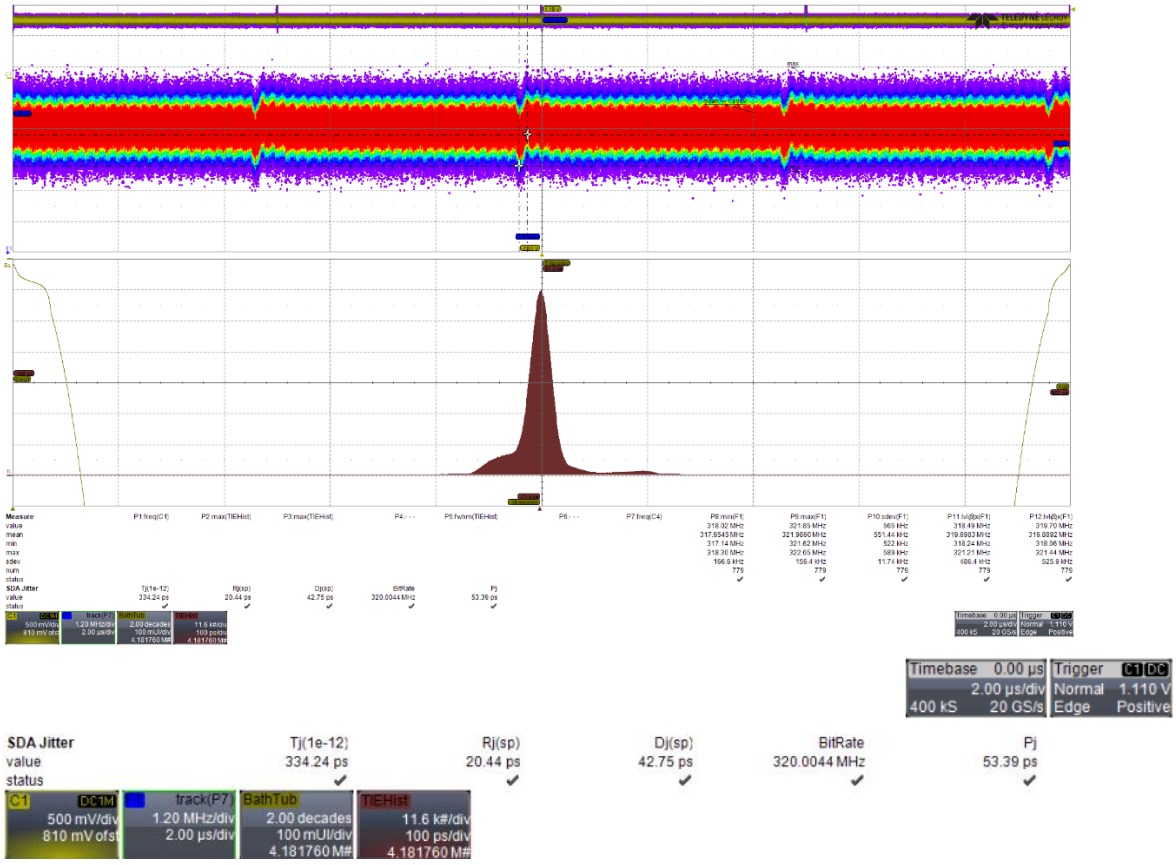


Fig 12. CLKPLL: TIE histogram and instantaneous clock frequency-tracking (base configuration with PIX_LOAD)

6.2. ADDITIVE EFFECT OF A SINGLE SEQUENCER FUNCTION ON JITTER (2/2)

The following Table 9. shows measured jitter values when one of the sequencer functions is disabled at a time. The default configuration values differs slightly (25 ps) from the values presented in the previous chapter. The main jitter source of the sequencer block is the PIX_LOAD function.

Table 9.CLKPLL Jitter performance versus sequencer activity (one function disabled at a time)

Sequencer function disabled	TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
DEFAULT CONFIGURATION	528	28.7	121.0	175.68
PIX_LOAD_A =0x0, PIX_LOAD_B = 0x0	322	15.77	97.22	127.95
DP_TOKEN_A=0x2, DP_TOKEN_A=0x3	465	27.3	76.4	134.57
PIXREAD_A=0x0, PIXREAD_B=0x61	536	29.2	119.7	179.03
DPEND_A=0x63, DPEND_B=0x64	412	21.19	109.51	161.58
PIXRSTB_A=0x62, PIXRSTB_B=0x63	529	33.0	58.5	93.89
MKSEQ1_A=0x0, MKSEQ1_B=0X2	517	28.6	108.5	166.11
MKSEQ2_A=0x0, MKSEQ2_B=0X2	537	30.8	97.6	162.98

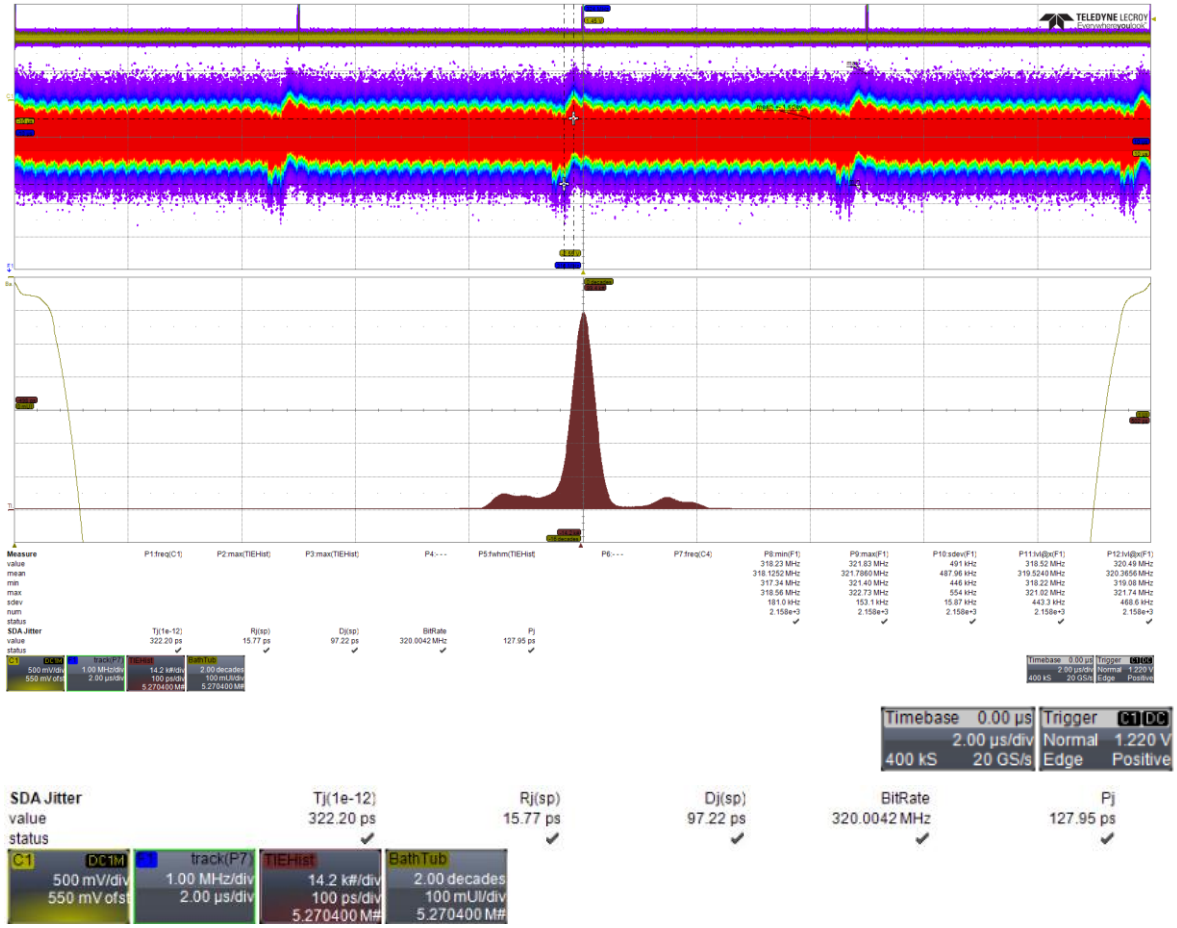


Fig 13. CLKPLL: TIE histogram and instantaneous clock frequency-tracking (default configuration without PIX_LOAD)

7. CLKPLL JITTER PERFORMANCE VERSUS INPUT CLOCK WITH ADDITIONAL RANDOM JITTER

The jitter performance of the PLL depends of the quality of the input clock signal. In following measurements, the Gaussian noise is added to the reference clock signal generated by the SI5344-D-EVB4 board via an adapter board for RJ injection (ADAPT_SMA_RJ_NOISE). The ADAPT_SMA_RJ_NOISE board is shown in Fig. 14.

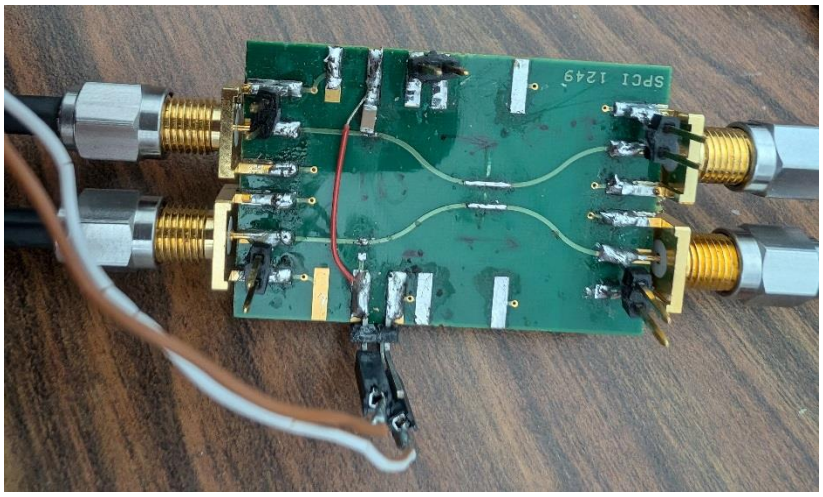


Fig 14. Adapter board for RJ injection (ADAPT_SMA_RJ_NOISE)

The Gaussian noise signal generated by the Agilent 33250A Function Generator is injected via a SMD capacitor (1 uF, X7R, ref. KEMET C1206C105K3RACAUTO) to the positive clock output signal of the SI5344-D-EVB4 board. The offset voltage of the noise signal is fixed to 620 mV with output Z = 50 ohm and the amplitude of the noise signal is set to values shown in the following Table 10.

Table 10. Jitter Measurement of the clock reference with injected noise

Noise amplitude, VAMP (mV)	TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
1	69	4.684	2.296	5.90
50	80	5.47	1.86	5.61
100	105	7.34	0.00	4.51
200	169	11.87	0.00	1.83
300	244	17.11	0.00	2.04
400	322	22.59	0.00	3.13
500	403	28.29	0.00	2.99

The Table 10. shows measured jitter parameters in listed noise amplitude values. The Random Jitter is only present starting from the noise amplitude value of 100 mV.

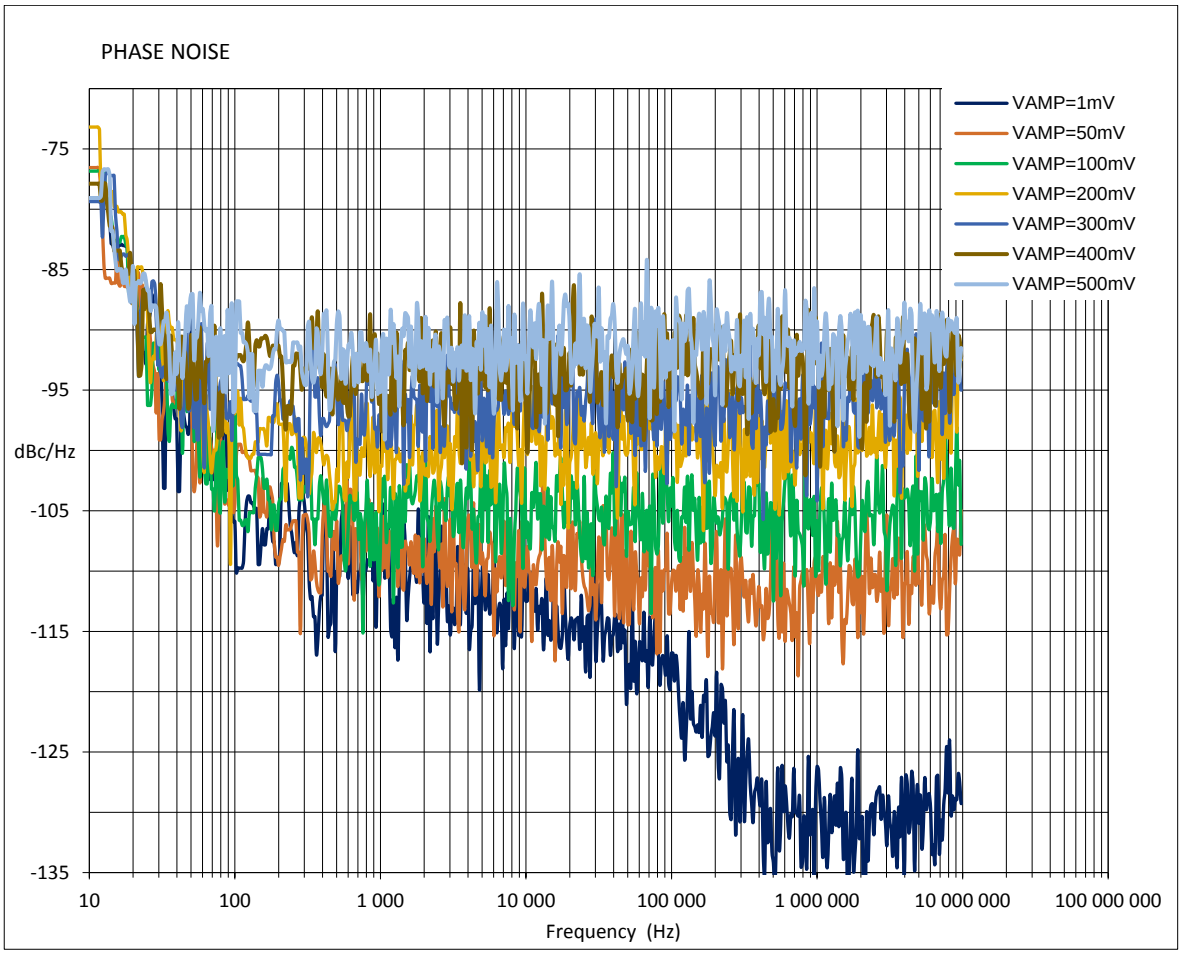


Fig 15. Phase noise plot of the reference clock with additional RJ noise amplitude level.

Table 11.Phase noise Measurement of the clock reference with injected noise

Noise amplitude (mV)	Integrated Phase noise (deg RMS)	Random Jitter (ps RMS)	Max Periodic Jitter (ps)
1	0.11	7.5	58
50	0.86	59.619	148
100	1.66	115.6	318
200	3.71	257.6	344
300	4.77	330.9	842
400	6.17	428.6	884
500	8.0	555.3	1056

The operating conditions were the same as it described in Chapter 6. “CLKPLL JITTER PERFORMANCE VERSUS SEQUENCER ACTIVITY”, except the chip is not started in this measurement.

In Fig. 16 is shown measured Total Jitter TJ(BER=1e^{-12}) versus amplitude of Gaussian noise injected to the reference clock signal. The obtained results in different IREFPLL bias current conditions are presented in Chapters 7.1 to 7.3.

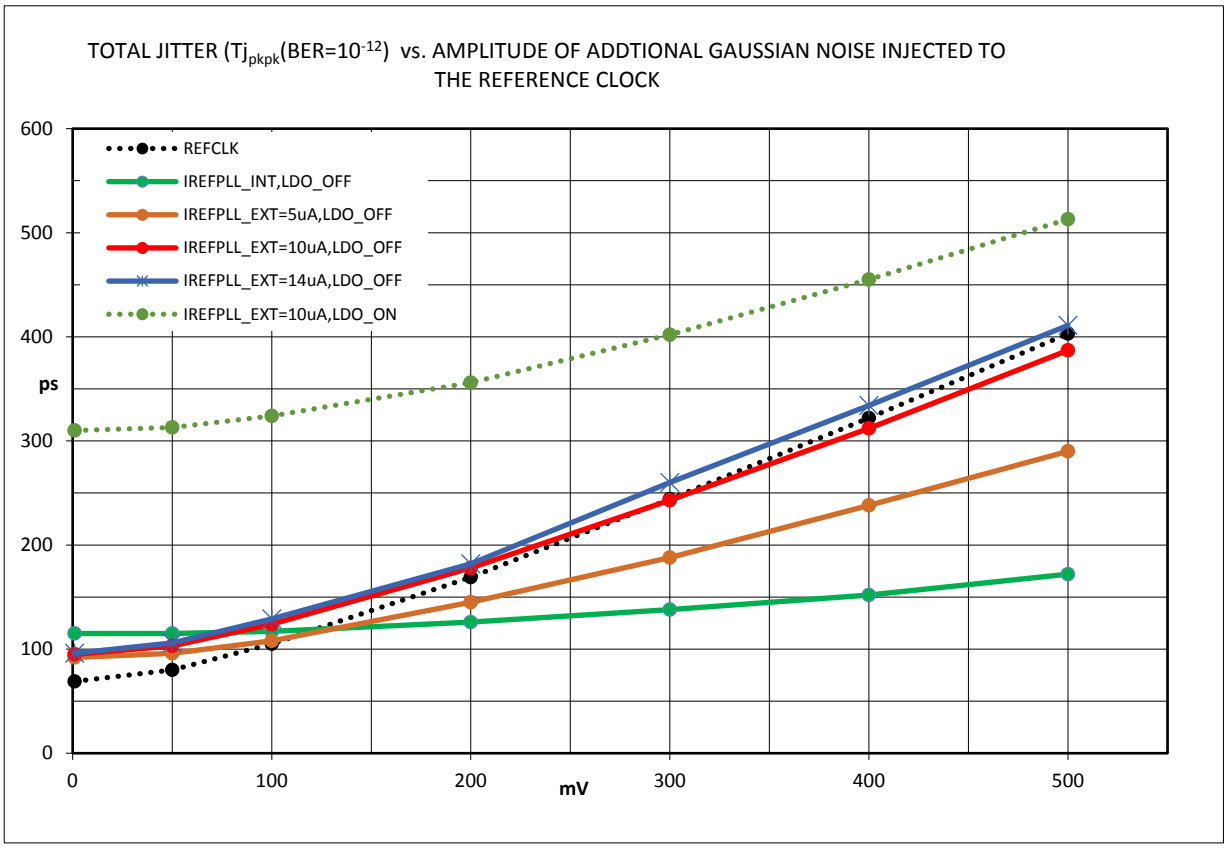


Fig 16. TJ(BER=1e^{-12}) versus amplitude of Gaussian noise injected to the clock reference signal

7.1. INTERNAL IREFPLL AND LDO DISABLED

The VDDA power supply noise related to the sequencer block activity is not present because the chip was not started. The Random Jitter on the reference clock signal is filtered out by PLL (loop BW = 1 MHz).

Table 12. CLKPLL Jitter performance versus reference clock with RJ (internal IREFPLL, LDO disabled)

Noise amplitude (mV)	Ref clock TJ(BER=1e^{-12}) (ps)	TJ(BER=1e^{12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
1	69	115	7.28	11.18	19.47
50	80	115	7.28	11.42	19.34
100	105	117	7.46	10.48	19.50
200	169	126	8.07	10.39	20.22
300	244	138	9.00	9.88	20.54
400	322	152	9.78	12.55	21.62
500	403	172	11.22	12.03	22.93

7.2.EXTERNAL IREFPLL AND LDO DISABLED

The adjustment of the IREFPLL bias current is shown in Appendix A.1. The measurements were carried out with three values of IREFPLL: 5 uA, 10 uA and 14 uA. Increasing the IREFPLL current increases the loop bandwidth of the PLL and consequently it decreases the jitter attenuation on the reference clock, transferring more jitter from the reference clock to the PLL's output. If the reference clock has a significant amount of jitter and the VCO noise contribution is relatively low, using a low PLL bandwidth is normally recommended.

External IREFPLL = 5uA

Table 13.CLKPLL Jitter performance versus reference clock with RJ (external IREFPLL=5uA, LDO disabled)

Noise amplitude (mV)	Ref clock TJ(BER=$1e^{-12}$) (ps)	TJ(BER=$1e^{12}$) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
1	69	92	5.25	17.01	25.49
50	80	96	5.60	16.16	24.90
100	105	108	6.64	13.12	23.03
200	169	145	9.53	8.79	21.17
300	244	188	12.73	6.87	20.52
400	322	238	16.43	3.51	19.88
500	403	290	20.31	0.00	18.00

External IREFPLL = 10uA

Table 14.CLKPLL Jitter performance versus reference clock with RJ (external IREFPLL=10uA, LDO disabled)

Noise amplitude (mV)	Ref clock TJ(BER=$1e^{-12}$) (ps)	TJ(BER=$1e^{12}$) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
1	69	95	5.04	23.00	32.31
50	80	103	5.72	21.87	31.63
100	105	124	7.34	19.82	31.11
200	169	178	11.53	13.70	27.78
300	244	243	16.75	4.17	25.36
400	322	312	21.84	1.35	22.40
500	403	387	27.12	0.00	17.05

External IREFPLL = 14uA

Table 15.CLKPLL Jitter performance versus reference clock with RJ (external IREFPLL=14uA, LDO disabled)

Noise amplitude (mV)	Ref clock TJ(BER=$1e^{-12}$) (ps)	TJ(BER=$1e^{12}$) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
1	69	96	4.98	25.32	33.09
50	80	106	5.77	24.00	33.62
100	105	129	7.61	20.81	32.65
200	169	182	12.24	14.66	29.67
300	244	260	17.86	4.93	25.64
400	322	334	23.46	0.02	21.11
500	403	411	28.83	0.00	15.38

7.3. EXTERNAL IREFPLL AND LDO ENABLED

Additional Jitter measurements were performed with the voltage regulator enabled.

External IREFPLL = 10uA and LDO enabled

Table 16.CLKPLL Jitter performance versus reference clock with RJ (external IREFPLL=14uA, LDO enabled)

Noise amplitude (mV)	Ref clock TJ(BER=$1e^{-12}$) (ps)	TJ(BER=$1e^{12}$) (ps)	RJ (ps)	DJ (ps)	PJ (ps)
1	69	310	21.08	9.32	24.12
50	80	313	21.45	6.73	21.81
100	105	324	22.18	8.30	20.13
200	169	356	24.33	8.59	17.55
300	244	402	28.18	0.25	13.14
400	322	455	31.62	3.76	10.91
500	403	513	36.00	0.00	8.58

8. DUTY CYCLE RATIO VERSUS INPUT CLOCK FREQUENCY

The Duty Cycle is a ratio between the positive pulse duration and the total period of a clock cycle. The measurements have carried out in the same conditions as described in Chapter 3.

8.4.PLL LDO DISABLED (DIS_PLL_LDO = 1)

Table 17.CLKPLL Duty cycle ratio versus input clock frequency (DIS_PLL_LDO=1)

F_{in} (MHz)	F_{out} (MHz)	Duty Cycle Ratio (%)	F_{in} (MHz)	F_{out} (MHz)	Duty Cycle Ratio (%)
24	192	42.8	45	360	48.3
25	200	43.1	47	376	48.9
26	208	43.2	50	400	49.7
27	216	43.5	55	440	52.2
30	240	44.0	60	480	55.0
32	256	44.5	65	520	56.9
35	280	45.0	70	560	59.5
37	296	45.6	75	600	63.9
40	320	46.4	80	640	68.2
42	336	47.3			

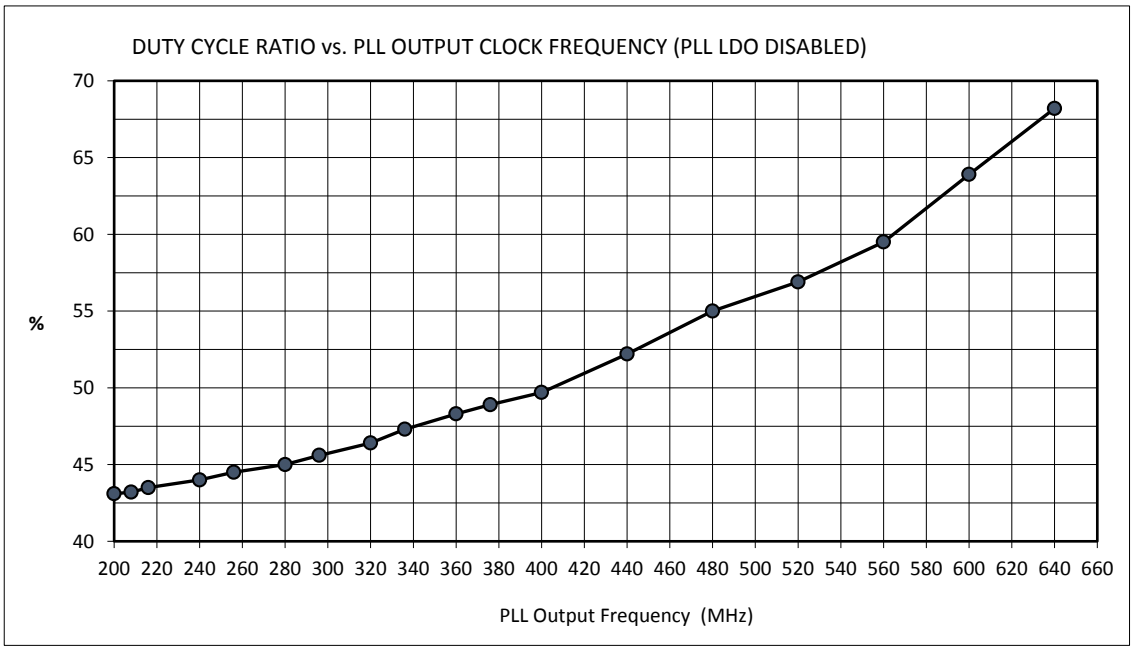


Fig 17. CLKPLL Duty cycle ratio versus input clock frequency (DIS_PLL_LDO=1)

8.5.PLL LDO ENABLED (DIS_PLL_LDO = 0)

The voltage regulator LDO is enabled in this measurement.

Table 18.CLKPLL Duty cycle ratio versus input clock frequency (DIS_PLL_LDO=0)

F_{in} (MHz)	F_{out} (MHz)	Duty Cycle Ratio (%)
25	200	40.7
30	240	41.9
40	320	44.0
50	400	48.0
60	480	53.0
65	520	55.6
66	528	56.0

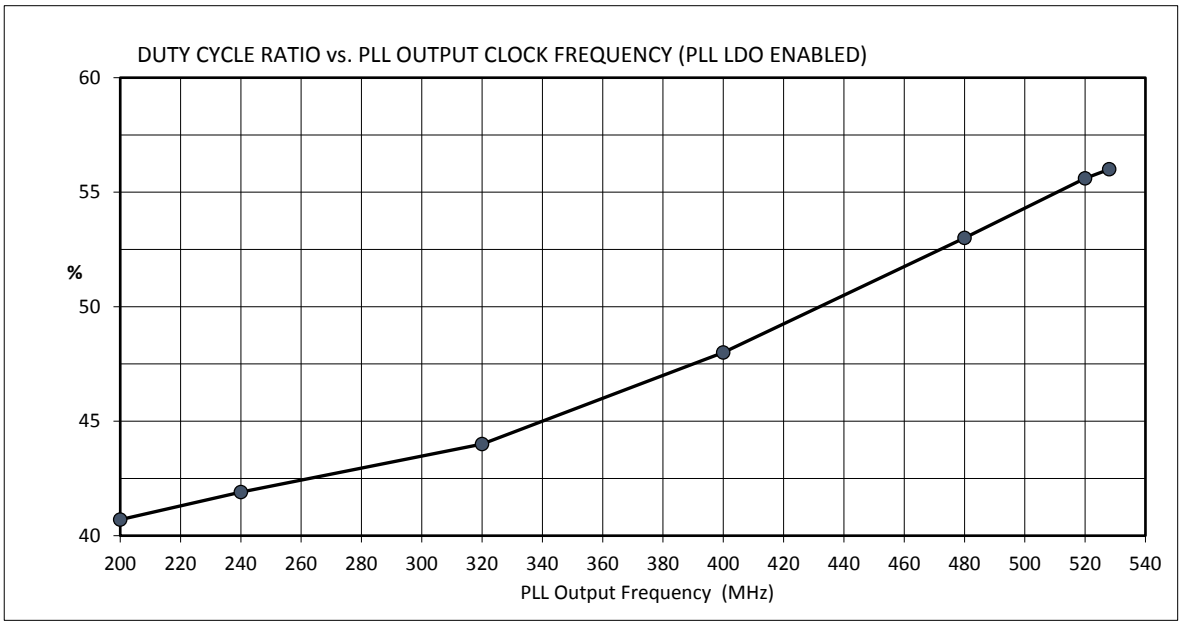


Fig 18. CLKPLL Duty cycle ratio versus input clock frequency (DIS_PLL_LDO=0)

9. PLL FREQUENCY RANGE

The practical lower frequency limit of the PLL is 192 MHz.

The high frequency limit depends the operation mode of the LDO voltage regulator of the PLL. When the LDO voltage regulator is enabled, the maximum output frequency is 528 MHz. Without the voltage regulator LDO, the PLL can generate an output frequency of at least 640 MHz. The upper frequency limit depends of the power supply voltage of the VCO block. The output voltage of the LDO voltage regulator is 1.5V while the VDDA power supply line provides a voltage of 1.8V.

10. LOCKING TIME

10.1. LOCKING TIME WITH THE INTERNAL IREFPLL BIAS CURRENT

The measured locking of the PLL is approximately 4.6 us (the frequency of the output clock changes from 178 MHz to 320 MHz). The Locking time is estimated from the frequency tracking data of the PLL output signal during the input signal locking process. The PLL using the internal IREFPLL current source and the trim parameter of the PLL is set to value of 5. The voltage regulator LDO is disabled.

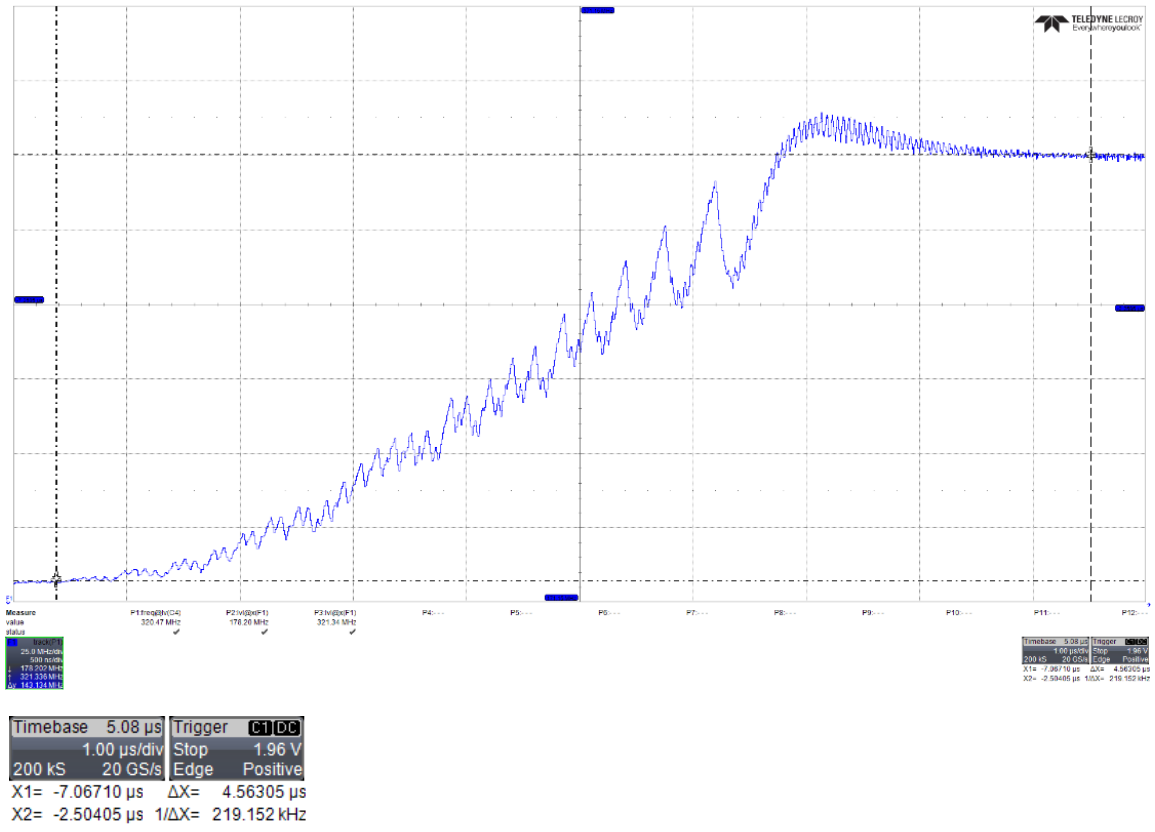


Fig 19.CLKPLL Frequency tracking plot during the PLL locking process (DIS_PLL_LDO=1)

10.2. LOCKING TIME WITH THE EXTERNAL IREFPLL BIAS CURRENT

In the following plot is shown the frequency tracking data of the PLL output signal during the locking process in different values of the IREFPLL bias current. The measured locking time values are presented in the Table followed by the plot. The adjustment of the IREFPLL bias current is explained In Appendix A.1. The voltage regulator LDO is disabled in this measurement.

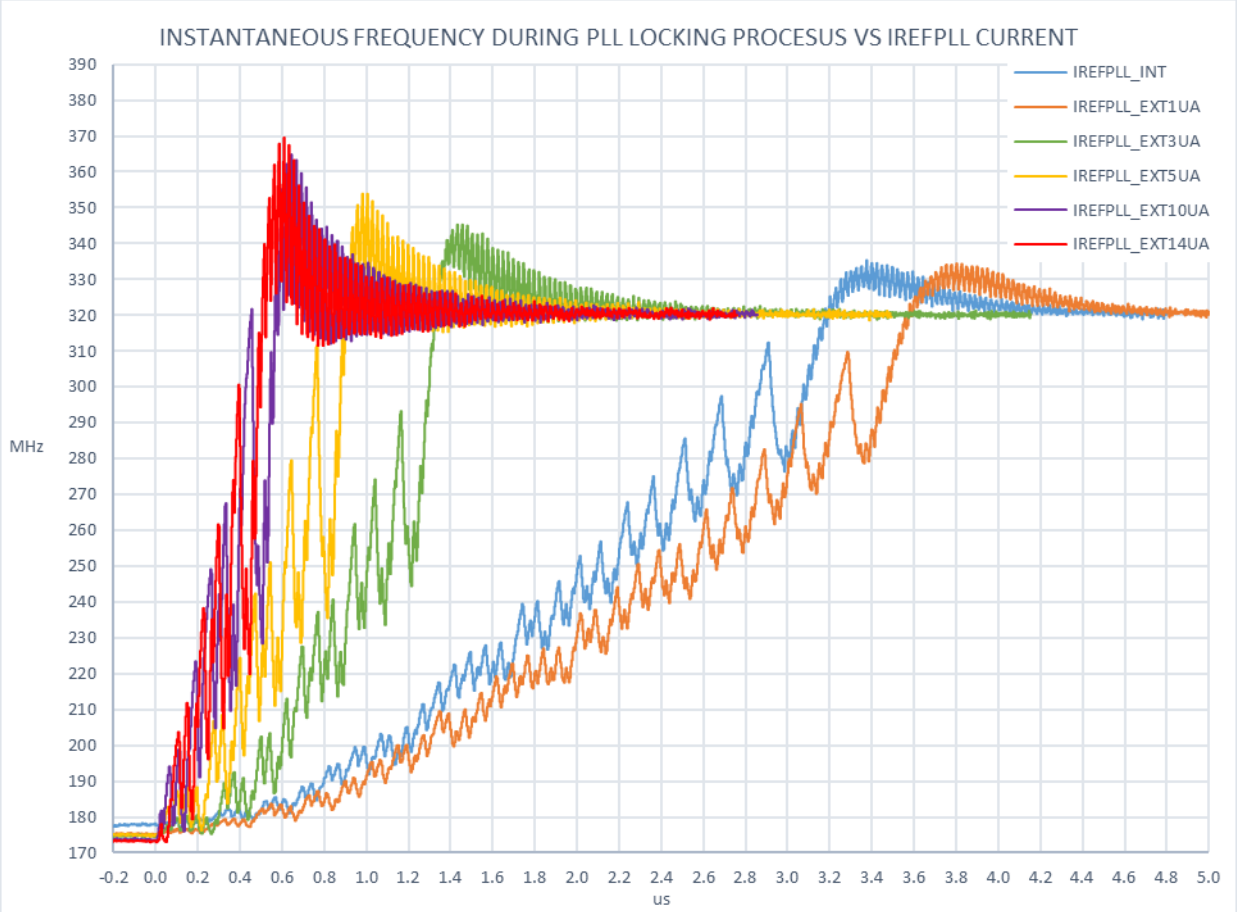


Fig 20.CLKPLL Frequency tracking plot during the PLL locking process in different external IREFPLL current adjustment

Table 19. CLKPLL PLL locking time in different external IREFPLL current adjustment

IREFPLL Mode	IREFPLL (uA)	F_{start} (MHz)	Locking Time (us)
Internal	-	178	4.6
External	1	175	4.9
External	3	175	3.5
External	5	175	2.8
External	10	174	2.7
External	14	173	2.6

11. JITTER PERFORMANCE VERSUS VDDA POWER SUPPLY VOLTAGE

In this measurement, an external power supply voltage were used for analog power supply voltage, VDDA. The measurements have carried out with MIMOSIS-2.1 chip N° 15.

The following operating conditions were applied:

- Chip is not started (the sequencer is not running)
- PLL output clock frequency is 320 MHz
- Clock Rescue disabled on S3 Lab board

11.3. PLL LDO DISABLED (DIS_PLL_LDO = 1)

Table 20.CLKPLL Jitter performance versus VDDA power supply voltage (internal IREFPLL, LDO disabled)

VDDA power supply voltage (mV)	TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)	CLKPLL amplitude (mV)	Duty Cycle
1600	132	8.85	5.57	15.05	321	46.6
1650	130	8.75	5.03	14.52	335	46.7
1700	127	8.51	5.72	15.29	348	46.8
1750	125	8.30	6.48	14.90	363	46.9
1800	121	8.06	6.45	14.12	378	47.0
1900	116	7.59	7.51	15.24	406	47.2
2000	113	7.28	9.83	19.06	434	47.3

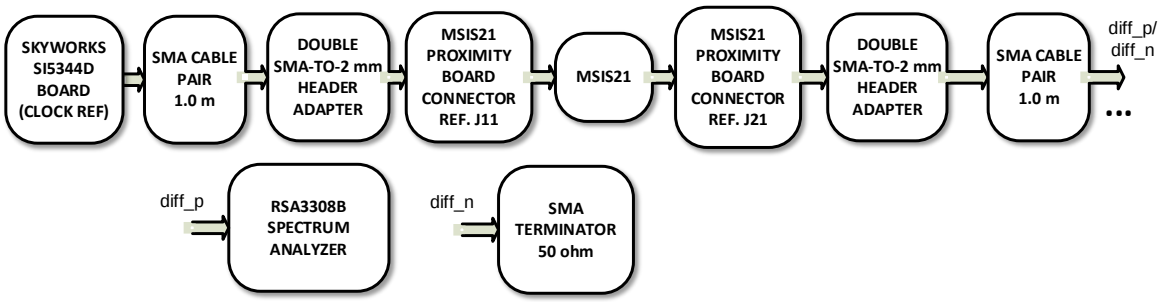
11.4.PLL LDO ENABLED (DIS_PLL_LDO = 0)

VDDA power supply voltage (mV)	TJ(BER=1e^{-12}) (ps)	RJ (ps)	DJ (ps)	PJ (ps)	CLKPLL amplitude (mV)	Duty Cycle
1600	-	-	-	-	-	-
1650	1336	81.4	174.4	193.8	334	46.3
1700	1394	87.1	152.7	188.1	347	46.1
1750	1446	92.7	123.0	200.8	360	45.8
1800	1467	88.6	204.5	199.4	374	45.5
1900	1493	93.0	167.5	207.0	400	44.9
2000	1434	86.7	197.7	202.9	427	44.1

12. PHASE NOISE

Phase noise measurements were carried out with Tektronix RSA3308B Real-time Spectrum Analyzer.

Signal Path Diagram



12.1. PHASE NOISE WITH INTERNAL IREFPLL BIAS

The output frequency of the PLL (CLKPLL) is 320 MHz.

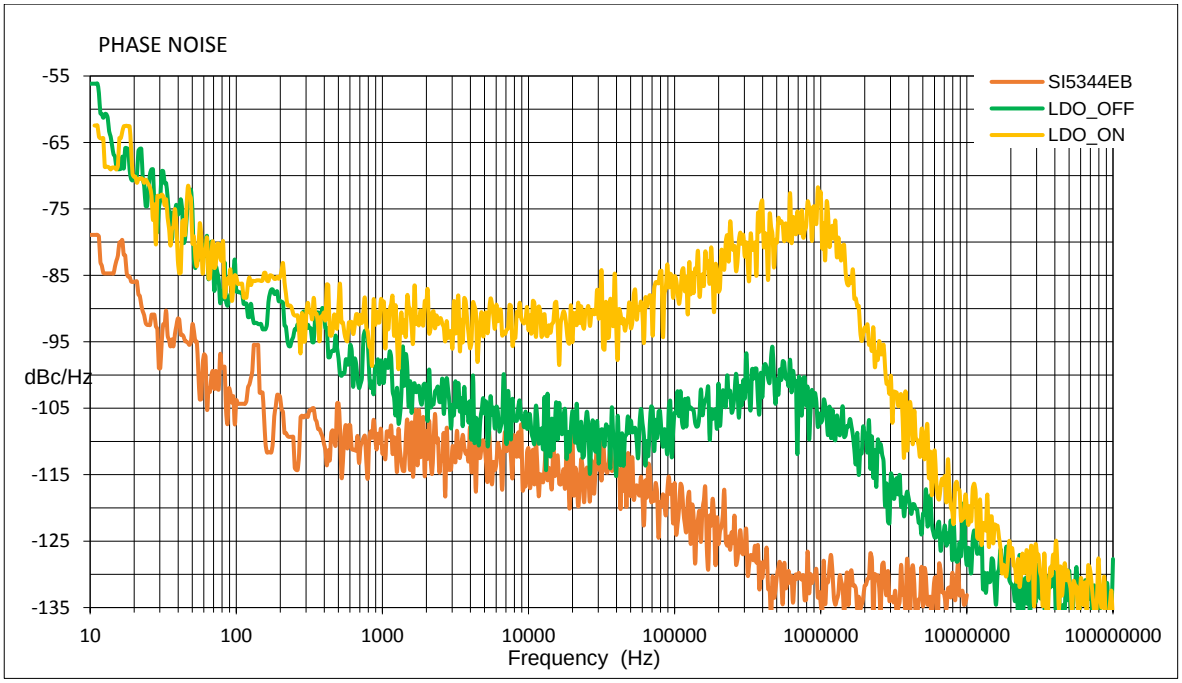


Fig 21. Phase noise measurements with the reference clock and CLKPLL

Table 21. Phase noise measurements with the reference clock and CLKPLL

Signal	Integrated Phase noise (deg RMS)	Random Jitter (ps RMS)	Max Periodic Jitter (ps)
CLKREF SI5344EB (40MHz)	0.09	6.4	23
CLKPLL (LDO OFF)	0.83	7.2	41
CLKPLL (LDO OFF)	12.75	110.7	200

12.2. PHASE NOISE VERSUS EXTERNAL IREFPLL BIAS CURRENT

The following operating conditions were applied:

- PLL output clock frequency is 320 MHz
- Low noise operation conditions
  1) MIMOSIS-2.1 main clock input source is “clock rescue” and there is no clock signal at the input.
  2) Chip is not started.
- LDO of the PLL is enabled, except Reference measurement “IREFPLL_INT, LDO OFF”: internal IREFPPL source selected and the voltage regulator LDO is disabled
- Phase noise measurement: Tektronix RSA3308B (Real-time Spectrum Analyzer (DC - 8 GHz)

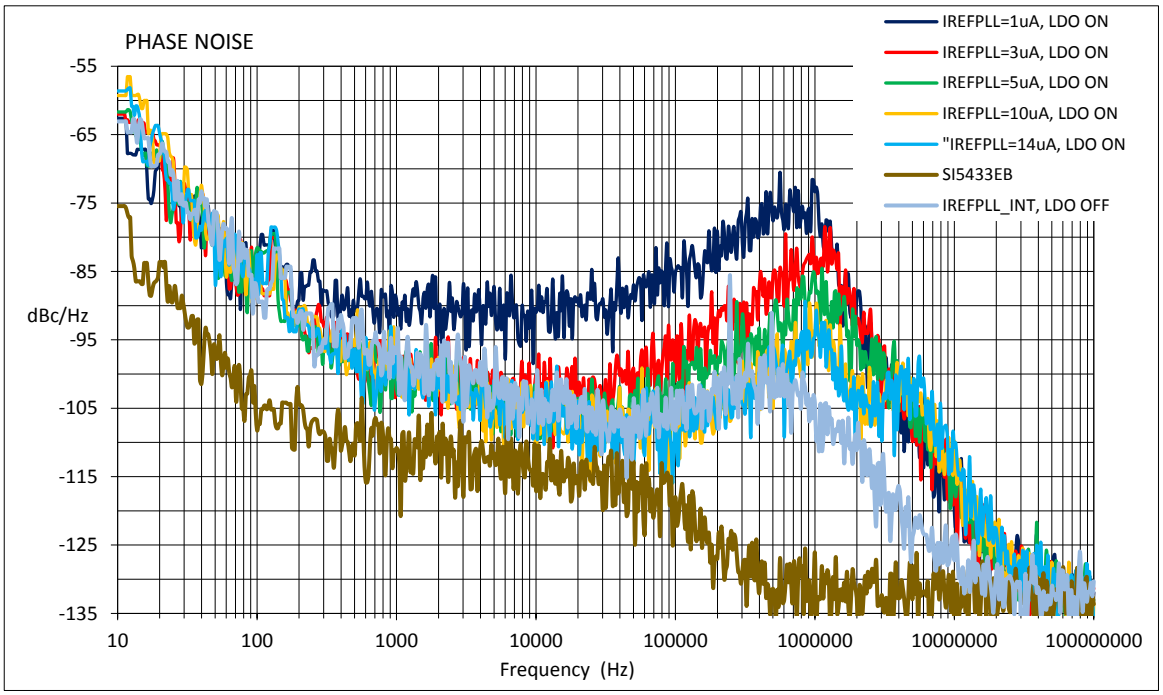


Fig 22. CLKPLL Phase noise measurements in different external IREFPLL current adjustment

Table 22.CLKPLL Phase noise measurements in different external IREFPLL current adjustment

Signal	IREFPLL Current (uA)	Integrated Phase noise (deg RMS)	Random Jitter (ps RMS)	Max Periodic Jitter (ps)
CLOCK REFERENCE 40 MHz SI5344EB	-	0.09	6	23
CLKPLL (IREFPLL_INT, LDO OFF)	1	0.88	8	101
CLKPLL (IREFPLL_EXT, LDO ON)	1	13.94	121	292
CLKPLL (IREFPLL_EXT, LDO ON)	3	6.56	57	140
CLKPLL (IREFPLL_EXT, LDO ON)	5	3.76	33	115
CLKPLL (IREFPLL_EXT, LDO ON)	10	2.15	19	90
CLKPLL (IREFPLL_EXT, LDO ON)	14	2.13	19	87

13.TIE TRACKING OF PLL CLOCK OUTPUT IN CLOCK CYCLE BASIS

Time Interval Error (TIE) of an edge is the time deviation of that edge from its ideal position measured from a reference point.

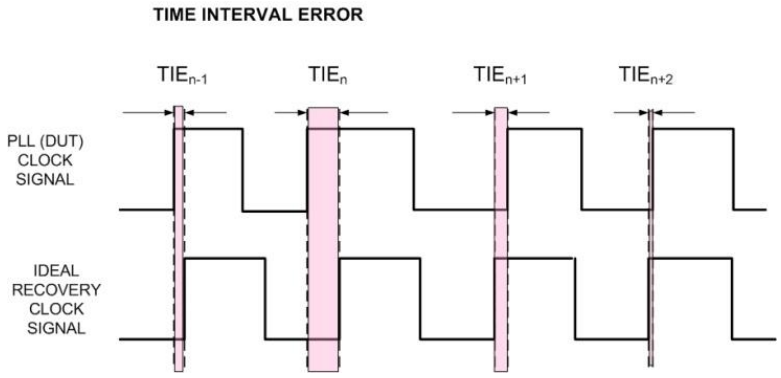


Fig 23. Example of Time Interval Error

The operation conditions described in the Chapter 3 were used in this measurement.

Tie tracking measurement means to acquire all the TIE value in clock cycle basis in given time interval. In the following Fig. 24, the TIE track plots are shown in two conditions: PLL LDO enabled (LDO ON) and PLL LDO disabled (LDO OFF). The RMS values of the TIE Tracking for LDO_OFF and LDO_ON are 6 ps and 120 ps respectively.

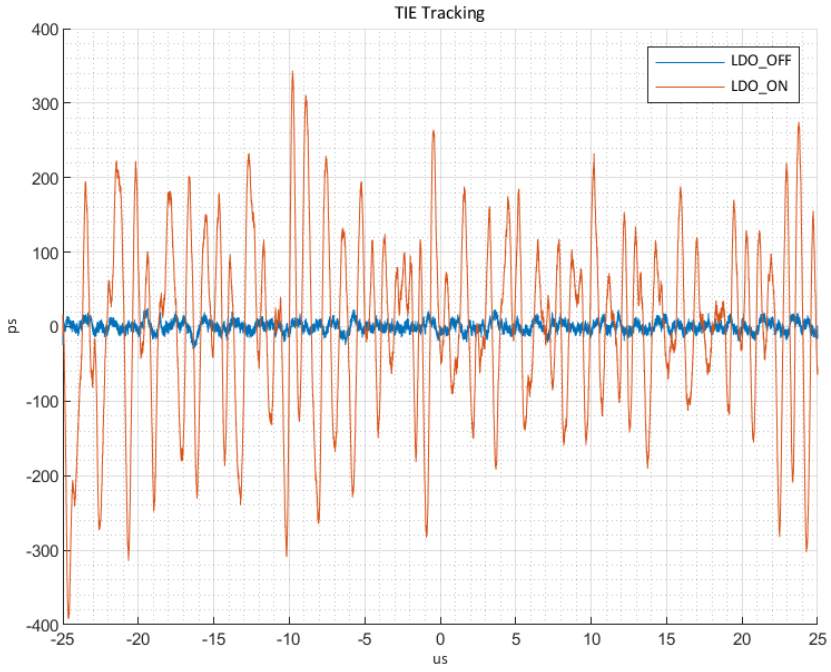


Fig 24. Tie tracking plot of CLKPLL output with and without LDO

The TIE tracking plot shows in time domain that the LDO is not capable maintain the voltage regulation for the VCO with the default IREFPLL current value of 1uA.

14.CONCLUSION

The test results presented in this document were obtained with MIMOSIS-2.1 sensors mounted on the Proximity boards N° 15 and N° 60.

Despite the test results shown in this document, the limitations of the jitter performance of PLL do not exclude a possibility that the PLL could be used as a clock reference for the sensor. The PLL was tested in a quite ideal test environment regarding for example the quality of the reference clock signal. In the final detector system, the PLL clock signal is not present directly, but it is used as a reference clock for the output data serializer circuitry of the sensor. The inadequate jitter performance of the PLL output clock signal may be considered as a partial cause for the issues related to the data acquisition chain, e.g., bit errors in serial output data.

The integrated LDO (low-dropout voltage regulator) has been pointed out as an origin of an inadequate jitter performance of the PLL. The principal objective of the LDO is to provide a stable and a low-noise power supply for the PLL. The low-noise power supply requirement is especially important what is concerning the VCO circuitry. The test results obtained with MIMOSIS-1 PLL or MIMOSIS-2 PLL have already shown a jitter performance issue related to the operation of the integrated LDO. The corrections carried out on the LDO circuitry of the PLL in MIMOSIS-2.1 were not adequate: in the default operation mode, the integrated LDO can be considered as a noise source for the VCO circuitry of the PLL.

A temporary solution concerning the jitter performance issue of the PLL of MIMOSIS-2.1 has been explored. The jitter performance of the MIMOSIS-2 PLL can be considerable improved by using an external reference current mode of the PLL. In this operating mode, by using a single external resistor, the reference current (IREFPLL) can be increased (from 1 uA to 14 uA) allowing a reduction of the Total Jitter (TJ(BER=$1e^{-12}$) from 1.5 ns (0.48 UI) to 0.3 ns (0.1 UI) in low noise reference clock conditions. The obtained improvement of the Total Jitter performance should be adequate for qualifying the PLL with the external reference current mode as a clock reference for output data serialization. However, the increased reference current affects also the function of the control loop of the PLL and its stability. In addition, the increased PLL loop bandwidth will reduce its ability to attenuate the jitter contained in the reference clock signal, especially Random Jitter.

The final qualifying of the PLL as a clock reference requires carrying out tests in the final detector system.

APPENDIX A: GENERAL CONFIGURATIONS FOR MEASUREMENTS

APPENDIX A.1: EXTERNAL IREFPLL BIAS CURRENT ADJUSTMENT

By default, the internal IREFPLL current source (IREFPLL_INT) is selected with the reference current of 1 uA. The externally adjusted IREFPLL current reference (IREFPLL_EXT) can be selected by MIMOSIS2.1 Slow Control Config02 register. When the IREFPLL_EXT is selected, the IREFPLL reference current can be adjusted by using an external resistor connected between the pin IREFPLL and GND. The IREFPLL pin provides a bias reference voltage of 1.2V for adjustment. To obtain the reference current of 1 uA, two resistors (ref. R88 and R89) of 604 kohm are mounted in series on the MIMOSIS Proximity board. To increase the PLL reference current, an additional resistor can be connected in parallel with the mounted resistors by using the pin 4 and pin 10 of the connector J23. The following Table shows the resistor values used in characterization of the PLL.

Table 23. Additional resistor value for IREFPLL adjustment

IREFPLL additional resistor (ohm)	**IREFPLL (uA)**
None	1
600k	3
300k	5
130k	10
91k	14

APPENDIX A.2: SEQUENCER REGISTER CONFIGURATIONS

The sequencer registers are programmed by the slow control interface (I2C).

APPENDIX A.2.1: NOMINAL SEQUENCER CONFIGURATION

Table 24. Nominal configuration values of the sequencer registers

Register	**Value**	**Register**	**Value**	**Register**	**Value**
PIXLOAD_A	0x0	PIXRSTB_A	0X62	MKSEQ1_A	0x0
PIXLOAD_B	0x1	PIXRSTB_B	0X63	MKSEQ1_B	0x2
DPSTART_A	0x1	PIXPULSEA_A	0x0	MODMKSEQ1	0x0
DPSTART_B	0x2	PIXPULSEA_B	0x0	MKSEQ2_A	0x0
DPTOKEN_A	0x2	PIXPULSEB_A	0x0	MKSEQ2_B	0x2
DPTOKEN_B	0x3	PIXPULSEB_B	0x0	POLARITY	0x5
PIXREAD_A	0x0	PIXPULSED_A	0x0	FRAMELENGTH	0x64
PIXREAD_B	0x61	PIXPULSED_B	0x0	MAXFRAME	0x0
DPEND_A	0X63	MODPULSE	0x0		
DPEND_B	0X64	MODPIXRSTB	0x0		

APPENDIX A.2.2: BASE SEQUENCER CONFIGURATION

Table 25. Base configuration values of the sequencer registers

Register	Value	Register	Value	Register	Value
PIXLOAD_A	0x0	PIXRSTB_A	0x0	MKSEQ1_A	0x0
PIXLOAD_B	0x0	PIXRSTB_B	0x0	MKSEQ1_B	0x0
DPSTART_A	**0x1**	PIXPULSEA_A	0x0	MODMKSEQ1	0x0
DPSTART_B	**0x2**	PIXPULSEA_B	0x0	MKSEQ2_A	0x0
DPTOKEN_A	0x0	PIXPULSEB_A	0x0	MKSEQ2_B	0x0
DPTOKEN_B	0x0	PIXPULSEB_B	0x0	POLARITY	0x5
PIXREAD_A	0x0	PIXPULSED_A	0x0	FRAMELENGTH	**0x64**
PIXREAD_B	0x0	PIXPULSED_B	0x0	MAXFRAME	0x0
DPEND_A	0x0	MODPULSE	0x0		
DPEND_B	0x0	MODPIXRSTB	0x0		

The nominal configuration values are used in normal operating mode of the MIMOSIS-2.1 chip. The Base configuration is the minimal configuration that allows the sequencer block to be used e.g. generating data marker signals without the pixel matrix being active.

APPENDIX A.3: DAC REGISTER CONFIGURATION

The DAC registers are programmed by the slow control interface (I2C).

APPENDIX A.3.1: NOMINAL DAC REGISTER CONFIGURATION

Table 26. Nominal DAC register configuration

DAC register	value	DAC register	value
IBIAS	64	VCASNA	75
ITHR	52	VCASNB	75
IDB	28	VCASNC	75
VRESET	171	VCASND	75
VPL	70	VCASN2	83
VPH	85	VCLIP	50
VPHFINE	245	IBUFBIAS	125
VCASP	67		

The nominal DAC configuration values are used in normal operating mode of the MIMOSIS-2.1 chip. The low activity DAC register configuration is purposed to limit the activity the pixel matrix by setting the values of the VCASN[A:D] registers to the minimum (1).

APPENDIX A.3.2: LOW ACTIVITY DAC REGISTER CONFIGURATION

Table 27. Low pixel activity DAC register configuration

DAC register	value	DAC register	value
IBIAS	64	VCASNA	1
ITHR	52	VCASNB	1
IDB	28	VCASNC	1
VRESET	171	VCASND	1
VPL	70	VCASN2	83
VPH	85	VCLIP	50
VPHFINE	245	IBUFBIAS	125
VCASP	67		

APPENDIX A.4: GENERAL STEERING REGISTER CONFIGURATION

For the details, see the document “MIMOSIS1 I2C controller’

APPENDIX A.4.1: PLL REGISTER

LDO DISABLED

Table 28.PLL register (LDO disabled)

Register parameter	**value**
ENLOCKPLL	0x1
EN_CLKPLL	0x1
TRIM_ REFCURPLL	0x5
DIS_PLL_LDO	**0x0**
EN_PLL_VCO	0x1

LDO ENABLED

Table 29.PLL register (LDO enabled)

Register parameter	**value**
ENLOCKPLL	0x1
EN_CLKPLL	0x1
TRIM_ REFCURPLL	0x5
DIS_PLL_LDO	**0x1**
EN_PLL_VCO	0x1

APPENDIX A.4.2: PLL LOCK REGISTER

The PLL lock module is not use in measurement.

Table 30.PLL lock register

Register parameter	value
GAIN	0x0
THRESHOLD	0x0

APPENDIX A.4.3: OUTPUT REGISTER

Data Marker mode is enabled and Output mode with two outputs is selected.

Table 31. OUTPUT register

Register parameter	value
EN_SEQMARKER2	0x0
EN_SEQMARKER1	0x0
EN_DATAMARKER	0x1
EN_ALWAYS_DATA	0x0
EN_SOFT_OUTPUTMODE	0x1
OUTPUTMODE	0x1

APPENDIX B: IMPROVEMENT SUGGESTIONS FOR DESIGN

APPENDIX B.1: SEPARATE CURRENT REFERENCE FOR THE LDO AND THE PLL, IREFPLL AND IREFLDO

In the current PLL implementation, a common reference current, IREFPLL, is used for the LDO and for the PLL. The increase of the IREFPLL current from its default value (1 uA) allows the LDO to operate in nominal operation mode, but it also affects the parameters of the control loop of the PLL. For this reason, two separate adjustments for IREFLDO and IREFPLL could be more advantageous.

Because there is only pin available for the external current adjustment (IREFPLL), the current adjustments IREFLDO and IREFPLL should be implemented internally. The external, switchable IREFPLL adjustment could be used for a common coarse adjustment if necessary.

APPENDIX B.2: INCREASE ADJUSTMENT STEP OF PLL TRIM

The PLL TRIM adjustment range might be too narrow for practical use.

Reference: C4PI_MIMOSIS2_PLL_PRE_TESTS (2025-04-14)

PLATFORM C4PI - IPHC - IN2P3

MIMOSIS-2 PROTOTYPE

PRELIMINARY TESTS OF PLL

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