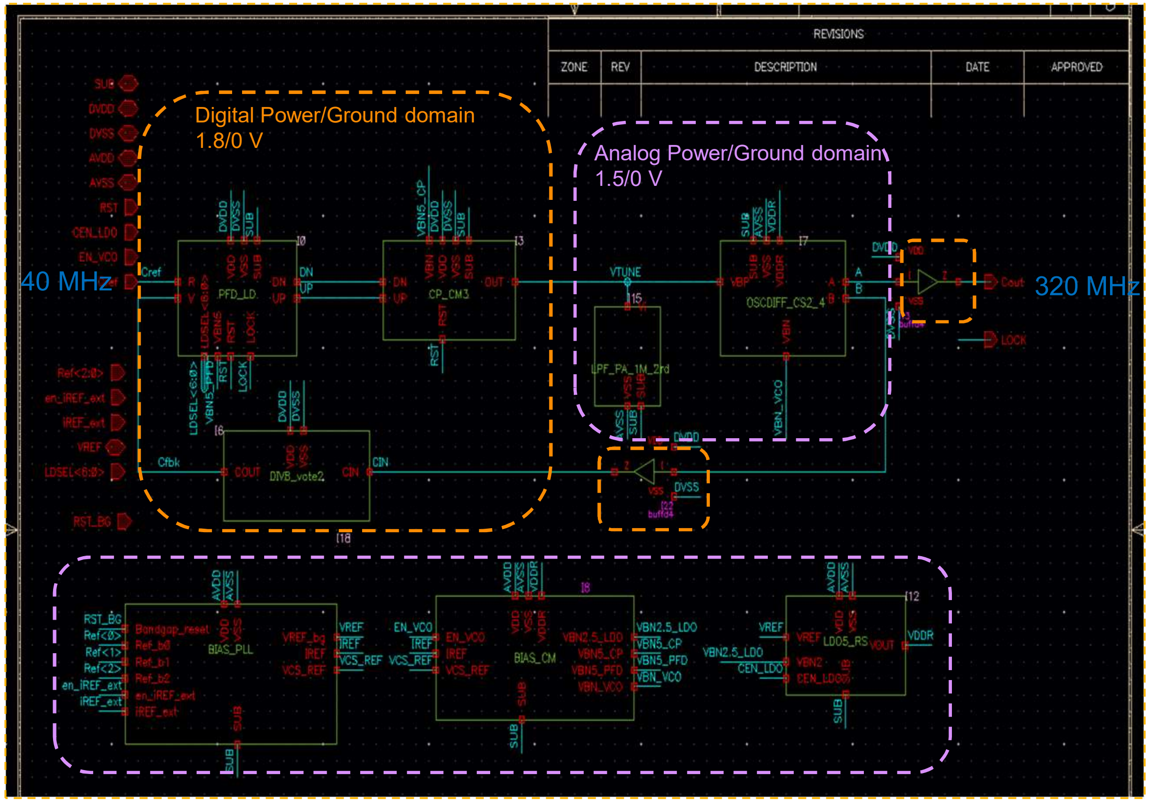
Simulation of the MIMOSIS2.1 PLL

Block diagram



Designed by Yue Zhao
(PhD, 2021)

Post-layout simulation at nominal condition

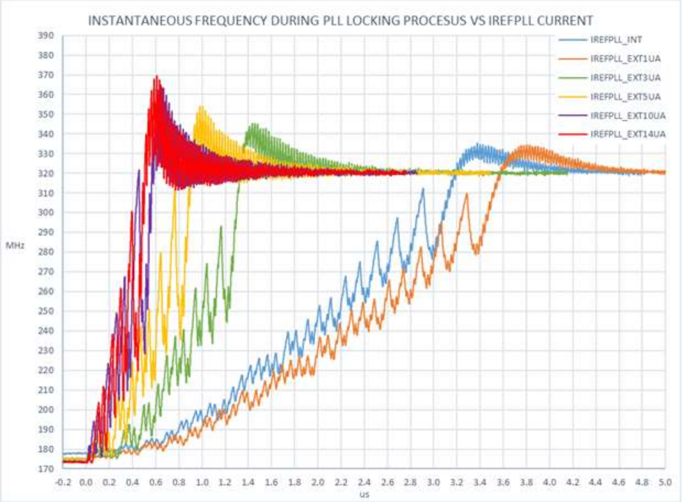
AVDD = 1.8 V, DVDD = 1.8 V, T = 27°C, Nominal corner

Comparison with PLL measurements (cf MIMOSIS21_PLL_PRELIMINARY_TESTS_250414_1100.pdf)

- Locking time
- Phase noise
- Random jitter

Locking time of the PLL

TEST



mode	Iref (uA)	Locking time (us)	Peak value (MHz)
int	-	4.6	335.3
ext	1	4.8	334.4
ext	3	3.2	345.3
ext	5	4.7 *	353.9
ext	10	4.1 *	364.8

The lock is achieved when $|\Delta f/f| < \pm 3\sigma$ with σ is calculated from the plateau at the end of the data set.

* A kind of frequency oscillation (instability) persists for much longer before disappearing.

Post-Layout SIM

mode	Iref (uA)	Locking time (us)	Peak value (MHz)
int	-	5.0	333
ext	1	4.9	334
ext	3	3.0	347
ext	5	2.6	352
ext	10	2.2	380

The PLL is locked when the signal Lock is detected

Simulation of Phase Noise for the closed-loop PLL

Time-domain noise analysis followed by FFT to calculate the PSD of the phase fluctuation

- Recommended for PLL simulation
- Performs with Spectre APS, conservative accuracy
- Post-layout simulation at nominal condition
- No noisy reference input frequency
- Very long runtime (~ 6d 3h)
    - → accuracy needed to capture all noise (noisefmax, max time-step control)
    - → large window size to ensure an offset frequency of a few tens of kHz (Fmin for PSD)
    - → chosen interval to allow accurate FFT: 10KHz – 10GHz

Comparison with the measurement

- Good correspondance for large frequency offsets (VCO phase noise dominant)

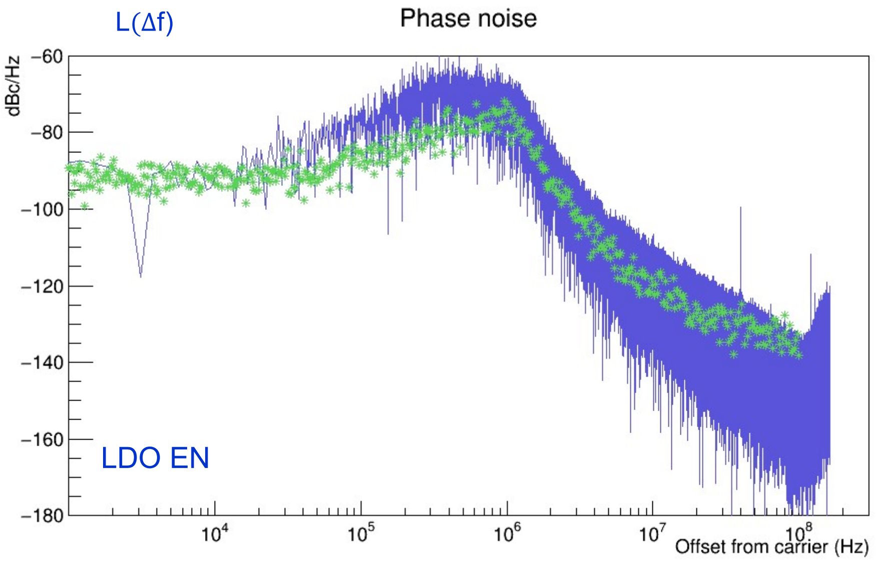
- For low offsets → less precision due to incompletely modeled random noise sources (correlated with simulation time)

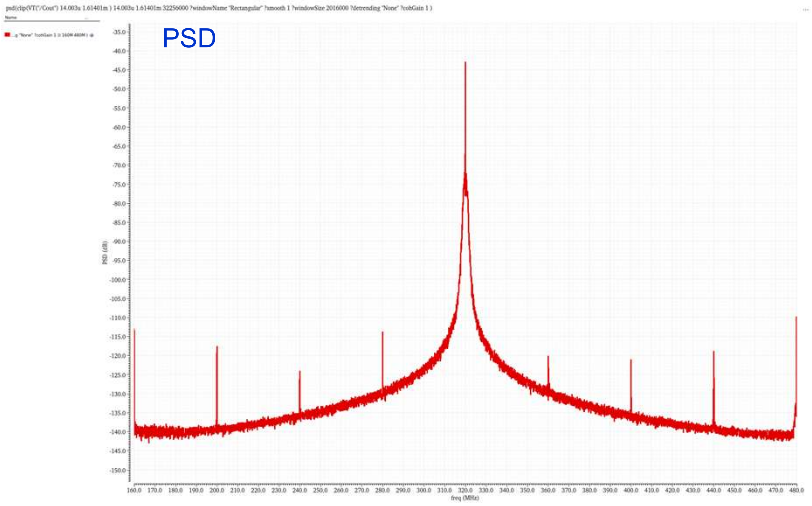
- Not a good match in the simulated response from 10kHz to 1 MHz

The estimated PLL bandwidth in simulation (~ 600 MHz) seems to be lower than in test (~ 800 MHz) → phase noise increase of ~ 10 dBc from 10kHz to 1 MHz → increase of random jitter

- Some spurs (due to periodic signals in the PLL) appears at reference frequency and its harmonics in the simulation (due to leakage or mismatch of the CP which causes FM modulation) but their contribution to the noise are negligible.
    - → can be filtered in measurement

Comparison of simulation (line) with test (*)





The simulated noise is higher than the measured noise unlike the case where the vCO is directly connected to the power supply

Simulation of Phase Noise – Setting optimisation

Optimised setting for noise transient analysis to have a reasonable runtime

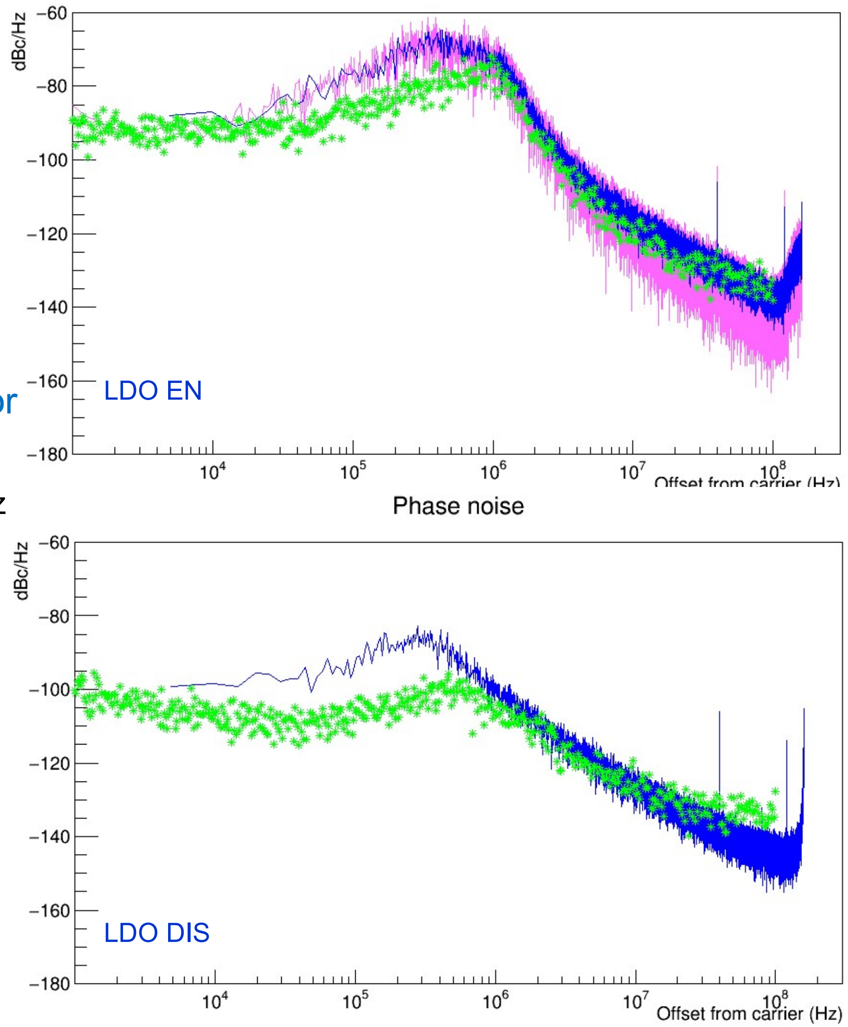
- Performs with SpectreX, moderate accuracy (AX)
- Post-layout simulation at nominal condition
- No noisy reference input frequency
- Chosen frequencies interval to calculate FFT: 20KHz – 10GHz
- Runtime (~ 20 h)

Simulated Phase noise spectrum with/without LDO regulator Comparison with the measurement

- Not a good agreement in the frequencies interval 20kHz to 1 MHz

→ Source of noise jitter

Comparison of simulation Spectre X line, Spectre APS line with test *



PLL ≡ high-pass filter for VCO. The phase noise of VCO is reduced within the loop bandwidth
PLL ≡ low-pass filter for phase noise from PFD, CP, LPF, DIV. These one determine the phase noise within the loop bandwidth.

Jitter definition

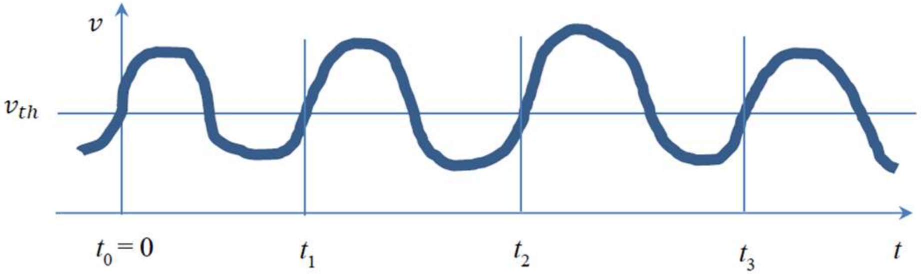
Random phase noise variation ↔ jitter in time domain

Equivalence between the jitter calculation in frequency domain by using the integration of power spectral density of the phase and with the abs_jitter function in time domain

Integration range : [20K-100M]

$$Rj_{rms} = \frac{\sqrt{\int_{f_1}^{f_2} PN(f)df}}{2\pi F_0}$$

Jitter ≡ random variation in threshold crossing (due to thermal and flicker noise in devices)



Absolute jitter (or edge to reference jitter, or edge jitter) is defined as:

$$J_a(n) = t_n - nT$$

The total jitter TJp-p is determined by the sum of the random jitter RJp-p at specific BER and the deterministic jitter DJp-p

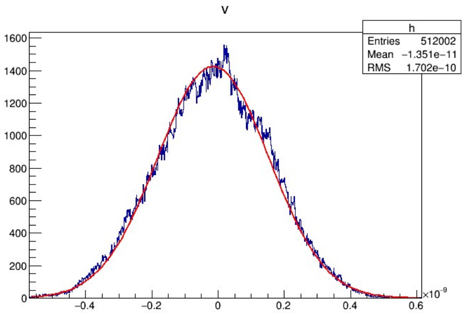
$$RJ_{p-p}(t)(BER) \triangleq K \times RJ_{RMS}(t)$$

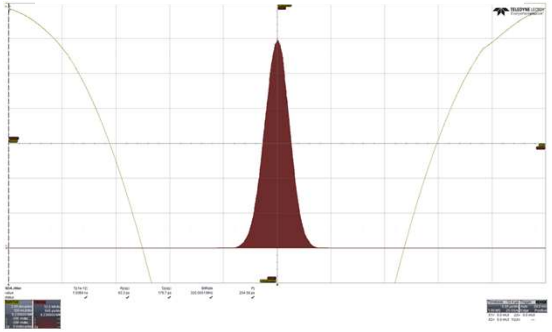
$$TJ_{p-p} = DJ_{p-p} + RJ_{p-p}(BER)$$

For a BER = 10-12, K =14,069 (Crest factor)

Random Jitter calculation with/without LDO

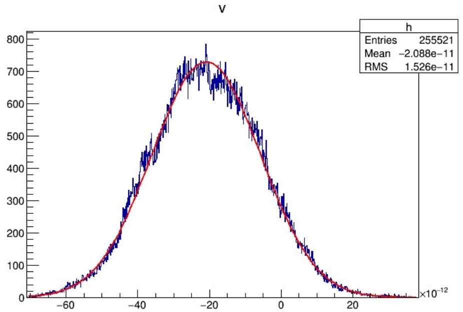
LDO EN

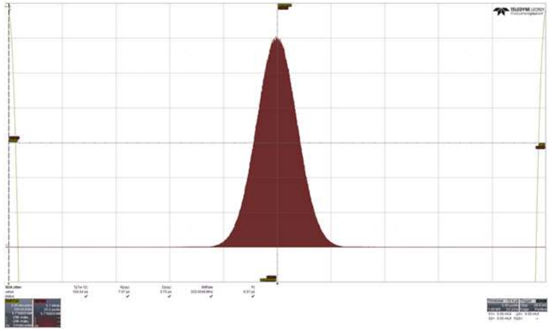




Measured Jitter in low power supply noise condition

LDO DIS





LDO EN	RJ rms (ps) (in time domain)	RJ rms (ps) (from phase noise)	RJ_{p-p} (ps) (BER= 10^{-12}) (in time domain)
Post-Layout SIM	170.2	170.2	2395
TEST	93.3	110.7	1312

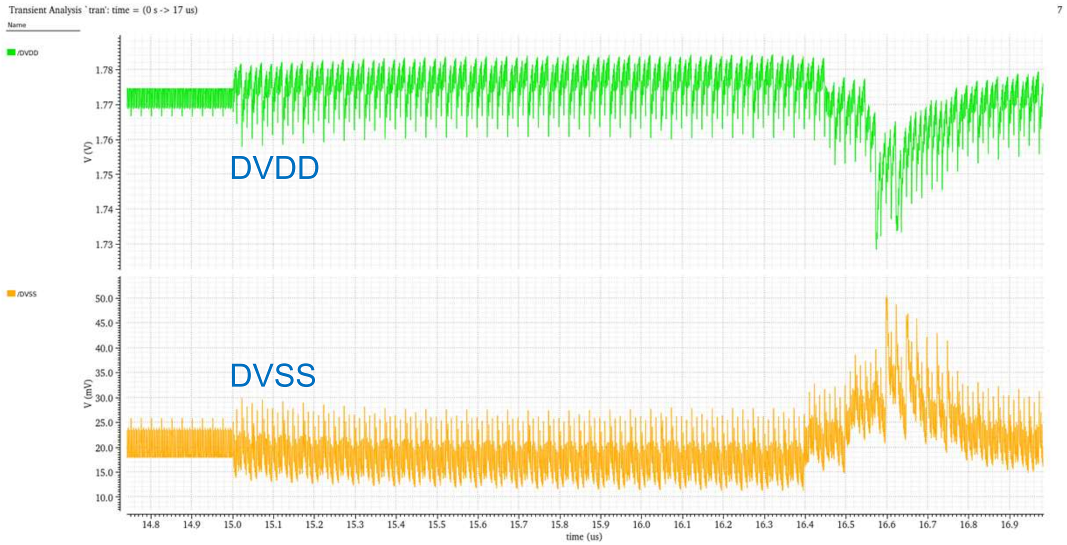
LDO DIS	RJ rms (ps) (in time domain)	RJ rms (ps) (from phase noise)	RJ_{p-p} (ps) (BER= 10^{-12}) (in time domain)
Post-Layout SIM	15.26	15.7	214.7
TEST	7.07	7.2	99.5

In simulation, the random jitter is multiplied by a factor of 11 when the LDO is enabled close to what we measured in test (factor of 13)

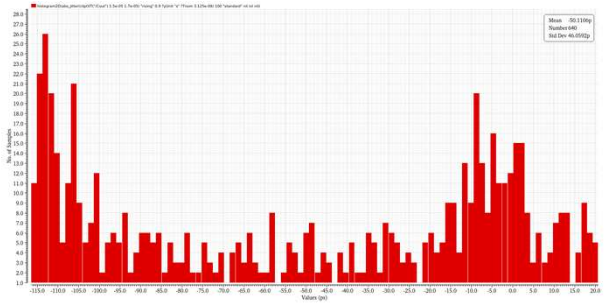
PLL simulation including coupling noise through the digital power/ground

- Dynamic rail analysis with Voltus
  - To extract the noise on the digital supply/ground due to chip activity
  - Full chip simulation

- First run
  - Transient simulation with these noise files for DVDD/DVSS during 2 µs
  - Absolute jitter calculated on 640 cycles
    - → Need to increase the number of cycles to evaluate accurately the jitter

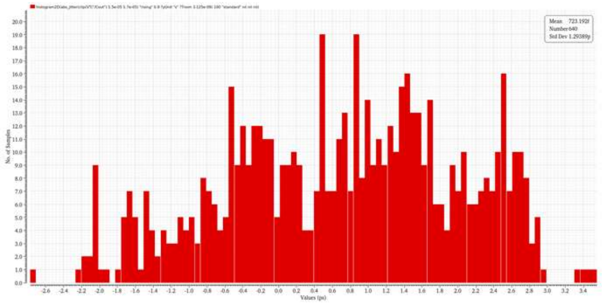


With noise in digital Pwr/Gnd
LDO on



p-p Abs_jitter = 137.2 ps

Without noise in digital Pwr/Gnd
LDO on



p-p Abs_jitter = 6.32 ps

Summary

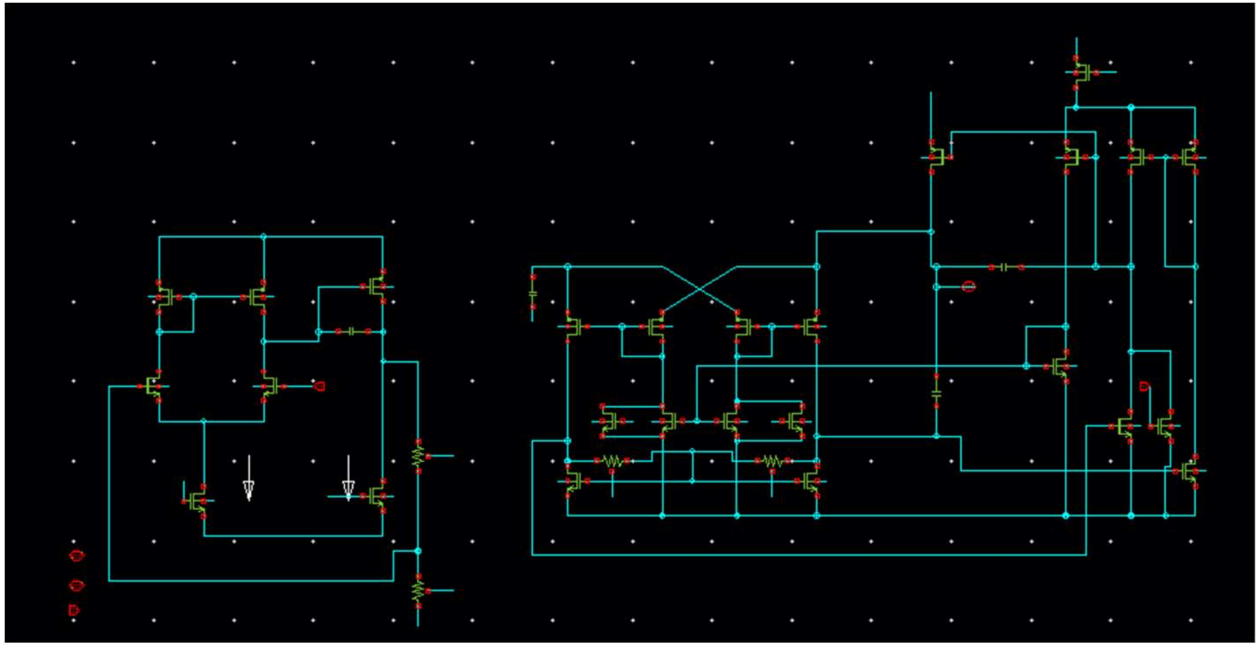
The transient noise analysis has a long runtime and need to be set correctly to achieve sufficient accuracy (which is an iterative processus). By using SpectreX (AX) one has an optimised setting which is a good compromise between accuracy and simulation time.

The simulated phase noise of the PLL is in pretty good agreement with the measurements except for the range of frequencies offset from 10kHz to 1Mhz which contributes to a significant increase in random jitter (~ factor of 2) . The PLL bandwidth appears to be lower than in test.

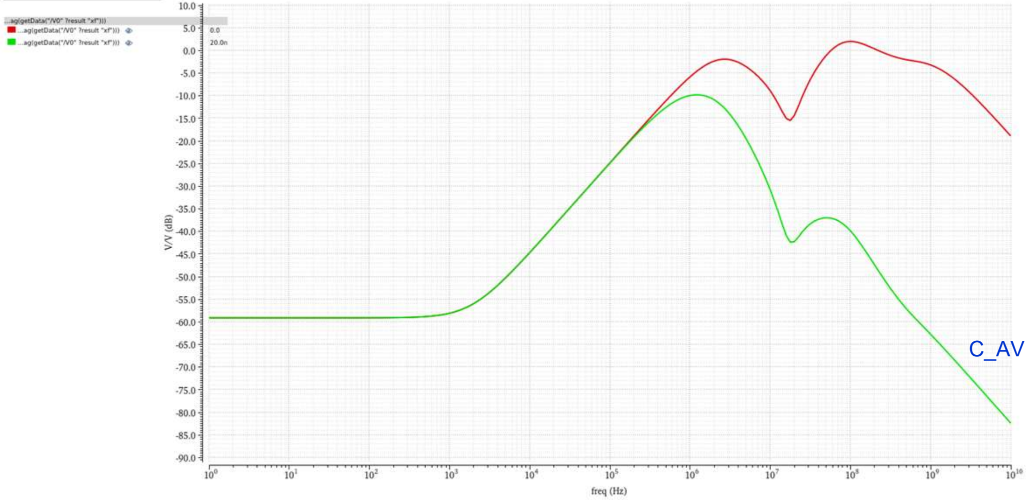
The aim of this study is to be confident to the simulation in order to validate the modifications that will be implemented in MIMOSIS-3 chip.

BACK UP

LDO Regulator

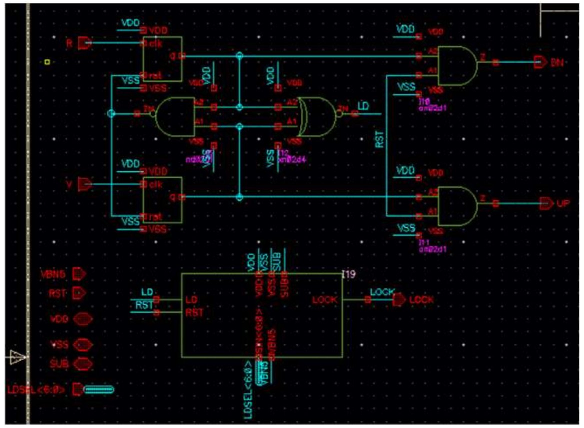


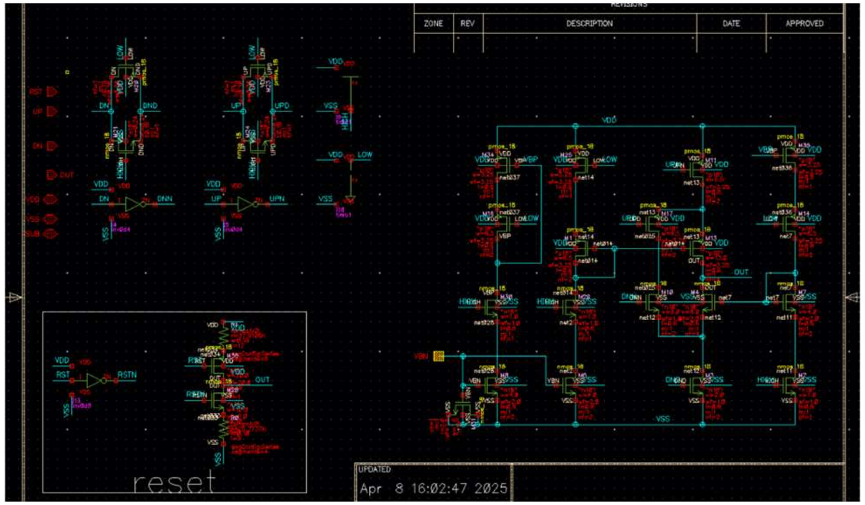
PSR (dB)

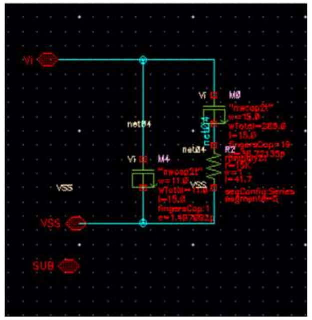


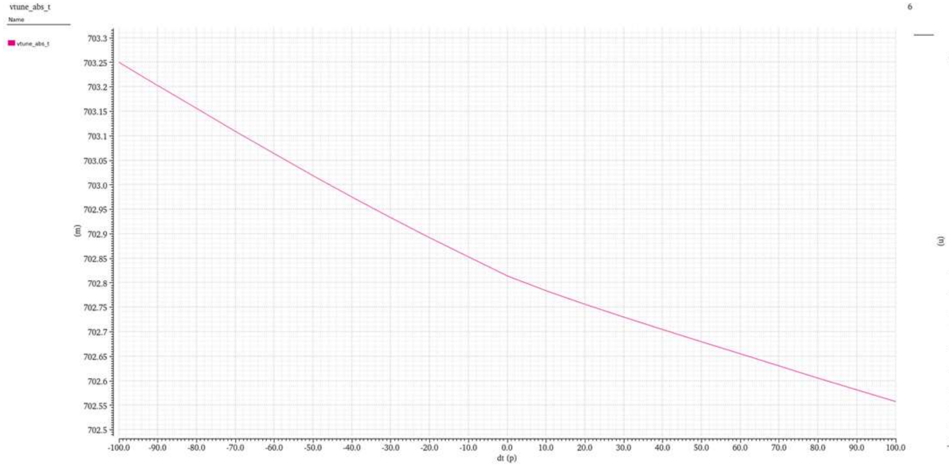
C_AVDD ~ 20 nF

PFD + CP + LPF

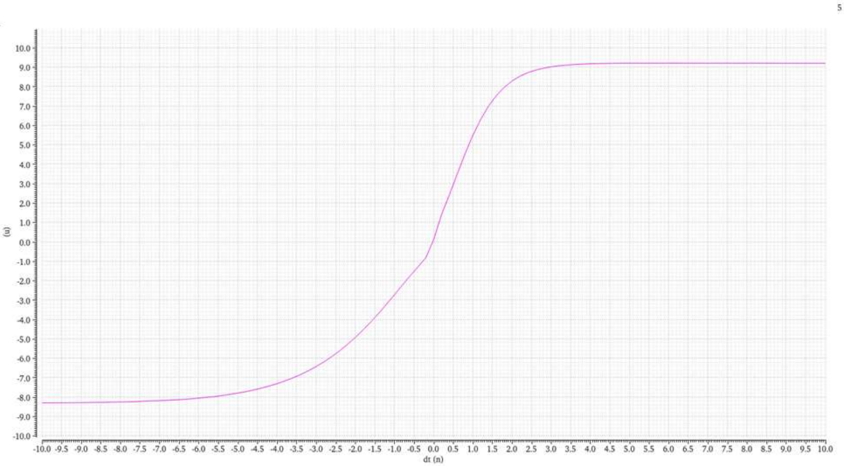








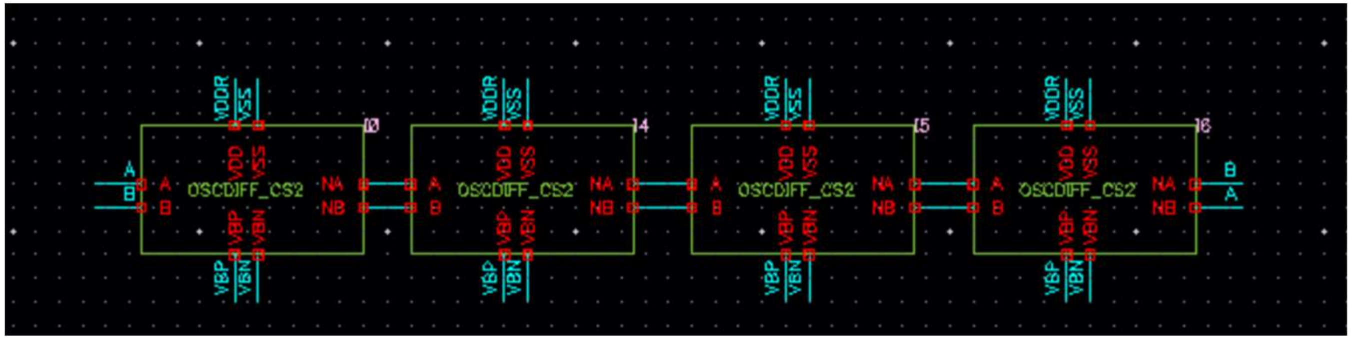
V_{tune} (mV) versus Δt (ps)
Phase range in deg : [-1.4 +1.4]

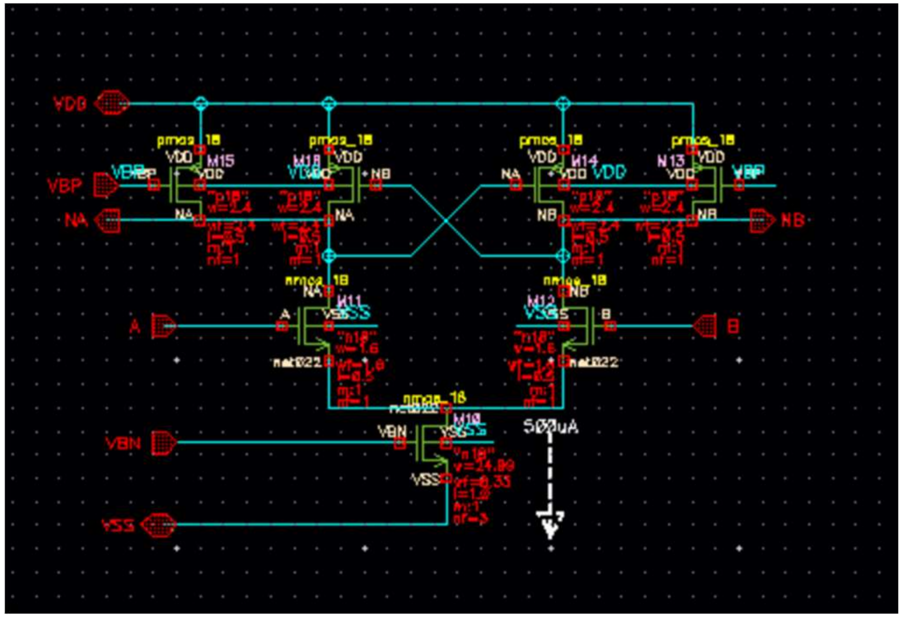


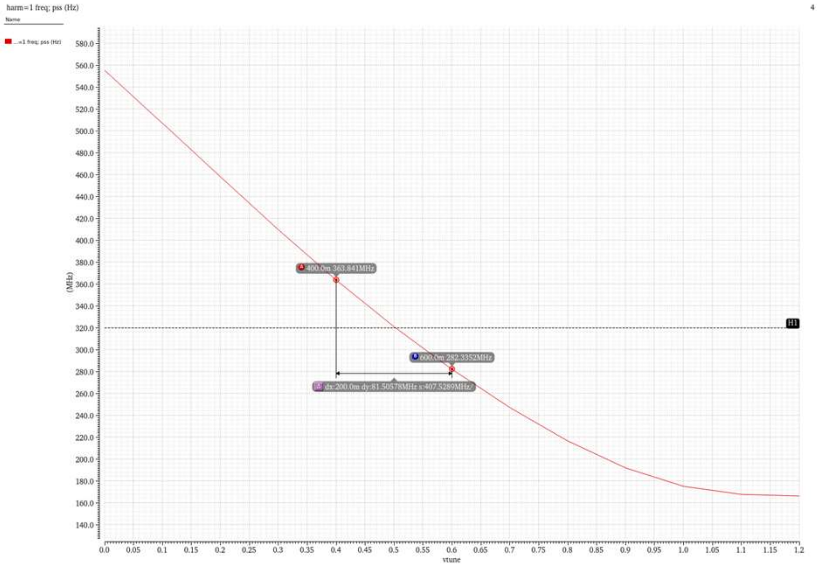
I_{charge}-$I_{discharge}$ (μA) versus Δt (ns)

Δt is the difference between rising edge of Cfbk and rising edge of Cref
Vtune is the voltage at the LPF node

VCO

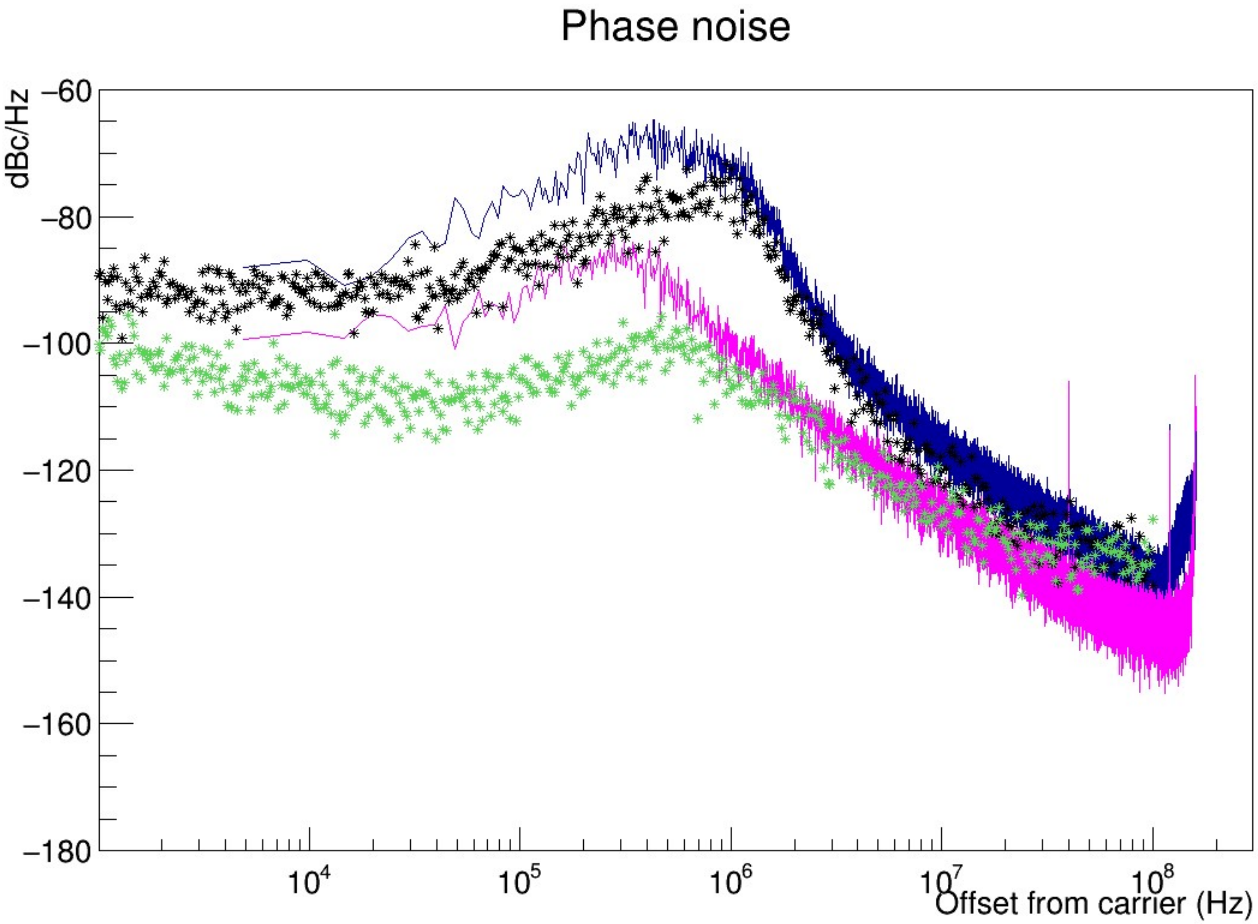






K_{VCO} ~ 400 MHz/V

Phase Noise


Phase noise
dBc/Hz
−60
−80
−100
−120
−140
−160
−180
10^4
10^5
10^6
10^7
10^8
Offset from carrier (Hz)