Front–end Electronics for Straw Tube Tracker in PANDA Experiment

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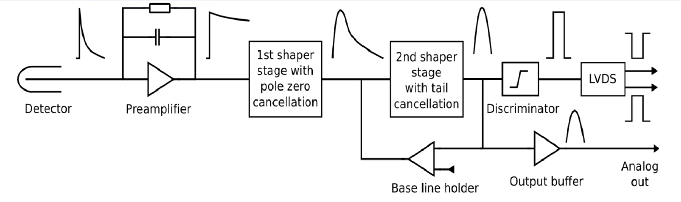
Outline

Specification



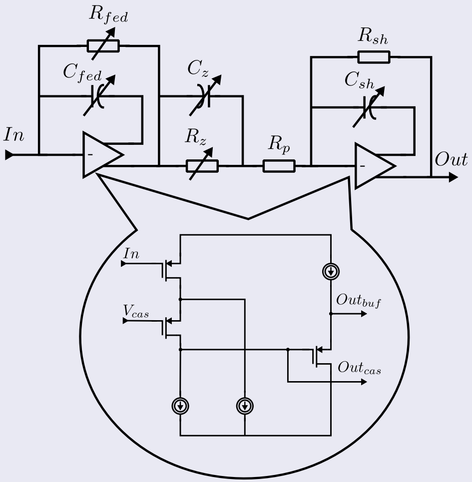
Features

- CSP with variable gain and time constant
- CR–RC^2 shaper with variable peaking time
- Ion tail cancellation circuit with trimming
- Baseline stabilized by BLH circuit
- Leading edge discriminator for time and ToT measurements
- Fast LVDS output
- Buffered analog output

Architecture

Preamplifier and Shaper

Schematic diagram



Features

- Variable charge gain: 0.5 – 4 mV/fC
- Variable preamp time constant: 25 – 800 ns
- PZC matched to various preamp settings
- 1^{st} shaper stage with T_P in range 10 – 40 ns

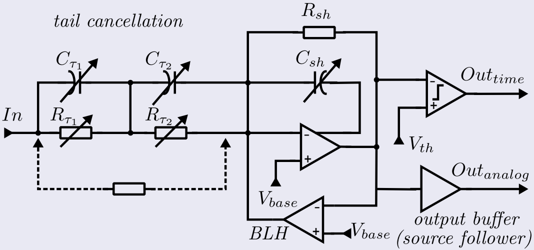
Input transistor

- Drain current = 2 mA
- W/L = $2000\mu/0.35\mu$
- Transconductance $\approx$ 26 mS

Architecture

Tail Cancellation and Output stages

Schematic diagram

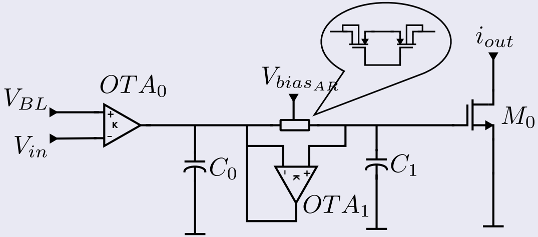


Tail cancellation

- 4 modes of operation:
  τ_1 & τ_2 TC, only τ_1 TC, only τ_2 TC, CR–RC^2 (no TC)
- Trimming time constants:
  $\tau_1 \in 3 - 43$ ns (6 bits)
  $\tau_2 \in 18 - 511$ ns (6 bits)

Architecture
Baseline Holder

Schematic diagram



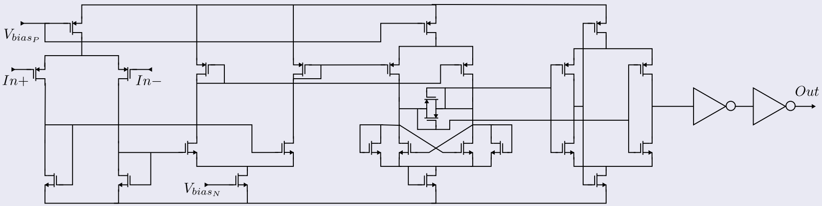
Components

- Nonlinear buffer (slew rate limited - OTA_0 and C_0)
- High value tunable active resistor for low pass filter
  (A. Tajalli, Y. Leblebici, E.J. Brauer, *Implementing Ultra-High-Value Floating Tunable CMOS Resistors*, Electronics Letters, 2008, pp. 349-350)
- Current sink controlling current in last stage feedback

Architecture

Leading Edge Discriminator

Schematic diagram



Stages

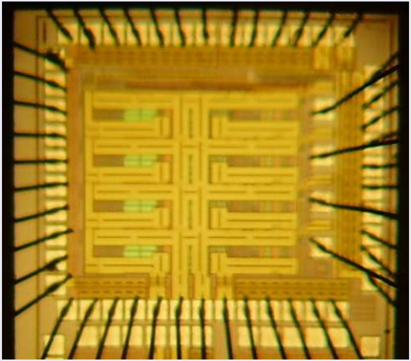
- Two low–gain preamplifing stages
- Latch stage with histeresis
- Self–biased amplifier
- Inverters

Measurement results

First prototype basic data

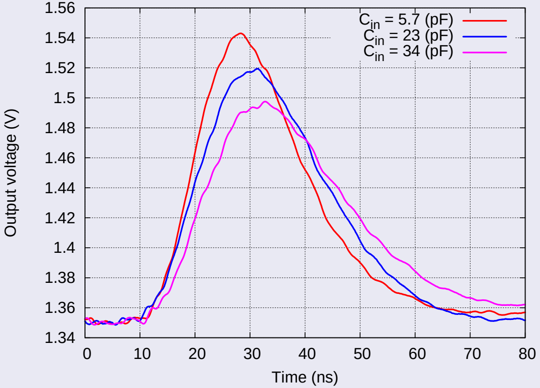
- AMS 0.35μm 2P–4M CMOS Process
- Four channels
- Channel size: 200×1130 μm^2
- Power consumption: $\sim$ 15.5 mW/ch + LVDS $\sim$ 12 mW $\approx$ 28 mW/ch
- Peripherals not yet designed, biasing and thresholds setting externally

Chip size: 1.5 × 1.2 mm^2



Measurement results
Pulse shapes

δ pulse response for 10ns T_P settings (CR–RC^2 mode – no TC)

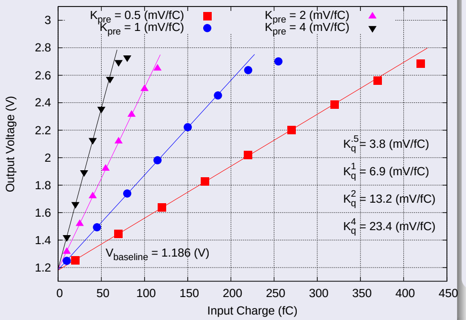


Response slower due to layout parasitics and output buffer performance

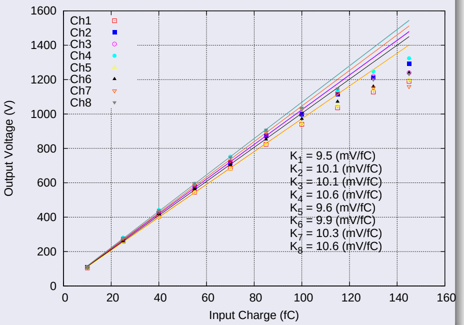
Measurement results

Linearity and Gain

Channel modes (CR–RC^2 mode – no TC)



Channel uniformity (with TC)

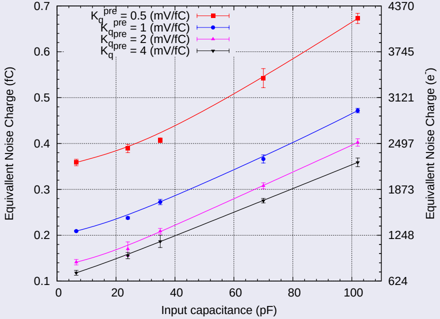


S–curves measurements

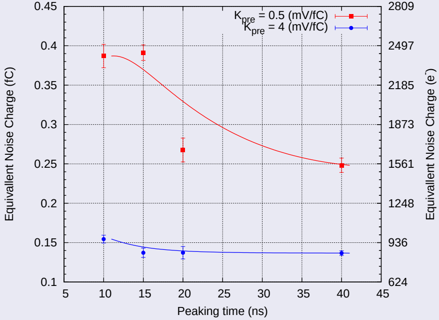
Analog buffer output

Measurement results
Noise

ENC vs input capacitance



ENC vs peaking time

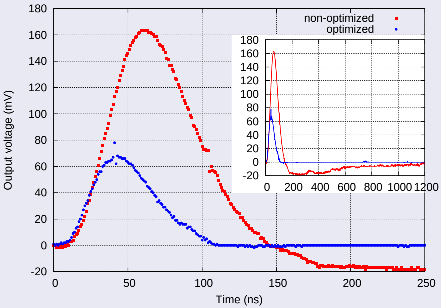


ENC $\approx$ 1000 e^- for default FE settings

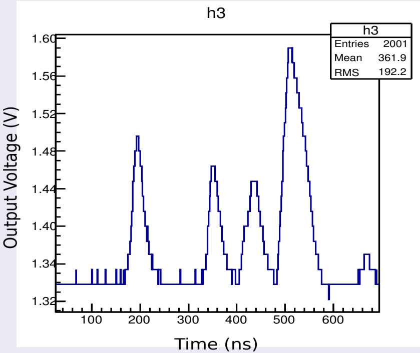
$(K_{pre} = 2mV/fC,\ T_P = 10ns \text{ and } C_{in} = 25pF)$

Measurement results
Tail cancellation

Responses for Fe^{55} X–rays

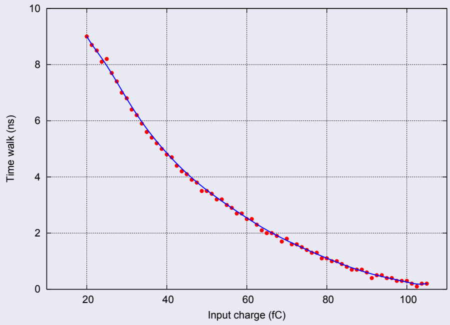


High rate

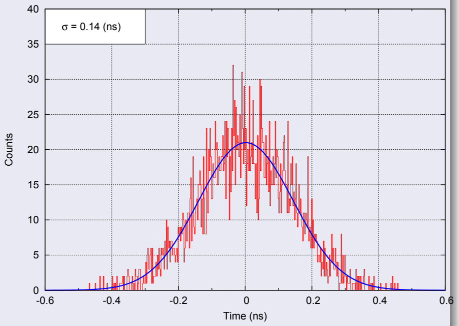


Measurement results
Time resolution

Time walk

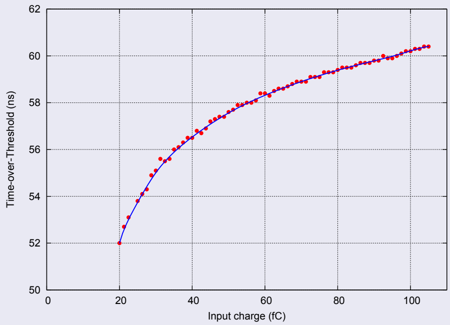


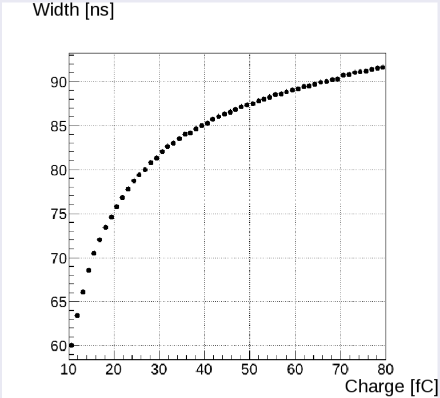
Jitter



1–2 ns time precision could be obtained by compensating time walk basing on amplitude information

Measurement results
Time–over–Threshold



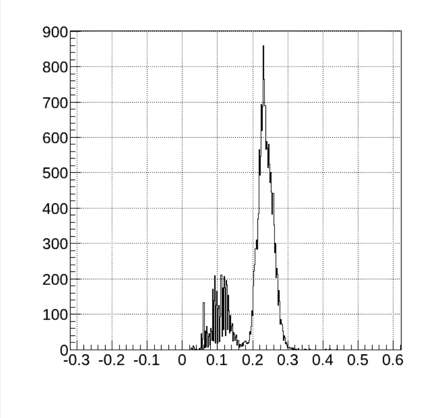


Results achieved for delta pulse and different FEE settings

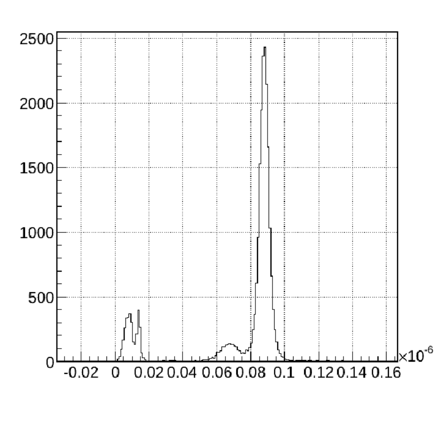
Measurement results

Fe^{55} X–rays spectrums

Amplitude spectrum



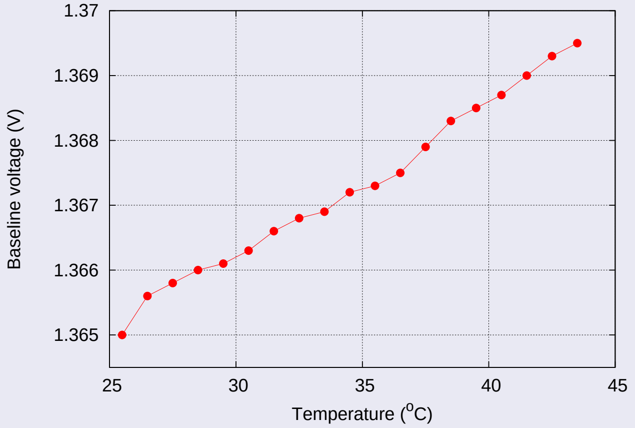
ToT spectrum



Good separation of Fe^{55} K–α and escape peaks for both methods

Measurement results
Baseline

Baseline level vs temperature



Measure after output buffer – V_{gs} and β variations

Measurement results

Summary of 1^{st} prototype

- 1^{st} prototype of STT front–end fully functional
- Variable gain 3 – 24 mV/fC and peaking time ~ 20 – 40 ns work well
- ENC ≈ 1000 e^- for default conditions ($K_{pre} = 2mV/fC$, $T_P = 10ns$ and $C_{in} = 25pF$)
- Tail cancellation works and could be trimmed to various types of input signals
- Readout module with 8 ASICs (32 channels) succesfully used in test-beam
- The front–end design and performance was presented at TWEPP–2013

Design of 2^{nd} Prototype

Features not implemented in 1^{st} prototype

- Lack of DACs for baseline control (high baseline dispersion was expected)
- Longer $\mathrm{T_P}$ (18 ns) in post–layout simulations

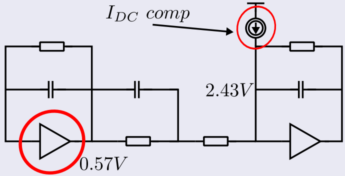
Issues found during tests

- Saturation of preamplifier for large signals
- Analog buffer not addapted for high capacitive load

Planned improvements

- Implementation of 8 channels
- Redesign of preamp/shaper for higher speed (T_P=10 ns)
- DAC addition and BLH modification for uniform baseline
- Improvement of analog buffer
- Elimination of saturation for large signals

Design of 2^{nd} Prototype
Preamplifier and shaper

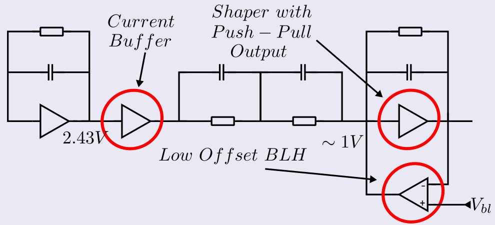


Planned Modifications

- Complementary architecture with pseudo Class AB Flipped Voltage Follower
- DC current compensation circuit
- Variable charge gain:
  1, 2 and 4 mV/fC
- Response rise time $\sim$ 5 ns ($3\times$ faster)

Design of 2^{nd} Prototype

Shapers and analog output

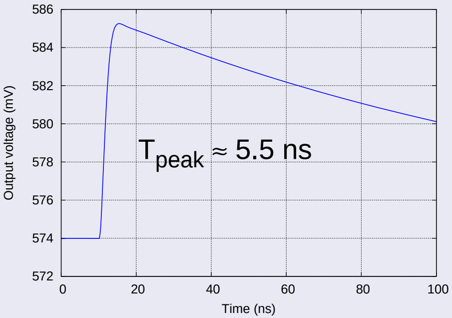


Planned Modifications

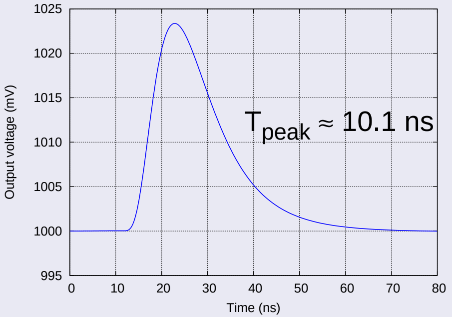
- Current buffer to separate 1^{st} shaper stage and tail cancellation (to avoid T_p walking vs TC settings)
- Improvments of BLH to minimize offset ($\sigma \approx 5$ mV)
- 2^{nd} shaper stage with high performance Push–Pull buffer

Design of 2^{nd} Prototype
Simulation results

Preamplifier



Analog output – δ pulse, CR–RC^2

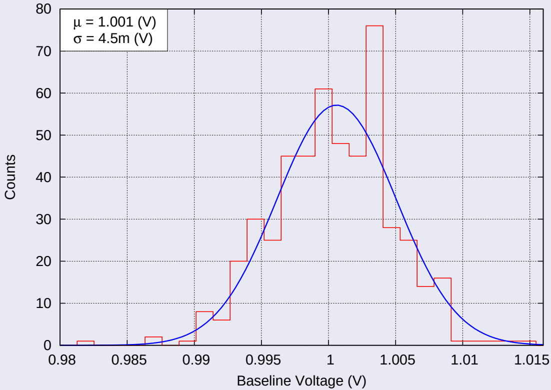


$T_P \approx 15$ ns in 1^{st} prototype

$T_P \approx 17$ ns in 1^{st} prototype

Design of 2^{nd} Prototype
Simulation results

Baseline dispersion



- Baseline dispersion one order of magnitude less than in 1^{st} prototype
- 4–bits DAC will be added for fine tunning

Summary and plans

Front–end development status

- 1^{st} prototype of STT front–end fully functional
- Variable gain 3 – 24 mV/fC and peaking time ∼ 20 – 40 ns work well
- ENC ≈ 1000 e^- for default conditions ($K_{pre} = 2mV/fC$, $T_P = 10ns$ and $C_{in} = 25pF$)
- Tail cancellation works and could be trimmed to various types of input signals
- Readout module with 8 ASICs (32 channels) succesfully used in test-beam

Future plans

- New improved front–end design in progress:
  - 8 channels
  - DACs for threshold and baseline settings
  - Faster preamp/shaper
  - Stronger output buffer
  - Better performance for large signals
- Submission of new prototype planned at the end of this year (if founds available)