Fachhochschule Dortmund
University of Applied Sciences and Arts

Efficient Powering of Inner Layer LHC Detector Electronics

SLDO & HF-DCDC

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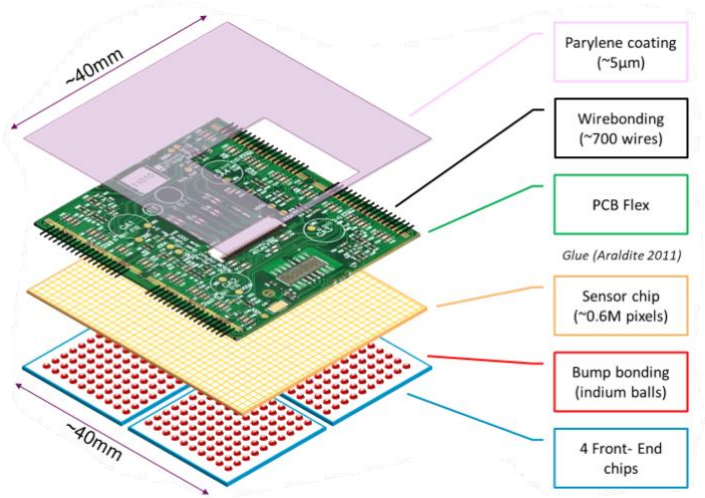
Power Demand of Pixel Detectors

- Hybrid-Pixel detectors are power hungry devices

Chip	Pixel Area	Current per Pixel	Current Density
FE-I3	50 x 400 µm^2	47 µA	1400 A/m^2
FE-I4	50 x 250 µm^2	16 µA	1280 A/m^2
RD53	50 x 50 µm^2	7 µA	2800 A/m^2

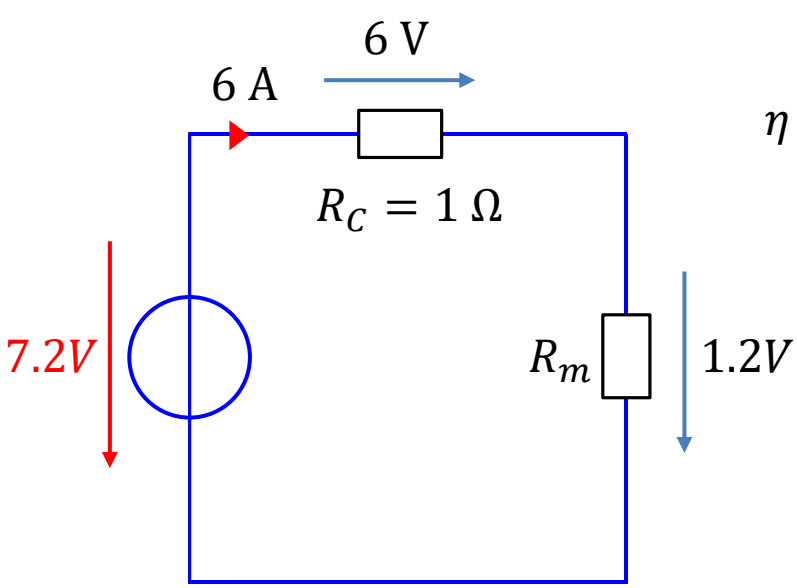
- Increased current consumption caused by
  - parasitic detector capacitances
  - additional digital functionality

- ITkPix quad-module expected to consume 4.5-7.5 A of current
  - Exact current consumption depends module position e.g. layer



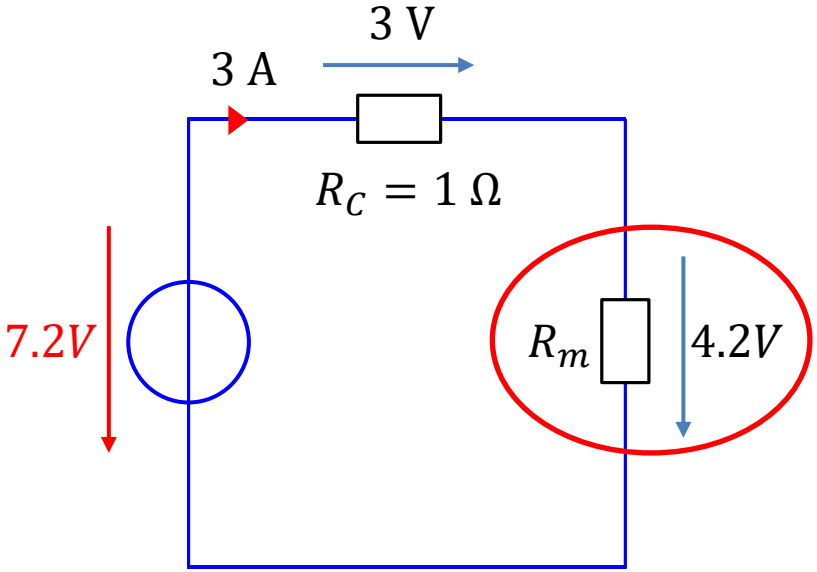
Need for Low Mass

- detector mass influences the tracking and calorimeter resolution
  - multiple-scattering, Bremsstrahlung, photon conversion
- limited material budget
  - affects available number and diameter of supply lines
  - no sense lines
- long supply lines
  - power supplies are outside the active area
  - assuming c.a. 200m aluminum of 5 mm^2 diameter gives 1Ω cable resistance

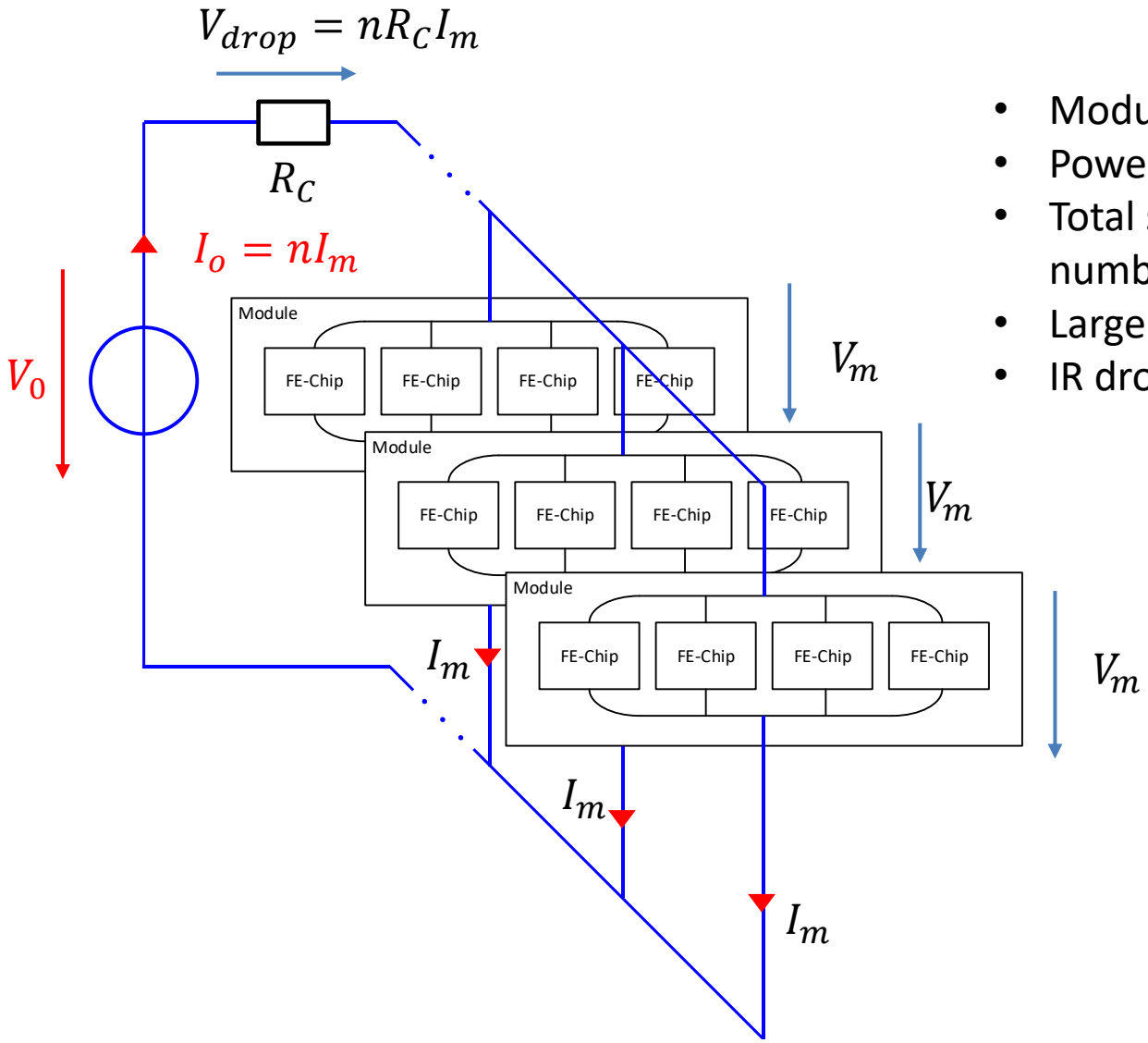


$$\eta = \frac{1.2V \cdot 6A}{7{,}2V \cdot 6A}$$

$$\approx 16.7\ \%$$



Power Efficiency of Conventional Power Scheme



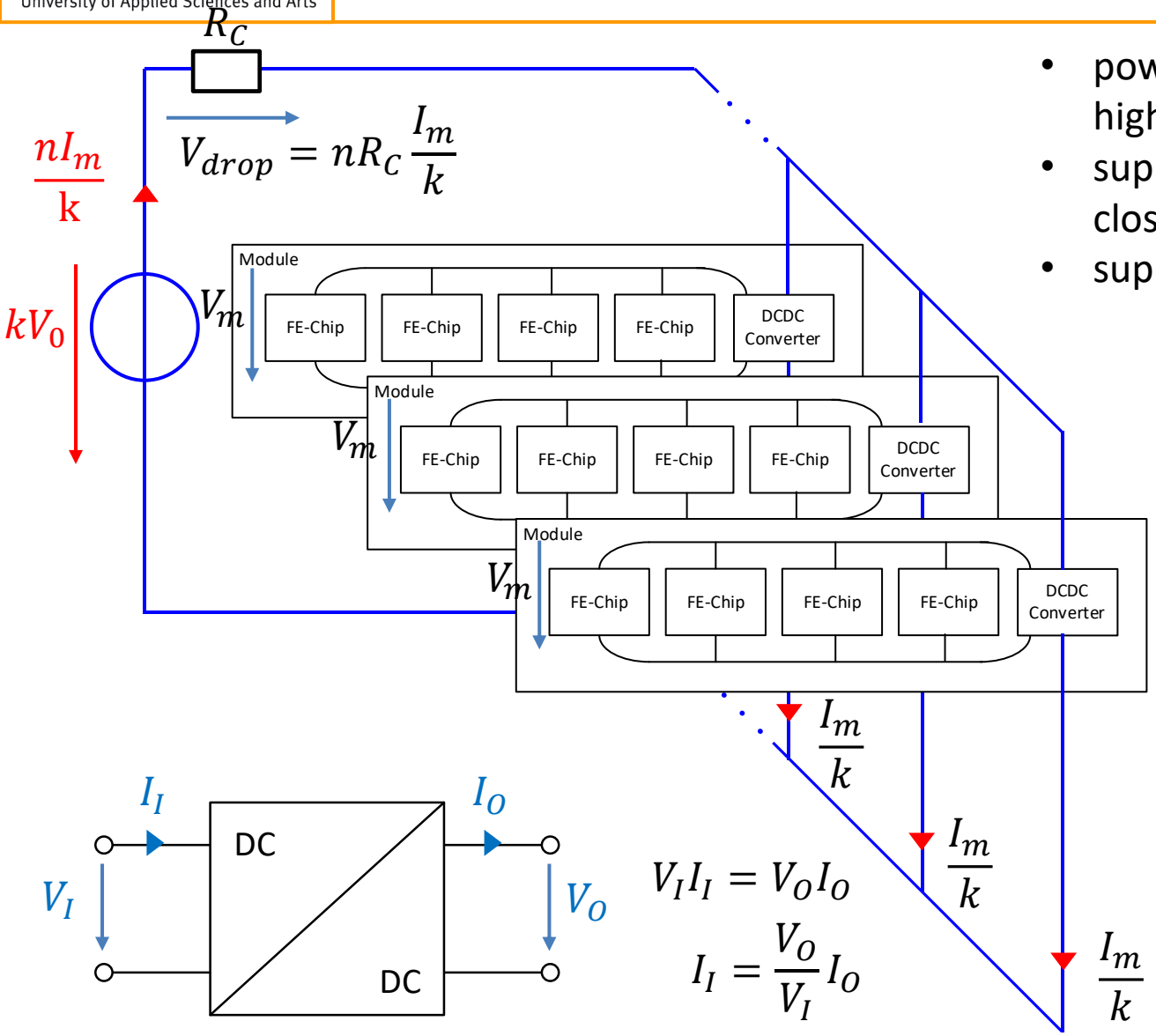
- Modules are connected in parallel
- Powered by constant voltage source
- Total supply current scales with the number n of modules
- Large supply currents affect efficiency
- IR drops on power cables

$$\eta = \frac{1}{1 + n\frac{R_C I_m}{V_m}}$$

$$\eta = \frac{1}{1 + 16\frac{1\Omega \cdot 6A}{1{,}2V}}$$

$$\approx 1.23\ \%$$

DC / DC Conversion



$$V_I I_I = V_O I_O$$

$$I_I = \frac{V_O}{V_I} I_O$$

- power is distributed at k-times higher supply voltage
- supply voltage is converted down close to the load
- supply current is reduced by k

$$\eta = \frac{1}{1 + \frac{n}{k^2} \frac{R_C I_m}{V_m}}$$

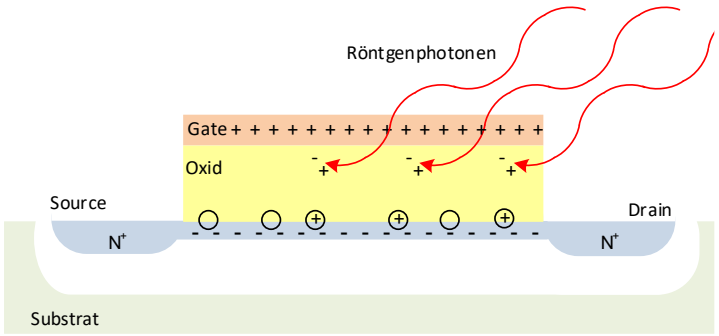
$$\eta_4 = \frac{1}{1 + \frac{16}{16} \frac{1\Omega \cdot 6A}{1.2V}}$$

$$\approx 16.7\ \%$$

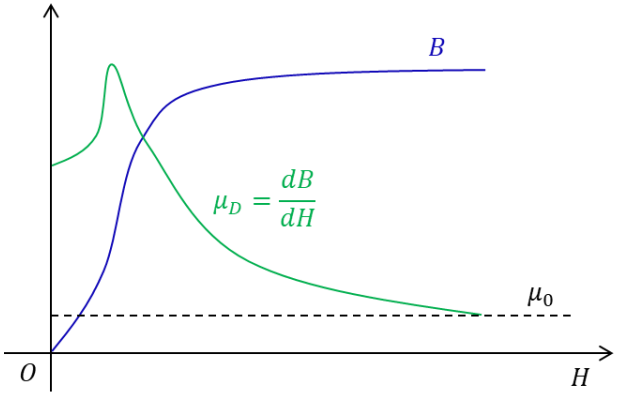
$$\eta_8 \approx 44.4\ \%$$

$$\eta_{16} \approx 76.2\ \%$$

Special Conditions in HEP Experiments

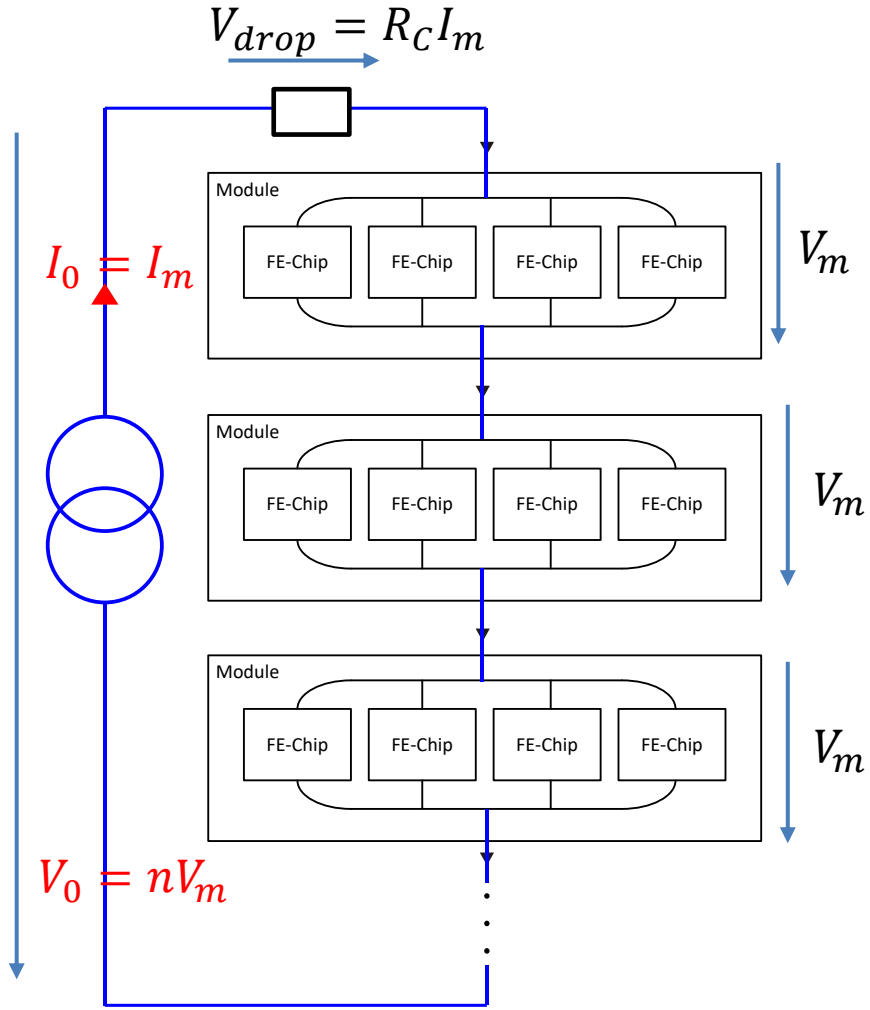


- 1 Grad (10 Msvt) of Total Ionizing Dose
- significant radiation induced threshold voltage shifts for gate-oxide thickness larger than 5nm



- High magnetic field to measure momenta and charge
- ferromagnetic materials saturate
- only air coils applicable
- air coils have larger dimensions than coils with core

Serial Powering



- modules are connected in series
- powered by constant current source
- total supply current is defined by maximum load current of a single module
- total supply voltage across the chain scales with the number of powered modules

$$\eta = \frac{1}{1 + \frac{R_C I_m}{n V_m}}$$

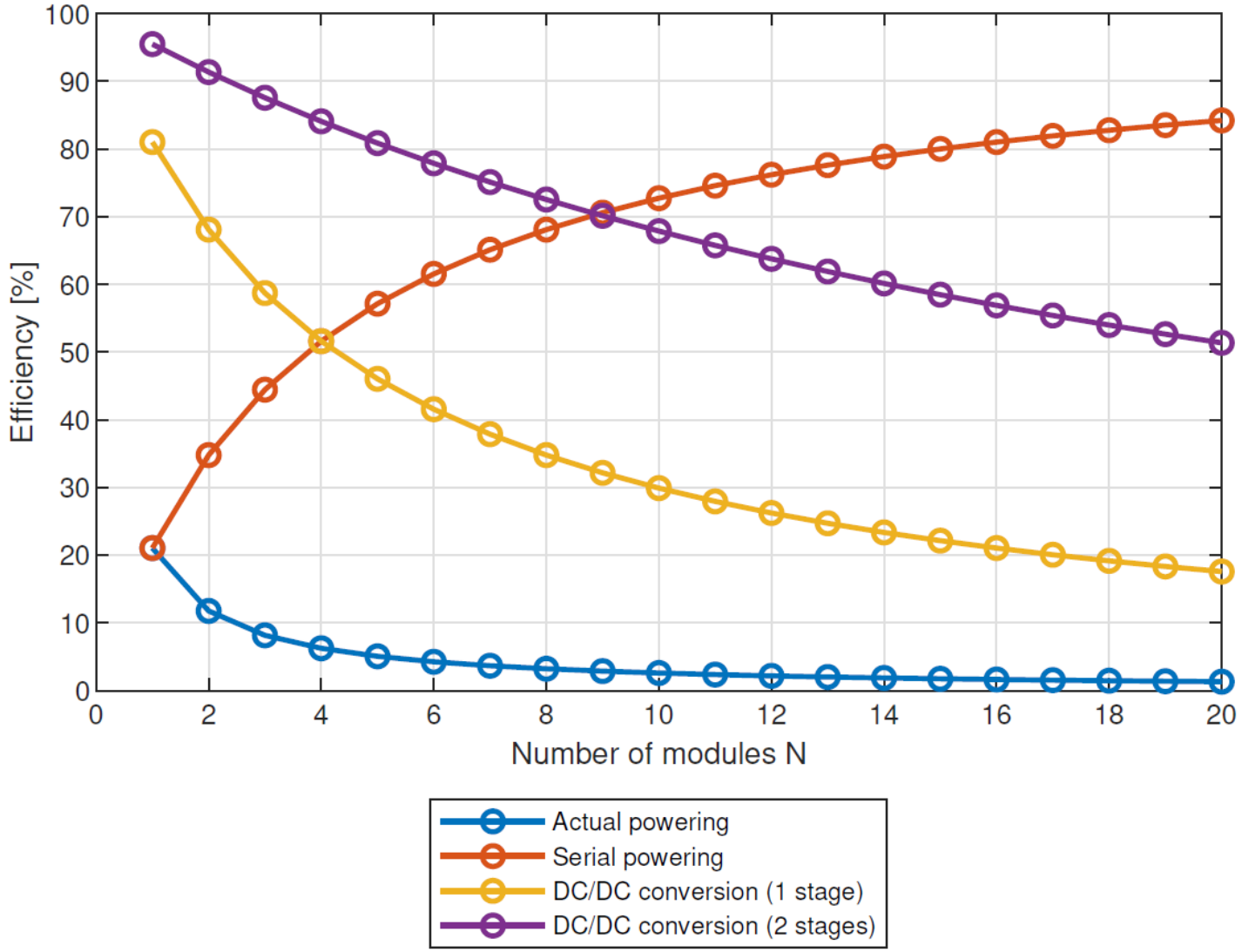
- regulator circuitry required to generate constant supply voltage out of constant current

$$\eta = \frac{1}{1 + \frac{1\Omega \cdot 6A}{16 \cdot 1.2V}}$$

$$\approx \frac{1}{1 + \frac{1\Omega \cdot 6A}{16 \cdot 1.2V}}$$

$$\approx 76{,}2\%$$

Efficiency of Different Power Supply Concepts

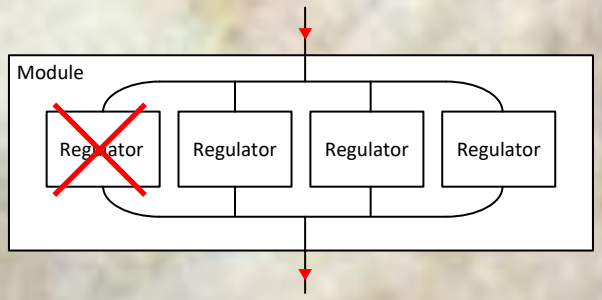


$V_m = 1.2V$
$I_l = 4.5\ A$
$R_c = 1\ \Omega$
$k_1 = 4$
$k_2 = 2.5$

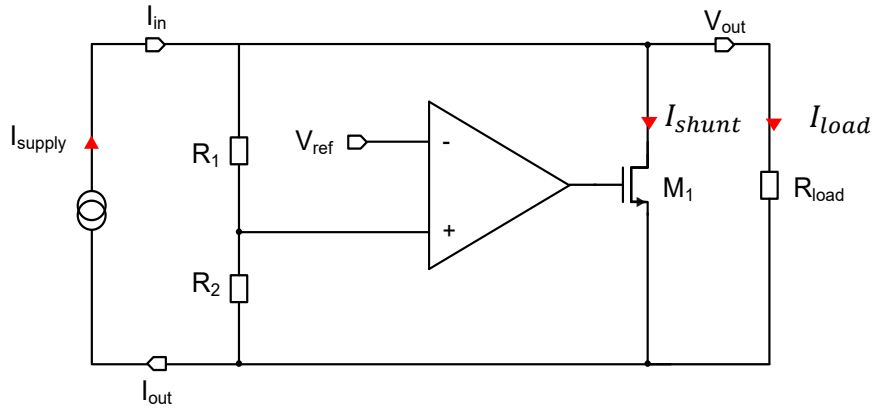
The Serial Powering Commandments

- **You shall prevent the break of the serial powering chain**
- **You shall avoid hot spots**
- **You shall distribute power equally across the chips and the module**
- **You shall avoid single point of failure**
- **You shall introduce redundancy**

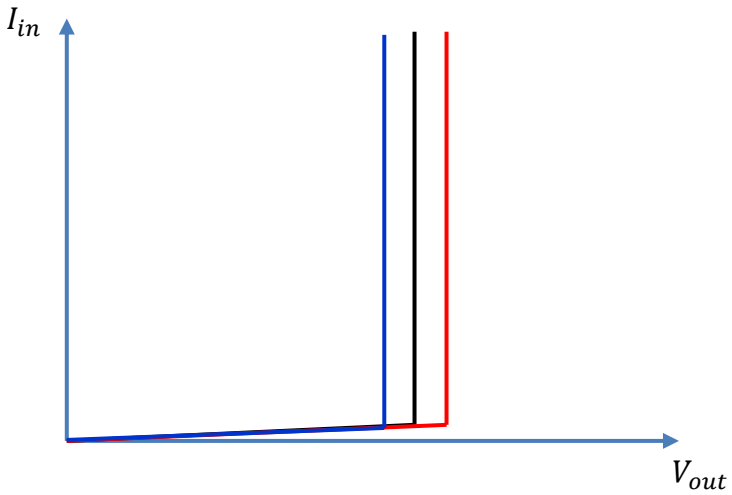
- **You shall operate several regulators in parallel on module level**



Shunt Regulator Operation Principle

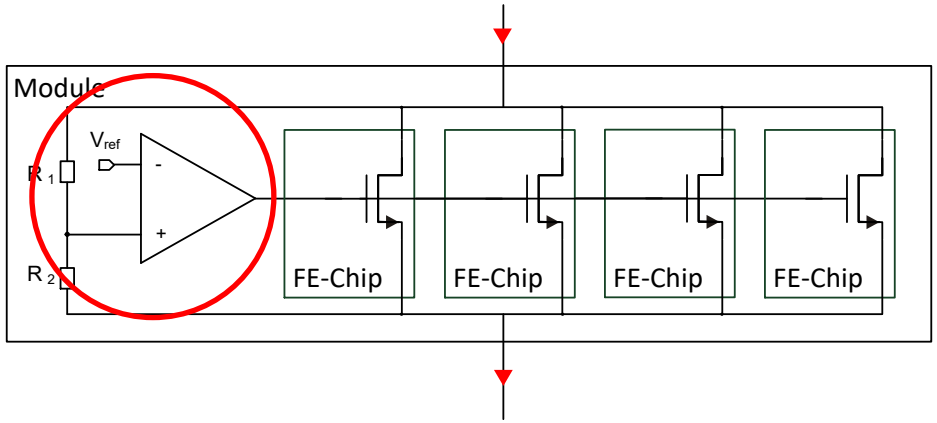


- Voltage regulation by current steering
- Current flow through load defines V_{out}
- Referenced voltage $V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$
- Excess current I_{Shunt} is shunted by M1
- $I_{in} > I_{load} \rightarrow \eta = \frac{I_{load}}{I_{in}}$

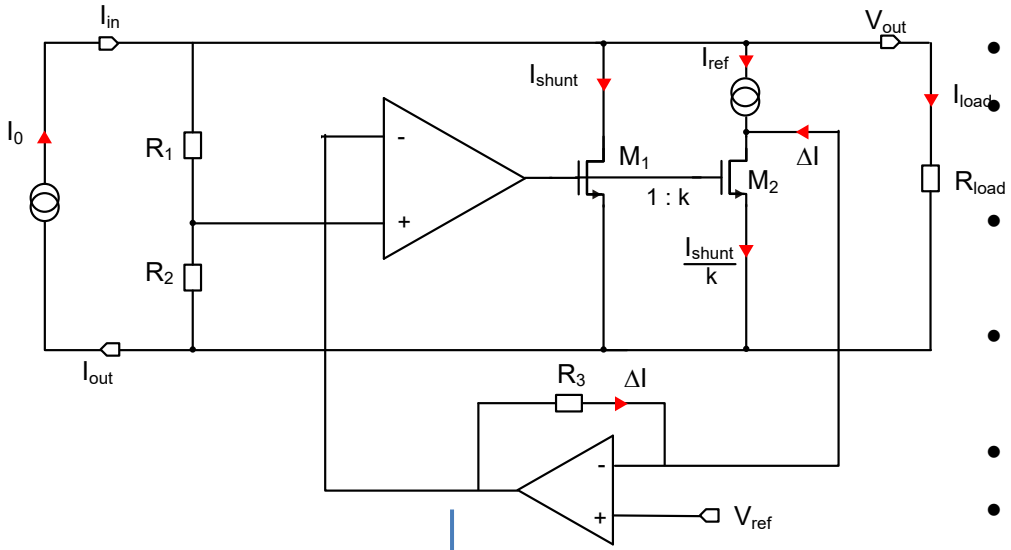


- Very steep voltage to current characteristic
- → Small voltage source output impedance ☺
- → Unbalanced current distribution across parallel placed regulators ☹
- Parallel placed regulators generate different V_{out}
  - voltage reference variations
  - error amplifier offset
  - resistor mismatch
  - ground shifts
- Current will flow through regulator with small V_{out}
- Regulator may be destroyed due to overload cond.

Known Methods to Combat Unbalanced Shunt Current Distribution



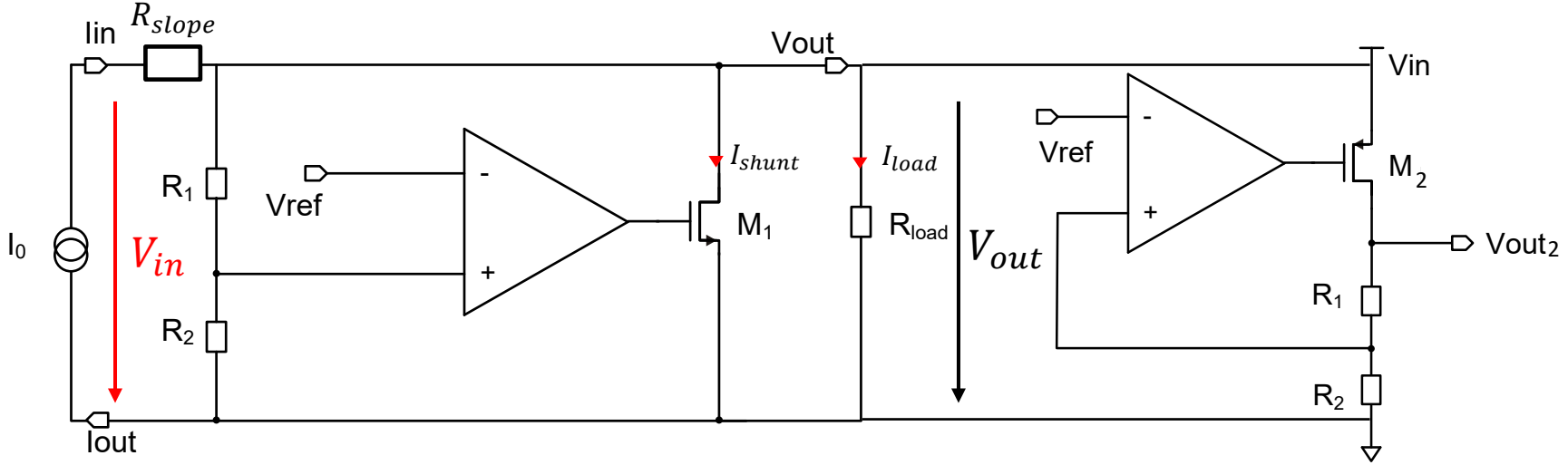
- Distributed shunt transistors but single control circuitry
- Balances shunt current across the module
- Achilles heel → control circuitry
- Malfunctioning control circuit leads to loss of module or even loss of complete chain
- Module parasitics complicate design

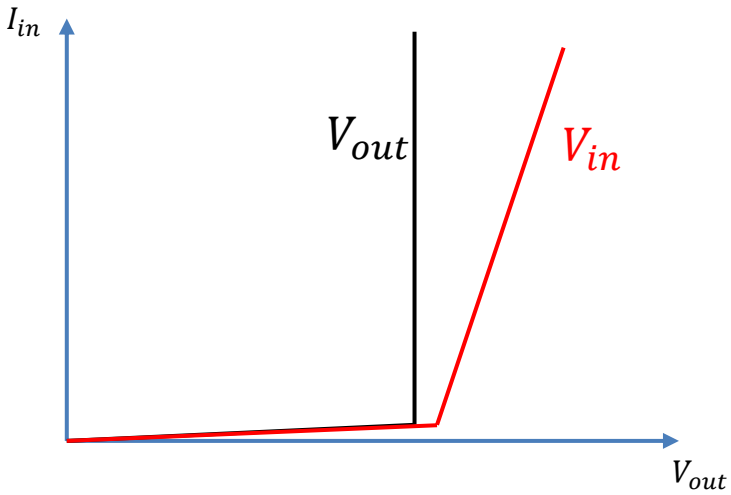


- Trimming of voltage reference
- Fraction of the shunt current is mirrored and compared with a current reference
- Current difference ΔI is read out by transimpedance amplifier
- Transimpedance amplifier voltage output is fed back to the error amplifier as reference
- Effective reference voltage rises with ΔI
- Vout increases → I_{Shunt} decreases ☺
- Vout depends on load current ☹ →Bad output impedance

simplified design don't try at home → won't work

FE-I3 Regulator Approach





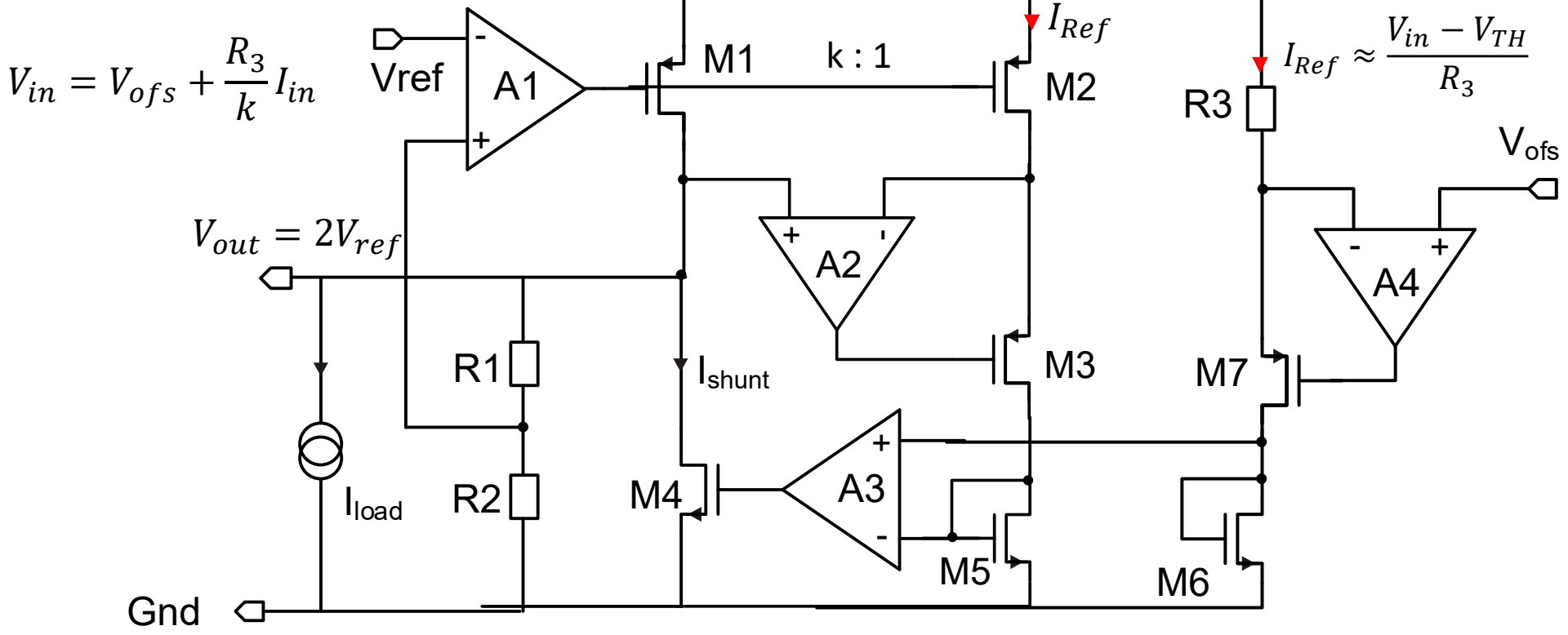
- Resistor R_{slope} is added to the current input
- R_{slope} decreases the IV-slope of V_{in}(not V_{out})
- R_{slope} helps distributing the shunt current between parallel placed regulators ☺
- Output impedance is not affected ☺
- R_{slope} decreases power efficiency ☹

- Additional supply voltage is generated by LDO
- Design Idea of Shunt LDO Regulator:
- Move shunt transistor M_1 to LDO load
- Replace R_{slope} by LDO pass transistor M_2

Design Concept

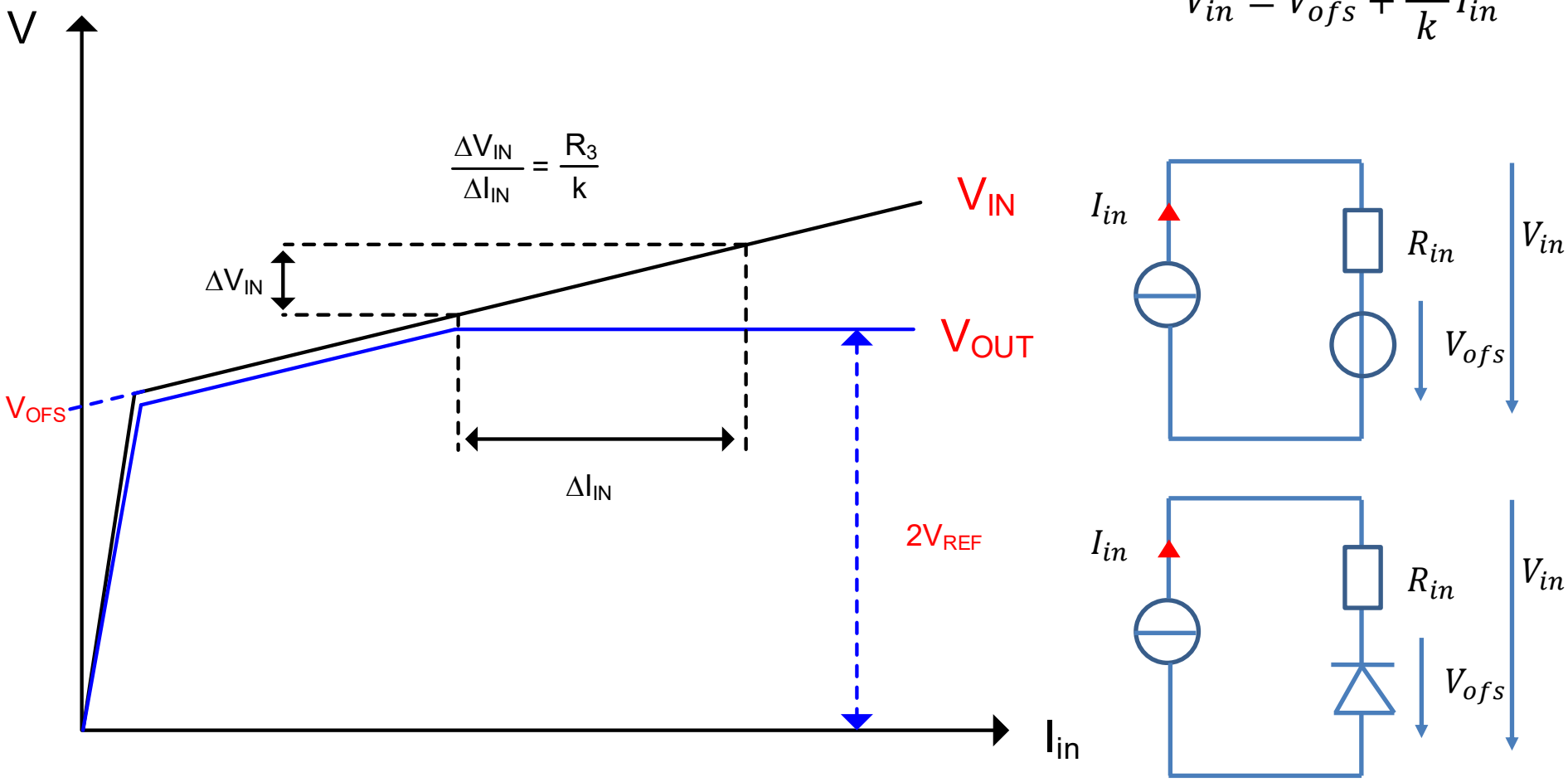
- The Shunt-LDO regulator combines the functionality of an LDO voltage regulator with the capability of a shunt regulator to drain a constant current
- Two control loops: 1) constant output voltage 2) constant current flow through the regulator

$$I_{in} \approx kI_{Ref} \approx k\frac{V_{in} - V_{ofs}}{R_3}$$



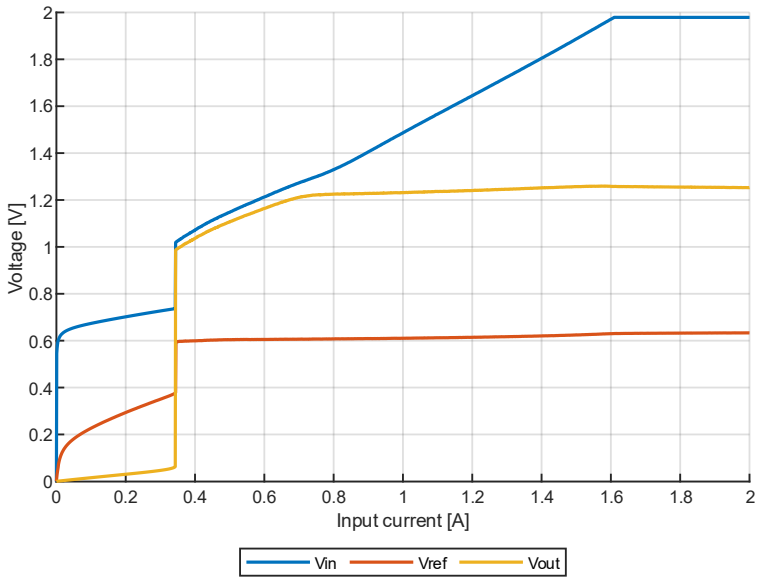
V/I Characteristic

$$V_{in} = V_{ofs} + \frac{R_3}{k} I_{in}$$

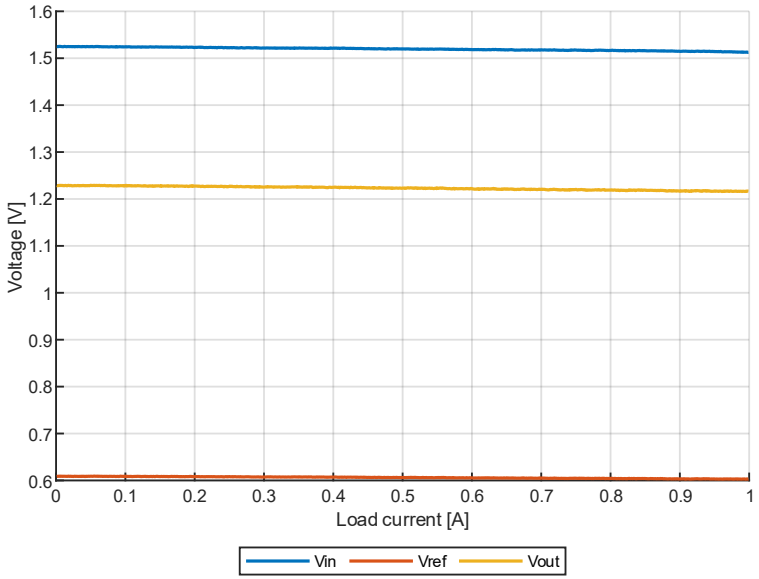


Measurements Line & Load Regulation

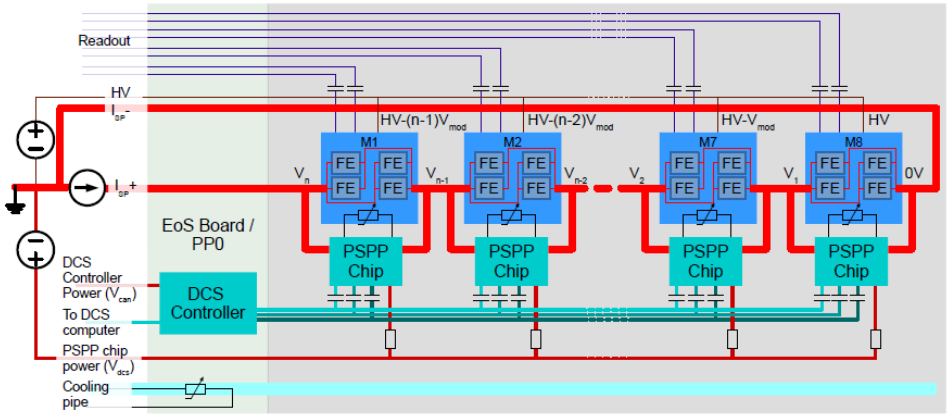
- Line Regulation $= \frac{\Delta V_{out}}{\Delta I_{in}} = \boldsymbol{25mV/A}$



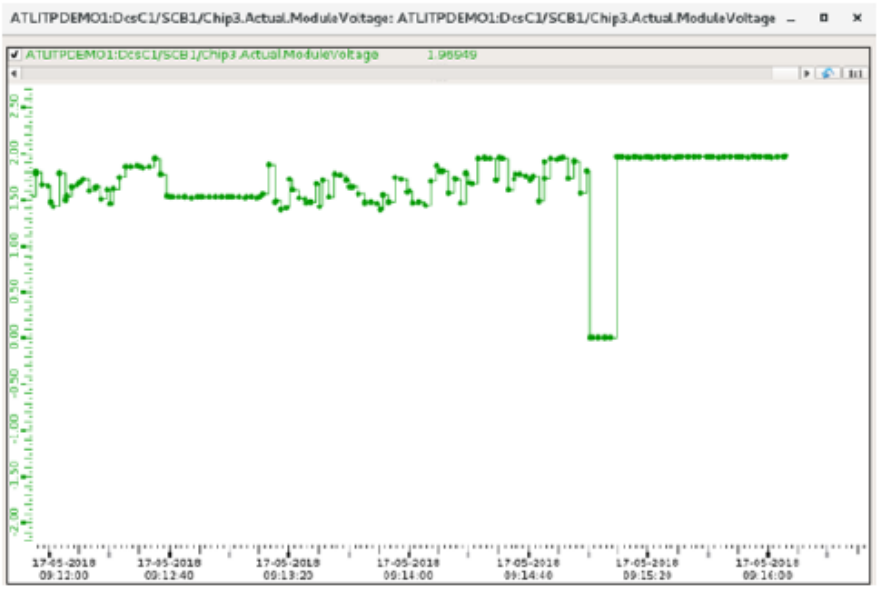
- Load Regulation $= \frac{\Delta V_{out}}{\Delta I_{load}} = \boldsymbol{11.5mV/A}$

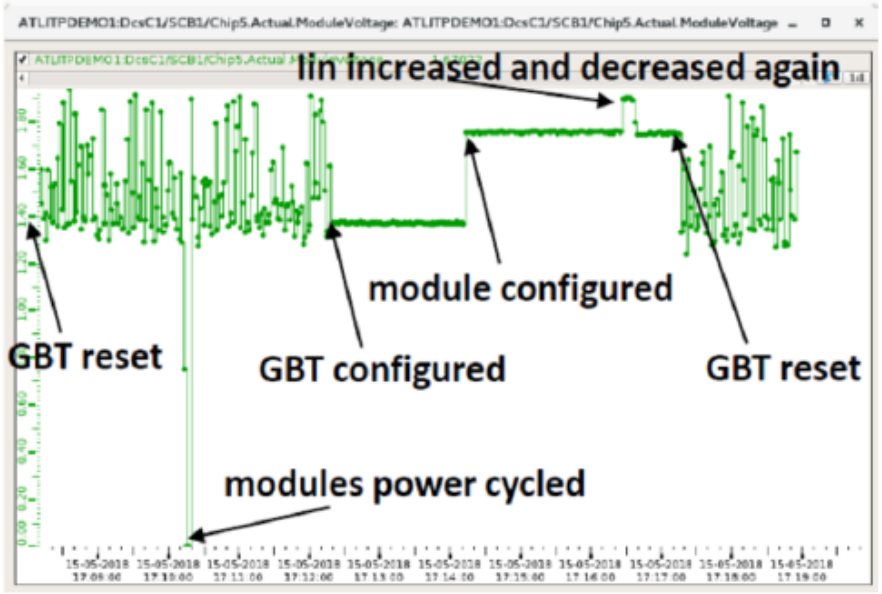


Lessons Learned Outer Barrel Demonstrator

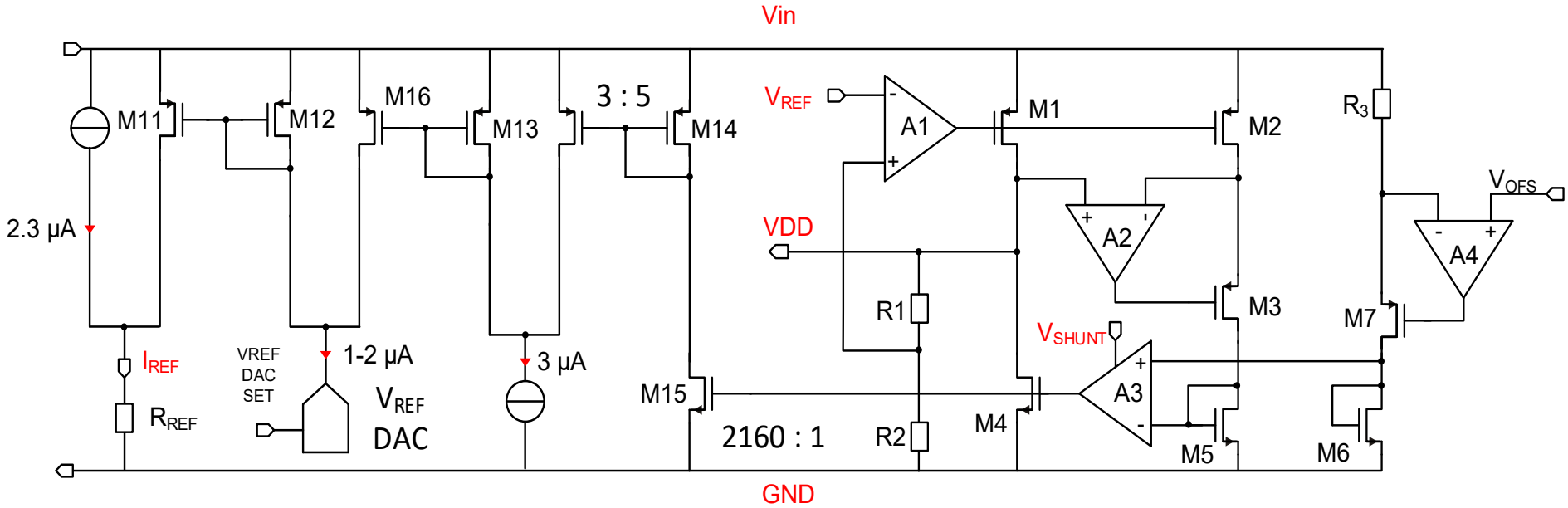


- FE-I4 quad module based serial chain
- Overload current situation reduces module (SLDO input) voltage
- Other modules in chain see overvoltage
- PSPP chip triggers and generates even more overvoltages





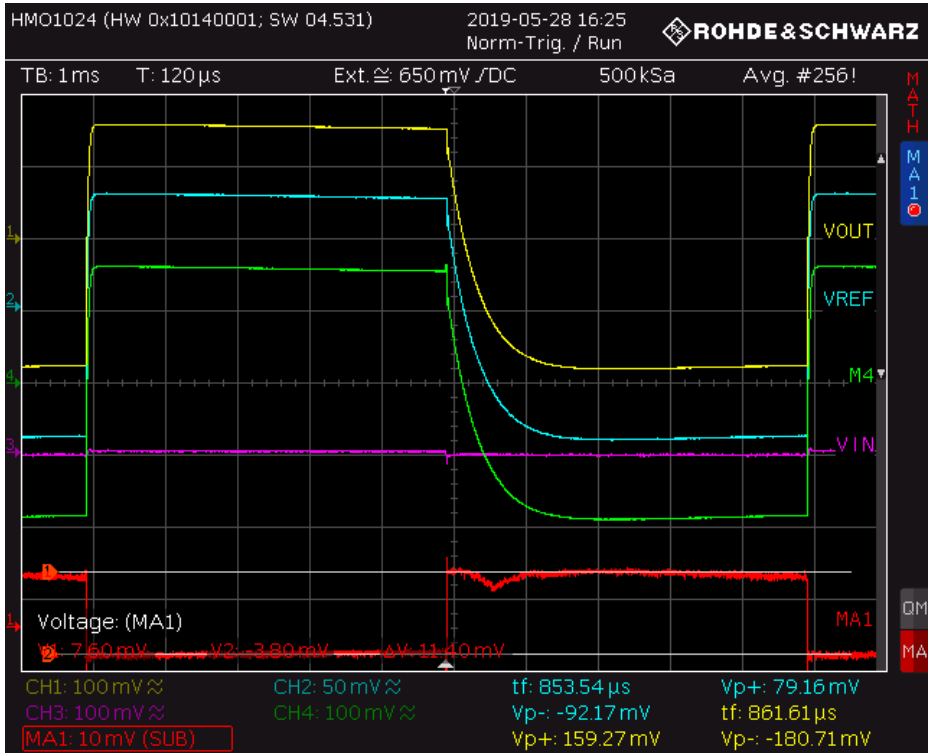
Protection Feature: Overload Protection



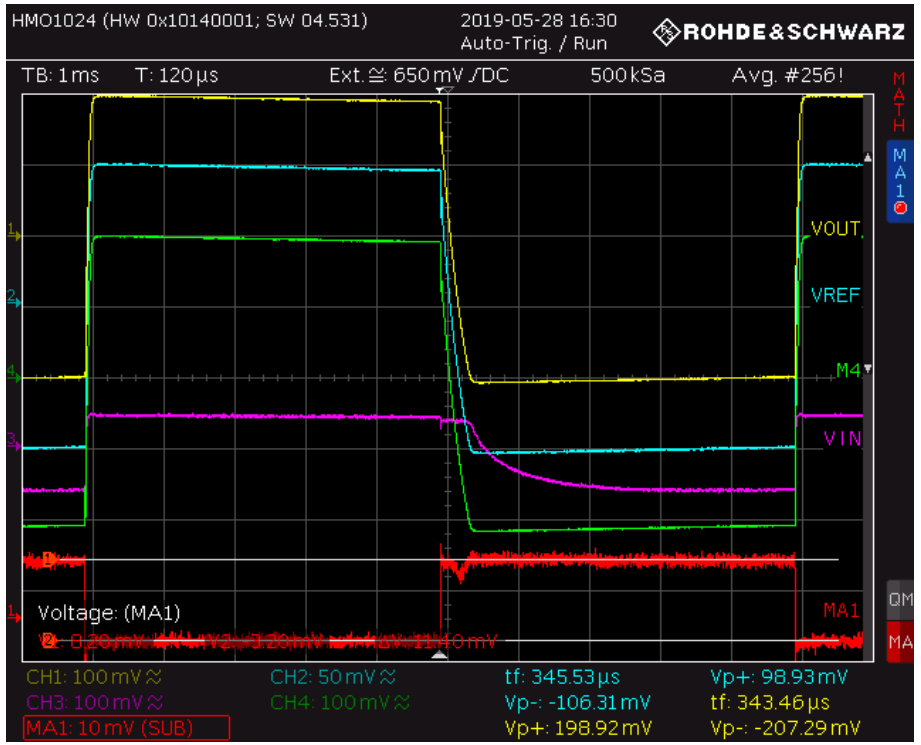
- With RD53A overload currents lead to collapse of regualtor input voltage
  - This lead to overvoltages at other modules in the serial chain
- RD53B protects against overloads which are considered as undershunt current scenarios
  - high load current reduces shunt current
- In undershunt current case Vout is reduced
  - Vout is lowered by lowering Vref
- Activation Threshold Ishunt < 10 mA
- Vout minimimum value 700mV → Vref minimum value 350 mV

Measurement of Overload/Undershunt Protection

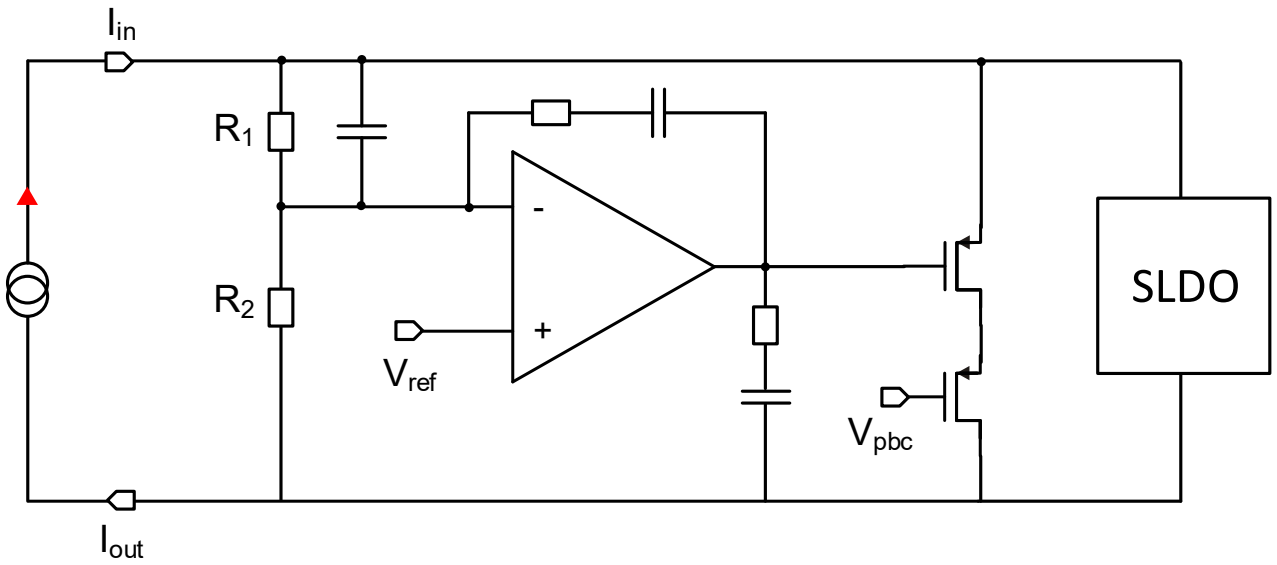
Enabled



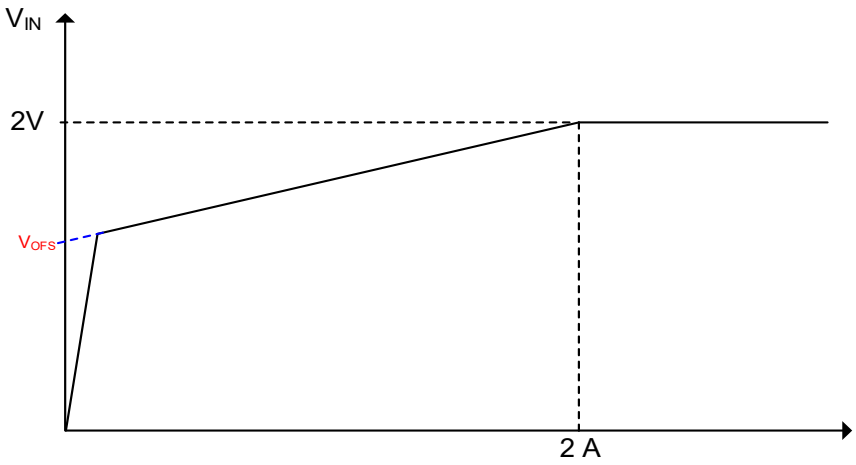
Disabled



Protection Feature: Overvoltage Protection Voltage Clamp

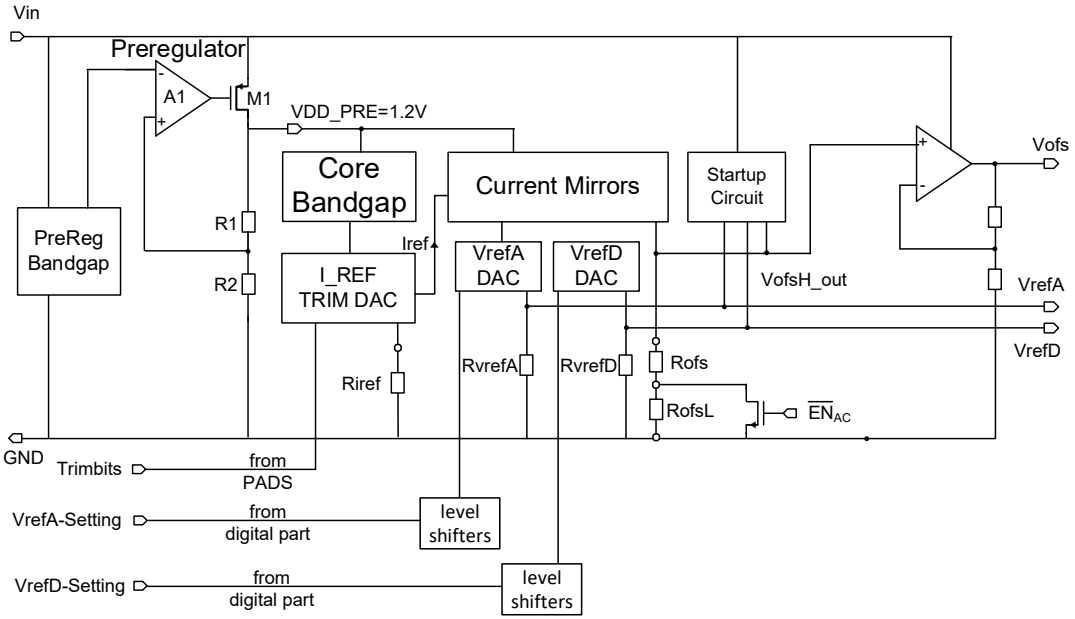


- voltage clamp implemented as shunt regulator
  - operated in parallel to SLDO
- takes all excess current in case Vin =>2v
- limits the voltage to 2V
- can absorb up to 2A additional current per chip
- OVP threshold defined by untrimmed bandgap
  - voltage limit can vary +/- 5%

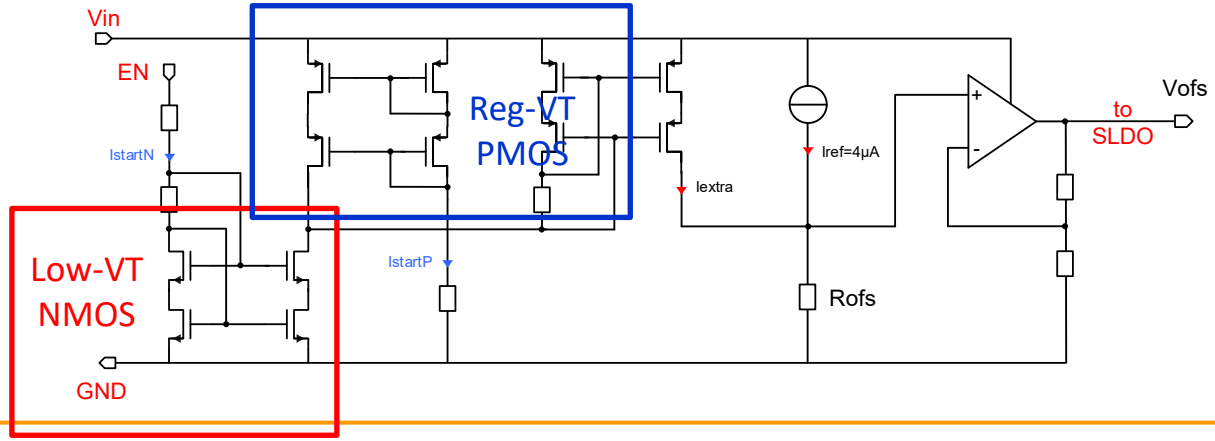


Startup Optimization

- Startup should not depend on too many bandgaps circuits

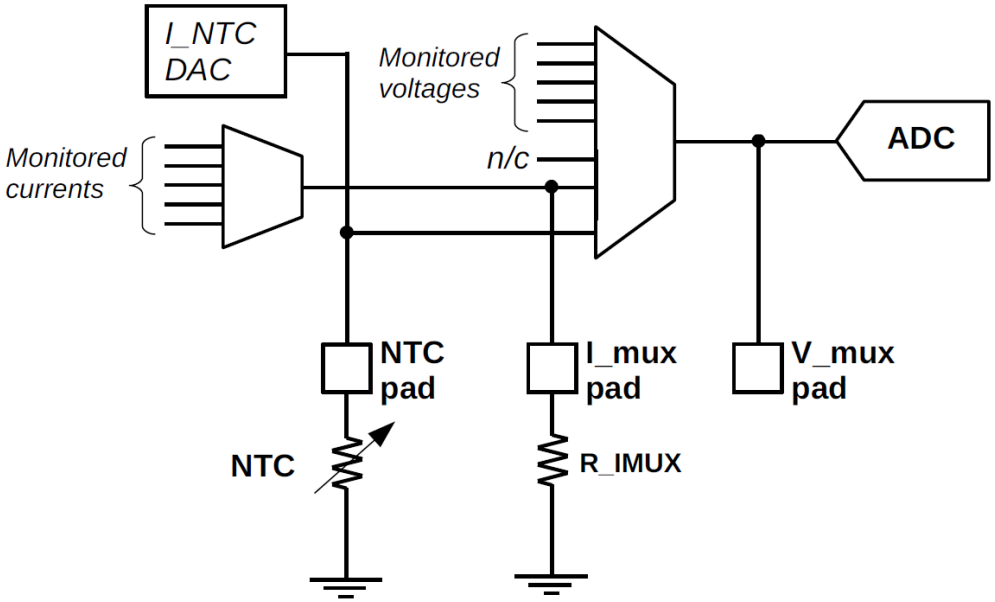


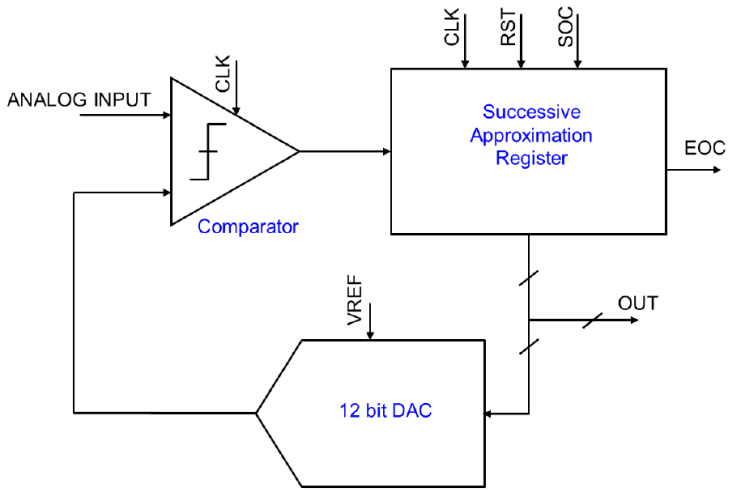
- SLDO must be in high-impedance during startup



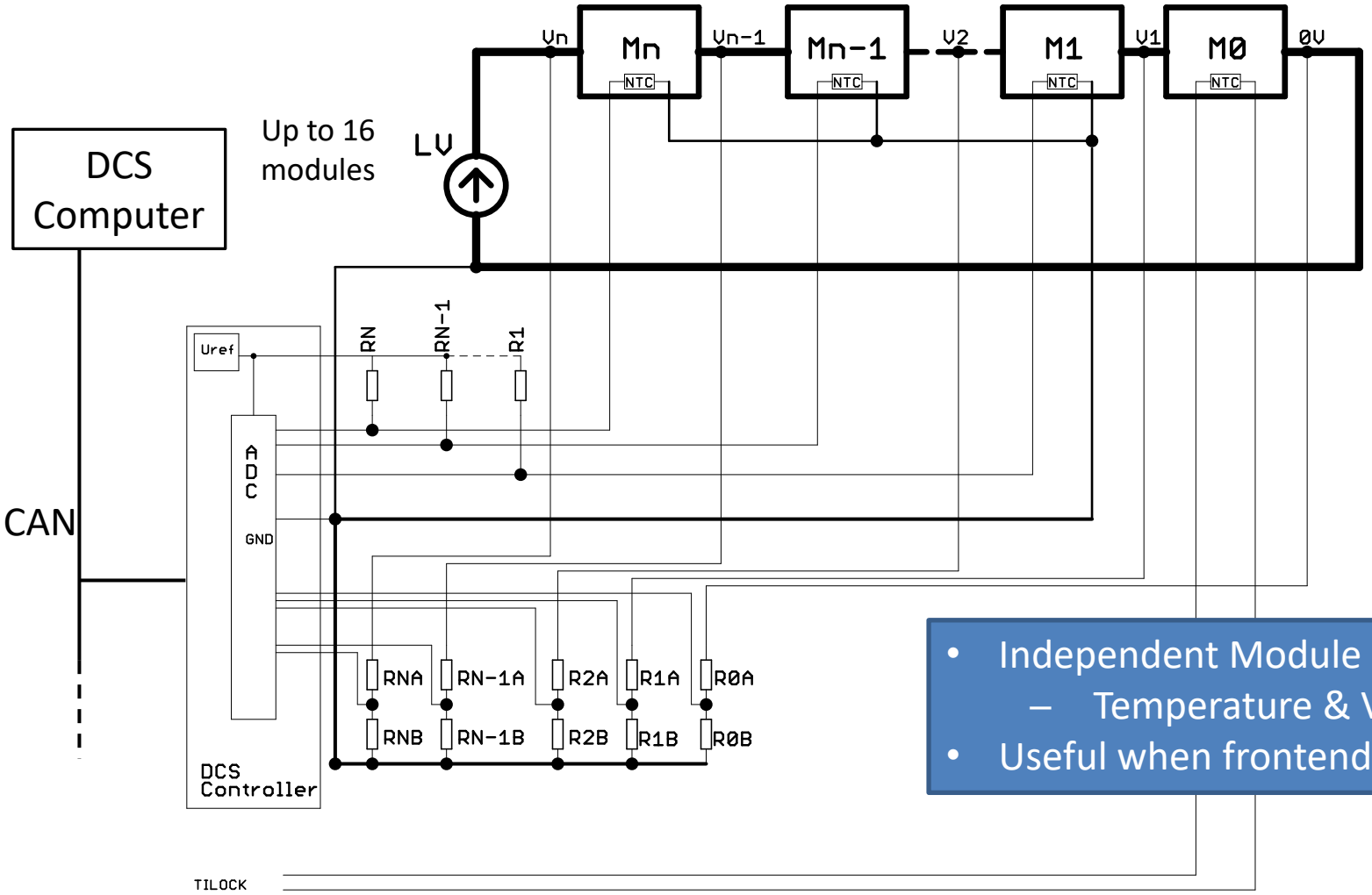
On-Pixel-Chip Monitoring

- Monitored SLDO properties
  - input/output voltage
  - shunt and total current
  - Vref and Vofs reference voltages



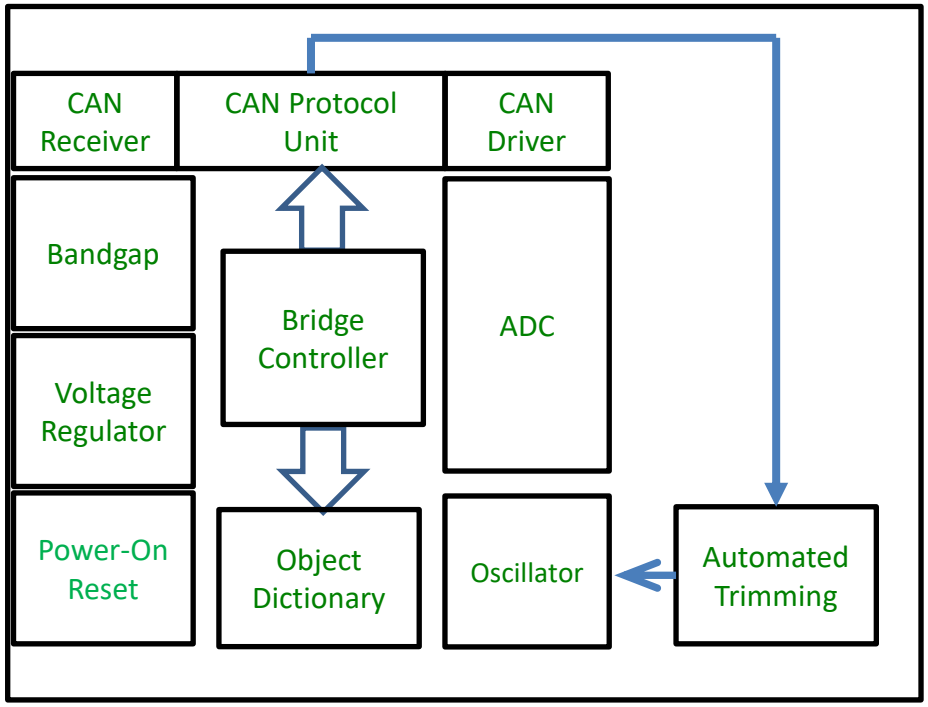


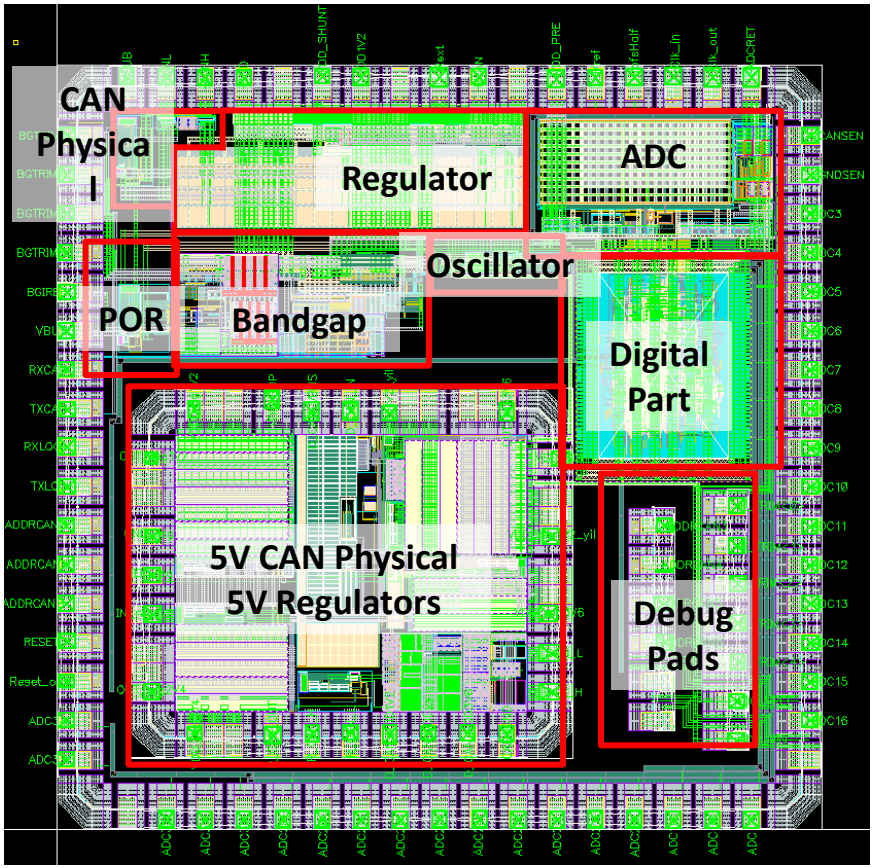
Monitoring of Pixel System



- Independent Module Monitoring
  - Temperature & Voltage
- Useful when frontends are offline

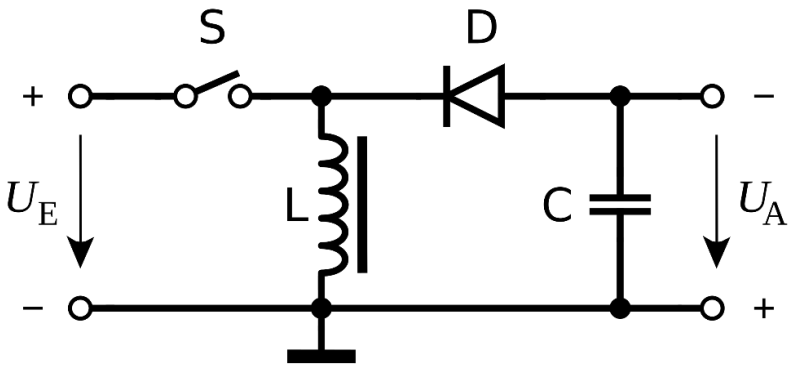
MOPS Chip

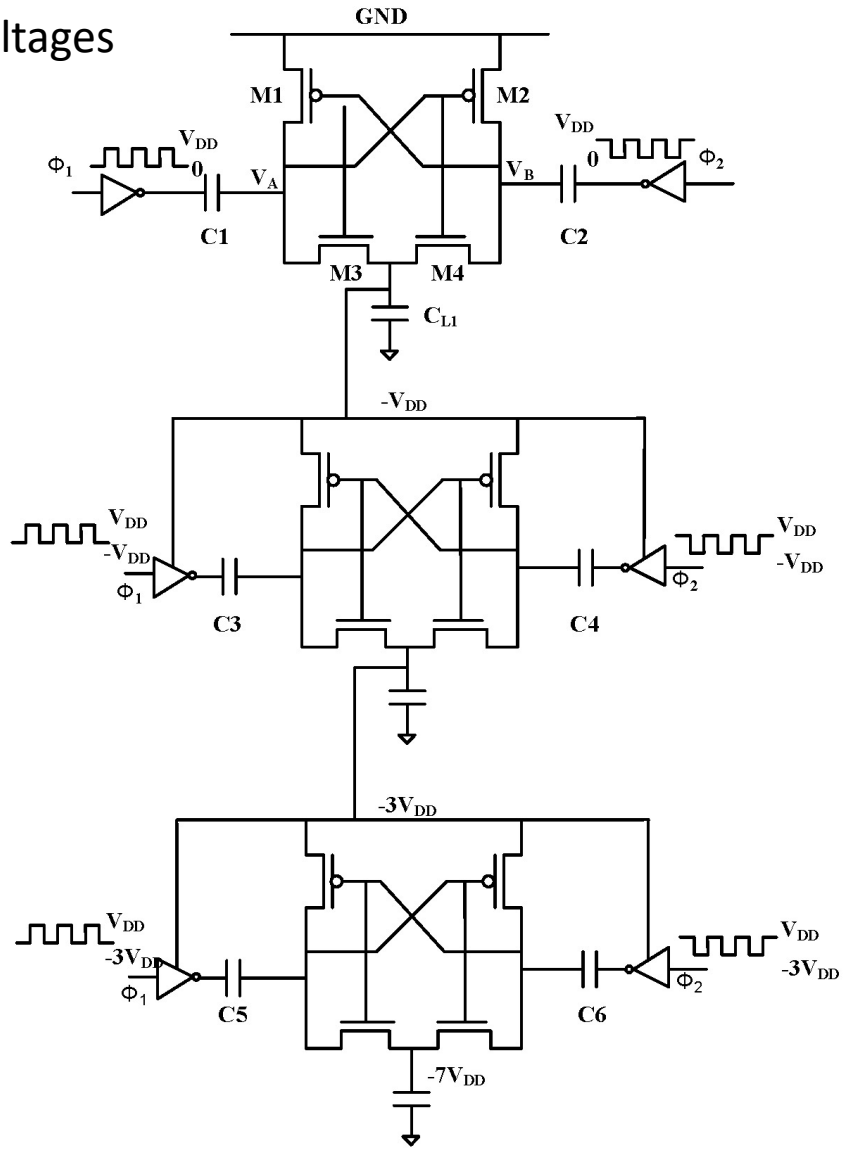

CAN Receiver
CAN Protocol Unit
CAN Driver
Bandgap
Bridge Controller
ADC
Voltage Regulator
Power-On Reset
Object Dictionary
Oscillator
Automated Trimming


CAN Physical
Regulator
ADC
Oscillator
POR
Bandgap
Digital Part
5V CAN Physical
5V Regulators
Debug Pads

Negative Bias Generator

- „preferred“ options for generation of negative voltages
  - inductive Buck-Boost converter
  - Cross-Coupeled Charge Pump
- Radiation-hard implementation
  - challenging but feasible

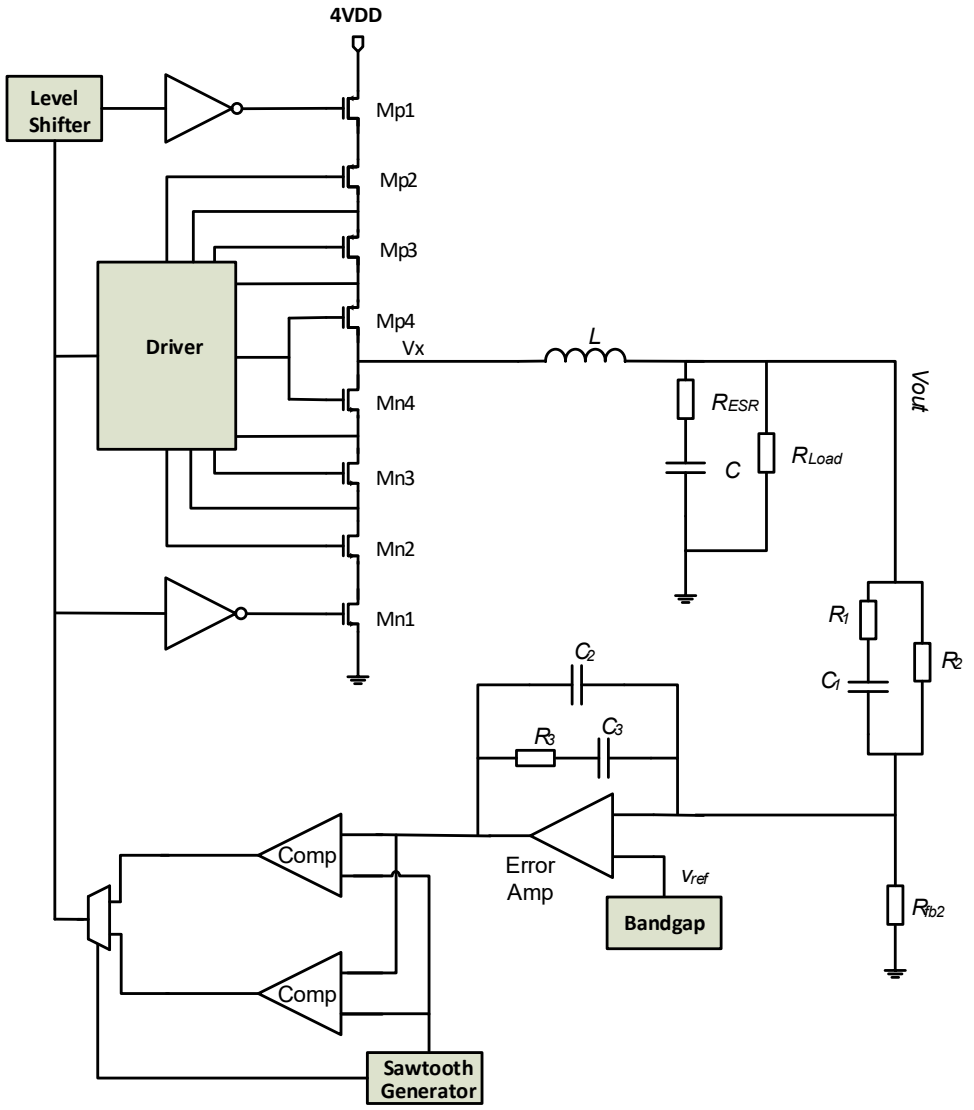




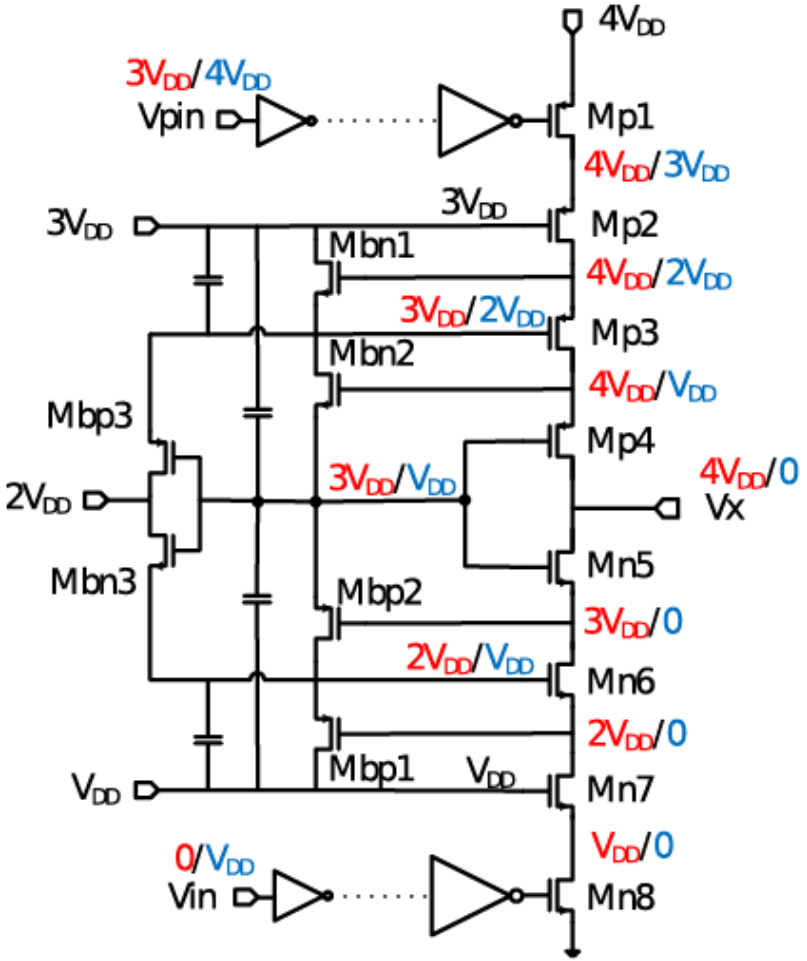
High-Frequency DCDC Buck Converter

- Cascoded switching stage
  - 4 NMOS (Mn1 - Mn4)
  - 4 PMOS (Mp1 - Mp4) Operation
- with quadruple nominal transistor voltage
- Voltage-controlled pulse width modulation (PWM)

Specification	
Input voltage	4.8V
Output voltage	1.2V
Swtiching frequency	100MHz
Max. load current	1A
Required inductance	**22nH**
Required capacutance	100nF
Efficiency @400mA	70%
Technology	TSMC 65nm (core Transistoren)
Nominal outout voltage	1.2V
Maximum voltage	1.32V

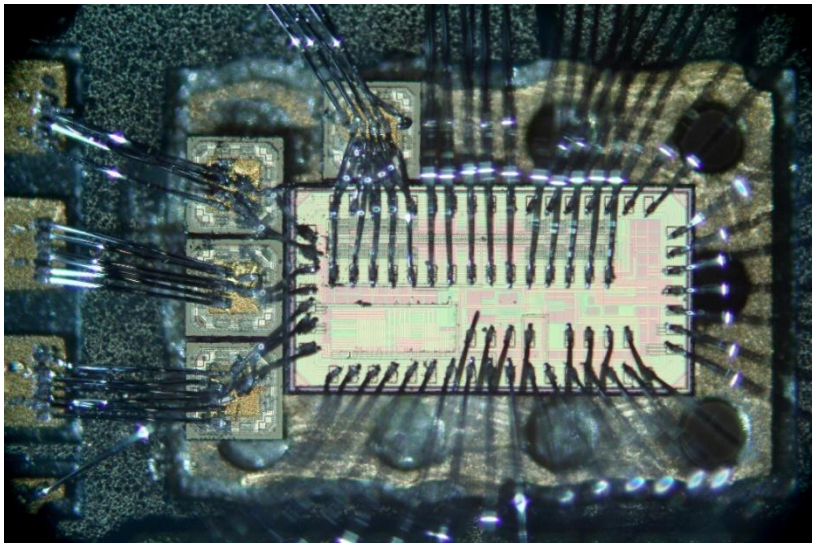


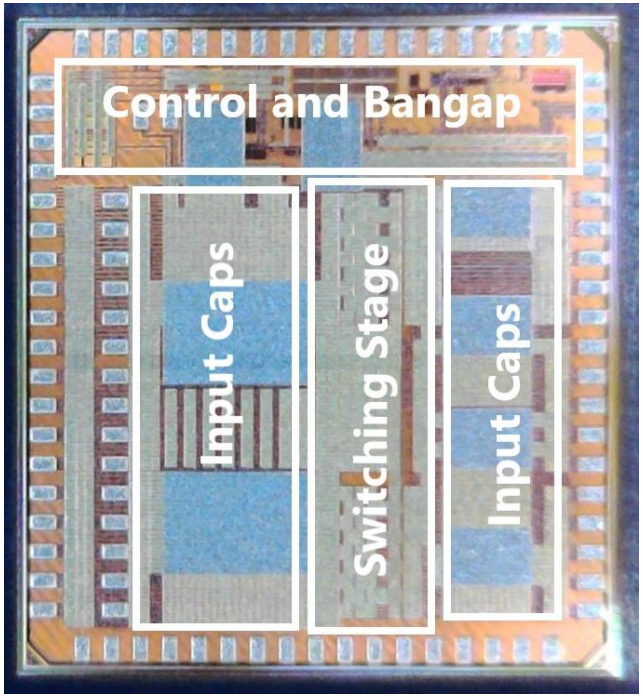
Cascoded Power Switch Stage



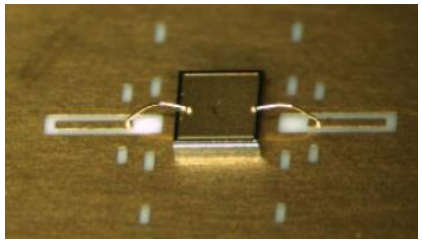
- 4 PMOS and 4 NMOS transistors each
- Core transistors (nominal voltage: 1.2V, max. voltage 1.32V)
- Circuit switches between HIGH state (red) and LOW state (blue)
- Control signals from Mp1 and Mn8 determine the state of the circuit
- Driver network ensures safe operation of the stacked transistors
- Network monitors the drain potentials of the stacked transistors and provides the required gate voltage
- Ensures that the transistors are within their voltage limits
- Auxiliary voltages VDD, 2VDD and 3VDD required

Decoupling Capacitors for High Freuqency Operation



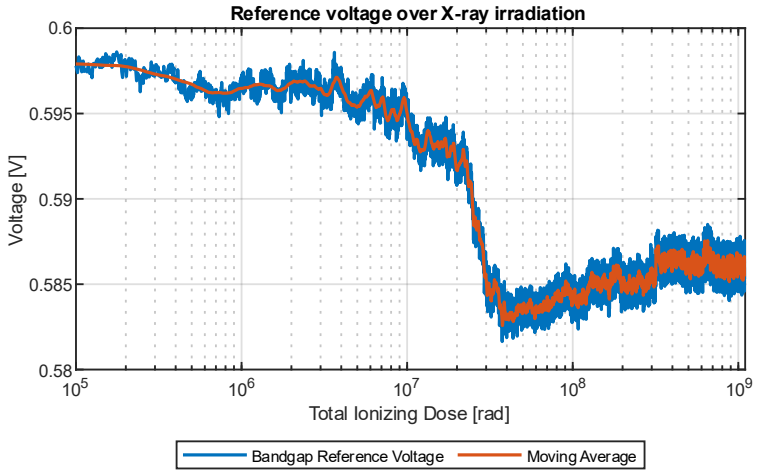


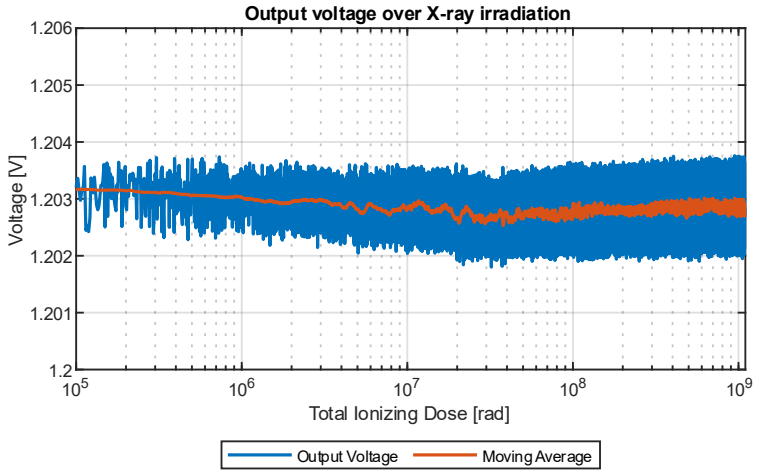
- **U**ltra large band **W**ire bondable **S**ilicon **C**apacitor UWSC
  - Murata
  - 10nF
  - 0202 (0.5 x 0.5mm)
  - Für Frequenzen bis 26GHz

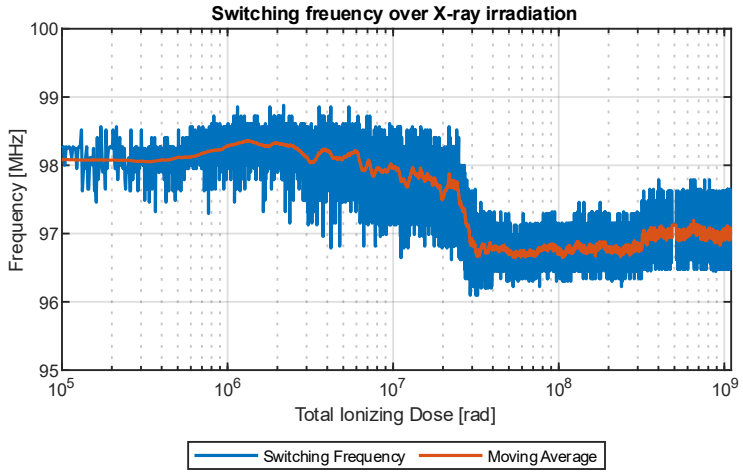


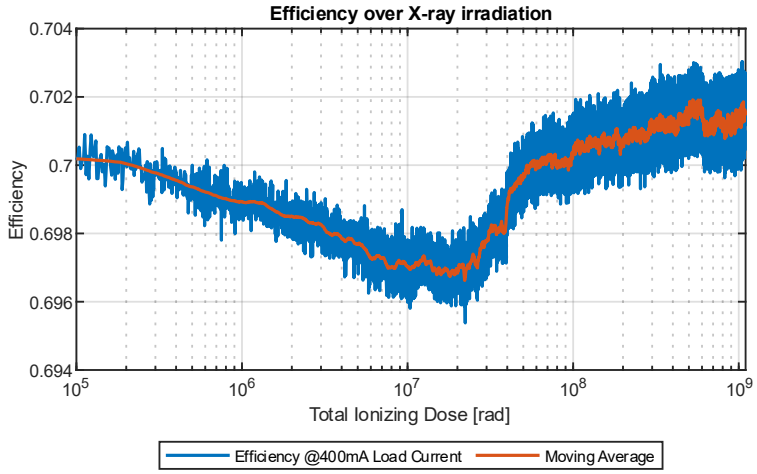
Testchip mit On-Chip capacitors (2.2 x 2 mm)

DC/DC Wandler | TID-Ergebnisse









Conclusion

- Power Aspects are always relevant and challenging
  - Especially due to additional constraints in HEP experiments
- Conventional parallel/voltage based powering scheme is not viable
  - Radiation hard custom made DC/DC converters are an option for outer layers
  - Serial Powering with SLDO are used in inner layers
- Hybrid/Resonant Converters may allow DC/DC conversion in hybrid-pixel detectors
  - e.g. as an alternative to short serial chains with 3D sensors

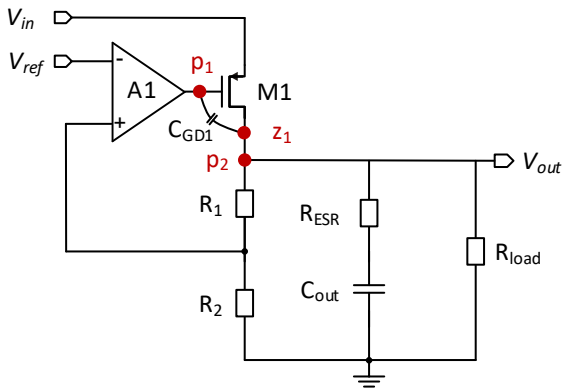
SPARE SLIDES

Serial Powering | Stabilisierung des LDO

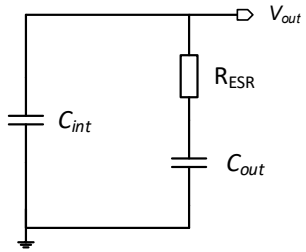
Pole und Nullstellen des LDOs:

- Verstärkerpol p1: $\omega_{p1} \approx \frac{1}{R_E[C_{GS1}+(1+g_{m1} \cdot r_{LG})C_{GD1}]}$
- Ausgangspol p2: $\omega_{p2} \approx \frac{1}{r_{LG} \cdot C_{out}}$
- RHP-Nullstelle z1: $\omega_{z1} = \frac{g_{m1}}{C_{GD1}}$
- Mit $r_{LG} = R_{load}||R_1 + R_2||r_{ds1}$
- R_E: Ausgangswiderstand des Verstärkers A1

- Für die Stabilität ist eine Phasenreserve > 60° im offenen Regelkreis erforderlich
  - Kompensationsnullstelle für Phasenanhebung
- Konventioneller Ansatz: Kompensation durch ESR-Nullstelle
  - Große On-Chip Kapazität (≈ 300nF) → ESR-Kompensation nicht möglich
  - Neues Kompensationsschema erforderlich



LDO mit Position der Pol/Nullstellen

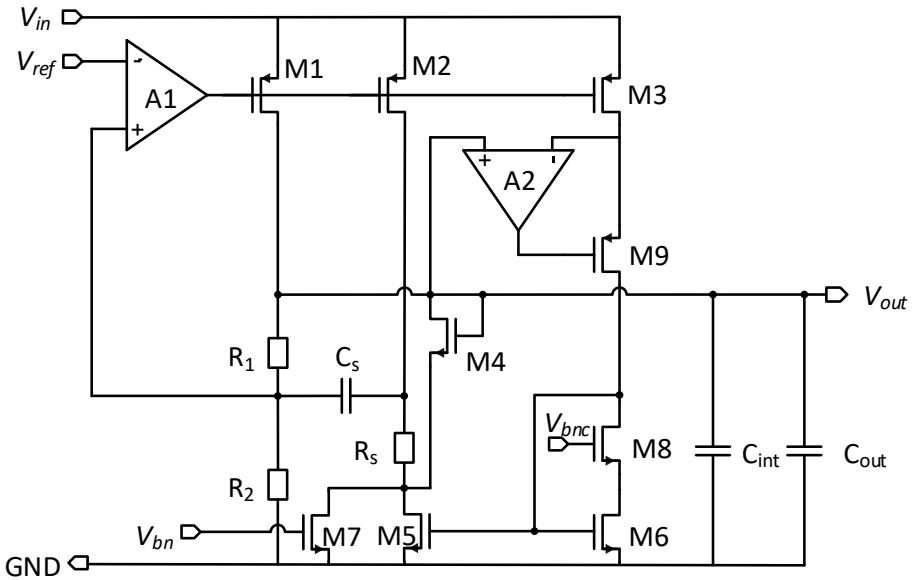


Kapazitive Last des LDO-Reglers

$$O(s) = \frac{1 + sR_{ESR}C_{out}}{s(C_{int} + C_{out})\left[1 + sR_{ESR}\frac{C_{int}C_{out}}{C_{int} + C_{out}}\right]}$$

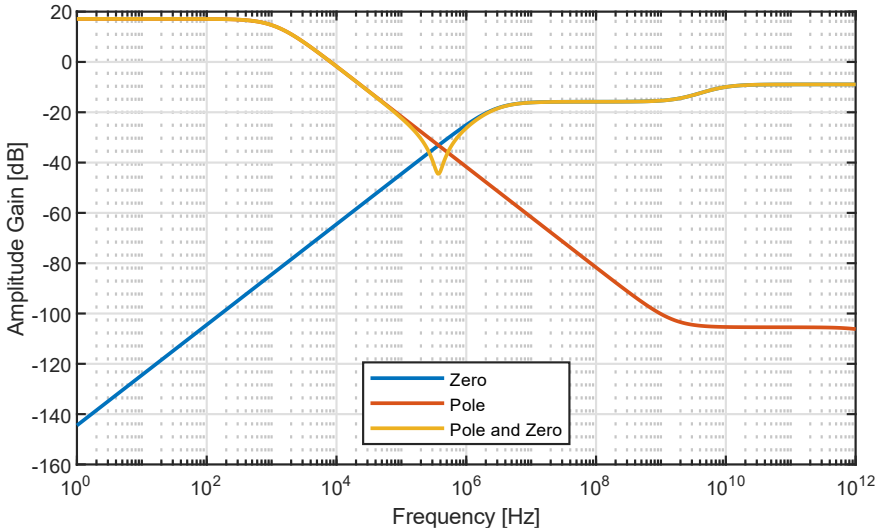
Serial Powering | LDO-Kompensation bei großer On-Chip Kapazität

- **Kompensationsnetzwerk:**
  - R_s/C_s erzeugen Nullstelle für Phasenanhebung
  - Stromspiegel: $M_1 \rightarrow M_2$
  - C_s koppelt Spannungsabfall an R_s über R_1/R_2 ein
- M_4 verbindet R_s mit Ausgangsspannung
  - Stellt sicher, dass M_2 in Sättigung bleibt
- Referenzpfad durch Stromspiegel M_3 stellt Stromfluss durch M_5 ein
- Verstärker A_2 stellt Stromspiegelgenauigkeit zwischen M_1 und M_3 sicher



SLDO Stabilization Strategy Bode Plots

$$\omega_{z,comp} = \frac{1}{\sqrt{2}C_{out}R_{LG}}\sqrt{-1+\sqrt{1+\frac{R_{LG}^4 g_{m1}^2 C_{out}^2}{g_{m2}^2 R_0^2 C_s^2 R_x^2}}}$$



Amplitudenantwort der Ausgangsstufe des LDOs (orange), Kompensationsschaltung (blau), beide Kombiniert (gelb)