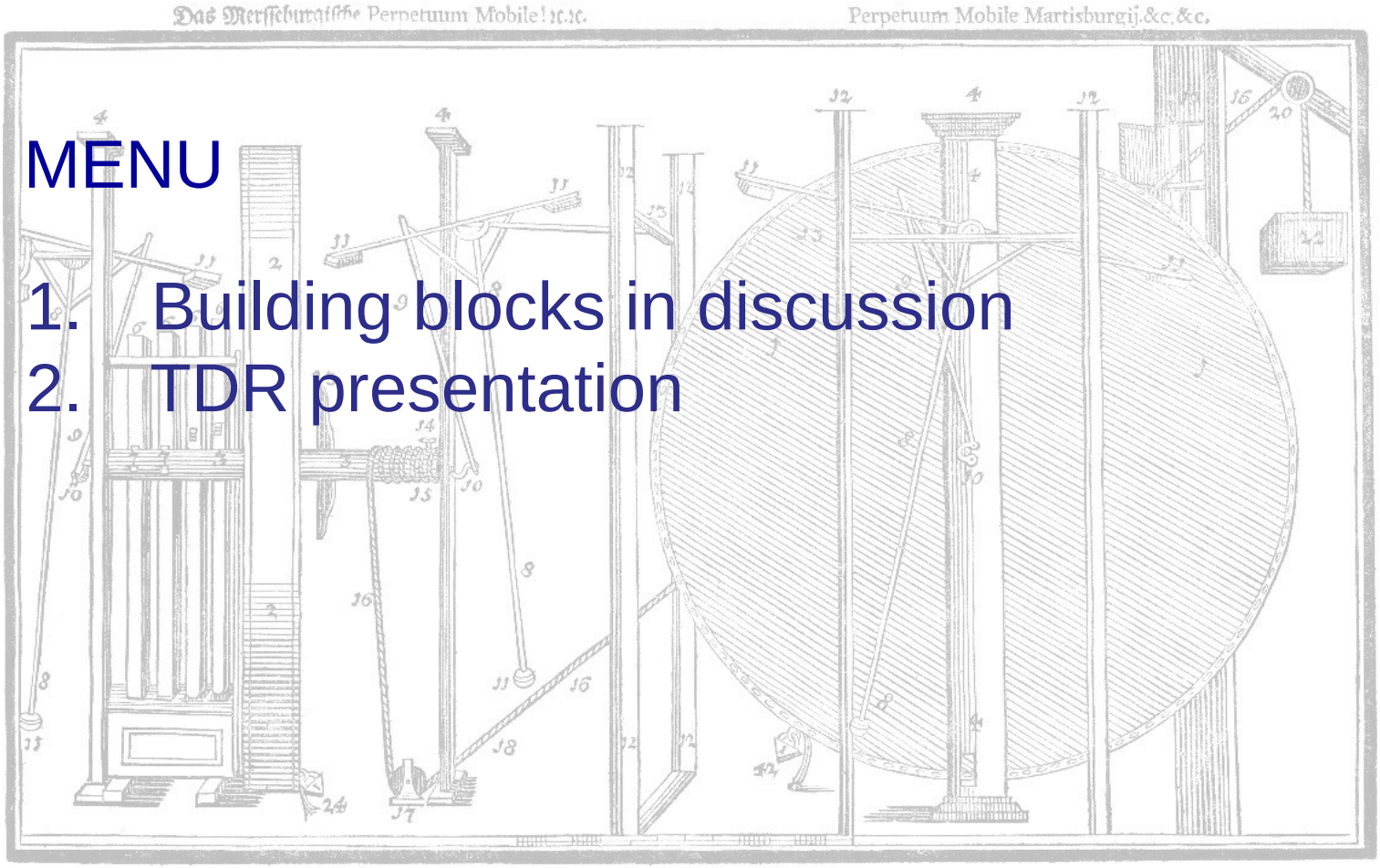
DAQ: WG issues & Status of TDR

H.Simon A. Charpy



MENU

1. Building blocks in discussion
2. TDR presentation

NUSTAR DAQ:
Providing building blocks and links …

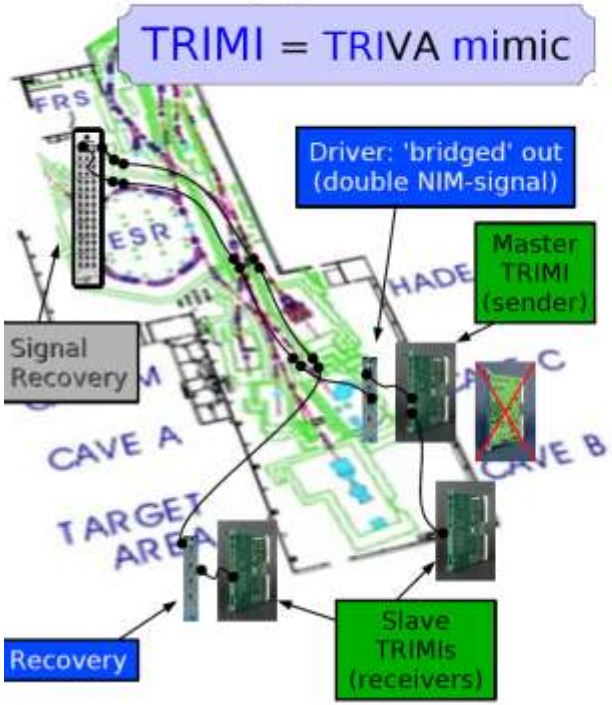
- Integration of ‚foreign' systems
  - GET, AGATA, …
- Flexible trigger scheme
- Time
  - event stamping and TOF
- Controls
  - run control, experiment control & accelerator
  - storage of parameters
- Data Flow

Flexible Coupling

- H.T. Johansson/CTH

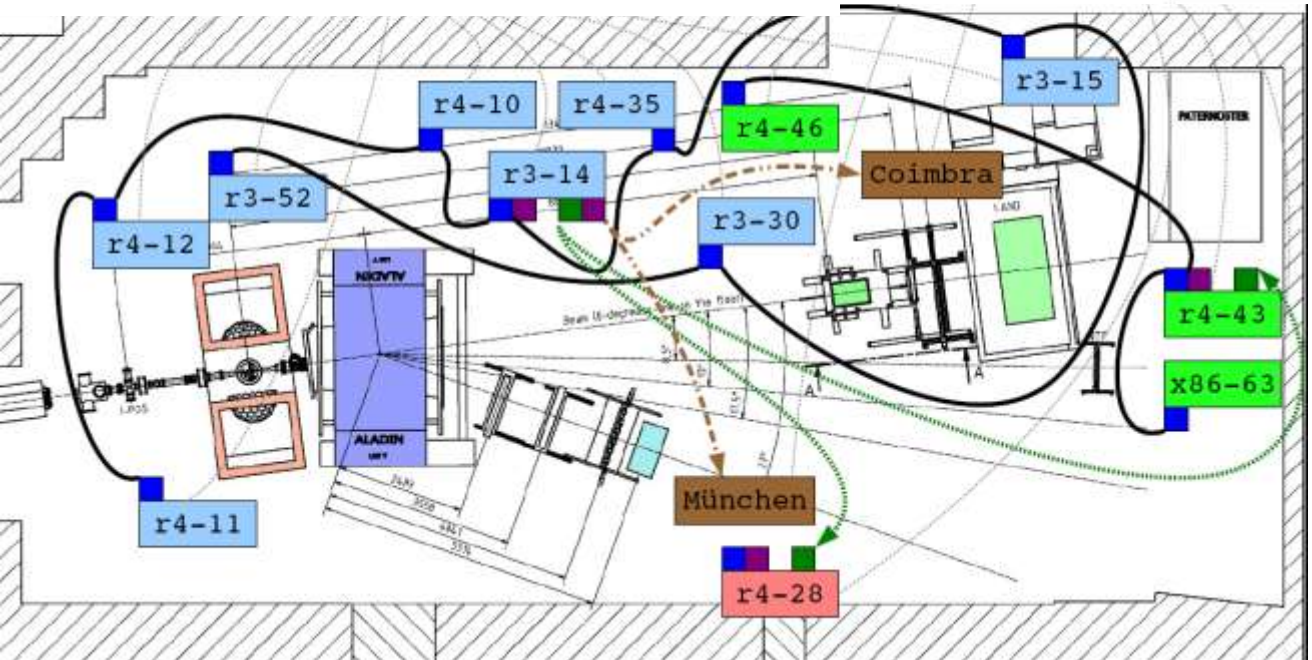
- Coupling with timestamps (TRB, indep. DAQs)
- Trigger/Timestamp distribution (several 100m)

Serial trigger Cave C - (FRS) - Cave C



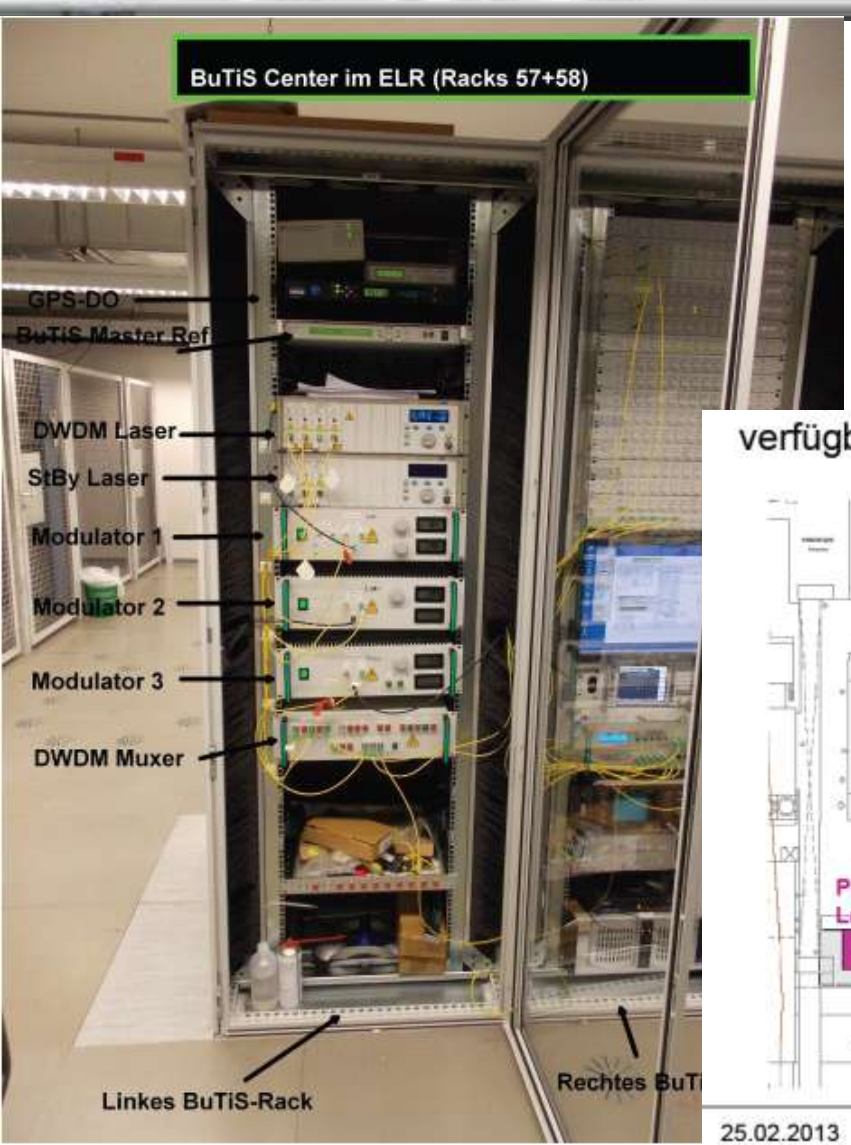
Easy deployment:

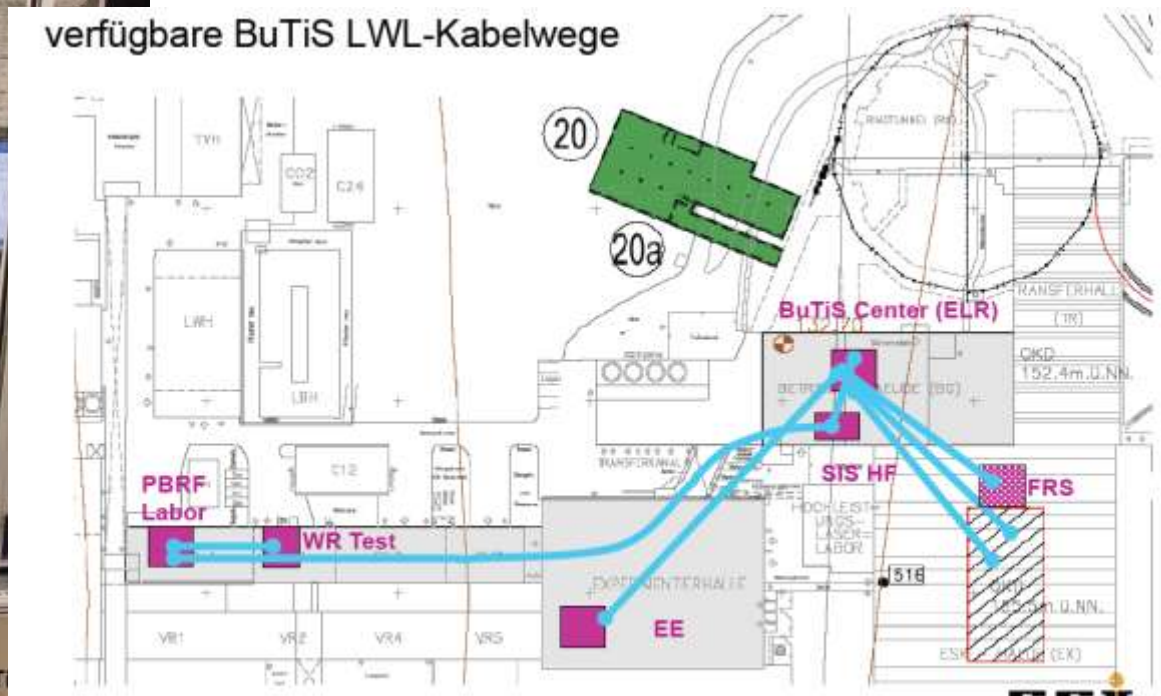
- Uni-directional protocol
- 1 cable of 'any' kind
- (DT return also needed) (2nd cable)
- No 'handshake' startup - easy setup:
  1. Start sender,
  2. Follow signal (scope),
  3. Receiver auto-sync ('any' frequency)
- Loss of ≤ 3 bits/msg → error-correction



Components & software are readily available

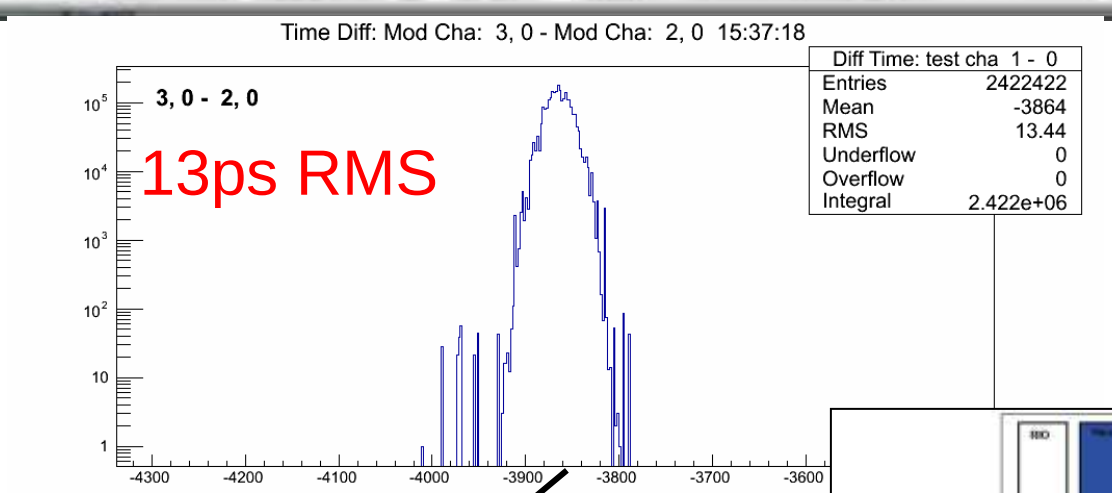
Time distribution:
(a) BuTiS

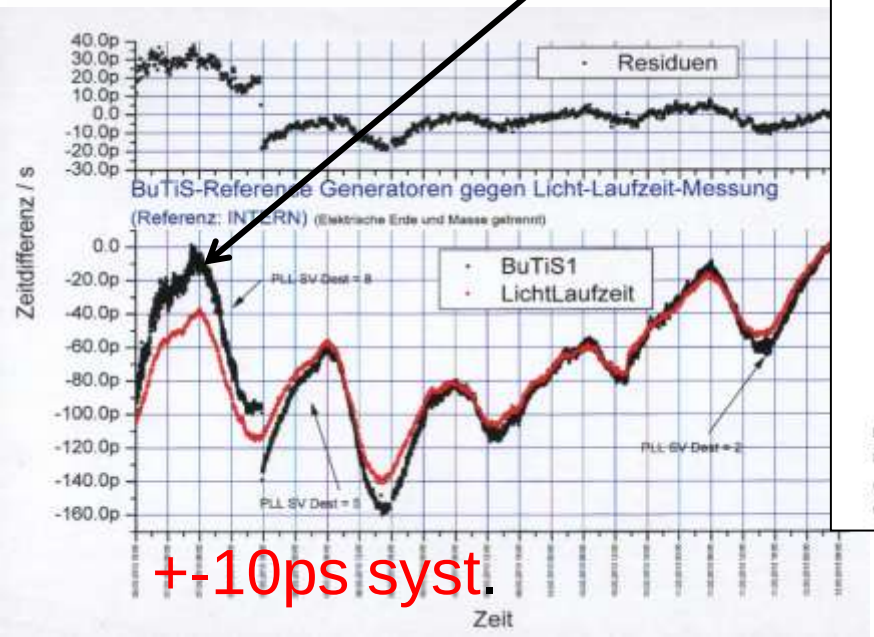




Performance: Accuracy and Precision …

J. Frühauf, K. Koch, N. Kurz, P. Moritz, B. Zipfel





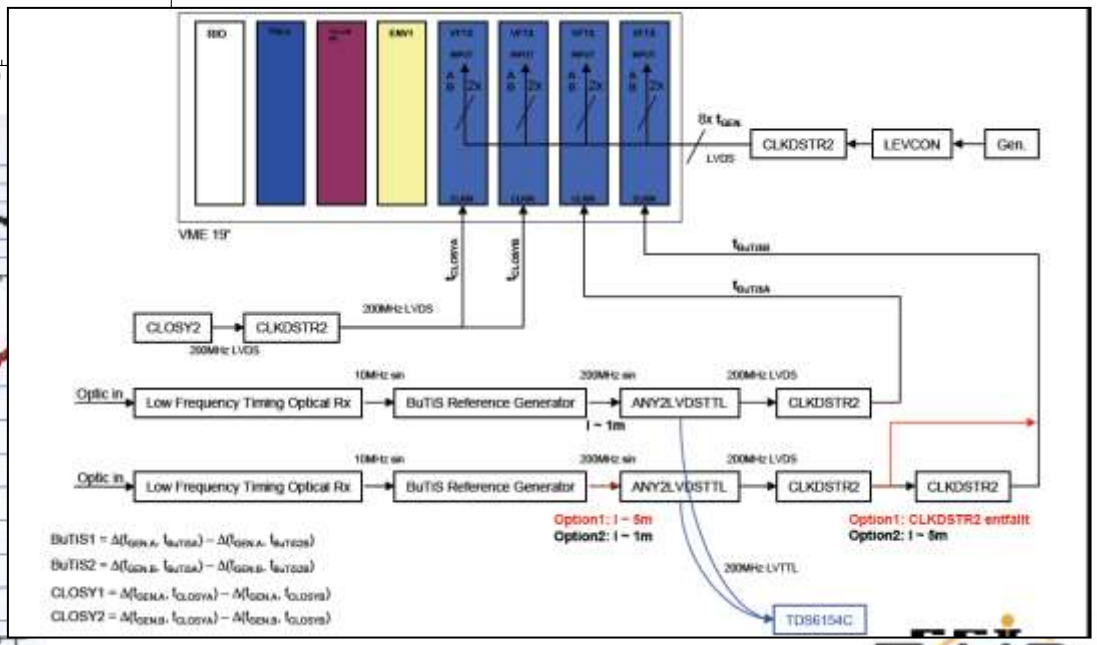
+-10ps syst.

Q1/2013

Optical distance ~2 km!

Path compensation

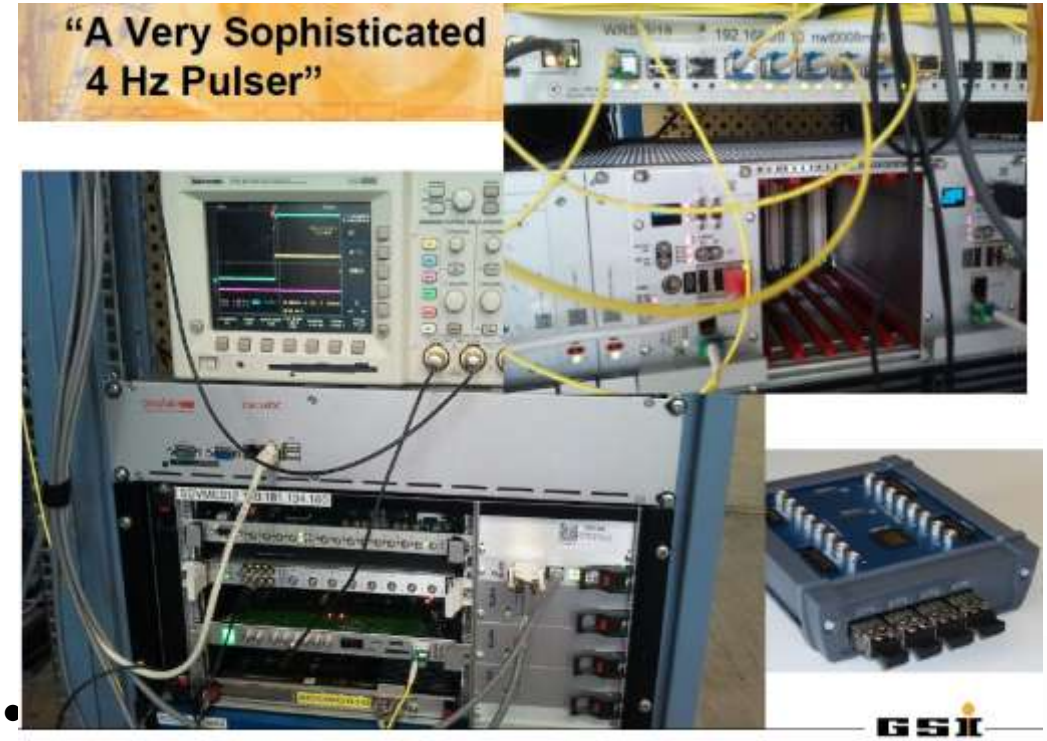
➔Better than 50ps design goal !



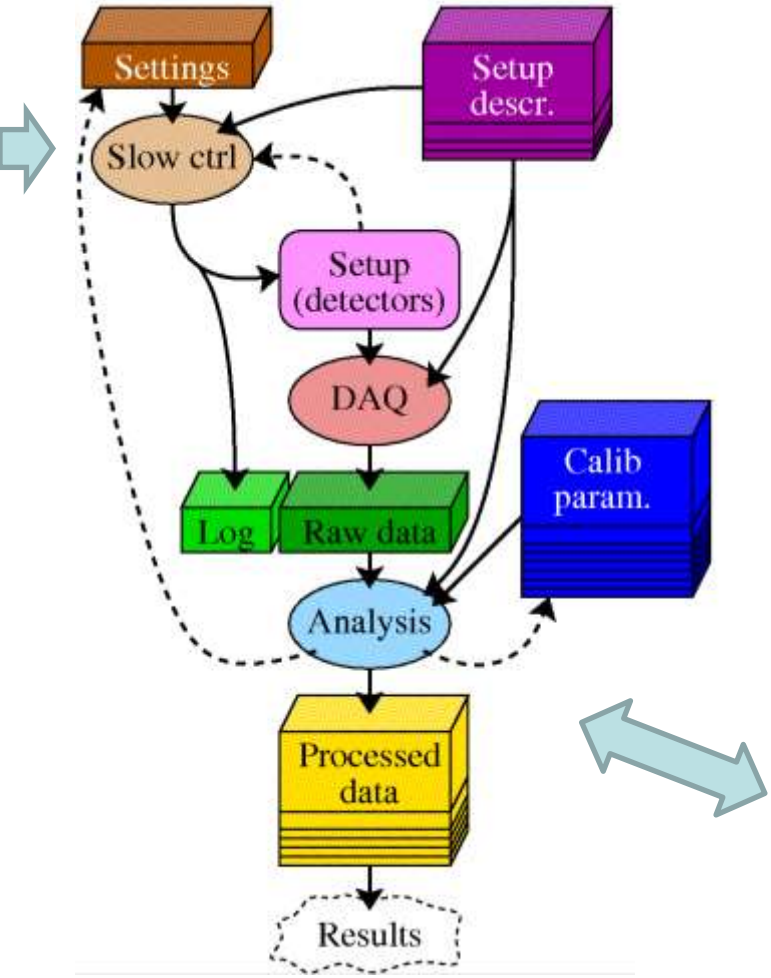
- NUSTAR Helsinki

(b) White Rabbit
- first implementations exist (D. Beck)

- Very good timing
- add. man power for latching (P. Schakel/KVI)



Open Issues (under discussion)



- Settings and Setup descr.:
  - -where and how to store them ?
- SCADA functionality
- Feedback Loops
  - -Interaction with controls

Common solutions (e.g. EPICS) again under discussion …

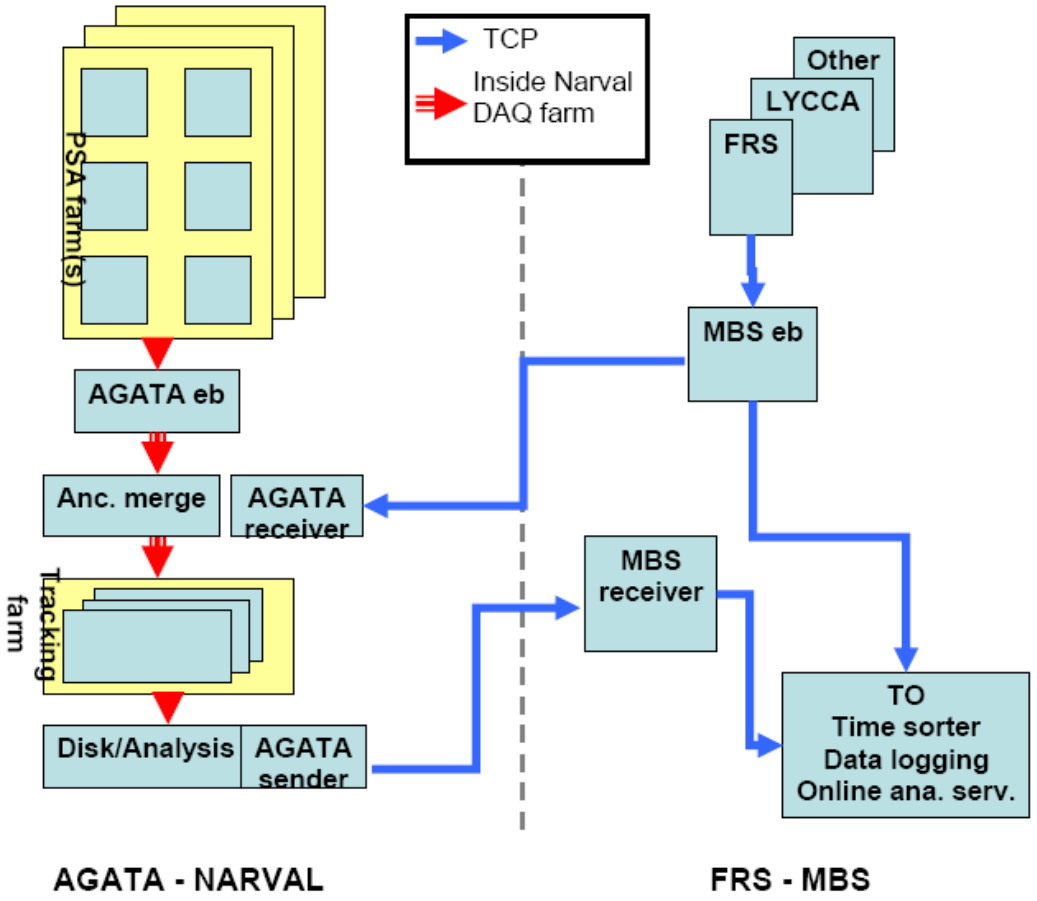
- -Interaction with accelerator controls
- -Middleware needed ?

So eventually we write it down !

➔ TDR ➔ Alexandre

AGATA coupling – data flow merging/coupling

N. Kurz, S. Pietri, H. Schaffner, X. Grawe



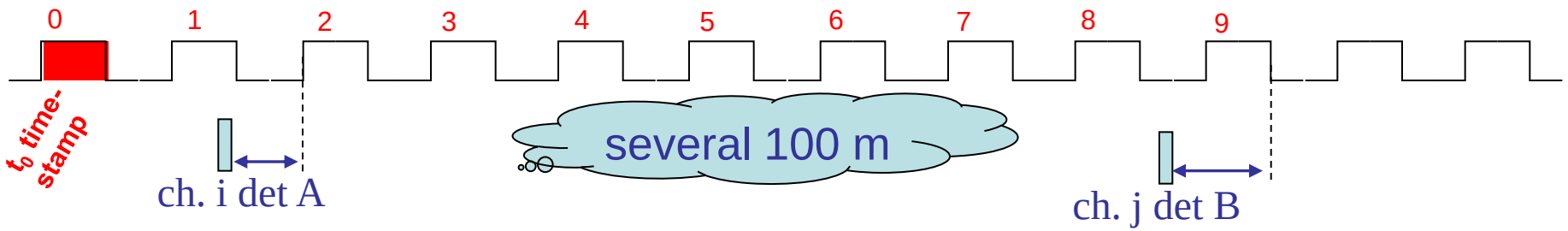
Two parallel data flows

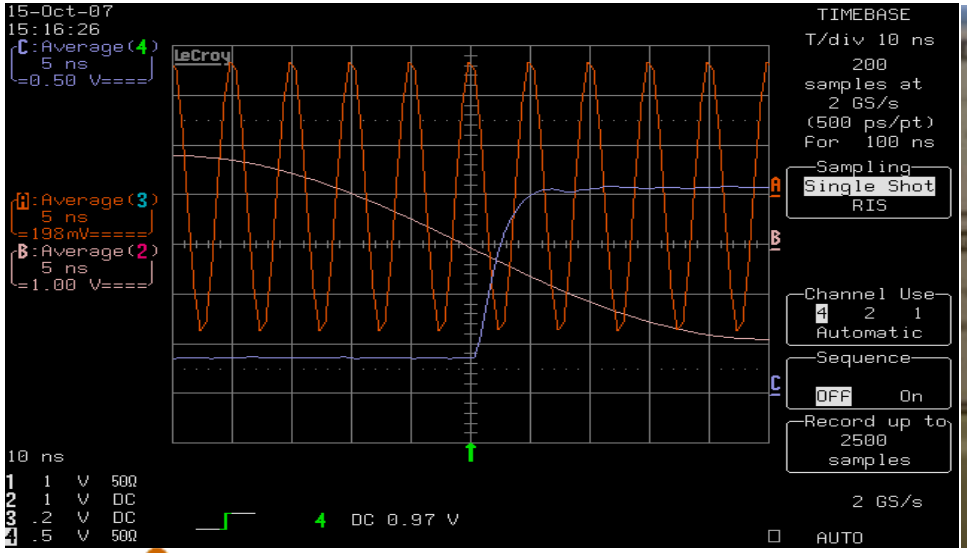
AGATA needs Tracking information for Doppler correction

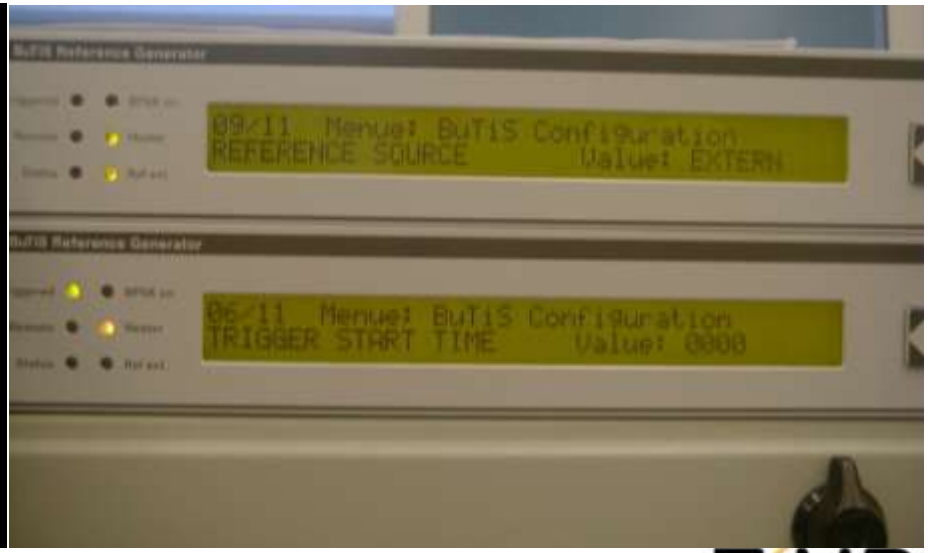
FRS needs Gamma data to optimize beam

Common time stamps

Precision timing (<50ps) vs. Campus Clock







BuTiS fibre distribution system

P. Moritz/B. Zipfel

BuTiS Master

↓ 0.01, 10, e.g. 200 MHz copper

LASER +
AM modulator

↓ opt. fibre (4 * 200GHz bands)

passive splitter
distribution 1..2 km

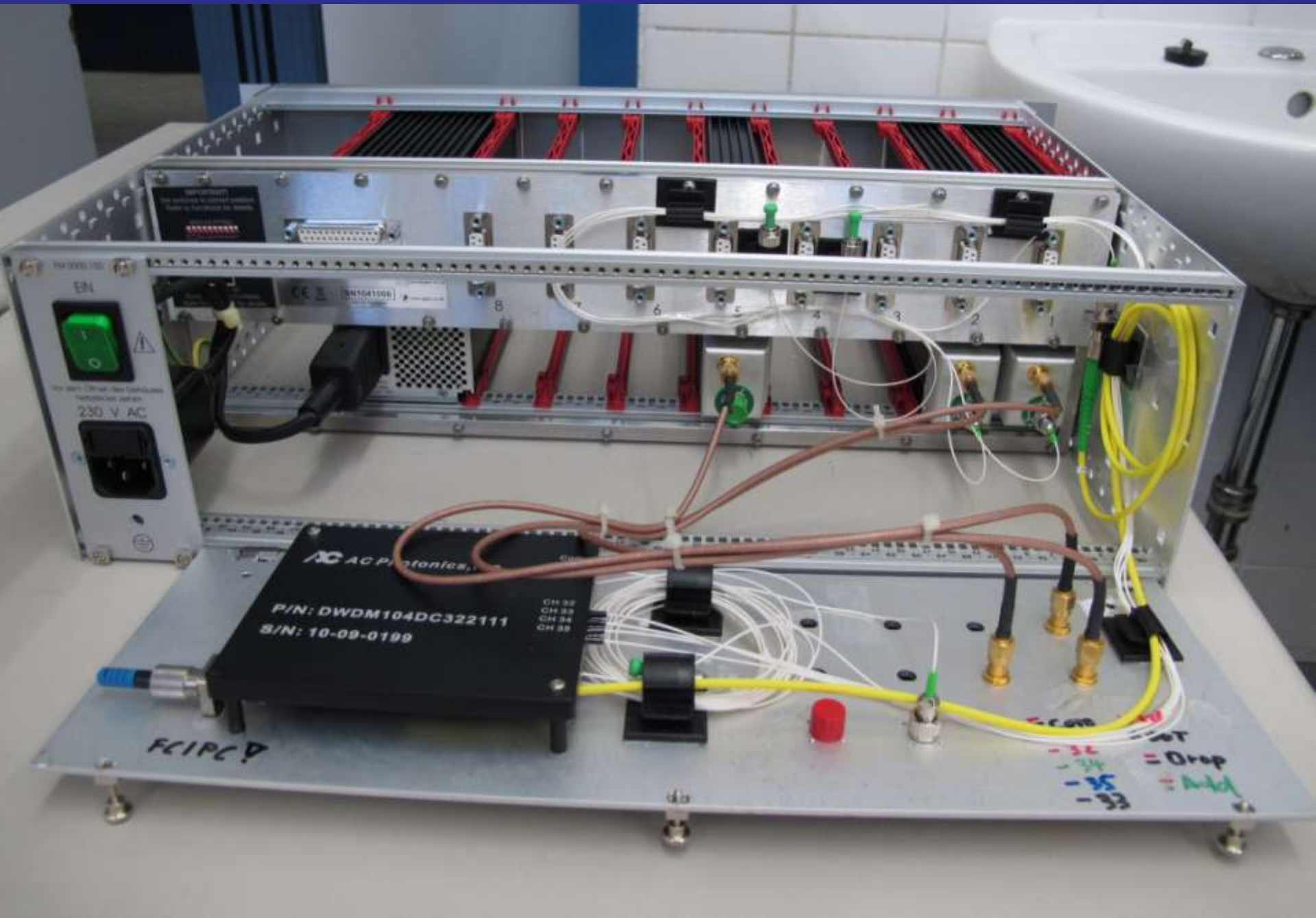
Demodulator + reflector (4th ch)

↓ 0.01, 10 MHz copper

BuTiS Slave osc.

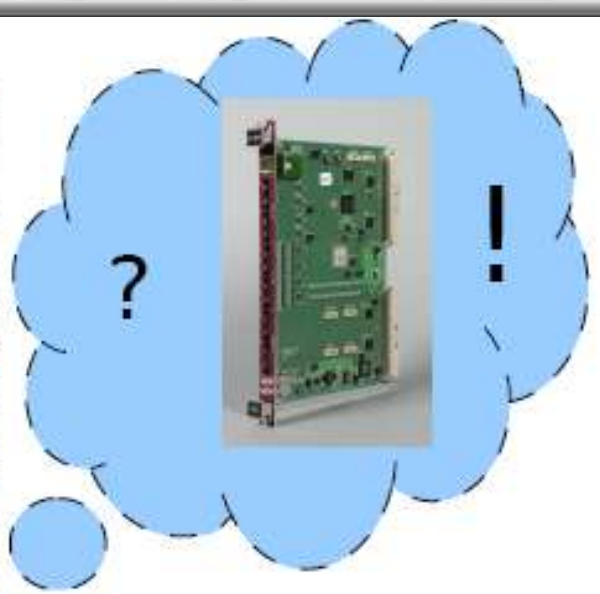
↘ 0.01, 10, e.g. 200 MHz copper ➔ **(local TDS) ?**

Optical Receiver Station Prototypes: 6/2011



Along the line: Flexible Trigger electronics

H.T. Johansson/CTH



VULOM
(VME universal logic module)

by J. Hoffmann, GSI

Original TRLO firmware
by J. Frühauf, GSI

VA-TA Si-Detector controlled by Logic Module

M.Holl /TU-Darmstadt P. Schakel / KVI

VA-TA ASIC

= Preamp

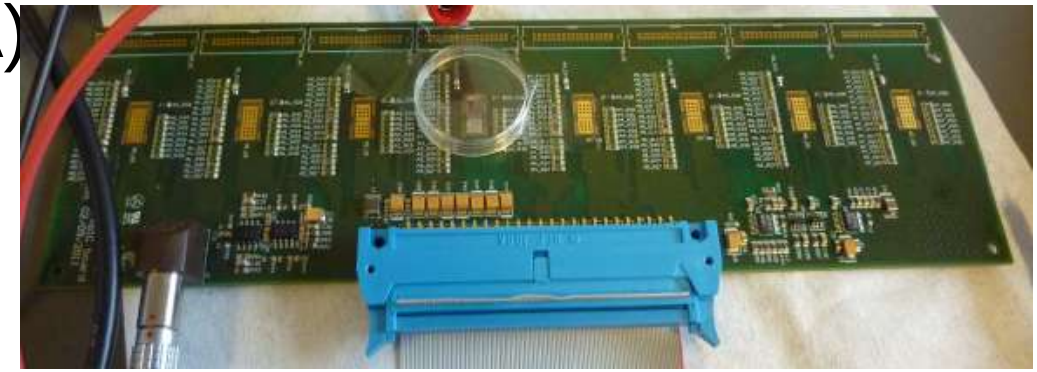
+ Trigger (TA)

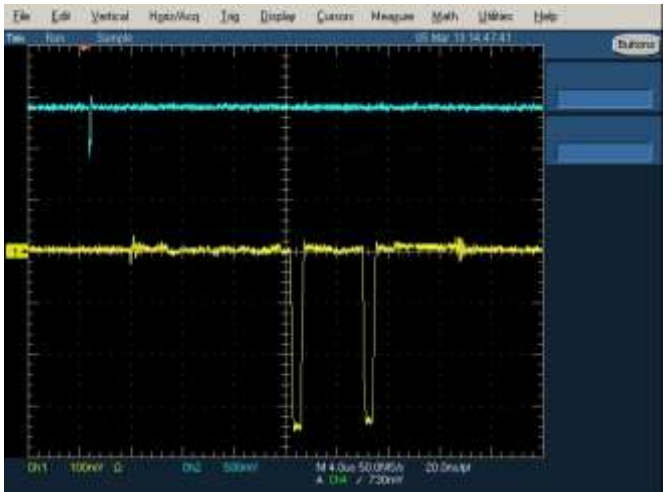
+ Sample & Hold (VA)

→ MUX out

Interface Board

VA/TA Board
(256 Channel)





Vulom (Sequencer)
+ SIS3302 (sampling ADC)
+ Firmware

Software ff.: New VME library

A. Charpy, B. Löher, H. Johansson (CTH&EMMI)

```
RIO4(r4-12)
{
   multi_event_mode = true;  // hmm, more global than this rio even?

   VME_CRATE(crate1)
   {


     CAEN_V775(tdc1)
     {
       address      = 0x00400000;
       virtual_slot = 1;
       setting_xy   = 100 ns;
       […]
     }

     CAEN_V785(adc1)
     {
       address      = 0x00410000;
       virtual_slot = 2;
     }
   }
}
```

DAQ mode

Module setup

Parsed Config file
→ no compilation !
sane defaults

Features:

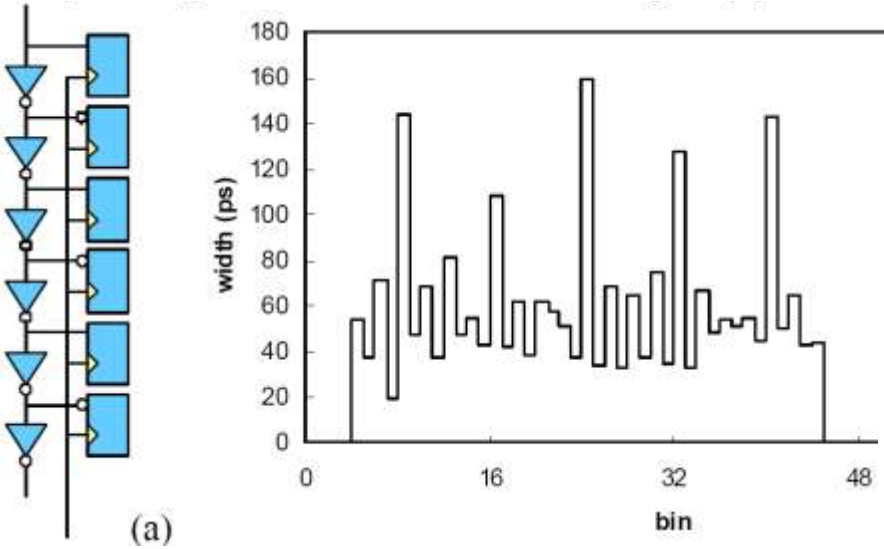
Config check &dump
Test programmes

Further steps: FPGA TDC; replacing TAC27 ASICS
➔ multihit/deadtime-free readout

The 10-ps Wave Union TDC:
Improving FPGA TDC Resolution beyond Its Cell Delay

Jinyuan Wu and Zonghan Shi

IEEE Nuclear Science Symposium Conference Record, 2008. NSS '08.



GSI implementation
E. Bayer, M. Traxler, N. Kurz

TABLE I
PARAMETERS OF SEVERAL TDC SCHEMES

Device: EP2C8T144C6, Price: $28 (April 2008),
Operating Frequency: 400MHz, Total Logic Elements: 8256

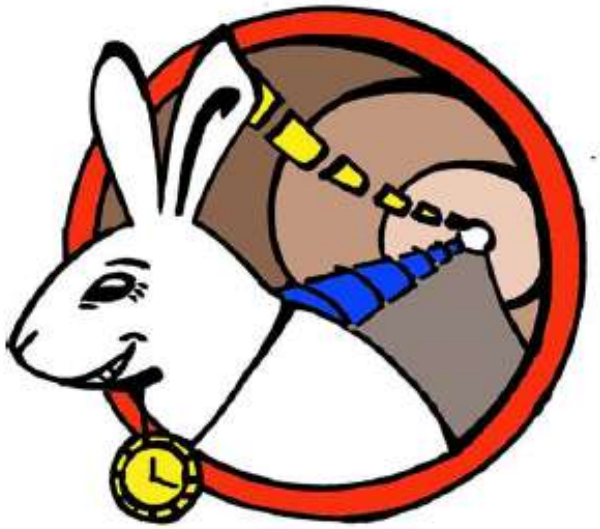
	Max bin width	Av bin width	ΔT RMS error	Dead Time	Delay Chain Length	Logic Element Usage
Un-calibrated TDC	165ps	60ps	58ps	2.5ns	64	1621 (20%)
Plain TDC	165ps	60ps	40ps	2.5ns		
Wave Union TDC A	65ps	30ps	25ps	5ns		
Wave Union TDC B			10ps	45ns		6851 (83%) 8 CH

Altera Cyclone II device (EP2C8T144C6)

First steps 09/2011 field test (J. Taieb/J. Belliure test exp.)

Event labels: White Rabbit

T. Włostowski/CERN



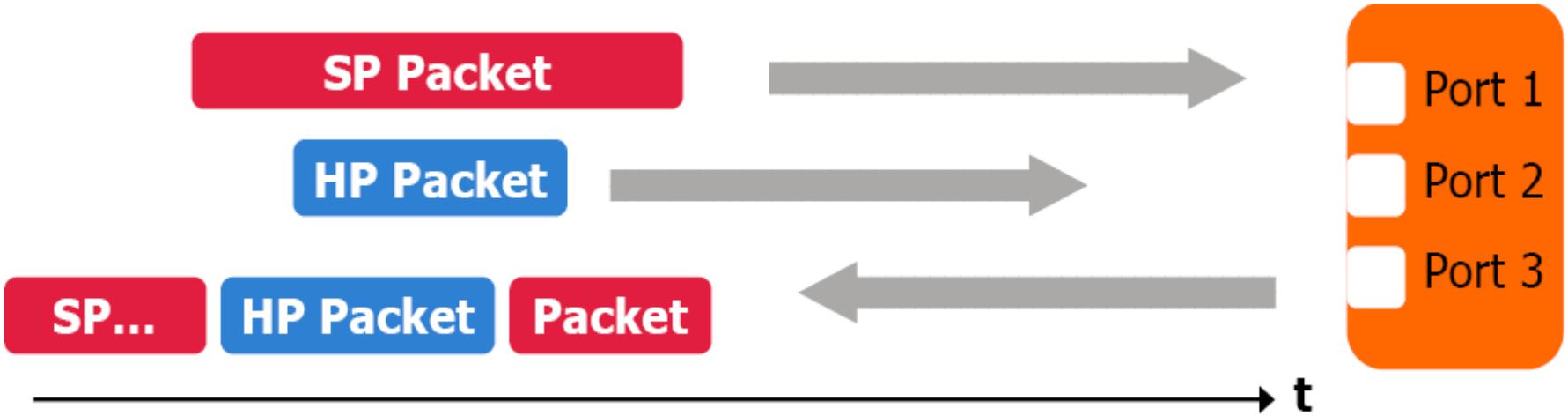
- Extension to Ethernet providing

1. A common clock via synchronous ethernet + compensation from PHY clock (PTPv2@125MHz IEEE1588 + compensation) 10MHz with ~1ns precision and ~100ps accuracy

2. A real time Protocol with guaranted latency

+ Fixed latency communication

- Functionality of the White Rabbit switch



SP packets are fragmented in the switch if they collide with HP packets

T. Fleck