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panda

MVD Strip ASIC (PASTA)

*Status Update of the **PA**NDA **St**rip **A**SIC*

André Goerres

10 September 2013

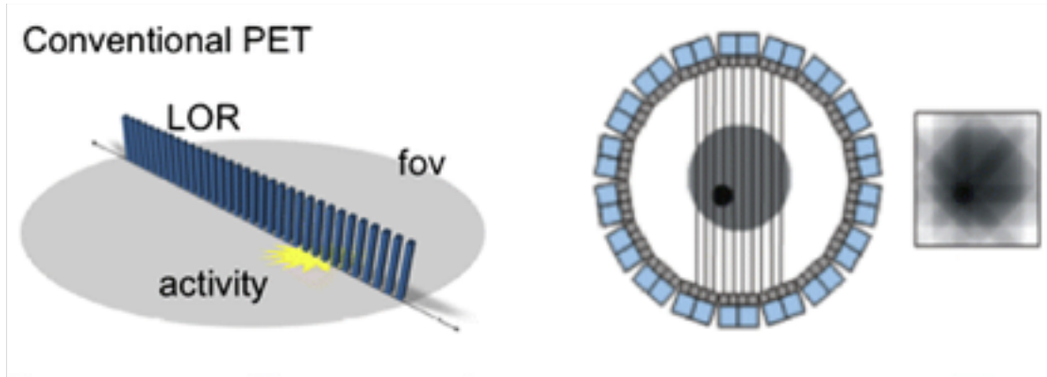
46. PANDA Meeting, Ruhr-University-Bochum

Content

- Introduction to TOFPET/PASTA
- Status of analogue part
  - Front-end and TDC
- Status of digital part
  - Meeting in Lisbon
  - Redesign of TDC Control

Motivation for using Time-of-Flight in PET

PET: **P**ositron **E**mission **T**omography



Normal PET operation

- Introduce positron-emitting radionuclide (β^+ decay) into patients body, detect annihilation gamma rays.
- Position of annihilation somewhere along the line of response (LOR).
- 2D information by superimposing different LORs.

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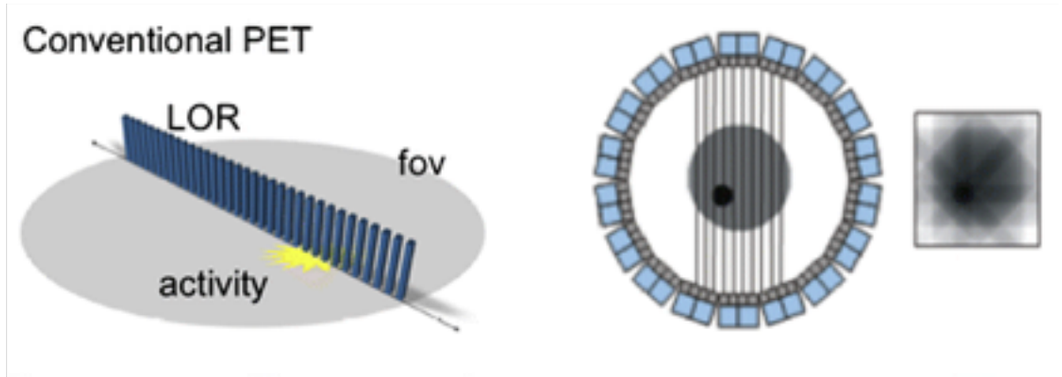

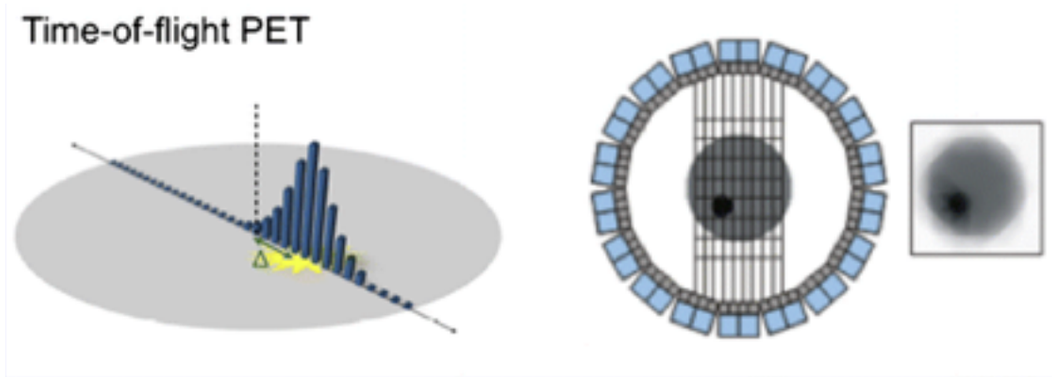

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PET using Time-of-Flight (TOF)

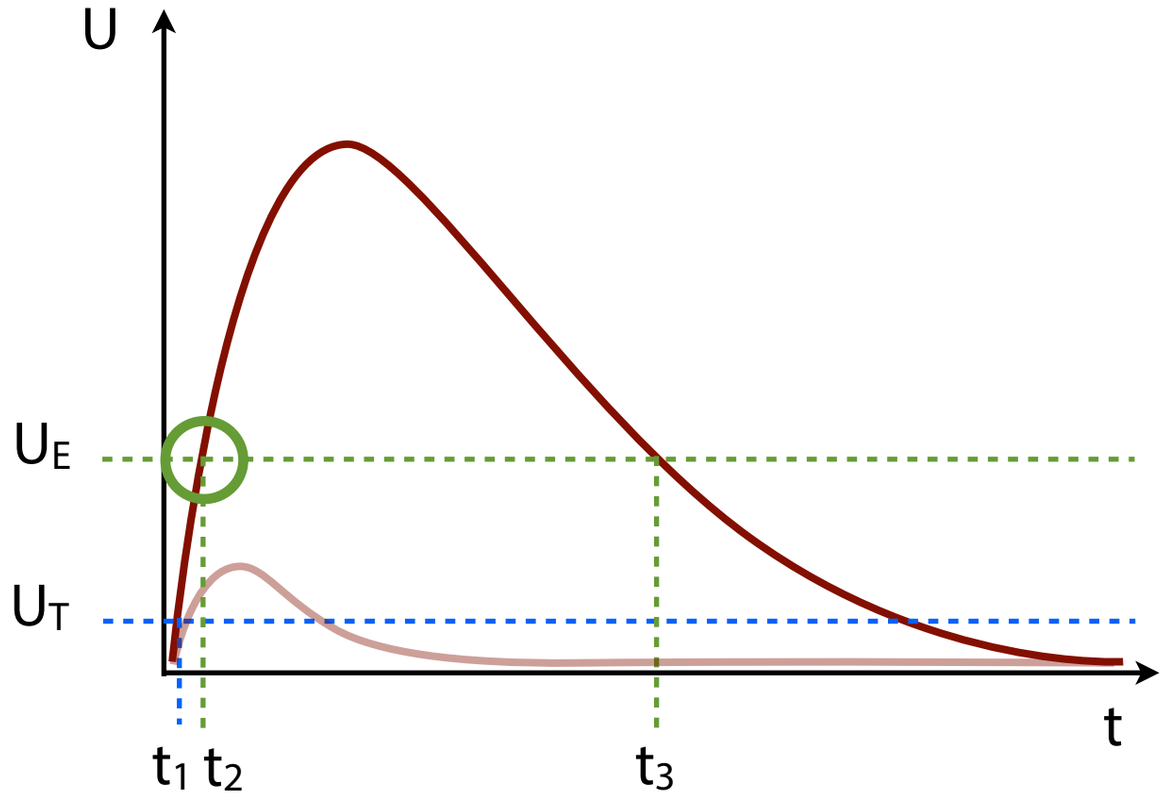
- Again, β^+ radionuclide in body.
- Measure time difference of arriving photons (accuracy ~200 ps ⇒ 3 cm).
- Additional position information alongside LOR.

⇒
- Higher SNR of reconstructed image
- Shorter exam time *and* reduced injected dose

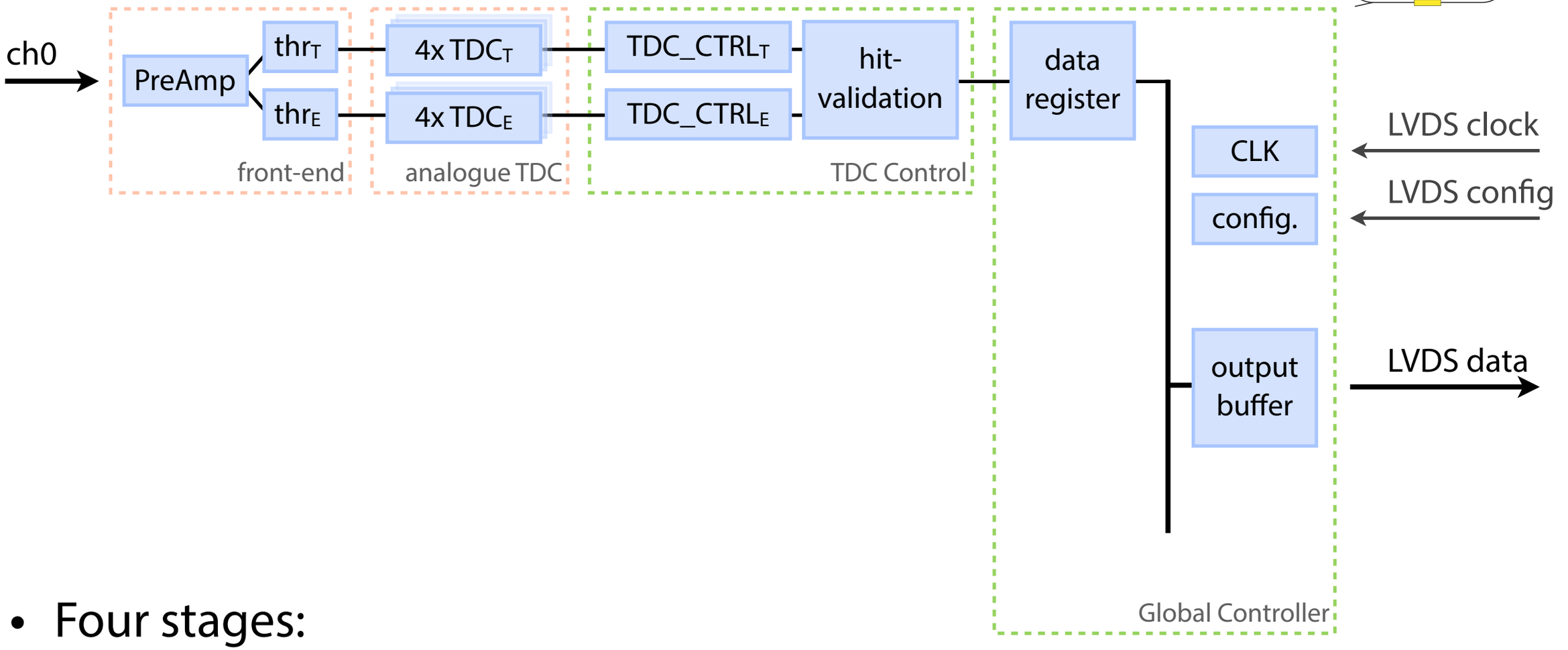
TOFPET ASIC developed by LIP Lisbon in the FP7/EndoTOFPET-US project

Concept of the ASIC

- Readout SiPM, achieve:
  - High time resolution and reduce dark count rate
- Two TDCs per channel
  - Time and energy branch
    (low and high threshold)
  - Energy trigger (t_2)
    validates time trigger (t_1)
- Charge by time-over-threshold (ToT)
  - ToT measurement: t_3 - t_1
  - Time binning: 50 ps (25 ps optional)

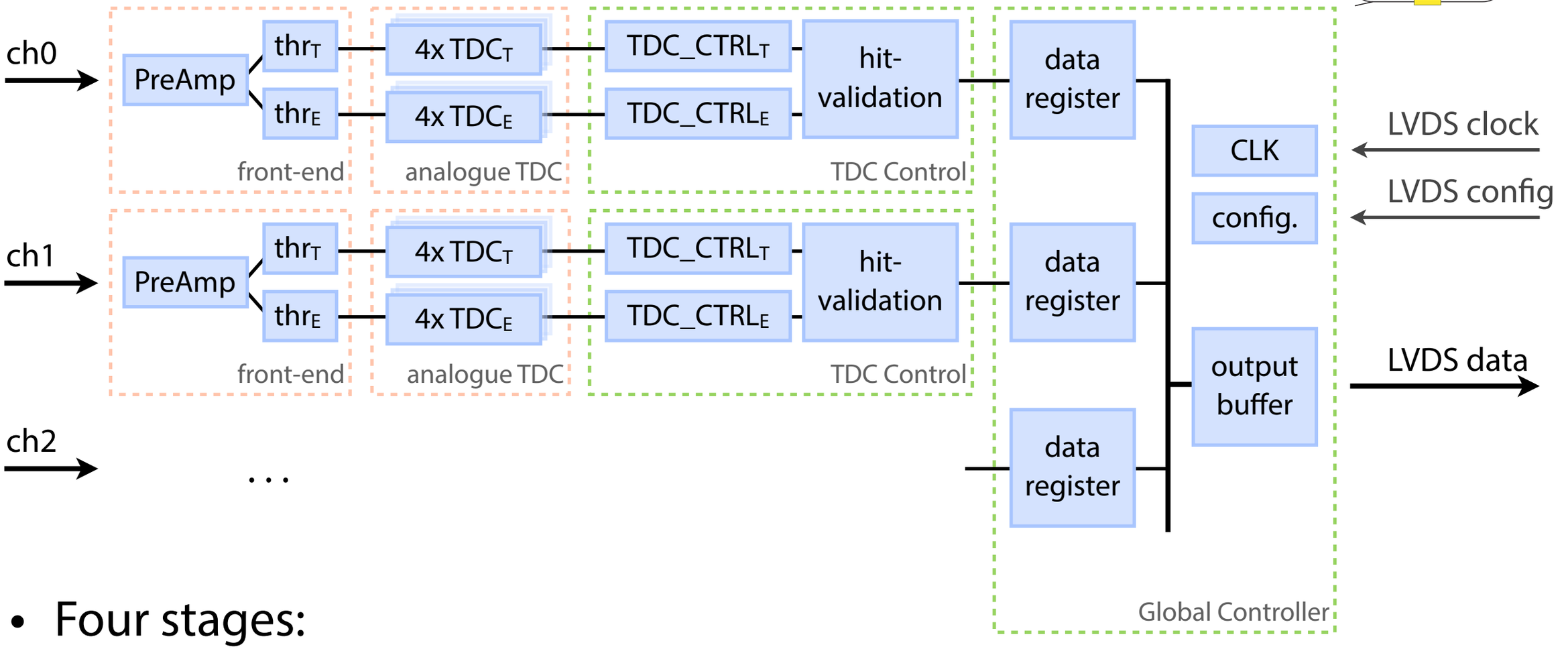


Concept of the ASIC



- Four stages:
  - **Front-end** (analogue)
  - **TDC** (analogue)
  - **TDC Control** (digital)
  - **Global Controller** (digital)

Concept of the ASIC



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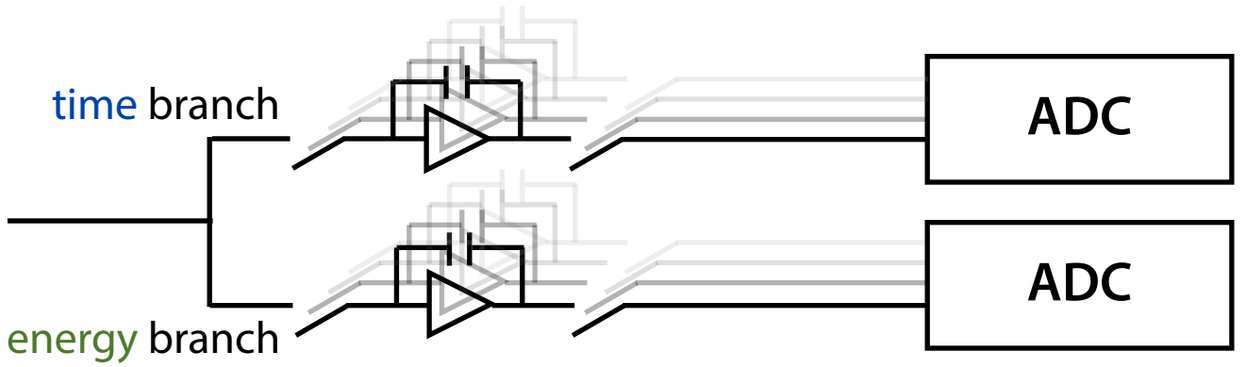
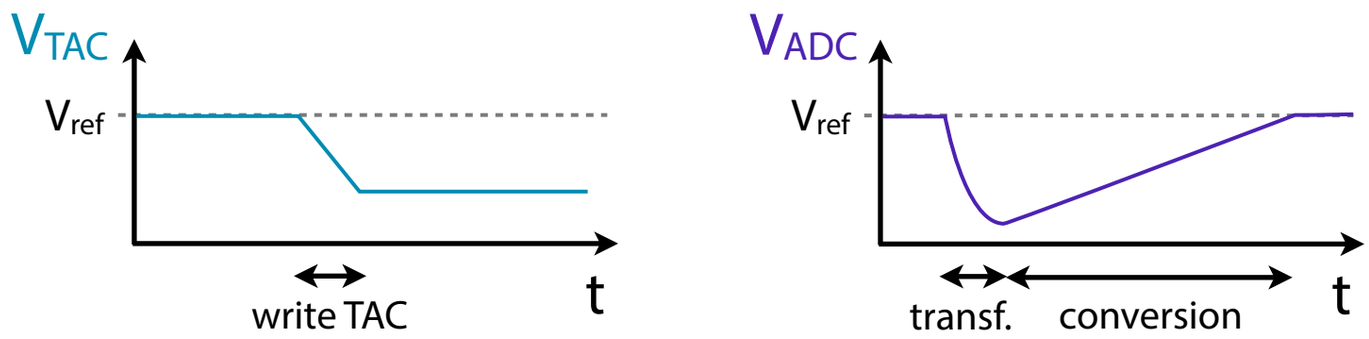
Analogue Time-to-Digital Converter





- Two stages: buffer and convert signal
  - Buffering: discharge a capacitor (TAC)
    - Start: threshold; End: rising edge of clock*
  - Transfer to 4x larger capacitor, linearly recharge with 32/64x smaller current (Wilkinson ADC)
- Increase time resolution by 128/256x (50/25 ps @ 160 MHz)
  - Conversion takes ~ 3 µs (@128x) → buffer multiplicity of 4

ADC: Analogue to Digital Converter
TAC: Time to Analogue Converter

*: Dynamic range 1-3 clock cycles

stage 1
front-end

stage 2
analogue TDC

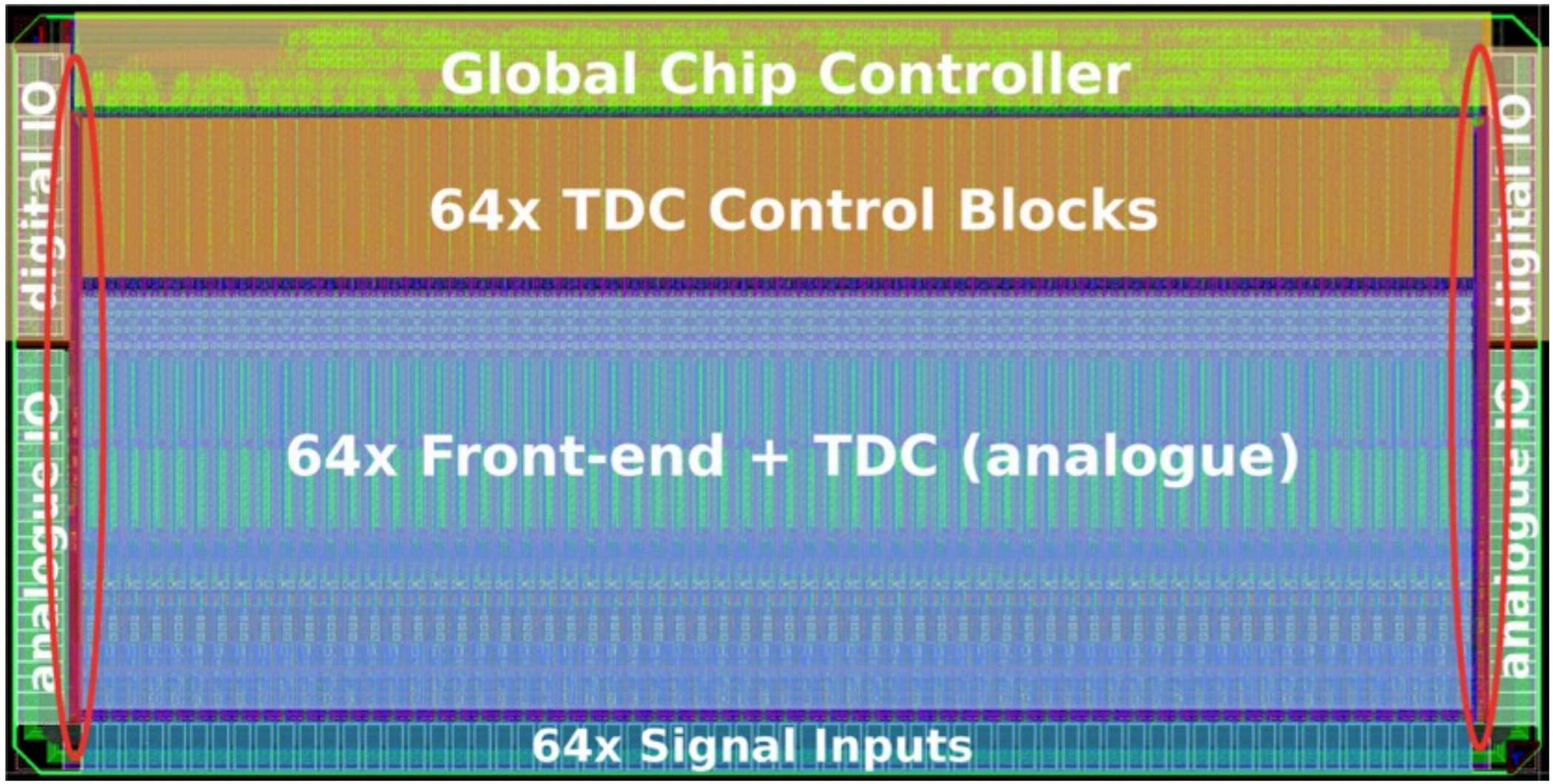
stage 3
TDC CTRL

stage 4
global CTRL

Floorplan of TOFPET ASIC v1

- CMOS 130 nm (IBM), 64 channels on 25 mm^2
- One pad-free edge to attribute two twin chips back-to-back

→ Discussion afterwards



Highlighted areas: bias and calibration circuitry

Readout of MVD Silicon Strips

- General parameters match the MVD requirements

	Area	Ch. pitch	Hit rate	Time bin.	CLK	Power
TOFPET	7.1 x 3.5 mm^2	102 µm	< 100 kHz	50 ps	80-160 MHz	7-8 mW/ch
MVD req.	< 8 x 8 mm^2	≈ 50 µm	< 40 kHz	< 20 ns	155.56 MHz	< 4 mW/ch

- Differences to solve:
  - Signal shape / capacitance ⇒ redesign analogue part
  - Channel pitch ⇒ tighter layout for channels? Positioning?
  - Power consumption ⇒
    - Bug in front-end stage
    - Slower clock (40 MHz?), clock gating
    - Redesign digital TDC control
    - Tune analogue part

➔ Discussion afterwards

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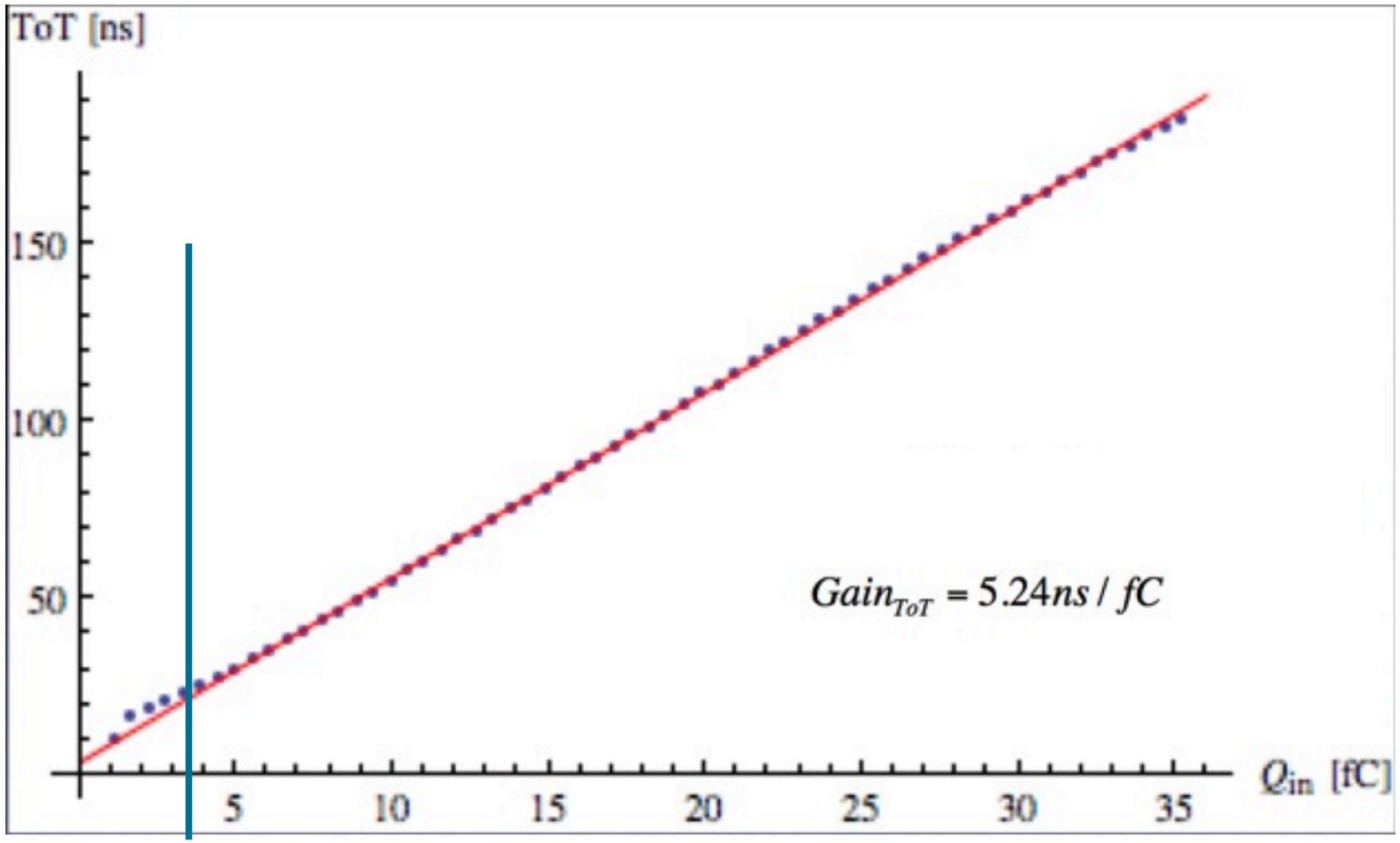
Analogue Part

Front-end: Complete Redesign

- Different signal shape lead to complete redesign of analogue front-end
  - Introducing a second amplifying stage (less cross talk)
- Linearity of input charges:

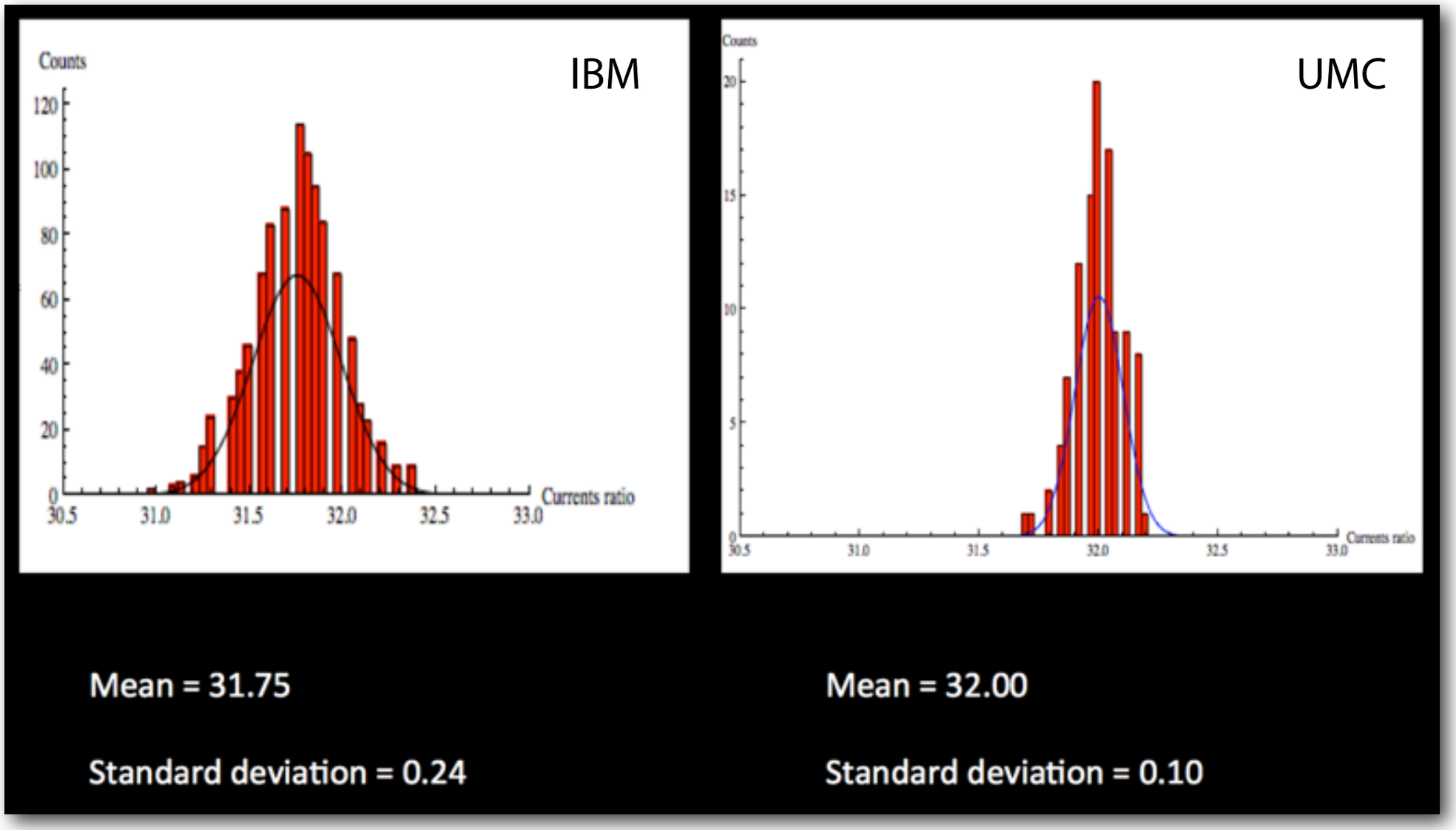


MIP signal

simulations by Valentino Di Pietro

Analogue TDC to UMC

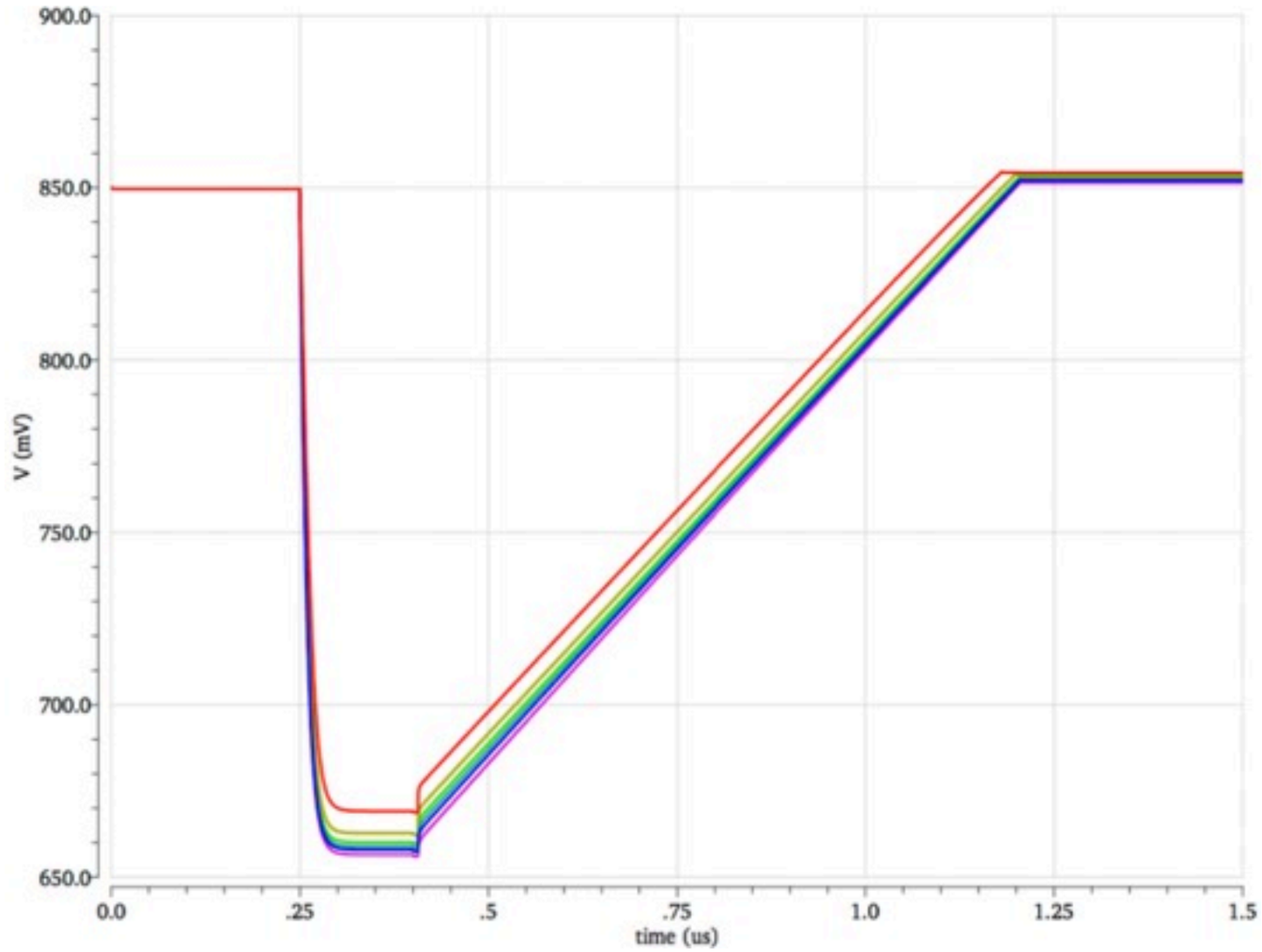
- Analogue converted to UMC
  - Included an additional current mirror
  - Stability of TDC charging current improved:



simulations by Alberto Riccardi

Temperature Stability of TDC

- Conversion time in TDC, depending on temperature



Temp. (°C)	EOC (bits)
0	0010111101
25	0011000000
50	0011000001
75	0011000001
100	0011000001
125	0011000001

simulations by Alberto Riccardi

- Above room temperature: change 1 LSB
  - Verified with tests of TOFPET

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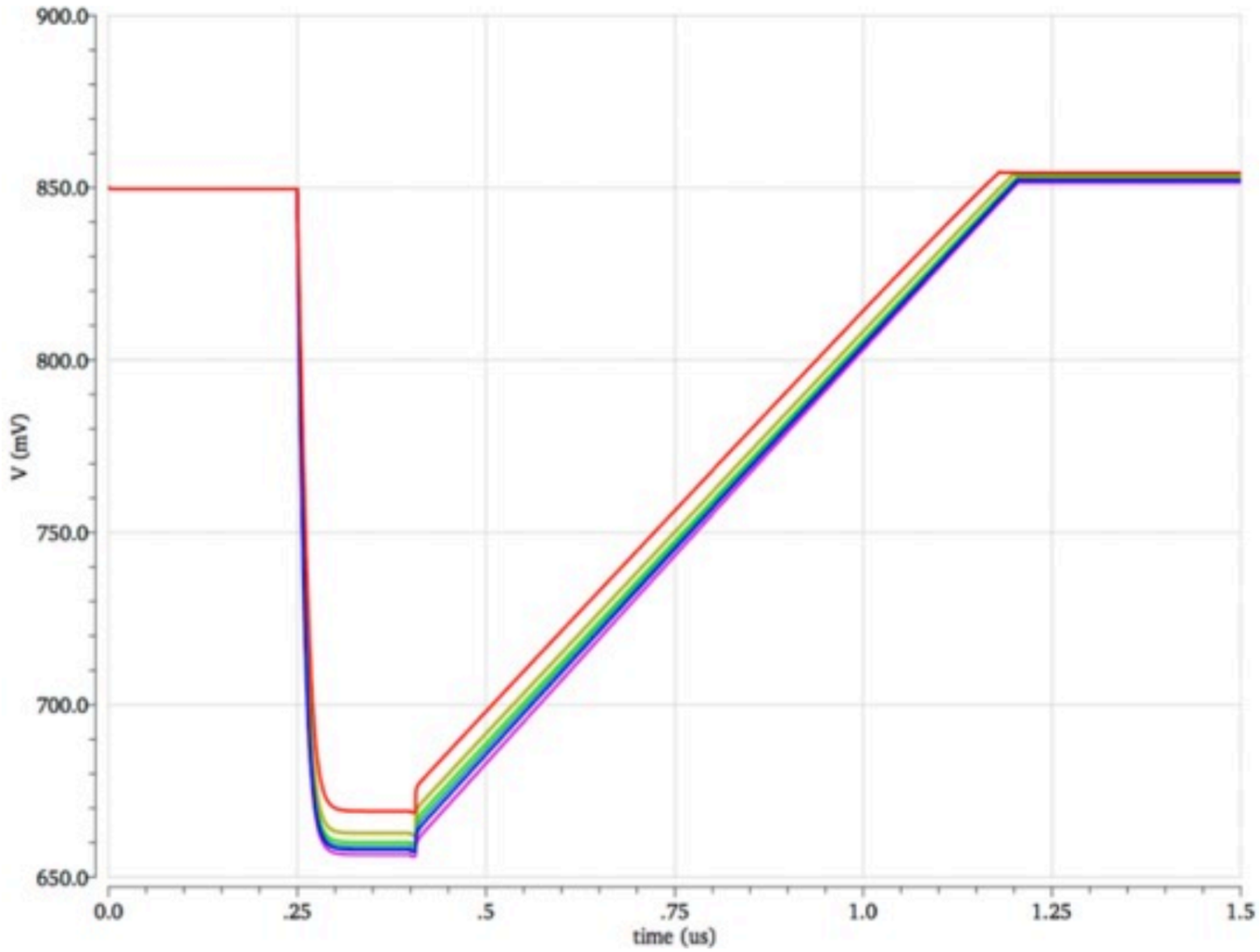

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Finer simulation grid
in room temp. regime

Current work (comparator) and outlook

- Concept for »hysteresis comparator« ready
  - More robust for re-triggering on the falling edge
  - Current status: layout (learning) phase
  - Plan: finished until end of September
- Starting in October with layout of Front-end

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Digital Part

Meeting with TOFPET People (Lisbon)

- Introduction into global controller and test benches
- Lot‘s of small, technical questions

- Structure of the digital part (esp. TDC Control)
  - Room for optimizations
    - Structure not clear
    - Some solutions too complicated
    - Things done multiple times at different locations
  - Leads to too much logic
    - Power
    - Area

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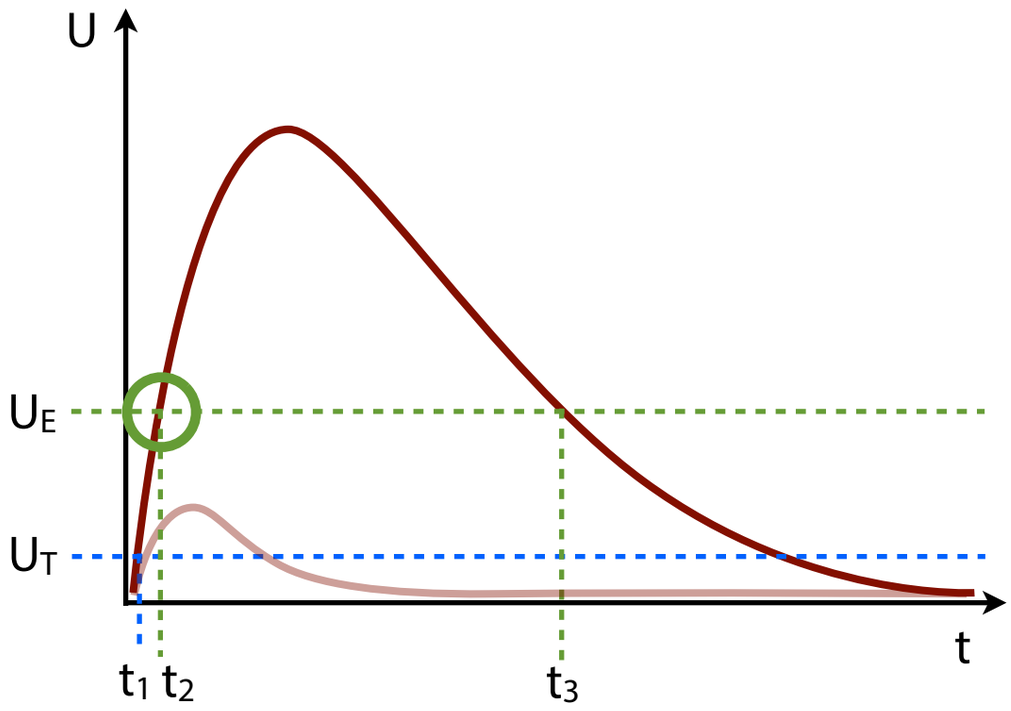
Rewrite digital TDC!

Some Conceptual Differences

- Switch to different technology
  - IBM 130 nm → UMC 110 nm
- Time buffers move to global controller
  - Saves connections
- Hit validation in two ways
  (delayed & synchronous)
- More flexibility what to store
  (t_1-t_3, t_1-t_2, test pulse)
- Optimization in charging time
- Refresh local instead global
  - Capacitors back to reference level after inactivity



Current Status of TDC Control

- Basic concept is implemented
  - Trigger, TAC selector, charge transfer and measurement, …
- Details are missing
- No SEU protection yet
- Current status:

	TDC_CTRL v1 (incl. SEU, IBM)	TDC_CTRL v1 (incl. SEU, UMC)	TDC_CTRL v2 (current status, UMC)
Occupancy (1.1 x 0.1 mm²)	84.8 %	37.0 %	no place & route yet
Cells	3155	2850	237
Power	1.57 mW/ch	1.78 mW/ch	0.03 mW/ch

@ 160 MHz

Estimate for final TDC Control:
Save up to 80-90% in terms of power/occupancy

Conclusion

- Analogue part
  - Front-end: concept ready, layout starts soon
  - TDC: switch to UMC complete, improved current stability
- Digital part
  - Switch to UMC: TDC CTRL (100%), GCTRL (0%)
  - Redesign started, current status promising (power/occupancy down to ~10-20%)
- **Discussion needed**
  - Geometrical descisions
    - Channel pitch
    - Position of bonding pads

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Thank you!

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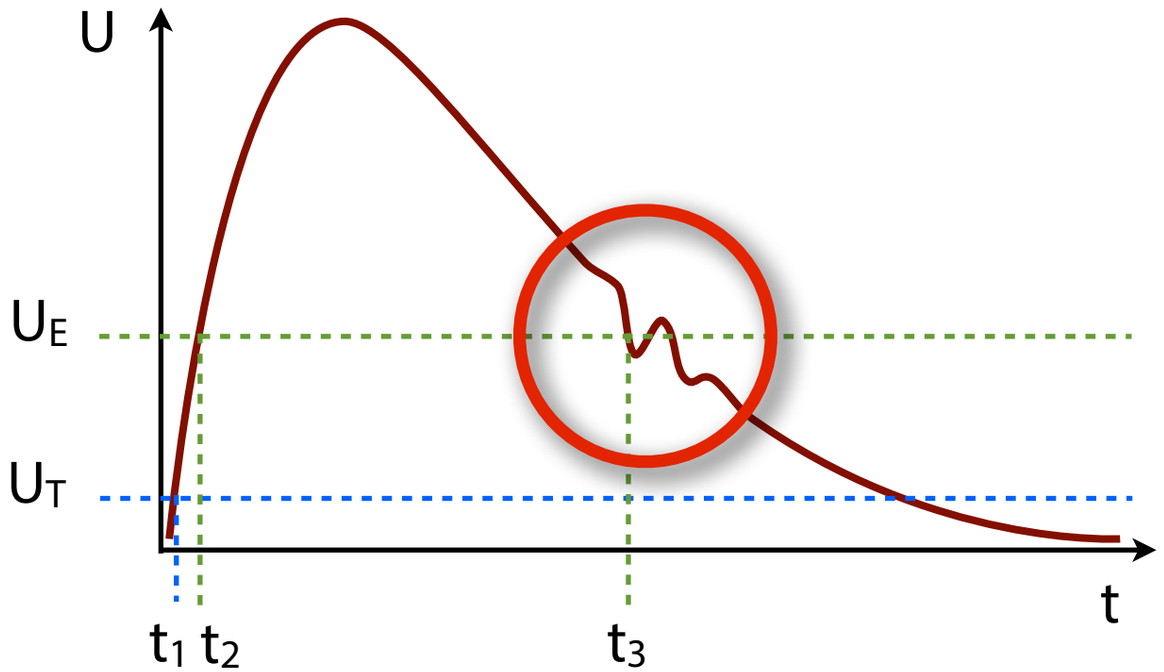
Backup

Hysteresis Comparator

- Problem:
  - Noise on the signal might lead to re-triggering



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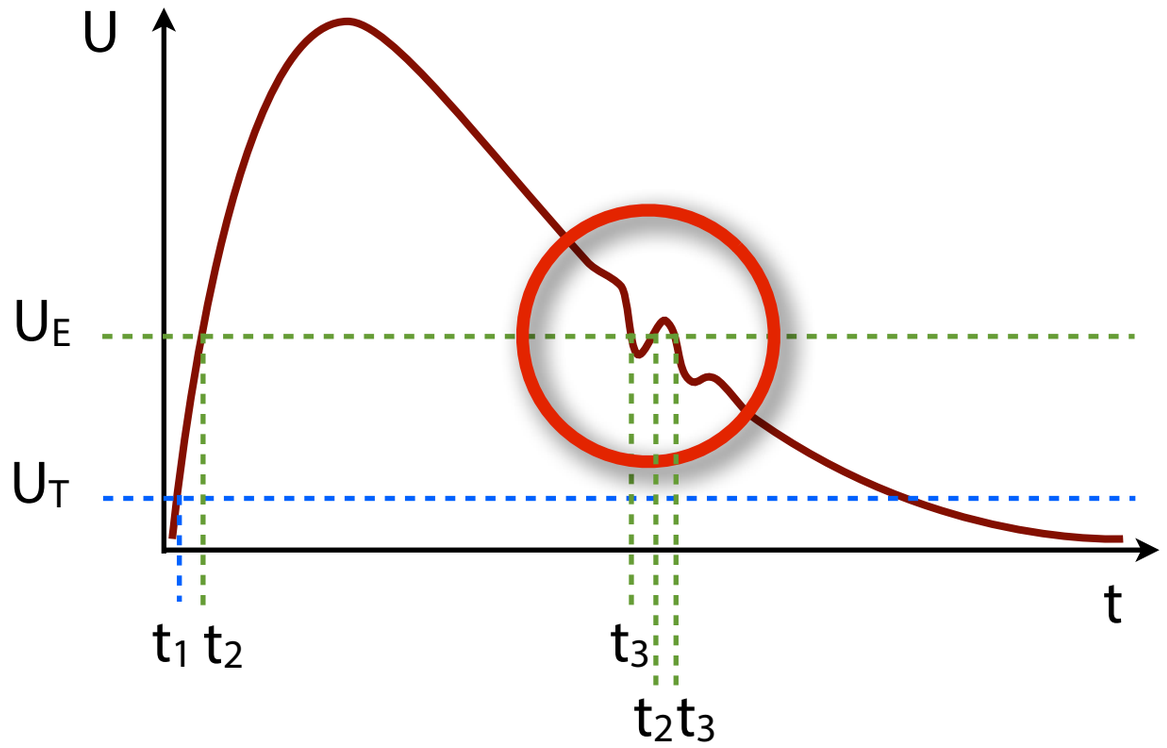

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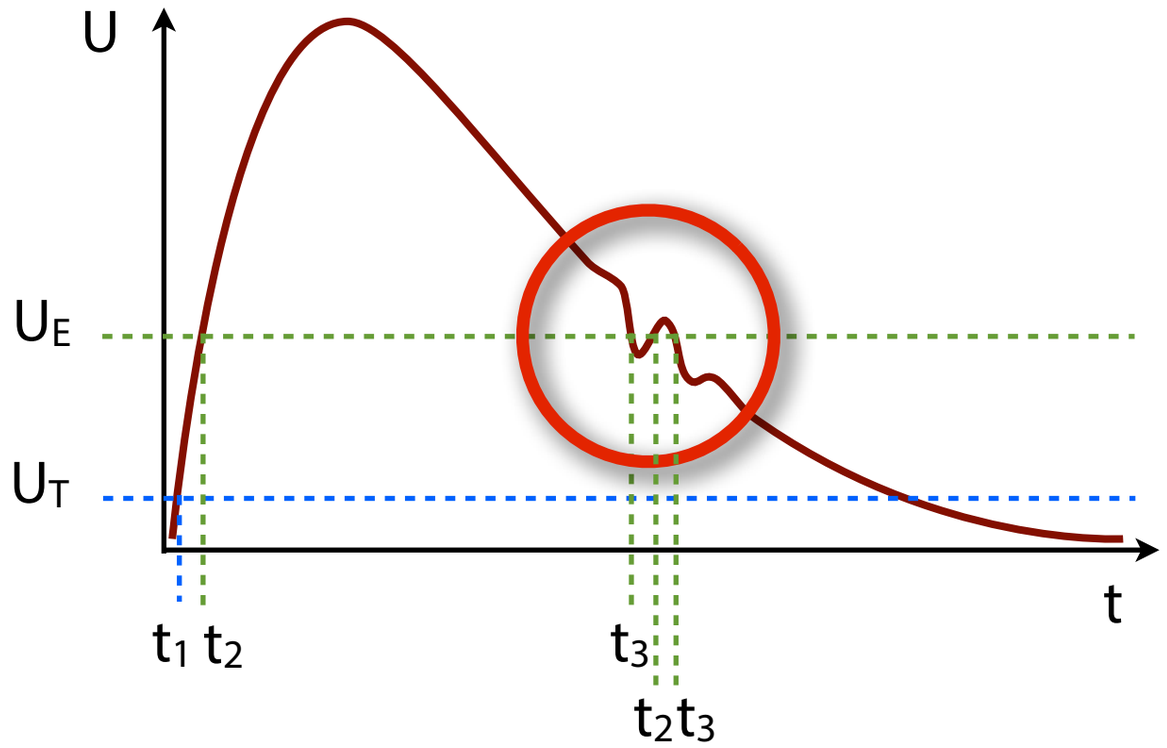

- Solution:
  - Different threshold levels for rising and falling edge
  - Re-triggering suppressed