FEE Workshop in ALBA: a short summary

Angelo Rivetti
INFN-Sezione di Torino, Italy

Outook

- **Three dedicated front-end session with 12 talks.**
- **Design reports (MVD, STT, Calorimeter)**
- **Requirements discussion (GEM)**
- **A brief review of the major points in the following**

MVD: pixels

PANDA FEE-DAQ Workshop

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Status report
of the
Silicon Pixel Detector
Readout Electronics

G. Mazza
on behalf of the Torino MVD pixel group

Gianni Mazza *PANDA FEE-DAQ Workshop, April 29th – 30th 2013*

ToPiX (1)

ToPiX v3 layout

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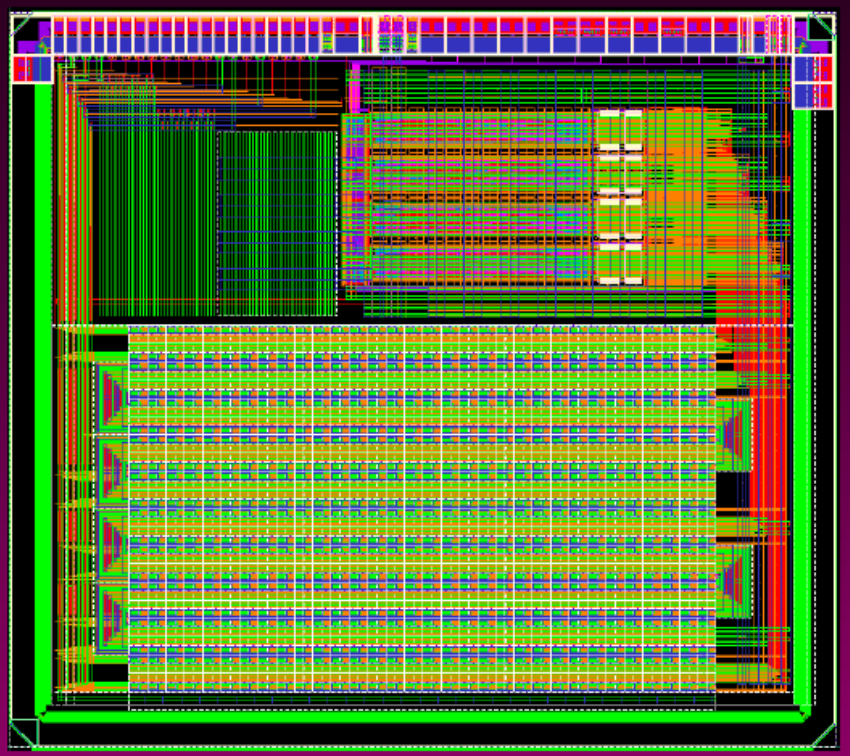

- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

Gianni Mazza

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ToPiX (2)

Timing issue

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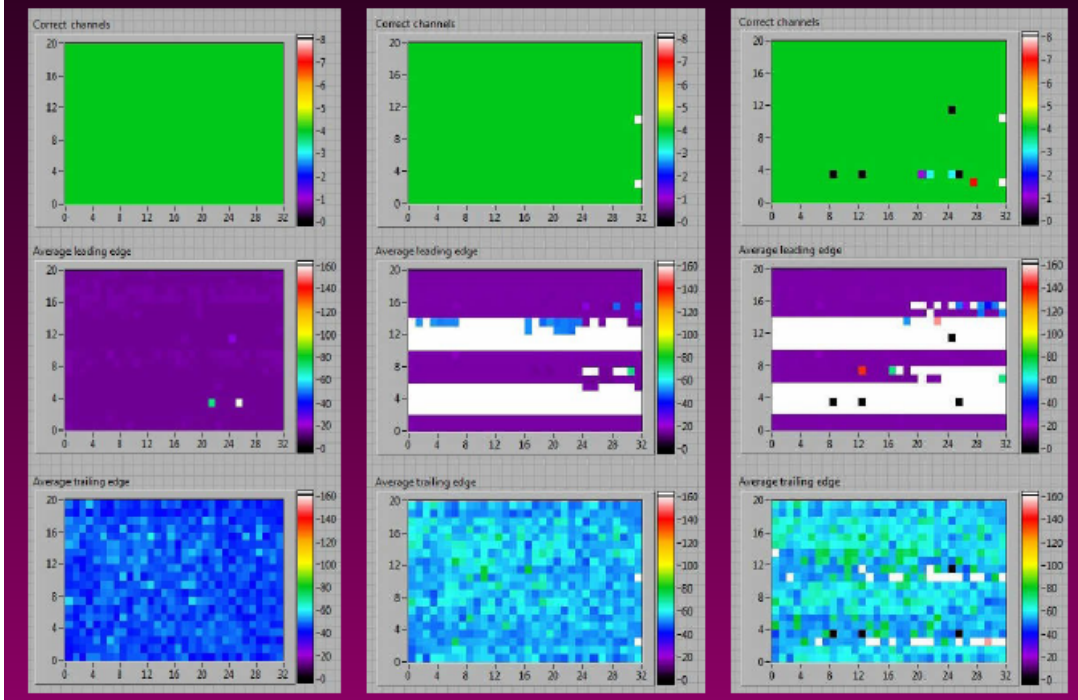
50 MHz 65 MHz 70 MHz



- Trailing edge still good @ 65 MHz
- Read leading edge cmd asserted at the same time as read cmd.
- Read trailing edge cmd asserted when read cmd is already high
- *Clock cycle to be inserted between read cmd and read leading edge cmd.*

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ToPiX (3)

ToPiX v4

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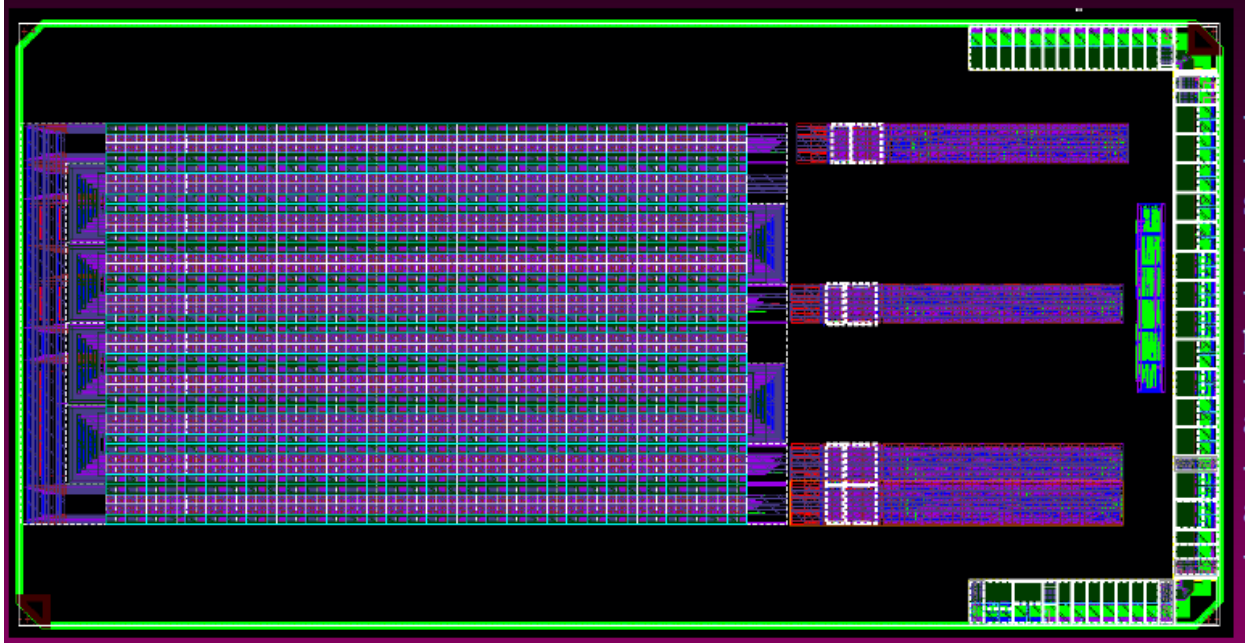

- Size : 6 mm × 3 mm
- Compatible with v3 sensors
- CMOS 130 nm
- New pixel SEU protection scheme
- New column bus Tx and Rx
- Timing optimization and bug fixing
- GBT e-link interface

Gianni Mazza

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APFEL (1)

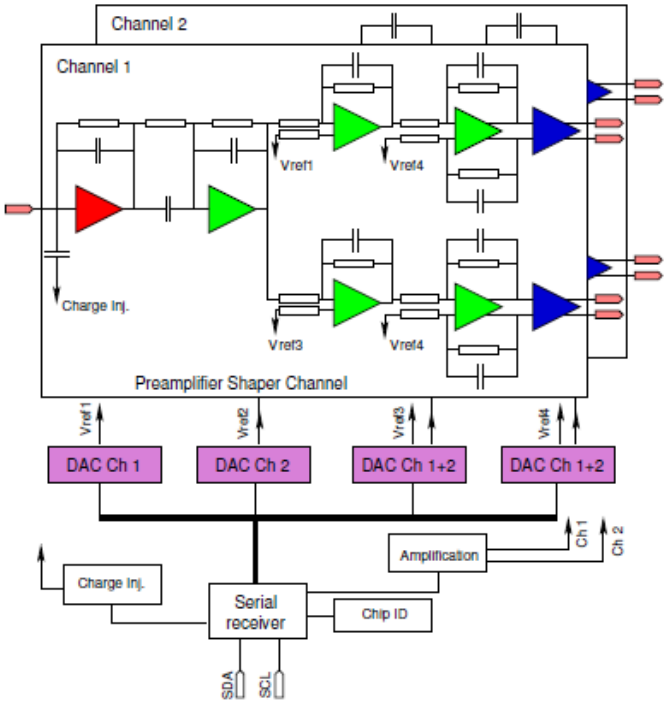
APFEL 1.5
An Integrated Preamp and Shaper for PANDA EMC

Holger Flemming, Peter Wieczorek
GSI - EE - ASIC-Design

29.04.2013

APFEL 1.5 Overview

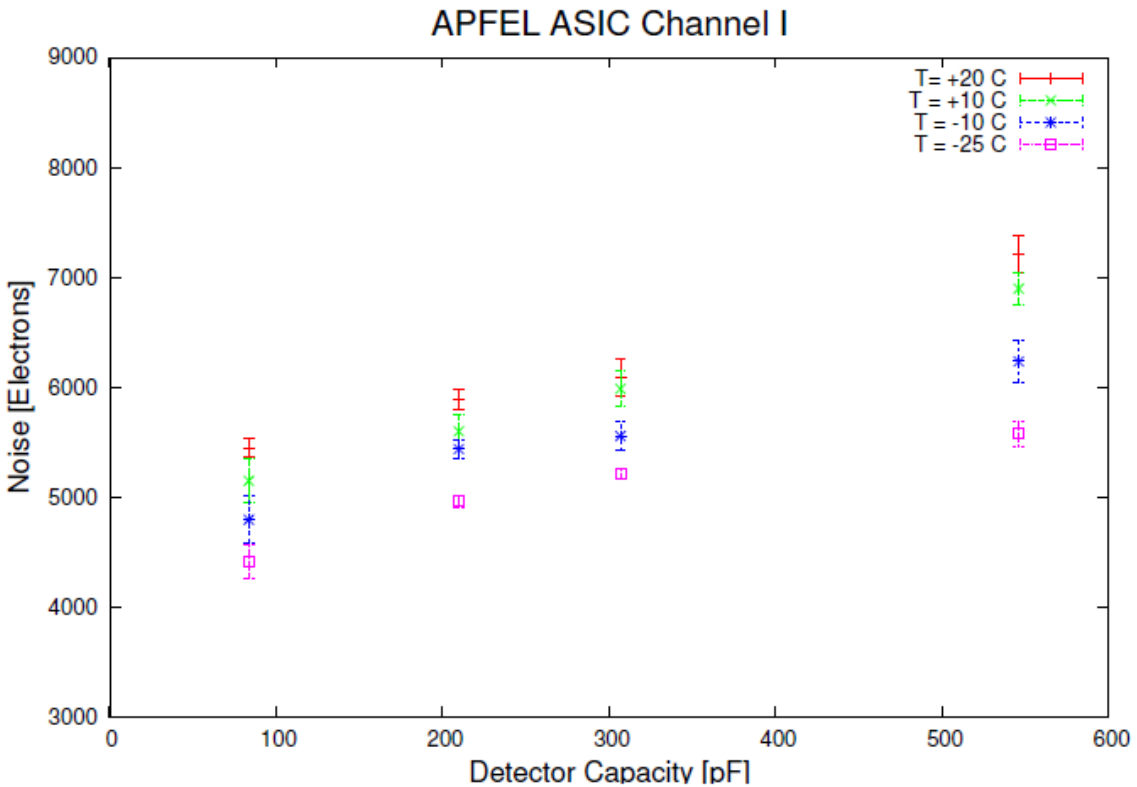
- Two independent channels
- Charge sensitive preamplifier
- CR-RC shaper with 3rd order integrator
- o' Conner schema pole-zero-cancellation
- Dual range output with configurable amplification: 16/32
- Configurable voltage references for baseline adjustment
- Configuration via three-wire serial bus



APFEL (3)

Measurements

Noise



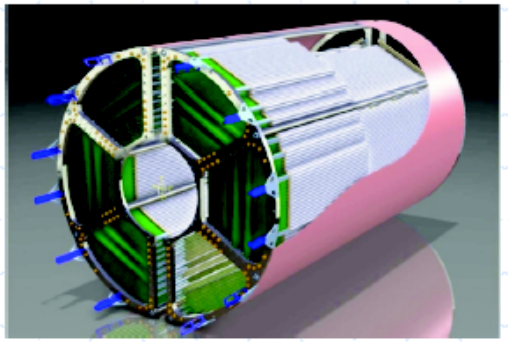
$$ENC = (4234 \pm 143)e^- + (3.3 \pm 0.31)\frac{e^-}{pF} \cdot C_{det} + (23.75 \pm 0.31)\frac{e^-}{K}(T - 246K)$$

$$C_{det} = 280pF,\ T = -25^\circ C \Rightarrow ENC = 5206 \pm 167e^-$$

Summary and Outlook

- Integrated preamplifier for PANDA EMC is available in fifth iteration
- Measured performance meets specifications

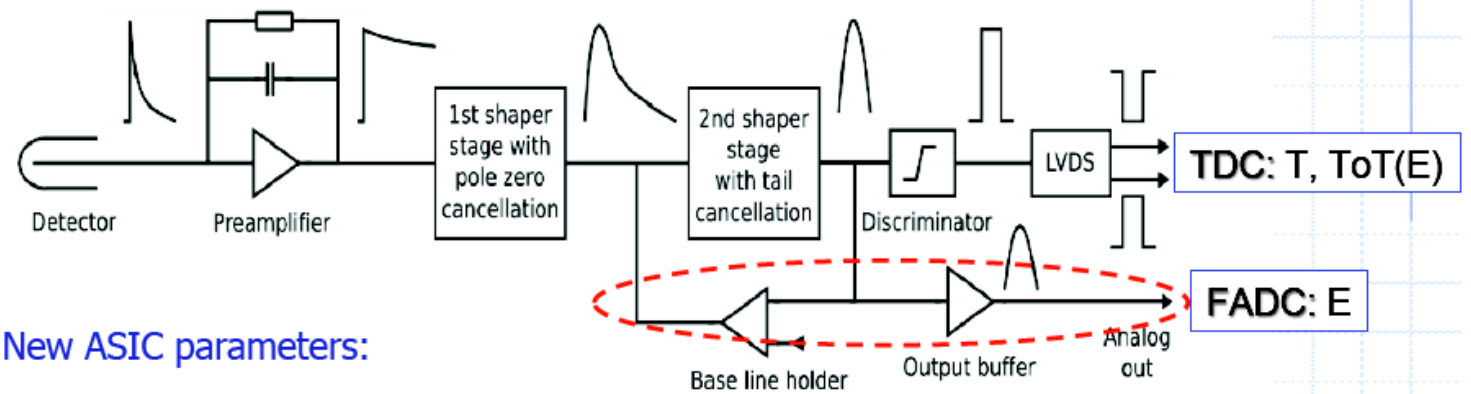
- Proto120 will be equipped with APFEL 1.4
- Beam tests hopefully end of this year



Updates on the STRAW front-end electronics

- STT layout;
- The readout concept;
- Electronics developments;
- Status and perspectives.

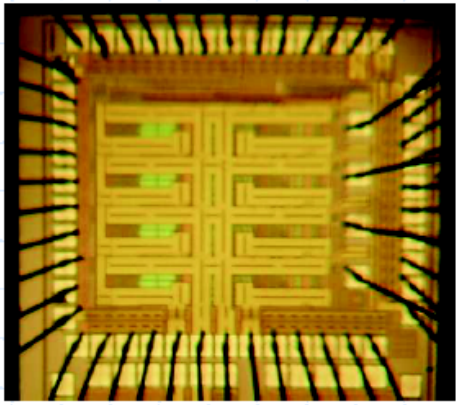
FEE readout concept



New ASIC parameters:

- Variable charge gain: 3 – 24 mV/fC
- Variable peaking time: 20 and 40 ns
- CR–RC2 shaping with Tail Cancellation
- BaseLine Holder – baseline independent on supply/temp. variation and high count rate
- Leading-Edge Discriminator for Time and ToT measurements
- Analog output

- AMS 0.35 μm CMOS
- Four Channels
- Channle Size: 1130Å~200 μm^2
- Power Consumption: 15.5 mW/ch + 12mW (LVDS)



II Version of STT ASIC

The following STT ASIC parameters have been fixed:

- nr of channels: 8
- outputs: we will keep both LVDS and analog
- noise: ENC of about 1.5fC is acceptable
- gain: new values to avoid preamp. saturation. The best option corresponds to the setting "1mV/fC" in the present ASIC
- detector capacitance: 15-25 pF
- tail cancellation: we will keep the present capabilities of setting two time constants in very wide range
- uniformity of base line between channels (and therefore threshold seetings.

A new production of 100 ASICS will be realized this year. The technology will remain CMOS 350 nm.

TOF-PET (1)

The TOFPET chip: a time based readout for radiation detectors

Manuel Dionisio Rolo, Ricardo Bugalho, Carlos Gastón,
Giovanni Mazza, Marco Mignone, Angelo Rivetti,
Jose Carlos da Silva, Rui Silva, Joao Varela, Richard Wheadon

LIP - Laboratorio de Instrumentacao e Fisica Experimental de Particulas
INFN - Istituto Nazionale di Fisica Nucleare sez. Torino

"The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/ 2007-2013) under Grant Agreement n°256984."

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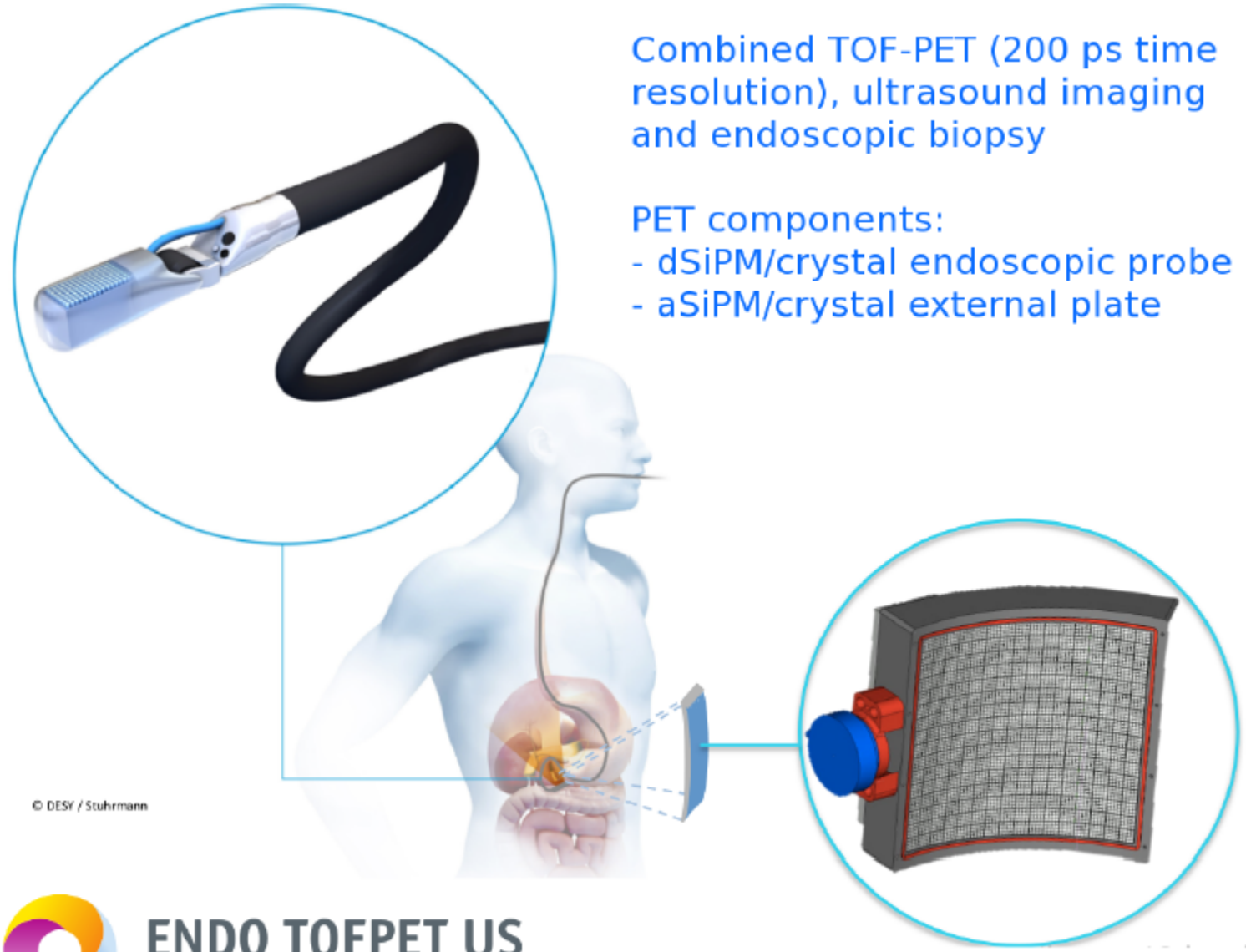
TOF-PET (1)

Combined TOF-PET (200 ps time resolution), ultrasound imaging and endoscopic biopsy

PET components:
- dSiPM/crystal endoscopic probe
- aSiPM/crystal external plate



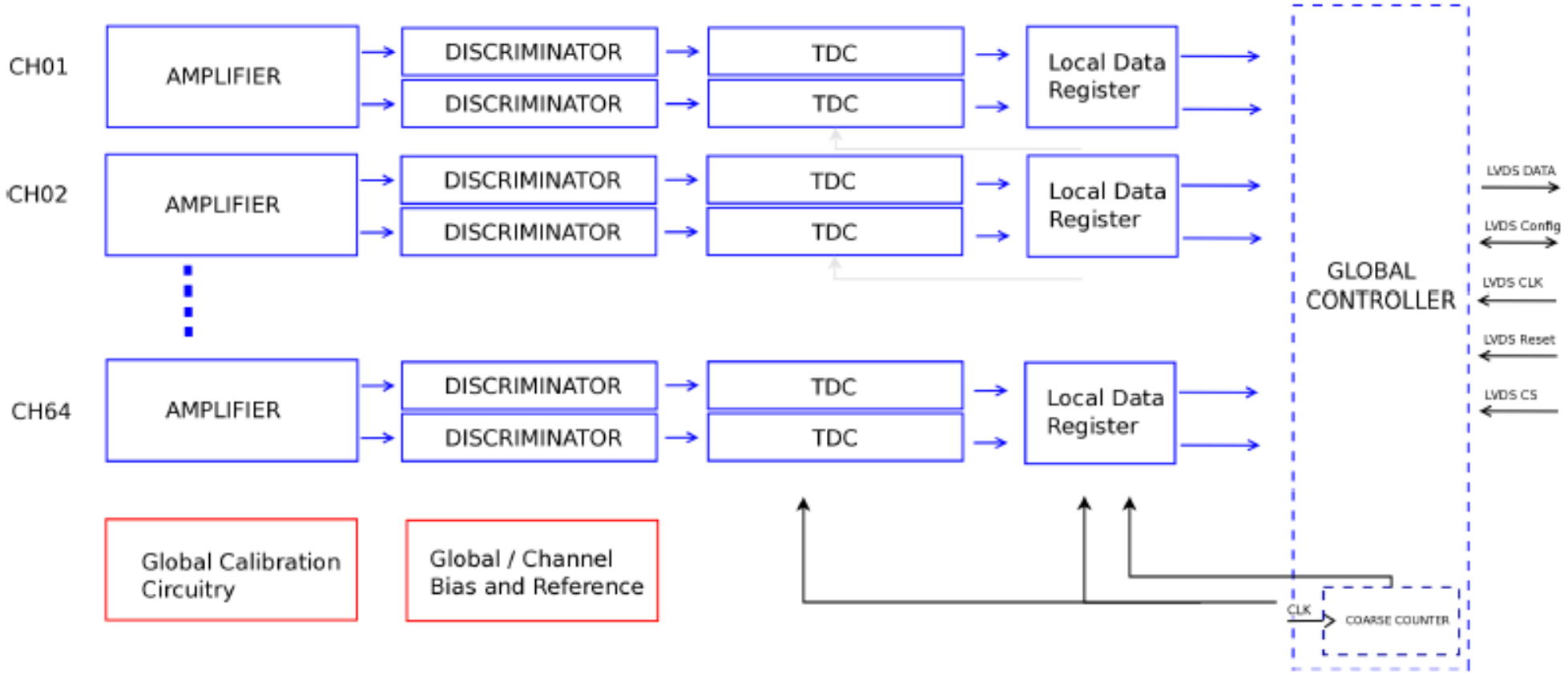
ENDO TOFPET US
Endoscopic TOFPET & Ultrasound

ASIC specifications

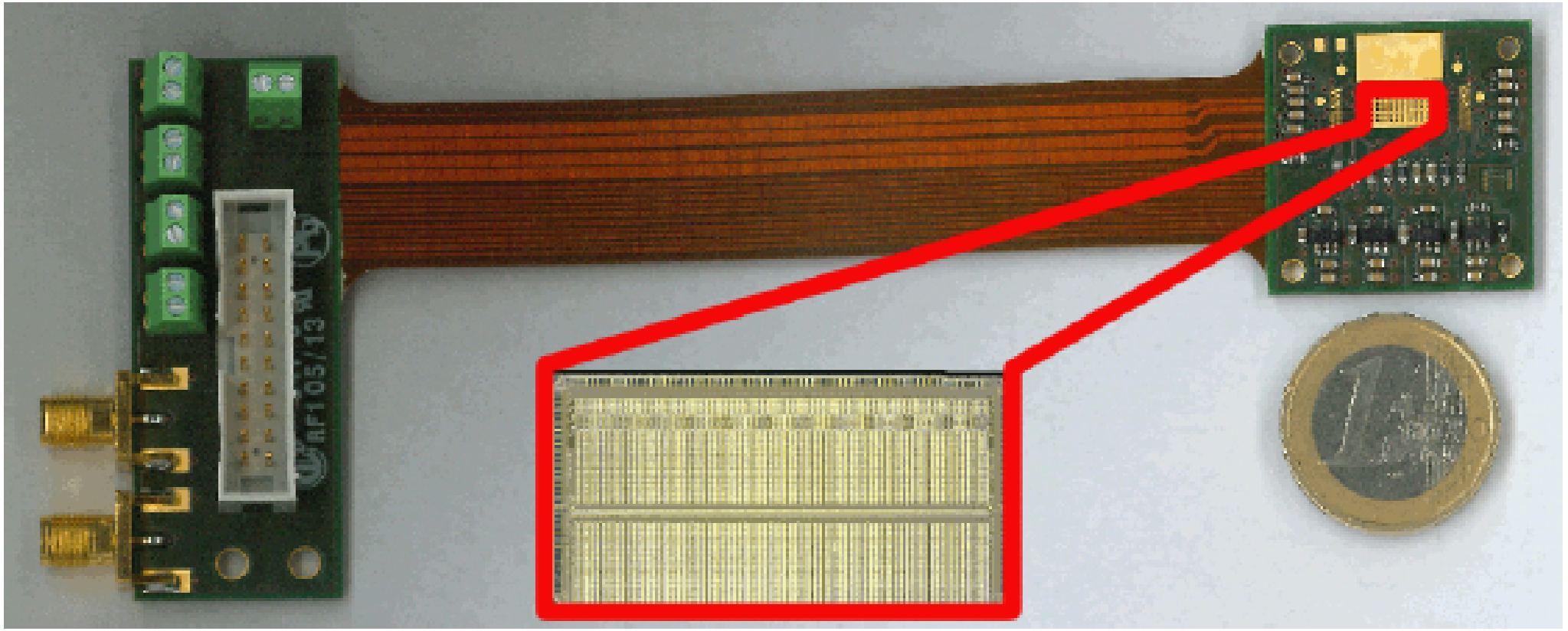
Parameter	Value
Number of channels	64
Clock frequency	80 – 160 MHz
Dynamic range of input charge	**300 pC**
SNR (Q_{in} = 100 fC)	> 20-25 dB
Amplifier noise (in total jitter)	< 25 ps (FWHM)
TDC time binning	**50 ps**
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. channel hit rate	100 kHz
Max. output data rate	320 Mb/s (640 w/ DDR)
Channel masking	programmable
SiPM fine gain adjustment	**500 mV (5 bits)**
SiPM	up to 320pF term. cap., 2MHz DCR
Calibration BIST	internal gen. pulse, 6-bit prog. amplitude
Power	**< 10 mW per channel**

How these specs impact the choice
of the readout chip architecture?

ASIC architecture

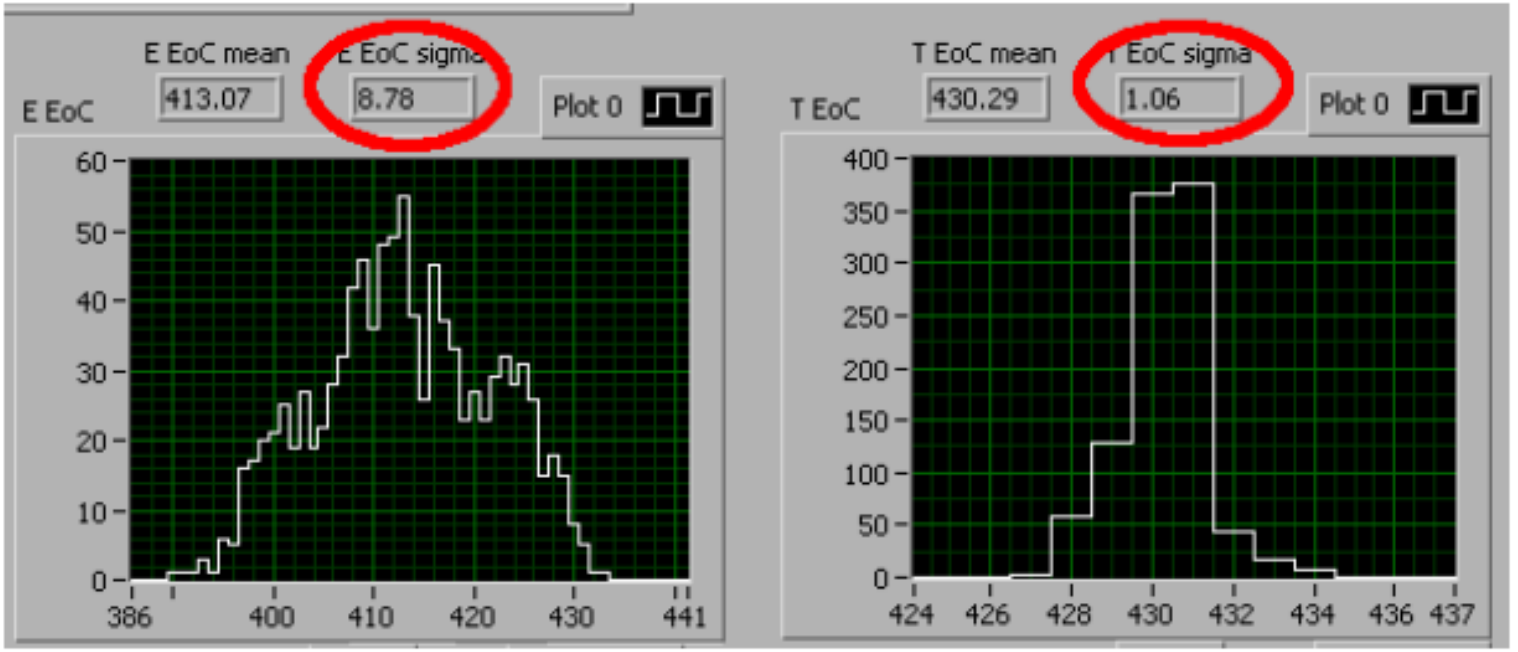


One of the test PCB



Other test PCBs developed at LIP (Lisbon) to accommodate packaged dies.

Some performance example



- **TP jitter + FE jitter + TDC noise ≈ 60 ps FWHM**, using the id of the TDC buffer.

PANDA microstrip (1)

Updates on the front-end electronics for the microstrip sensors of the MVD

MVD meeting, Alba 29 April 2013

INFN-Sezione di Torino

Speaker: Valentino Di Pietro

PANDA microstrip (2)