An alternative online tracking algorithm using STT

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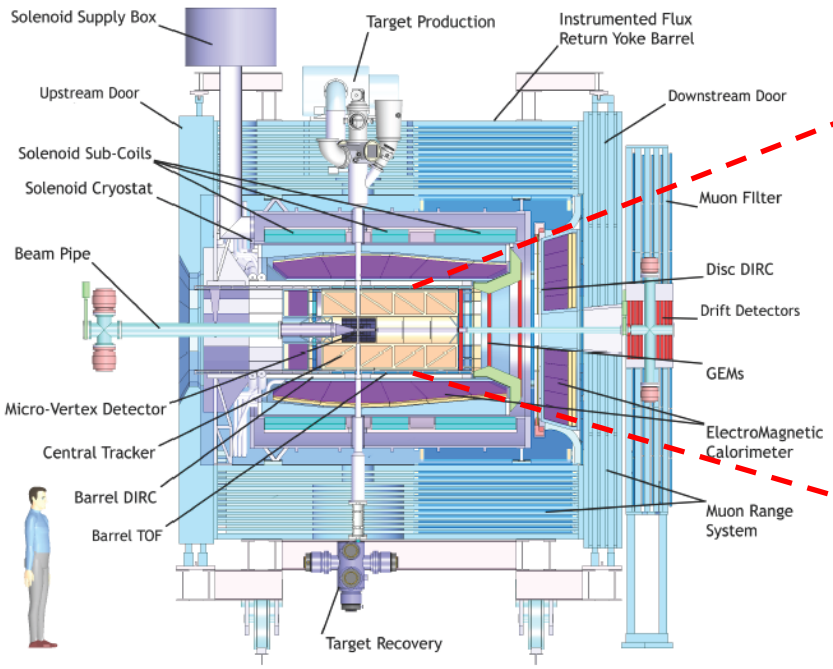
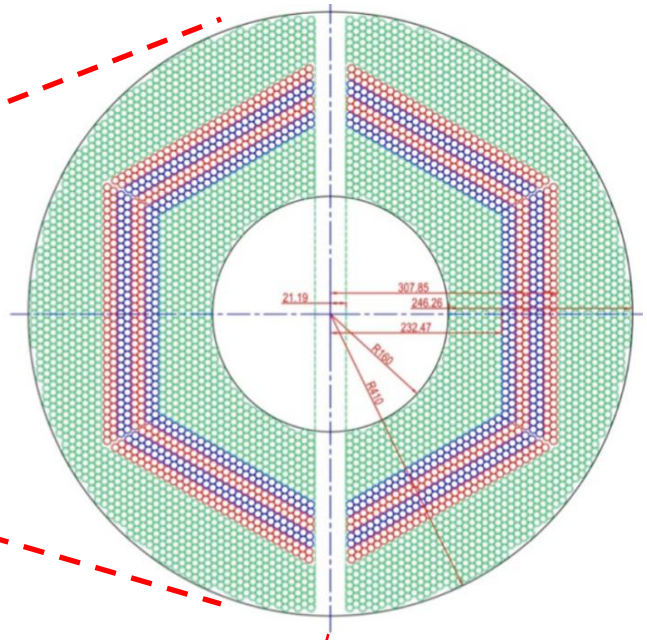
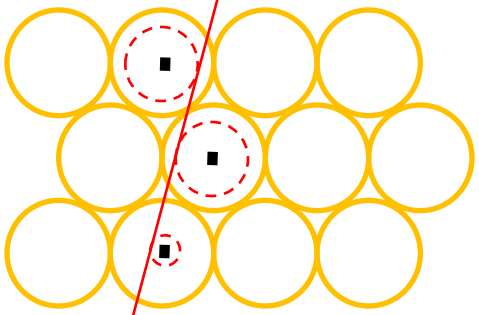
Outline

1. Introduction
2. Road finding and momentum calculation
3. Performance study
4. VHDL implementation
5. Summary and outlook

Straw Tube Tracker(STT)



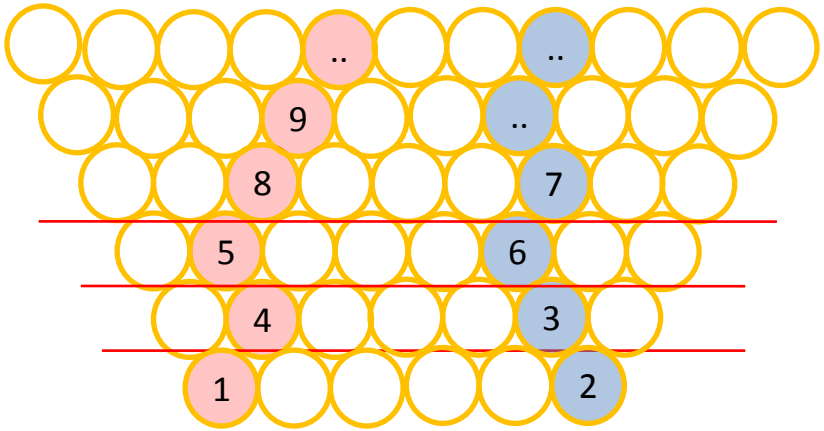




- ➢4636 Straw tubes
- ➢23-27 planar layers
- 15-19 axial layers(green) in beam direction
- 4 stereo double-layers for 3D reconstruction, with ±2.89 skew angle(blue/red)

From STT : Wire position + drift time

Road finding



1: Sort hits, and fill into array
array_layer_0 <= (1, 2)
array_layer_1 <= (3, 4)
array_layer_2 <= (5, 6)

2: Combine hits of two adjacent layers,
keep effective combinations (in red color)

Layer 0 & 1: 1->3 || 2->3 || 1->4 || 2->4
Layer 1 & 2: 3->5 || 4->5 || 3->6 || 4->6
Easy to parallel design.

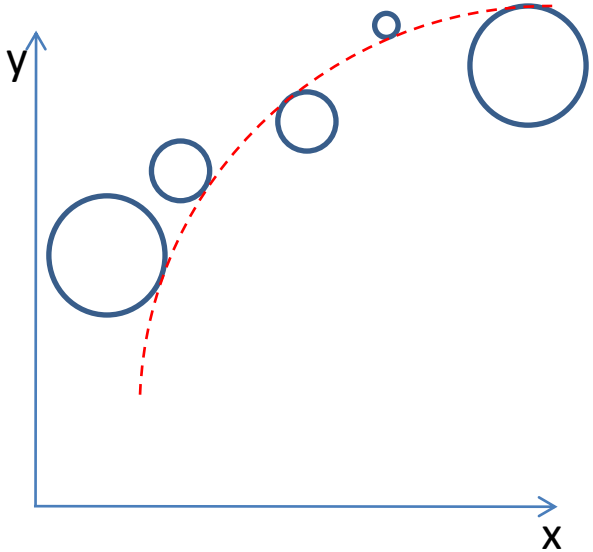
3: Connect these combinations and form tracklets

1->4 + 4->5 … = 1->4->5->8->9
2->3 + 3->6 … = 2->3->6->7…..

If some where broken, a further step to connect them…

4: Calculate momentum for each tracklet.

Calculation of circle parameters



Known : x_i , y_i , r_i

Question: To determine a circle,

$$x^2 + y^2 + ax + by + c = 0$$

Method: Minimize the equation

$$E^2 = \sum(x_i^2 + y_i^2 + a\, x_i + b\, y_i + c)^2$$

1) $c = 0$

2) include drift circle as weight, W_i

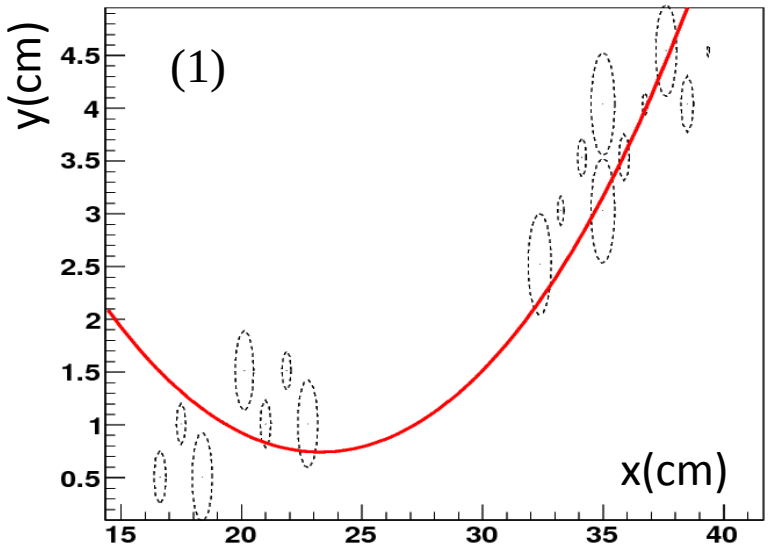
$$\begin{pmatrix} S_{xx} & S_{xy} & S_x \\ S_{xy} & S_{yy} & S_y \\ S_x & S_y & N \end{pmatrix} \begin{pmatrix} a \\ b \\ c \end{pmatrix} = \begin{pmatrix} -S_{xxx} - S_{xyy} \\ -S_{xxy} - S_{yyy} \\ -S_{xx} - S_{yy} \end{pmatrix}$$

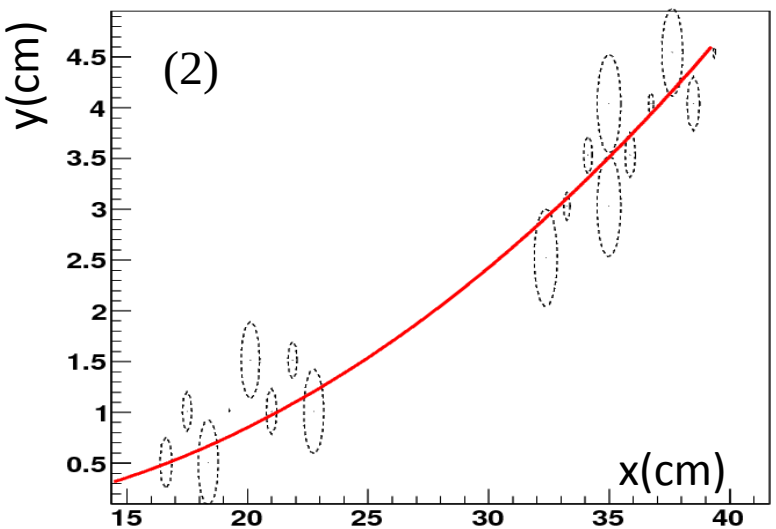
$S_x = \sum x_i \quad \ldots$

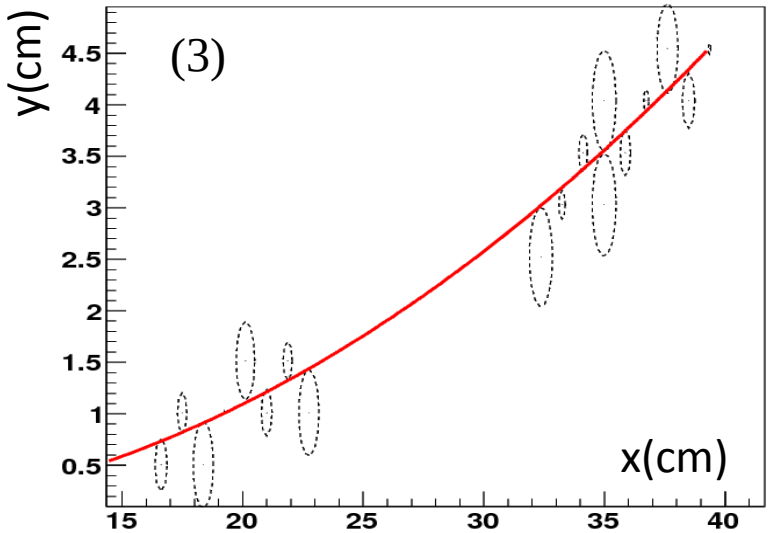
$S_{xx} = \sum x_i x_i \quad \ldots$

$S_{xxx} = \sum x_i x_i x_i \quad \ldots$

Performance study





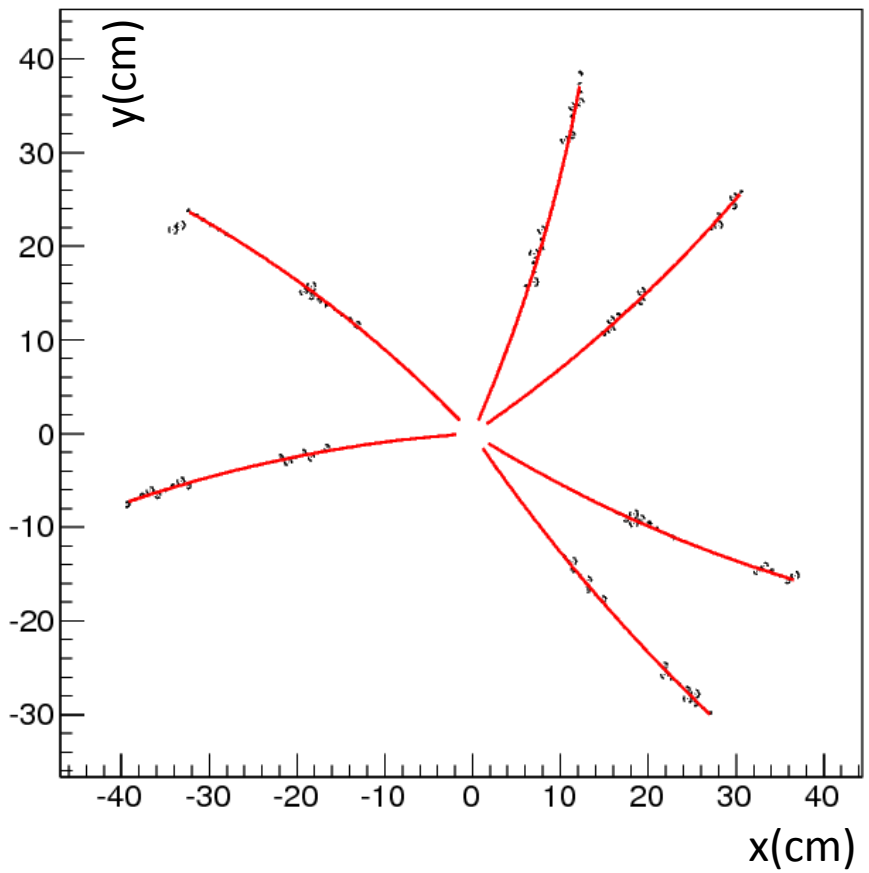


(2): $c = 0$

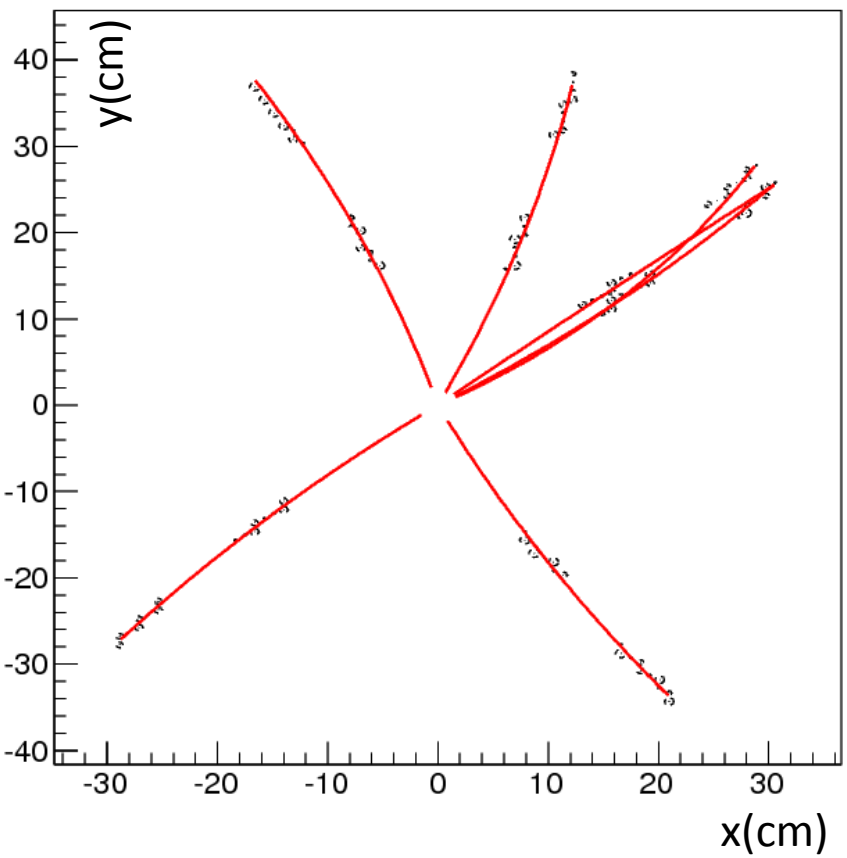
(3): $c = 0$, $W_i = (1/di)^2$

Performance study – multi tracks

Event example 1

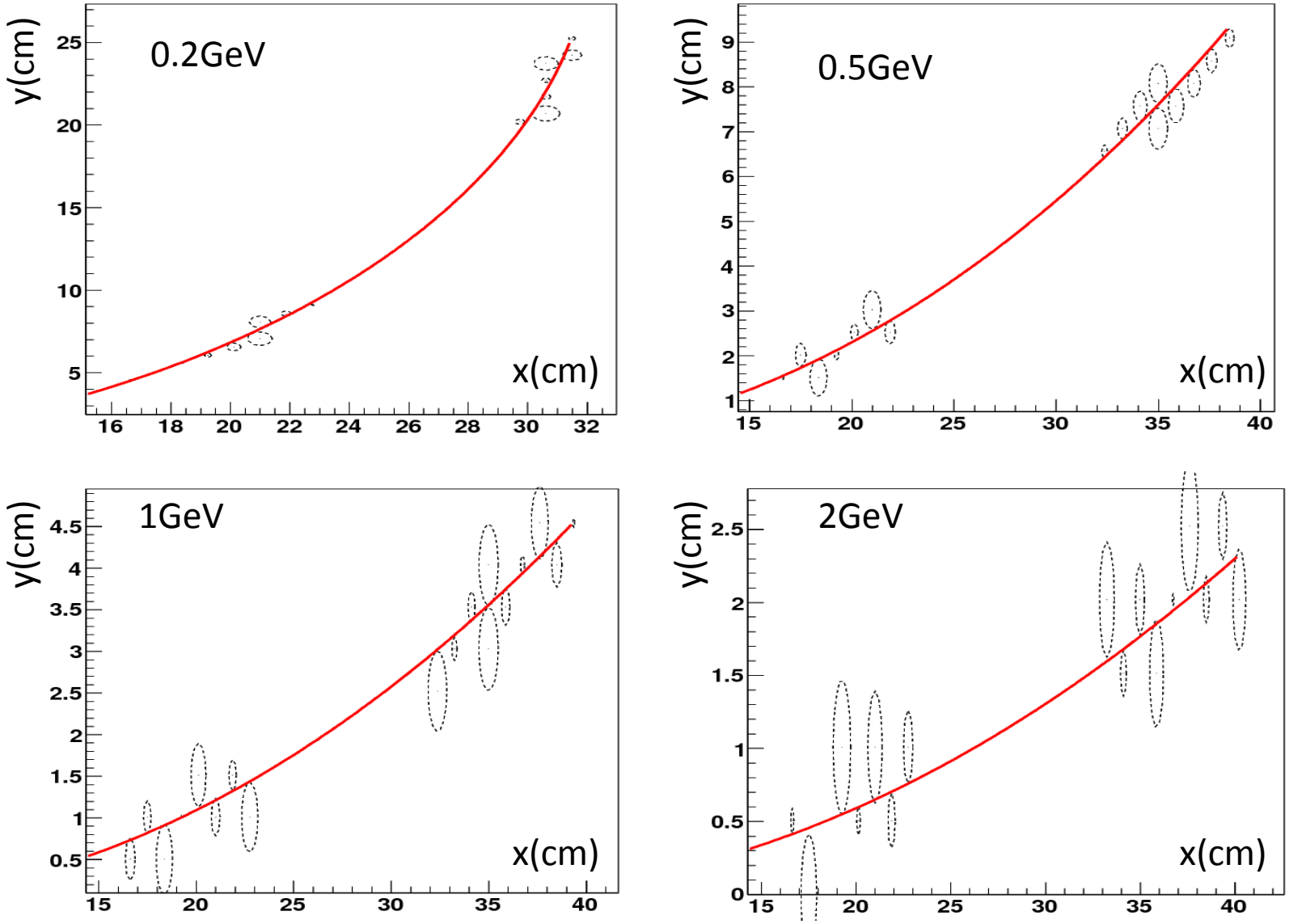


Event example 2

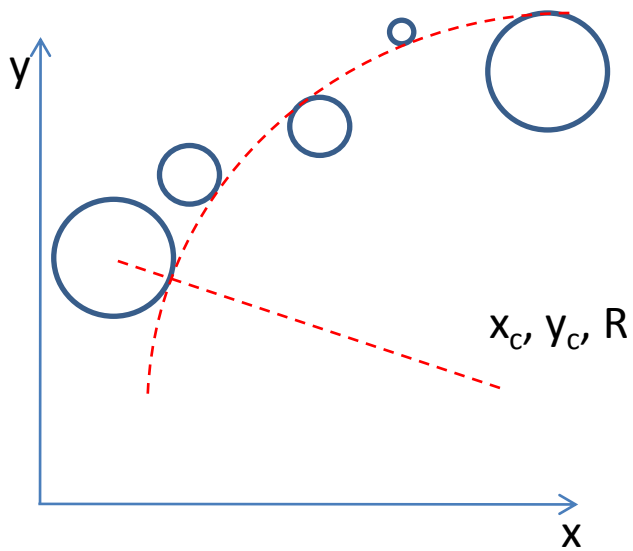


A further step to clean up fake tracks is not applied.

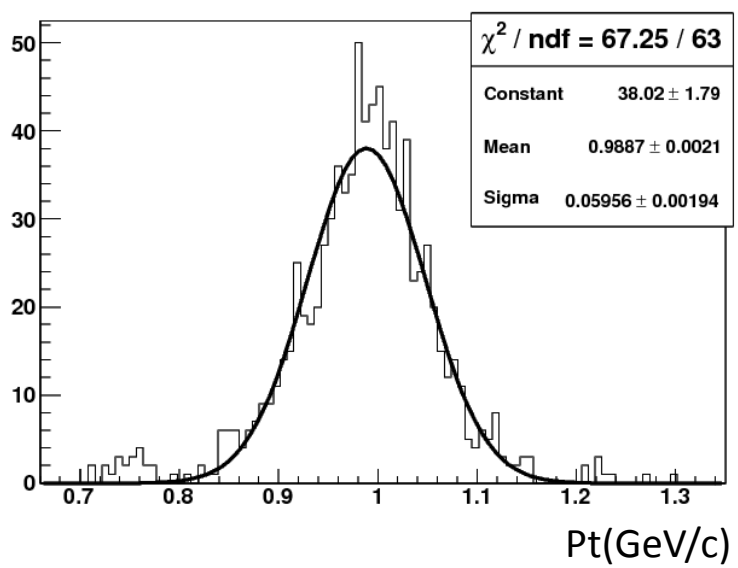
Performance study – single track

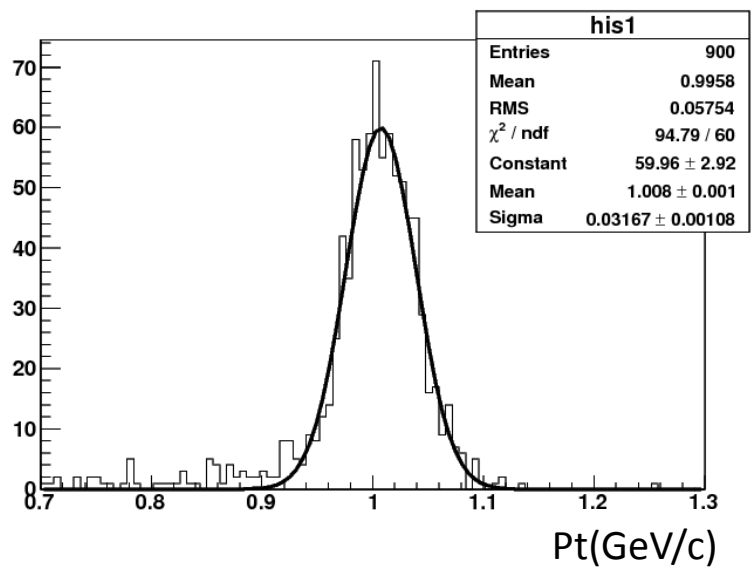


To improve the momentum resolution

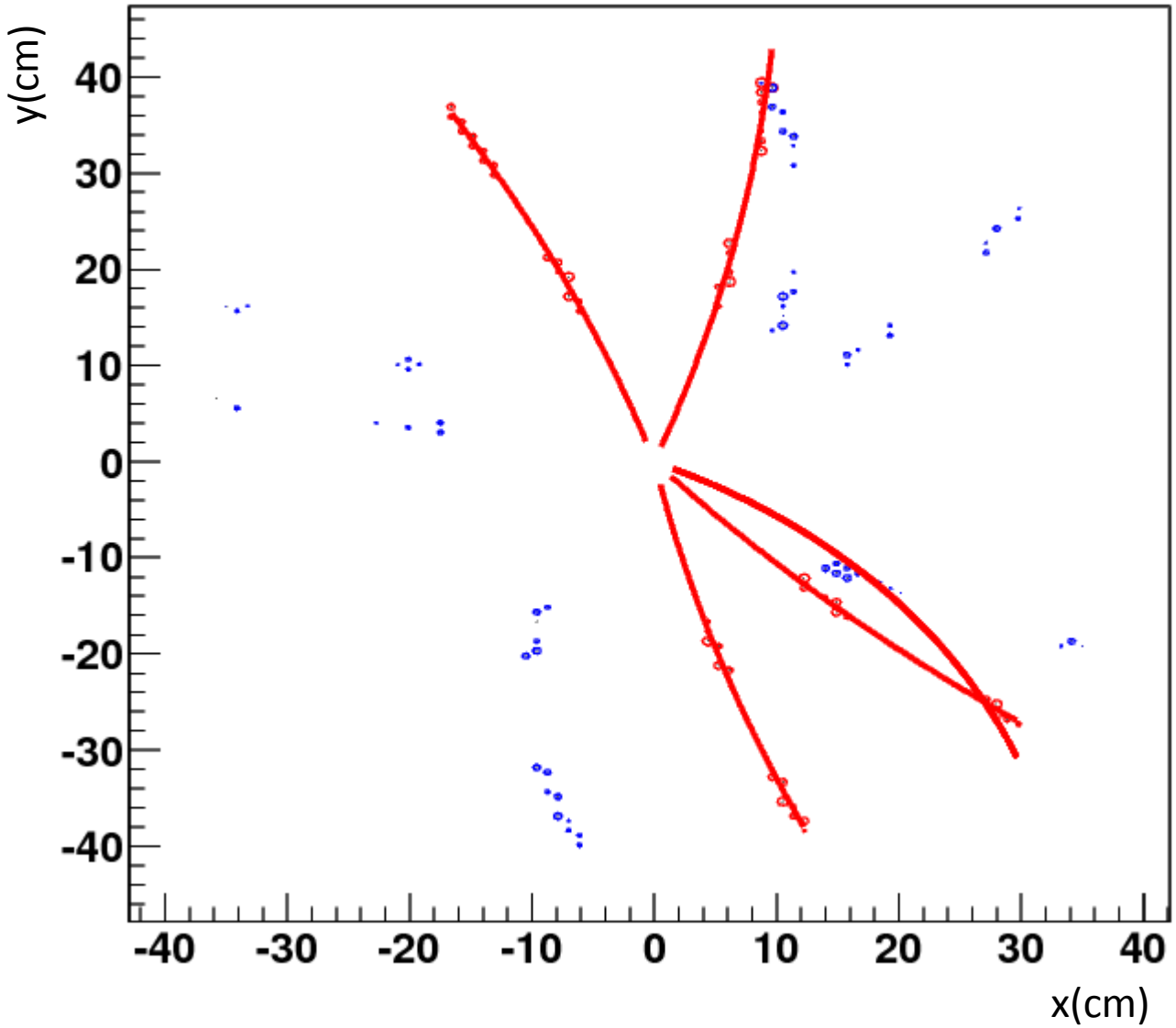


0.2GeV/c :	0.195	±0.0068	0.195	±0.0068
0.5GeV/c :	0.5	±0.0212	0.5	± 0.0164
1.0GeV/c :	0.99	±0.0595	1.0	± 0.0317
2.0GeV/c :	1.85	±0.213	2.0	± 0.073





Performance study – with background



red circles : signal event

blue circles: other events from naive time-based simulation

VHDL implementation

1: Road finding: Using status machine to control the following procedures.

1) Hit sorting: fill hit into array_layer_id according to layer ID

2) Combine hits from two adjacent layers

3) Form a tracklet by attaching hit layer by layer
   tracklet_inner : layer 0-7
   tracklet_outer: layer 8-15

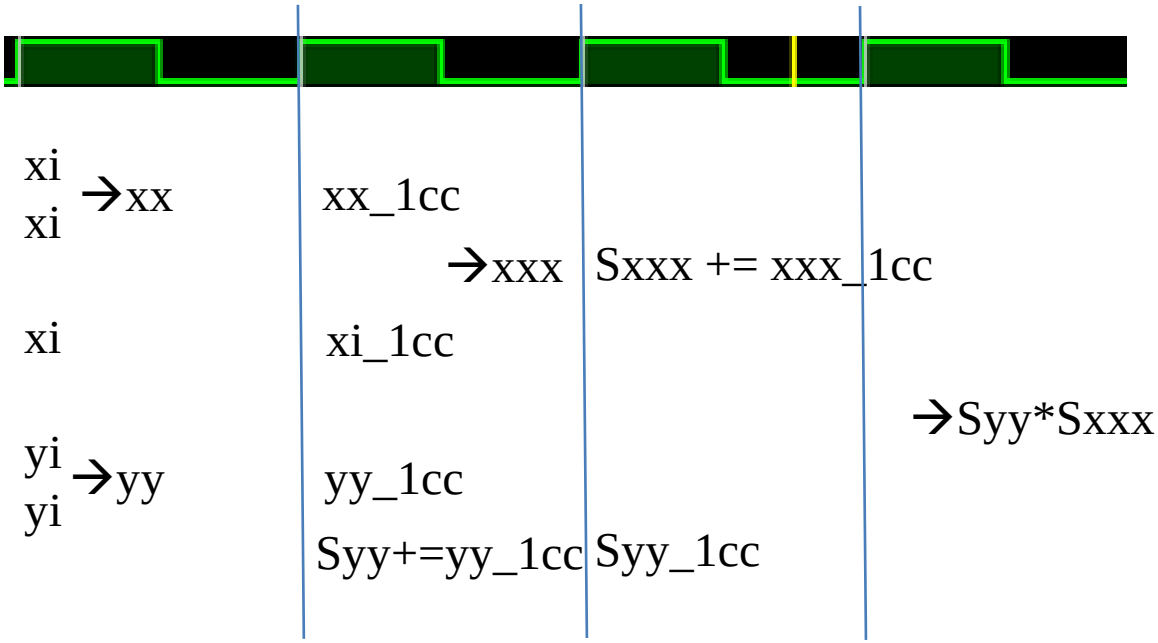
4) Combine tracklet_inner and tracklet_outer. Not done yet.

For one event with 100 hits: 1) 100 clock cycles (cc) 2) ~ 600cc 3) ~100cc
→ 8000 ns (if FPGA running at 100MHz)

VHDL implementation

2: Momentum calculation

a = Syy*(-Sxxx-Sxyy) - Sxy*(-Sxxy-Syyy);

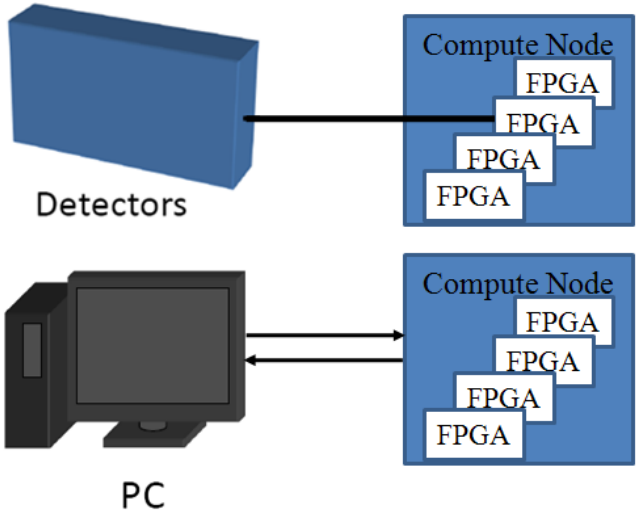


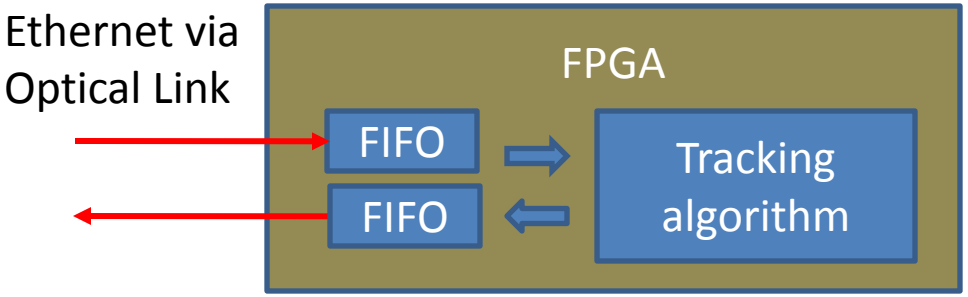
Pipelined, 4 clock cycles delay

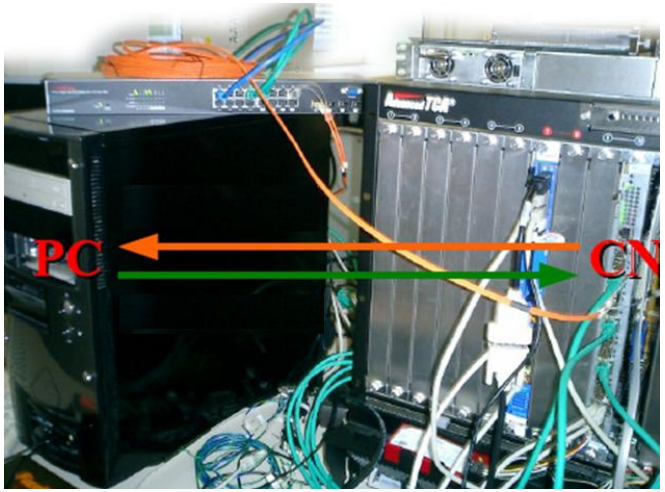
Setup and test

PC as data source and receiver.

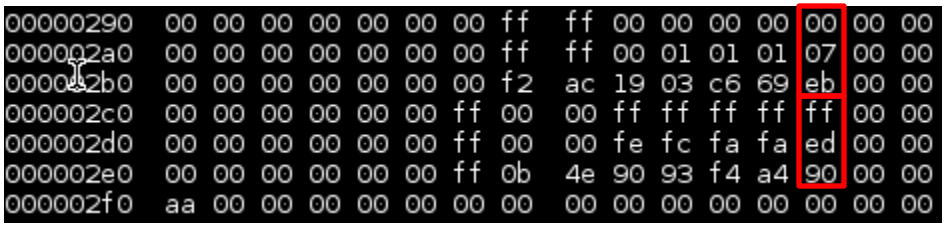
- Ethernet.
- Optical link (UDP by Grzegorz Korcyl) (not integrated yet)







Data Check



- Input package: 8-bit binary data
  00000000
  Flag bits: Bit 0,1
  01: head 00: body
  10: tail 11: invalid

- Output package: 8-bit binary data

x_c = a1/deta /(-2) := -71.48cm
y_c = b1/deta /(-2) := 106.32cm
R = sqrt(x_c^2+y_c^2) := 128.12cm

Device utilization Summary

Sitcp + Road finding + Momentum calculation

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	9,258	50,560	18%
DCM autocalibration logic	14	9,258	1%
Number of 4 input LUTs	18,291	50,560	36%
DCM autocalibration logic	8	18,291	1%
Number of occupied Slices	12,890	25,280	50%
Number of Slices containing only related logic	12,890	12,890	100%
Number of Slices containing unrelated logic	0	12,890	0%
Total Number of 4 input LUTs	18,832	50,560	37%

A: Only Sitcp B: Sitcp + momentum calculation module
C: Sitcp + Road finding + Momentum calculation

	A	B	C
Number of Slice Flip Flops :	9%	11%	18%
Number of occupied Slices:	14%	19%	50%

Summary and Outlook

- One new algorithm is studied, and looks promising.

  Road finding: Not all done yet

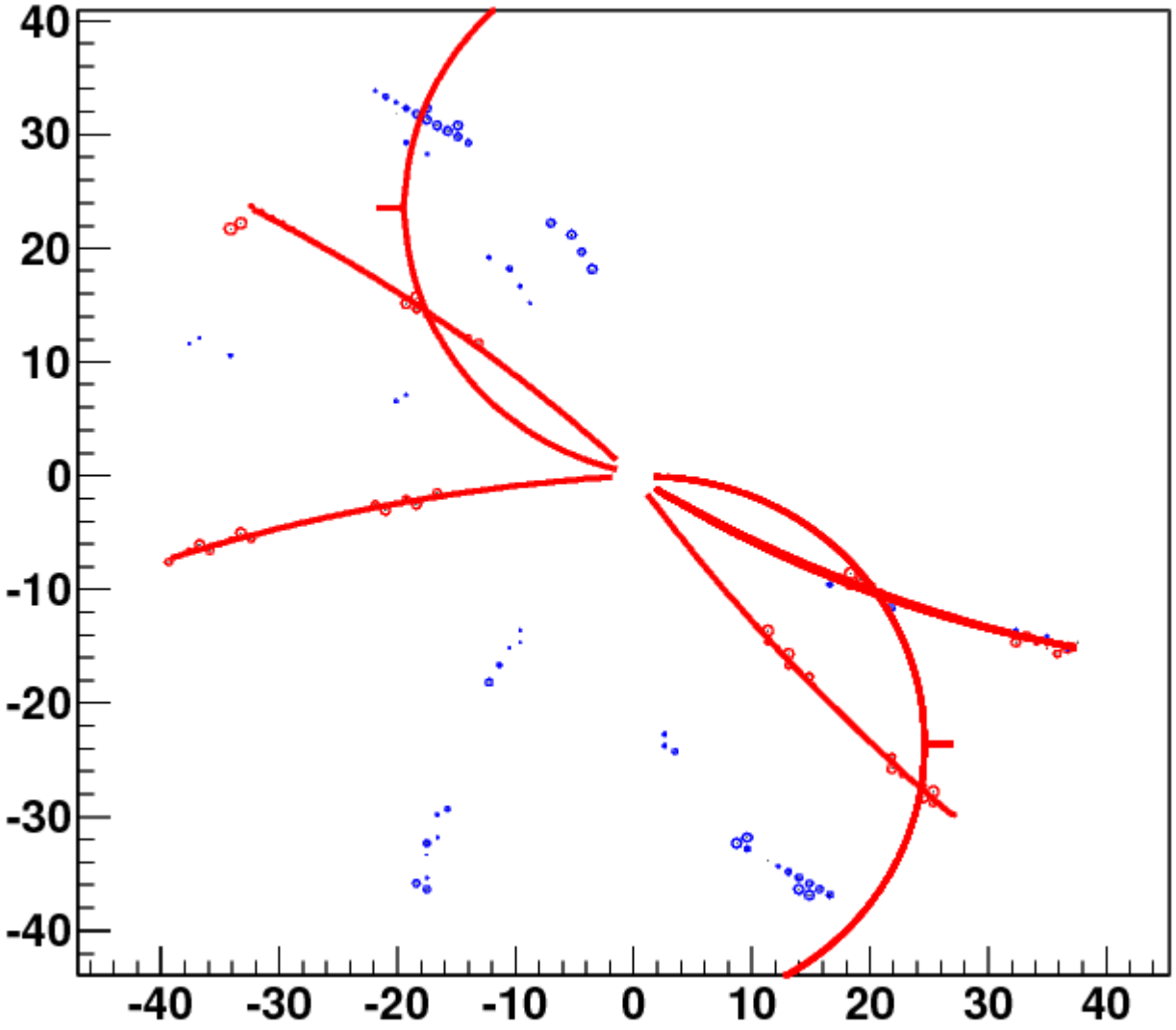
  Momentum calculation: small, fast, precise.

Next to do:

- Finish the road finding part.

Thank you

Calculation of circle parameters



```
00000400  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00
*
00000490  00 01 02 03 04 05 06 07  00 00 00 00 00 00 00 00
000004a0  10 11 12 13 14 15 16 17  00 00 00 00 00 00 00 00
000004b0  1f 20 21 00 00 00 00 00  00 00 00 00 00 00 00 00
000004c0  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00
```

PANDA@20MHz. $2*10^7$ events/second

1 event: ~3 tracks/event * ~16 hits/track * ~ 2 (overlap factor) → ~100 hits/event

When dividing STT into 16 layers, ~6 hits/layers. 6*6*15 = 540 combinations

~1~2 clock cycles/combination. → 500~1000 clock cycles/event

If FPGA running at 100MHz, (500~1000)*10ns/ 50ns → 100~200 FPGA → 25~50 CN

(Only momentum calculation part)

Device utilization Summary

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	4,584	50,560	9%
DCM autocalibration logic	14	4,584	1%
Number of 4 input LUTs	4,245	50,560	8%
DCM autocalibration logic	8	4,245	1%
Number of occupied Slices	3,705	25,280	14%
Number of Slices containing only related logic	3,705	3,705	100%
Number of Slices containing unrelated logic	0	3,705	0%
Total Number of 4 input LUTs	4,776	50,560	9%

Number of Slice Flip Flops	5,869	50,560	11%
DCM autocalibration logic	14	5,869	1%
Number of 4 input LUTs	5,963	50,560	11%
DCM autocalibration logic	8	5,963	1%
Number of occupied Slices	5,023	25,280	19%
Number of Slices containing only related logic	5,023	5,023	100%
Number of Slices containing unrelated logic	0	5,023	0%
Total Number of 4 input LUTs	6,500	50,560	12%

Number of Slice Flip Flops	9,258	50,560	18%
DCM autocalibration logic	14	9,258	1%
Number of 4 input LUTs	18,291	50,560	36%
DCM autocalibration logic	8	18,291	1%
Number of occupied Slices	12,890	25,280	50%
Number of Slices containing only related logic	12,890	12,890	100%
Number of Slices containing unrelated logic	0	12,890	0%
Total Number of 4 input LUTs	18,832	50,560	37%