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SODANET Specifications

And Current Status of the Implementation

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SODANET

Design considerations:

- Preserve readout topology as defined in the PANDA TPR
- Reuse as much as possible code of the TRBNET
- Key changes of the TRBNET compatible with the CBMNET protocol

Note on the synchronous optical link vith TRB boards:

Tested by Jan Michel and Michael Traxler (January 16):

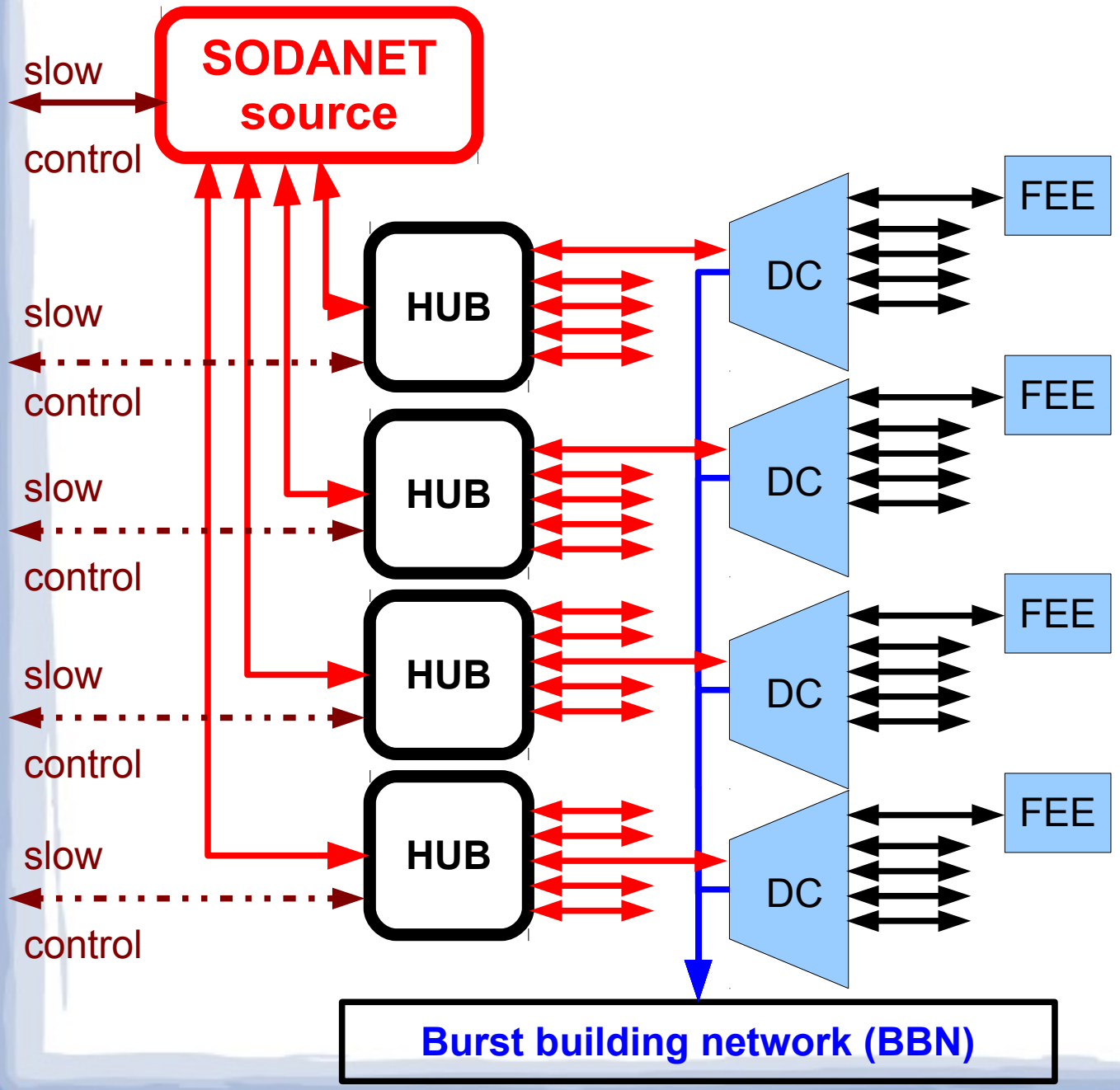
- Synchronous connection works for TRB V3
- First recovery of a clock: 30 ps jitter (10 ps from oscilloscope)
- 6 recoveries in chain: 40 ps jitter

SODANET Functionality

SODANET provides:

- synchronization of the FEE
- Continuous monitoring of the DC/FEE functionality
- Rough (initial) time calibration of the propagation time of the synchronization signal
- Transfer of a slow-control (FEE configuration/status) information: low priority, transmission of a slow-control package can be interrupted at any time by a synchronization package

SODANET Topology



SODANET link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization information and FEE configuration
  - DC → source: slow control, used for time calibration

Data link (DC → BBN):

- Unidirectional Ethernet

Link DC ↔ FEE:

- Bidirectional, synchronous
- Protocol up to subsystem

SODANET Synchronous Packages

SODANET protocol foresees two types of sync. packages:

- Command data: issued at any time
- Super-burst start (**super burst = 16 bursts of 2.4 μs**): issued at the beginning of each Super-burst

Package structure

K (FB)	Data 31-24	K (FB)	Data 23-16	K (FB)	Data 15-8	K (FB)	Data 7-0

Command package:

- Bit 31: 0
- Bit 30: Time calibration
- Bit 29: DAQ start
- Bit 28: DAQ stop
- Bit 27: Reset
- Bits 26-8: reserved
- Bits 7-0: CRC checksum (CRC8-CCITT)

Super-burst start package:

- Bit 31: 1
- Bits 30-0: Super-burst number

Synchronous Packages

- Have highest priority (interrupt any other transfer)
- Each received SODANET packed – acknowledged:
  continuous monitoring of the readout
  - Malfunction of one of the DC/FEE → trigger slow control;
    the malfunction DC – added to the list of non-uses recipients

- Burst counting (within Super-burst) – at each DC
  Error handling:
  - DC checks if received super-burst number is sequential
  - In case of error:
    - the DC uses number distributed by the SODANET,
    - set special error bit in the output data,
    - informs slow-control system
  - If part of SODANET message is missing:
    - DC uses super-burst number from a local counter,
    - reports problem to the slow-control system.

Time Calibration

- Dedicated “time calibration” command is defined
- Once the command is received:
  - reply sent to the transmitter side,
  - original message is forwarded further through the network.
- Propagation time:
  - calculated at the transmitter side
  - stored in a register
  - the register values – read out by a slow control system.
- The delay data – used to pre-calculate signal-propagation delays (~10 ns precision)
- Delay values – used at the DC to delay SODANET-synchronisation signals, before redistribution to FEE.
- The longest delay value – used by the SODANET source to **send synchronisation commands prior to a bunch crossing**

“Triggered” Mode

Compatibility mode of operation

- External “trigger” signal is feed to one of the DC/SODANET source
- “trigger” is timestamped, and sent to the burst-building network
- Event builder will select only hits with timestamps, which are in coincidence with the “trigger” signal

DC Output Data-format

- DC can start transmitting FEE data once it is available
  (without waiting till the end of a super-burst)
- If no data are available –
  DC sends an empty package at the end of the Super-burst

Data-package

31 16	15 0
last-packet flag; packet number	data size in bytes
Not used (same as HADES)	Not used (same as HADES)
Status and error	System ID
Super-burst number	
Data	

GbE paket builder in FPGA (HADES) can be reused to pack data

SODANET
Implementation status

- ✔ Cleaned-up SODANET VHDL repository (files, relevant only for the SODANET)
  - ✔ Implemented synchronous transmission at 100 MHz on the main and preferential FPGAs of a TRB board [hardware test]
- ✔ SODANET source
- ✔ SODANET Hub
- ✔ SODANET endpoint (hub/DC)
- ✔ Interface of the SODANET to the TRB slow control
- ✔ Feedback handler (time calibration, monitoring)
- ➔ Tests with hardware
- ➔ Incorporate SODANET endpoint to subsystems DCs
- ➔ Implement link to compute node
- • Fix synchronous-transmission frequency at 77.76 MHz
  (design does not work jet at 125 MHz)

TRB v3 as Data Concentrator

Advantages:

- Possibility of different configurations of the readout system

Disadvantages:

- Low optical-fibre speed:
  - max 3.2 Gb/s in asynchronous mode
  - max 2.5 Gb/s in synchronous mode
  - 4 SFPs are connected to a single quad-serdes – have to use same frequency
  - In case of usage of all FPGAs for the DC there might be problems with Ethernet connection (mandatory for the TRB) due to non-standard frequency

In case of usage of the SODANET frequency of 154.52 MHz:

- Maximum link speed for SODANET with TRBv3 is 1.54 Gb/s – might be too slow for the front-end
- Connection to compute node has to be at 3.08 MHz

Solution: – new hardware (required for the final version)
– usage of a standard frequenty

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Thank you for your attention!

Time-Synchronisation: Requirements

… To be precisely defined

- **Desired**:
  - Distribution of clock (154.52 SONET standard)
  - Distribution of synchronisation commands (Start, Stop, Calibration light-flash, etc.)
  - Acceptable jitter:
    - < 20 ps (TOF, DIRC)
    - < 100 ps (EMC)
    - < 200 ps (STT, MWD, etc.)
  - Signal distributed over an optical fibre

- **Optional**:
  - Measurement of a signal-propagation time (cable length)
  - Distribution of detector-configuration data
  - Configuration of the burst-building network
  - Slow control for small subsystems