

Status of the MVD Strip ASIC

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June 24th, 2013
PANDA Meeting, GSI Darmstadt

- Concept for MVD strip ASIC
 - Features of TOFPET ASIC
- Planned modifications
 - Current work
 - Radiation hardening
- Conclusion / Outlook

The MVD Strip ASIC...

- What to use for the MVD strip readout?

Existing ASIC

- + (almost) no development
- ASIC has to be available
- specifications maybe not matched completely

Modified existing ASIC

- + reduced development
- + adjustable to needs
- basis has to be available
- specifications maybe exaggerated

New development

- + matches needs
- + optimized for purpose
- much development

The MVD Strip ASIC...

- What to use for the MVD strip readout?

Existing ASIC

- + (almost) no development
- ASIC has to be available
- specifications maybe not matched completely

no suitable ASIC found

Modified existing ASIC

- + reduced development
- + adjustable to needs
- basis has to be available
- specifications maybe exaggerated

New development

- + matches needs
- + optimized for purpose
- much development

not enough time / developers

TOFPET ASIC
as basis

The TOFPET ASIC



Combined TOF-PET (200 ps time resolution), ultrasound imaging and endoscopic biopsy

PET components:

- dSiPM/crystal endoscopic probe
- aSiPM/crystal external plate

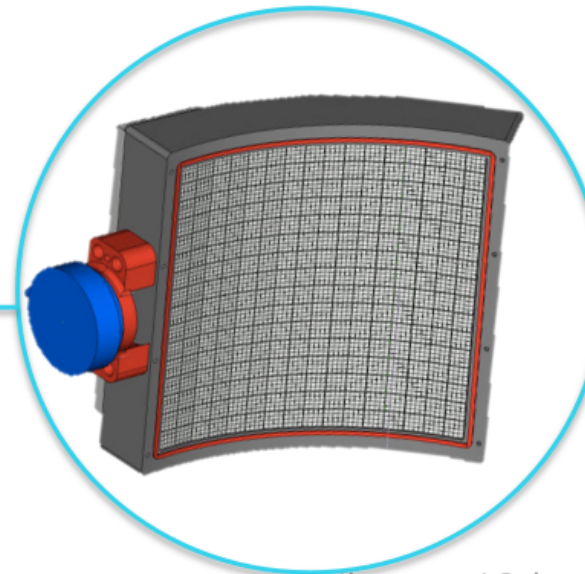
Development by:

- LIP Lisbon
- INFN Torino

© DESY / Stuhmann



ENDO TOFPET US
Endoscopic TOFPET & Ultrasound



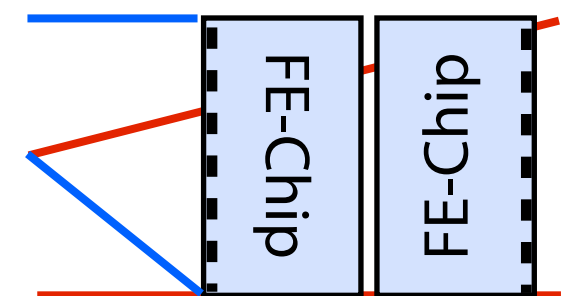
The TOFPET ASIC in detail

- Digitalization of signal with time of flight
 - high time resolution
 - low power consumption
- Only amplifier, capacitors and thresholds analogue
 - logic controls:
 - Charging, reset of capacitors
 - Threshold → timestamp
 - Common backend
 - flexible to adaptations

Parameter	TOFPET	MVD TDR
Number of channels	64	128
Channel pitch	102 μm	50, 65, 67 μm
Clock frequency	80-160 MHz	155,65 MHz
Power	8.7 mW/ch *	< 8 mW/ch
TDC time binning	50 ps	< 20 ns
Max. input hit rate	~ 300 kHz	40 kHz
Deadtime	~ 3 μs	< 6 μs

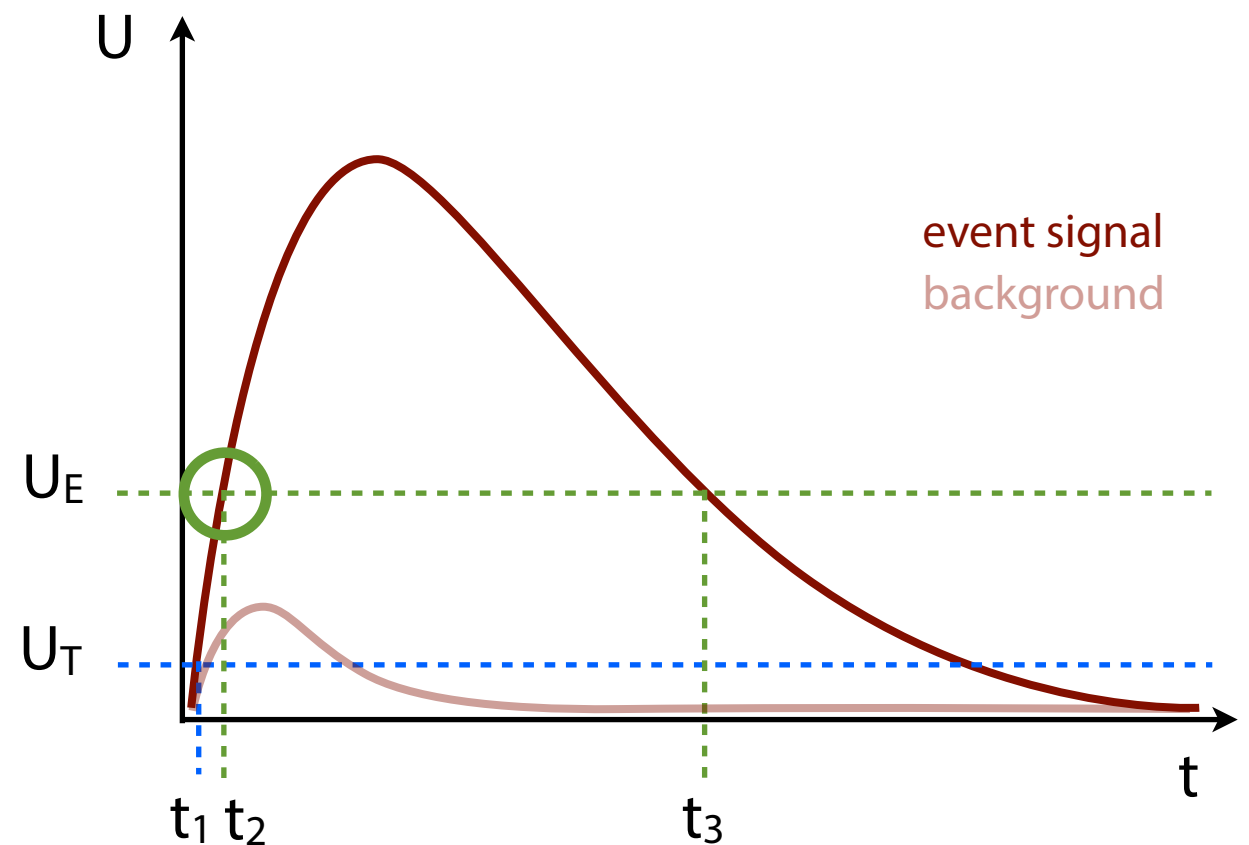
* powered two amplifiers per channel

Solution for higher channel pitch:



Function principle of TOFPET ASIC

- Two TDCs per channel
 - **time** and **energy**
(**low** and **high** threshold)
 - energy trigger (t_2)
validates time trigger (t_1)
- Charge with time-over-threshold
 - ToT meas.: $t_3 - t_1$
 - time binning: 50 ps

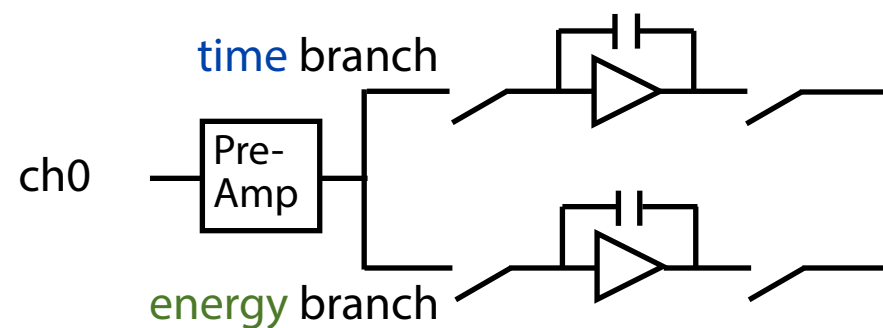


Structure for TOFPET ASIC

Analogue Frontend

Channel logic

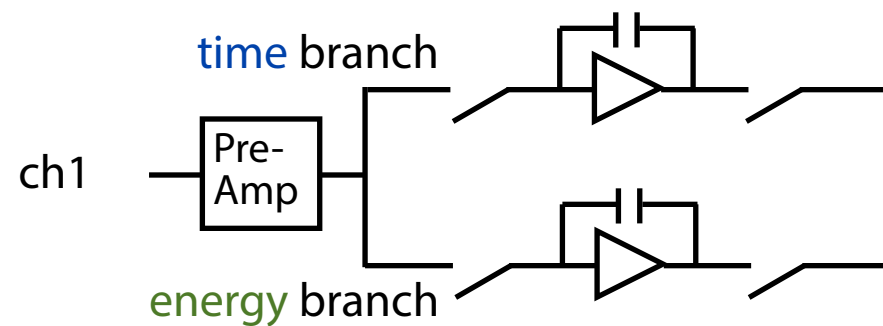
End of channel logic



TDC

TDC

local data
register



TDC

TDC

local data
register

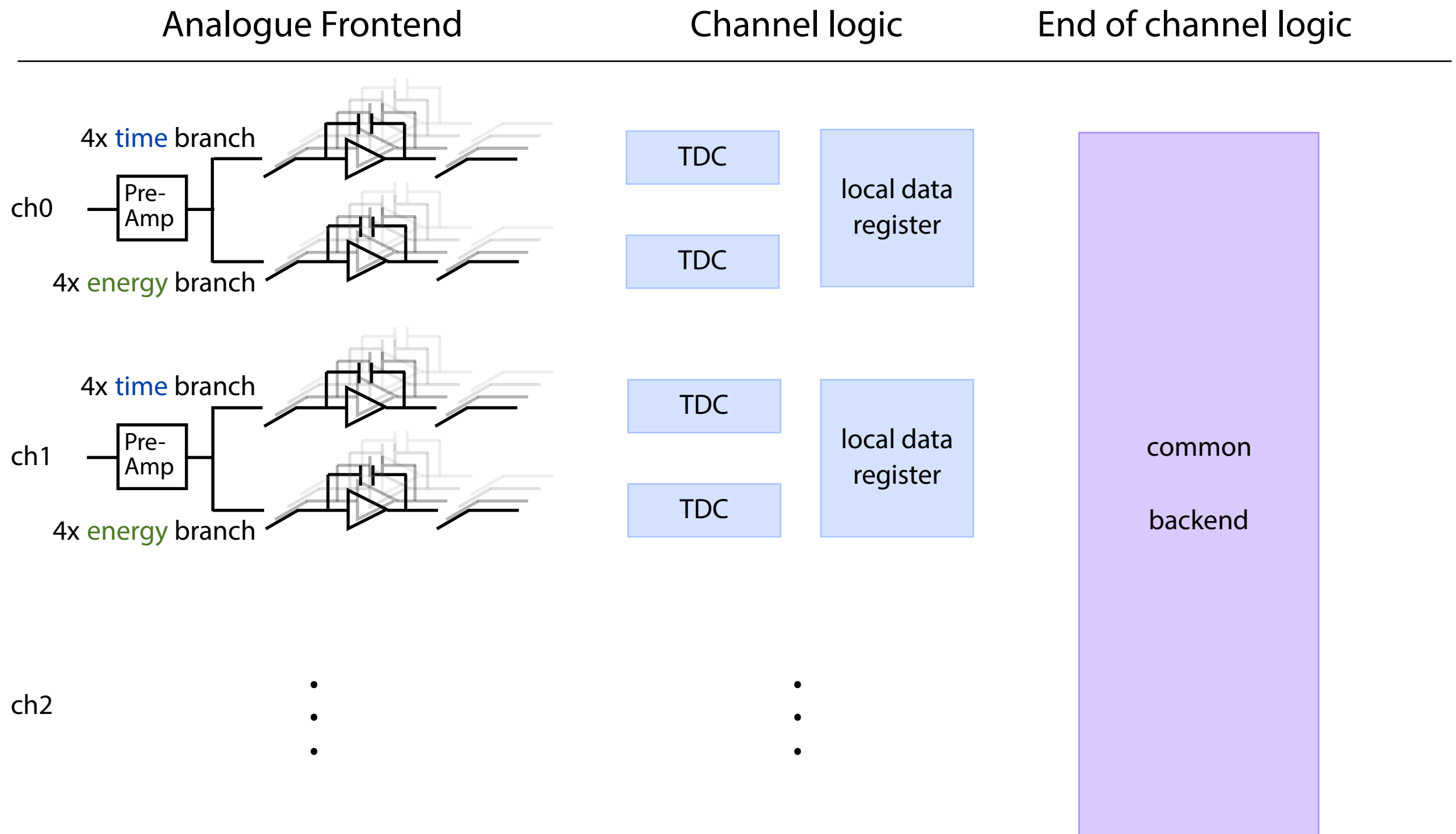
ch2

•
•
•

•
•
•

common
backend

Structure for TOFPET ASIC



Planned modifications to MVD strip ASIC

- Improve general functionality
 - Bugs, recalibration of capacitors, placement of digital part, ...
- Radiation hardening
 - Protect logic from single event upsets
- Change technology (IBM 130 nm → UMC 110 nm)
 - Supported by Europractice
 - Cost effective
- Adapt resolution and rate capability
 - Reduce clock speed (→ saves power)
 - Reduce time resolution (→ less data)

constantly
ongoing

TDC ctrl: almost
Backend: next

next step

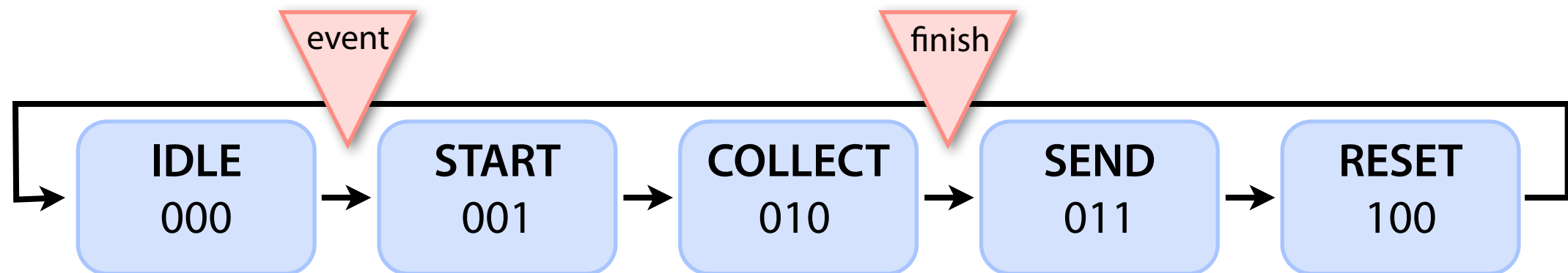
future

Types of radiation damage

- Charge deposition in electronics can lead to:
- Hard errors
 - Destruction of gates
 - Permanent damage
- Soft errors
 - Effect only temporary
 - Single Event Upset (SEU)
 - Change a value inside a flip flop (buffer)

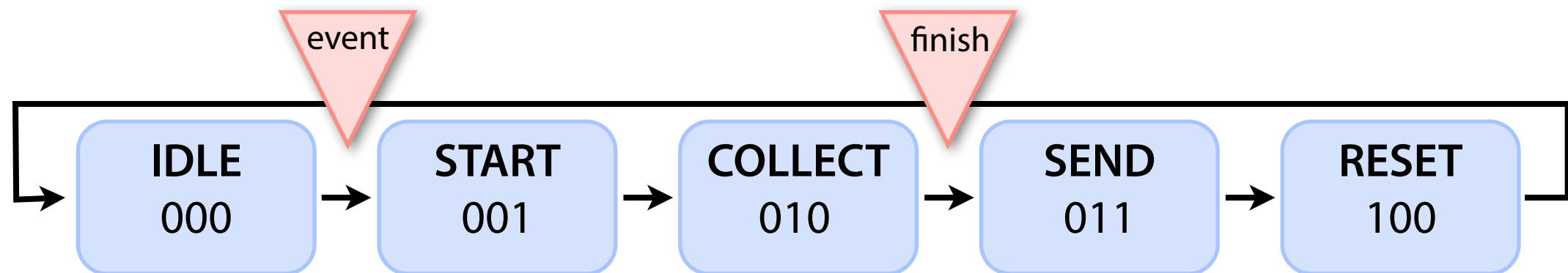
Single Event Upset

- *Example:* a fictional readout control
- Normal operation



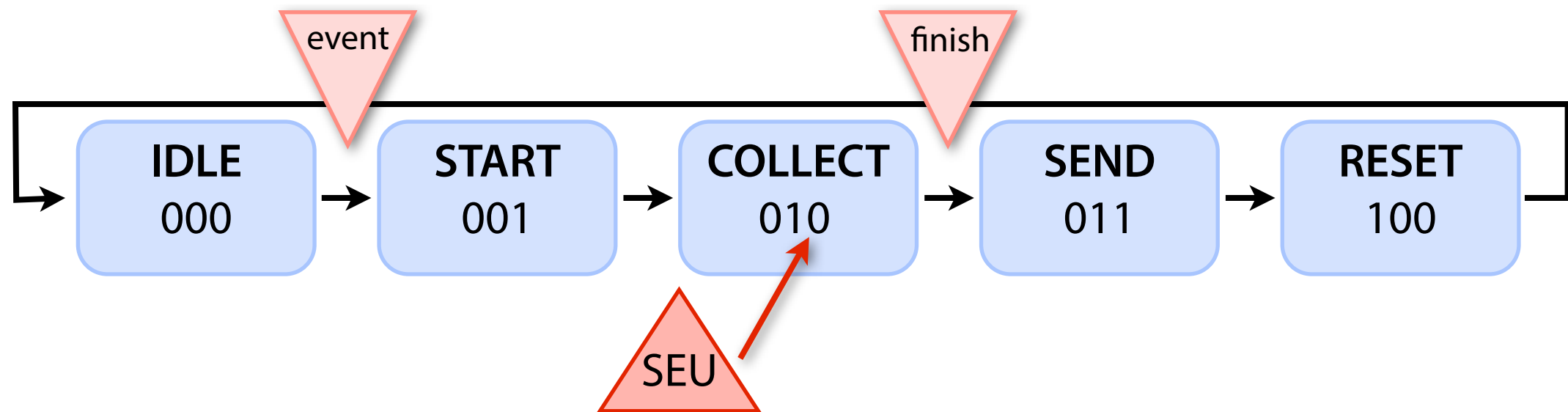
Single Event Upset

- *Example:* a fictional readout control
- **Radiation** environment



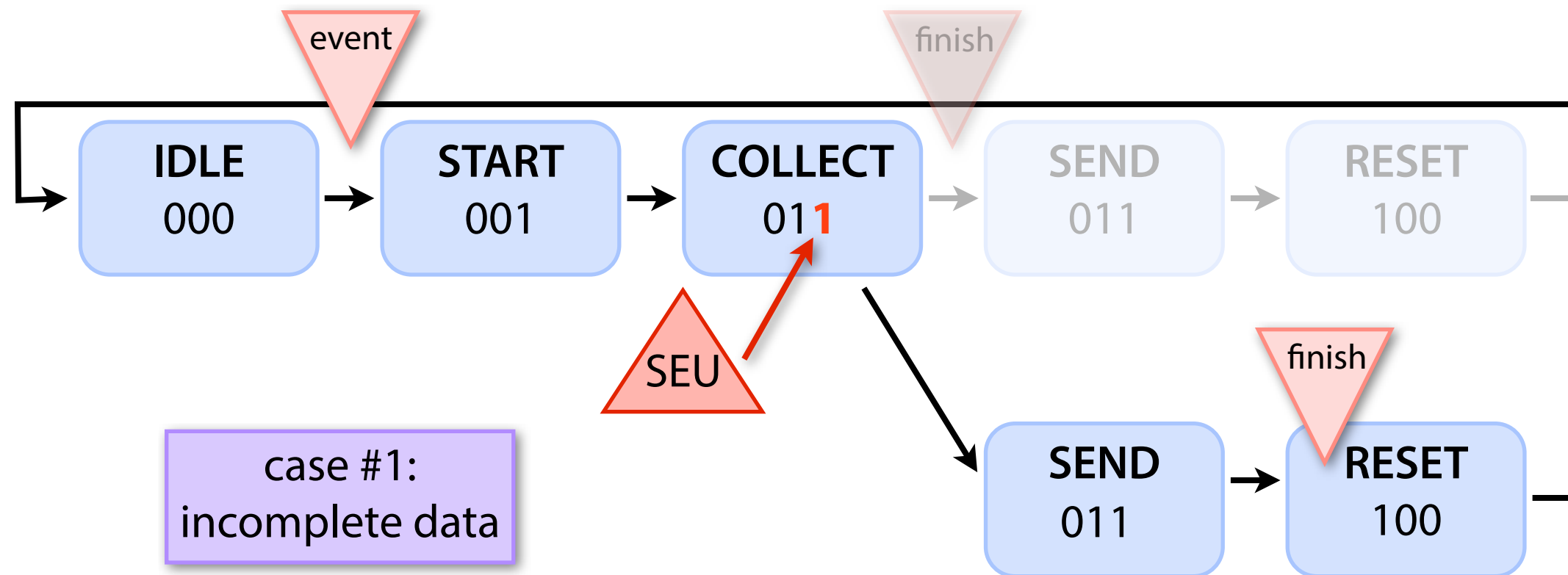
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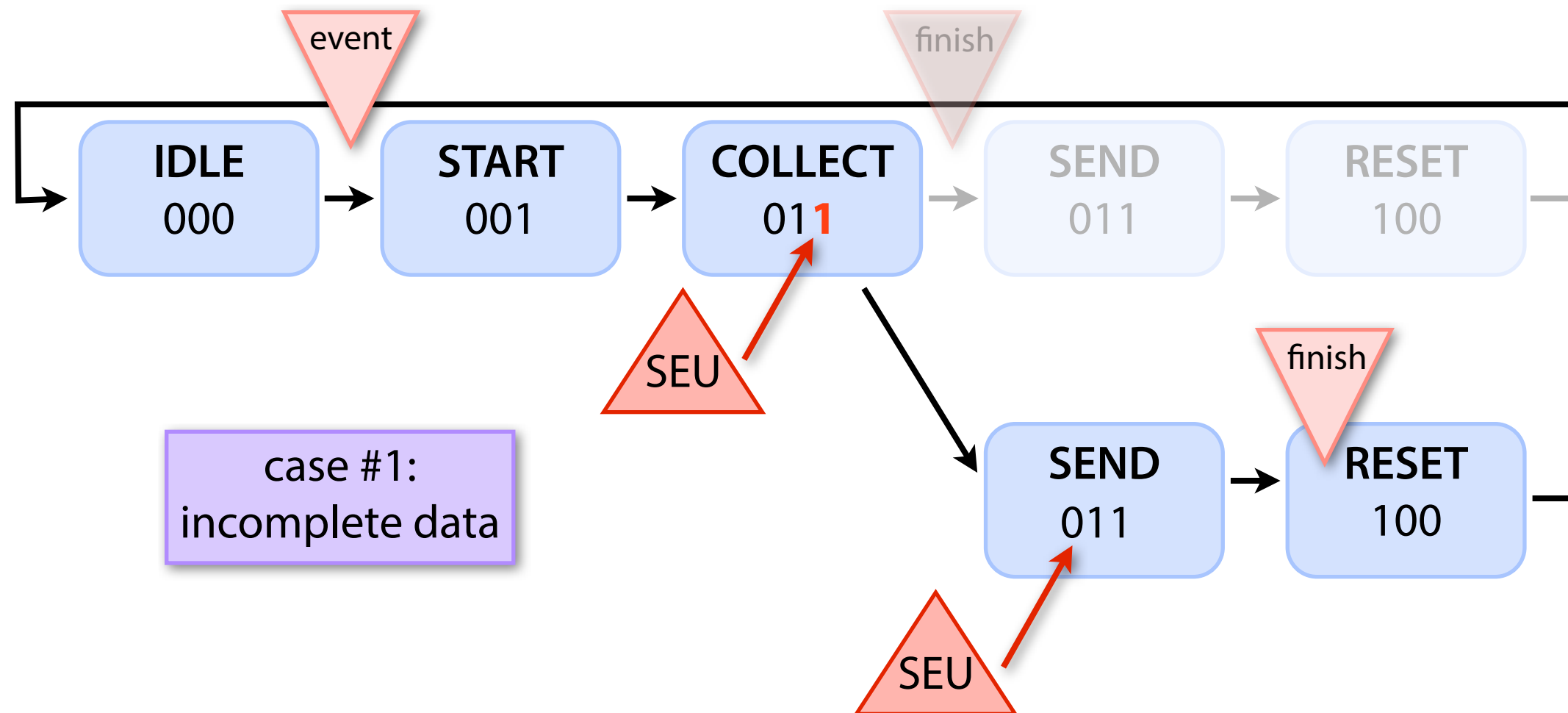
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- *Example:* a fictional readout control
- **Radiation** environment



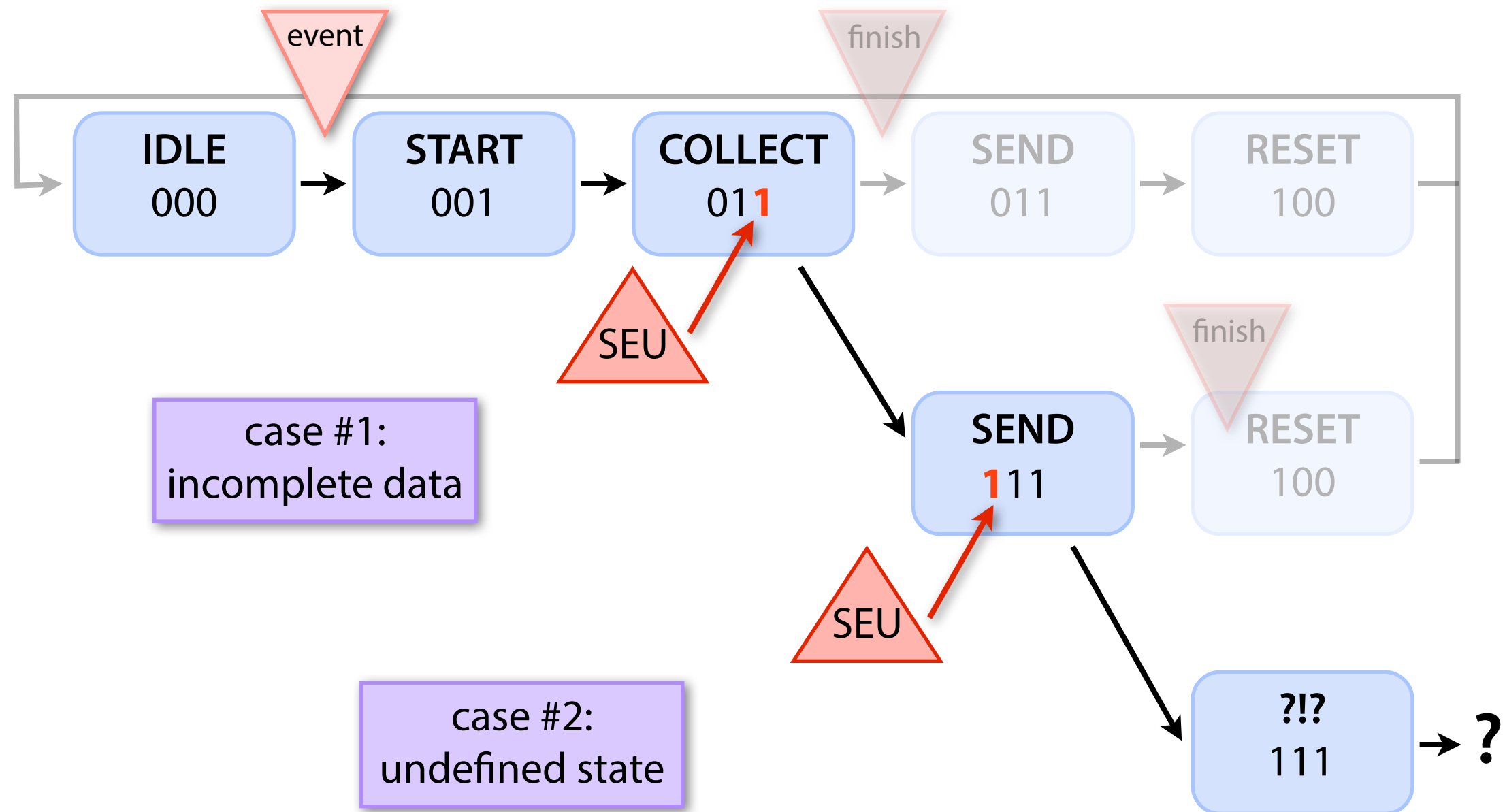
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- *Example:* a fictional readout control
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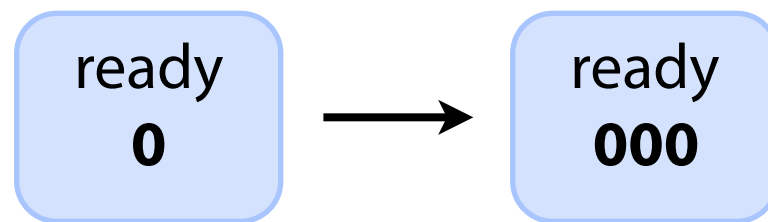
Single Event Upset

- *Example:* a fictional readout control
- **Radiation** environment



Prevent logic freeze

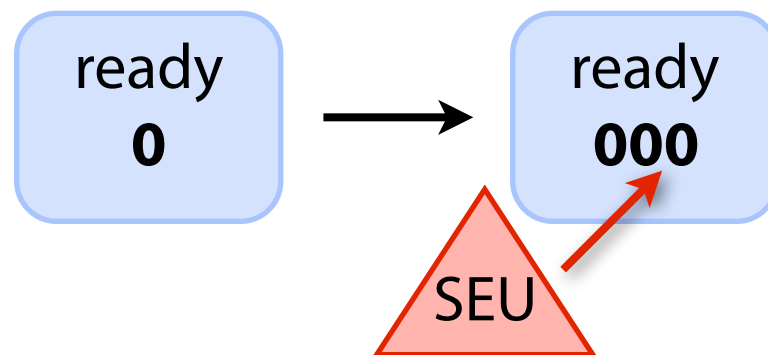
- Single bit:
 - Triple Mode Redundancy (TMR)



MVD Strip ASIC
Single bit FF: 140
TMR protected: 30

Prevent logic freeze

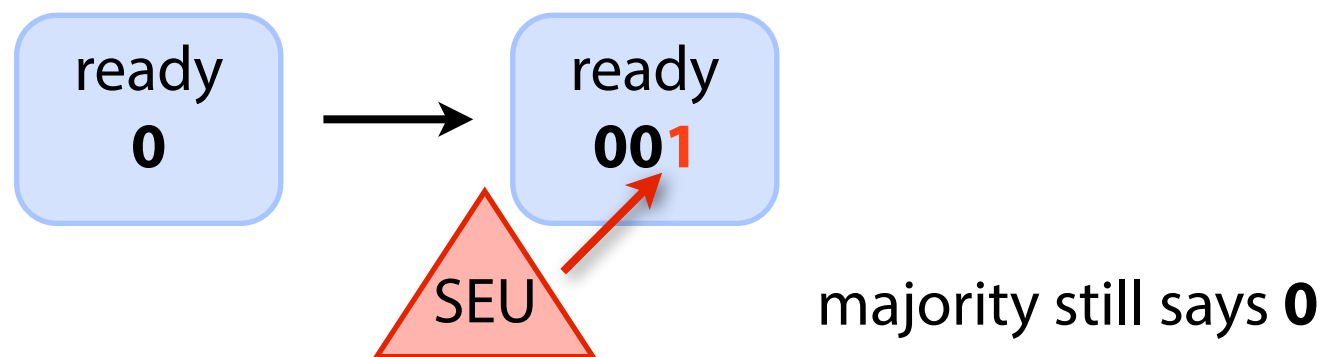
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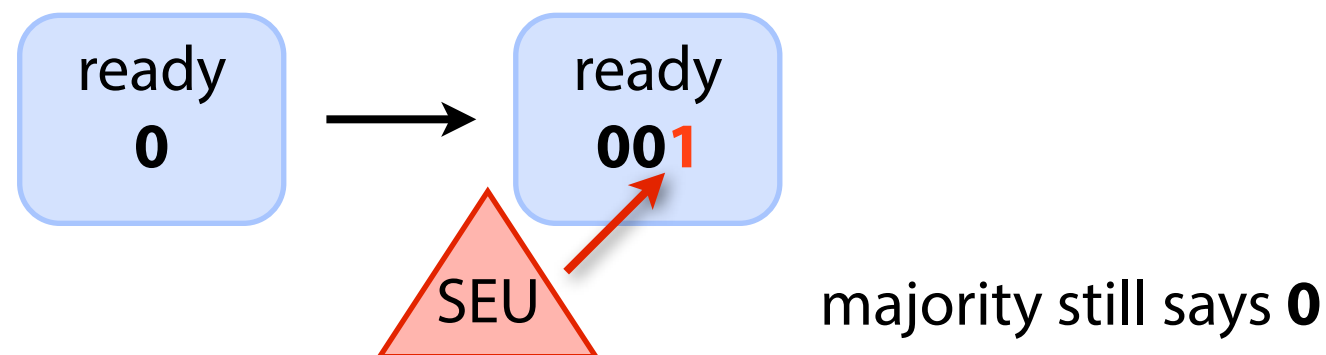
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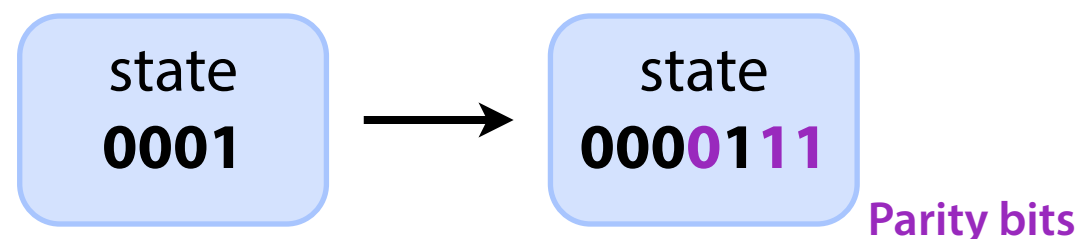
Prevent logic freeze

- Single bit:
 - Triple Mode Redundancy (TMR)



MVD Strip ASIC
Single bit FF: 140
TMR protected: 30

- Multiple bits (e.g. state machine):
 - Hamming encoded states



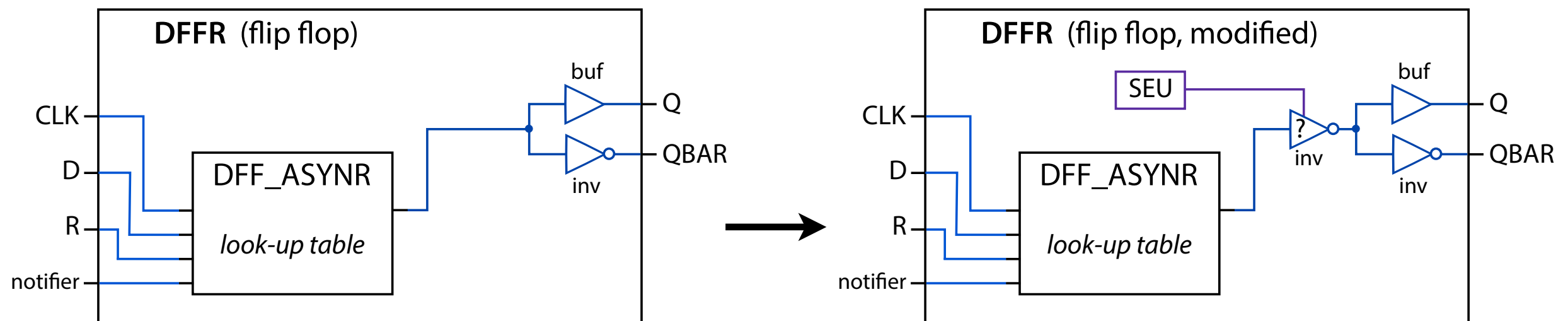
MVD Strip ASIC
Multiple bit FF: 320
Hamming protected: 133
(state machines: 100)

- additional parity bits to detect and correct SEU

- Protection of data inside the chip too expensive (area, power)
 - 5 times 10 bit timestamp buffers per channel
 - Hamming encoding: 20 additional bits + correction logic
- Detection of SEU desirable
 - Simple check: parity bit
 - even # of 1: parity 0
 - odd # of 1: parity 1
 - SEU: mismatch between data & parity
 - Implementation easy (xor) and small

data	→	data + parity
000101	→	000101 0
001101	→	001101 1

- Step 1: Ability to simulate a SEU
 - Functions of development environment »Cadence«
 - nc_force: forces a signal inside the logic to a given value
 - nc_release: releases a previous force
 - Problem: flip flop in simulation without internal memory
 - Flipped value in input wire
 - Modified standard cell library



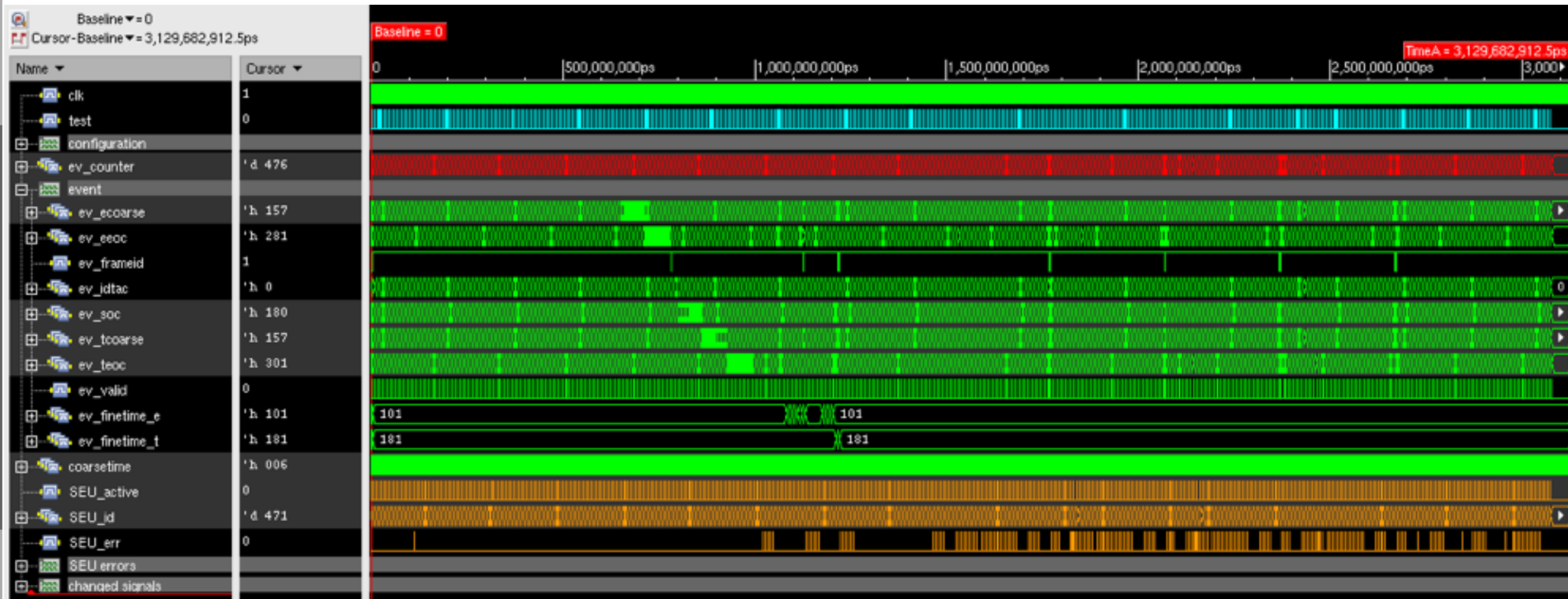
- ```

118 -- get a FLI flop name and path by its
119 function getFlipFlop (n : in Integer; seu_FF : in std_logic := '0')
120 return string is
121 begin
122 if seu_FF = '1' then
123 -- the variant with the modified std_cell, that has a SEU flag inside the FF
124 case n is
125 when 0 => return "rlast_TDC_CTRL_top.seu0_buf_Q_reg.18.SEU";
126 when 1 => return "rlast_TDC_CTRL_top.seu1_buf1_Q_reg.18.SEU";
127 when 2 => return "rlast_TDC_CTRL_top.seu2_buf2_Q_reg.18.SEU";
128 when 3 => return "rlast_TDC_CTRL_top.seu3_buf3_Q_reg.18.SEU";
129 when 4 => return "rlast_TDC_CTRL_top.seu4_gen_Q_reg.18.SEU";
130 when 5 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.falsehit_buf_Q_reg.18.SEU";
131 when 6 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.falsehit_buf1_Q_reg.18.SEU";
132 when 7 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.falsehit_buf2_Q_reg.18.SEU";
133 when 8 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.falsehit_buf3_Q_reg.18.SEU";
134 when 9 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.falsehit_gen_Q_reg.18.SEU";
135 when 10 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.validhit_buf_Q_reg.18.SEU";
136 when 11 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.validhit_buf1_Q_reg.18.SEU";
137 when 12 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.validhit_buf2_Q_reg.18.SEU";
138 when 13 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.validhit_buf3_Q_reg.18.SEU";
139 when 14 => return "rlast_TDC_CTRL_top.det_async_hitvalidation.validhit_gen_Q_reg.18.SEU";
140 when 15 => return "rlast_TDC_CTRL_top.det_coarsereg.mc_buf_Q_reg.18.SEU";
141 when 16 => return "rlast_TDC_CTRL_top.det_coarsereg.test_buf_Q_reg.18.SEU";
142 when 17 => return "rlast_TDC_CTRL_top.det_coarsereg.SIU_err_state_reg.18.SEU";
143 when 18 => return "rlast_TDC_CTRL_top.det_coarsereg.VAC_ID_buf_reg[0] .18.SEU";
144 when 19 => return "rlast_TDC_CTRL_top.det_coarsereg.VAC_ID_buf_reg[1] .18.SEU";
145 when 20 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[0] .18.SEU";
146 when 21 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[1] .18.SEU";
147 when 22 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[2] .18.SEU";
148 when 23 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[3] .18.SEU";
149 when 24 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[4] .18.SEU";
150 when 25 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[5] .18.SEU";
151 when 26 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[6] .18.SEU";
152 when 27 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[7] .18.SEU";
153 when 28 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[8] .18.SEU";
154 when 29 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_08_reg[9] .18.SEU";
155 when 30 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[0] .18.SEU";
156 when 31 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[1] .18.SEU";
157 when 32 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[2] .18.SEU";
158 when 33 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[3] .18.SEU";
159 when 34 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[4] .18.SEU";
160 when 35 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[5] .18.SEU";
161 when 36 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[6] .18.SEU";
162 when 37 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[7] .18.SEU";
163 when 38 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[8] .18.SEU";
164 when 39 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_01_reg[9] .18.SEU";
165 when 40 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[0] .18.SEU";
166 when 41 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[1] .18.SEU";
167 when 42 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[2] .18.SEU";
168 when 43 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[3] .18.SEU";
169 when 44 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[4] .18.SEU";
170 when 45 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[5] .18.SEU";
171 when 46 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[6] .18.SEU";
172 when 47 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[7] .18.SEU";
173 when 48 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[8] .18.SEU";
174 when 49 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_02_reg[9] .18.SEU";
175 when 50 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[0] .18.SEU";
176 when 51 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[1] .18.SEU";
177 when 52 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[2] .18.SEU";
178 when 53 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[3] .18.SEU";
179 when 54 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[4] .18.SEU";
180 when 55 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[5] .18.SEU";
181 when 56 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[6] .18.SEU";
182 when 57 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[7] .18.SEU";
183 when 58 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[8] .18.SEU";
184 when 59 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_03_reg[9] .18.SEU";
185 when 60 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_70_reg[0] .18.SEU";
186 when 61 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_70_reg[1] .18.SEU";
187 when 62 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_70_reg[2] .18.SEU";
188 when 63 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_70_reg[3] .18.SEU";
189 when 64 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_70_reg[4] .18.SEU";
190 when 65 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_70_reg[5] .18.SEU";
191 when 66 => return "rlast_TDC_CTRL_top.det_coarsereg.coarse_buf_70_reg[6] .18.SEU";

```

# Result of SEU tests

- Test of all 460 flip flops:



- No logic freeze
- Only corrupted data (→ parity bit)

# Name of MVD strip ASIC

- But how should we name it?
- My suggestion:  
PASTA – **P**anda **S**trip **A**SiC
- Robert's suggestion:  
STRATOS – **S**trip **A**SiC **T**orino **S**olution
- Other ideas?

- TOFPET ASIC as basic for MVD strip readout
- Modification in progress
  - Radiation hardening almost complete
  - Switch to different technology soon
- Further modifications for PANDA needs
  - Save more power and data
- We need a name...

- TOFPET ASIC as basic for MVD strip readout
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## Thank you!

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# Backup

# Pamareter comparison

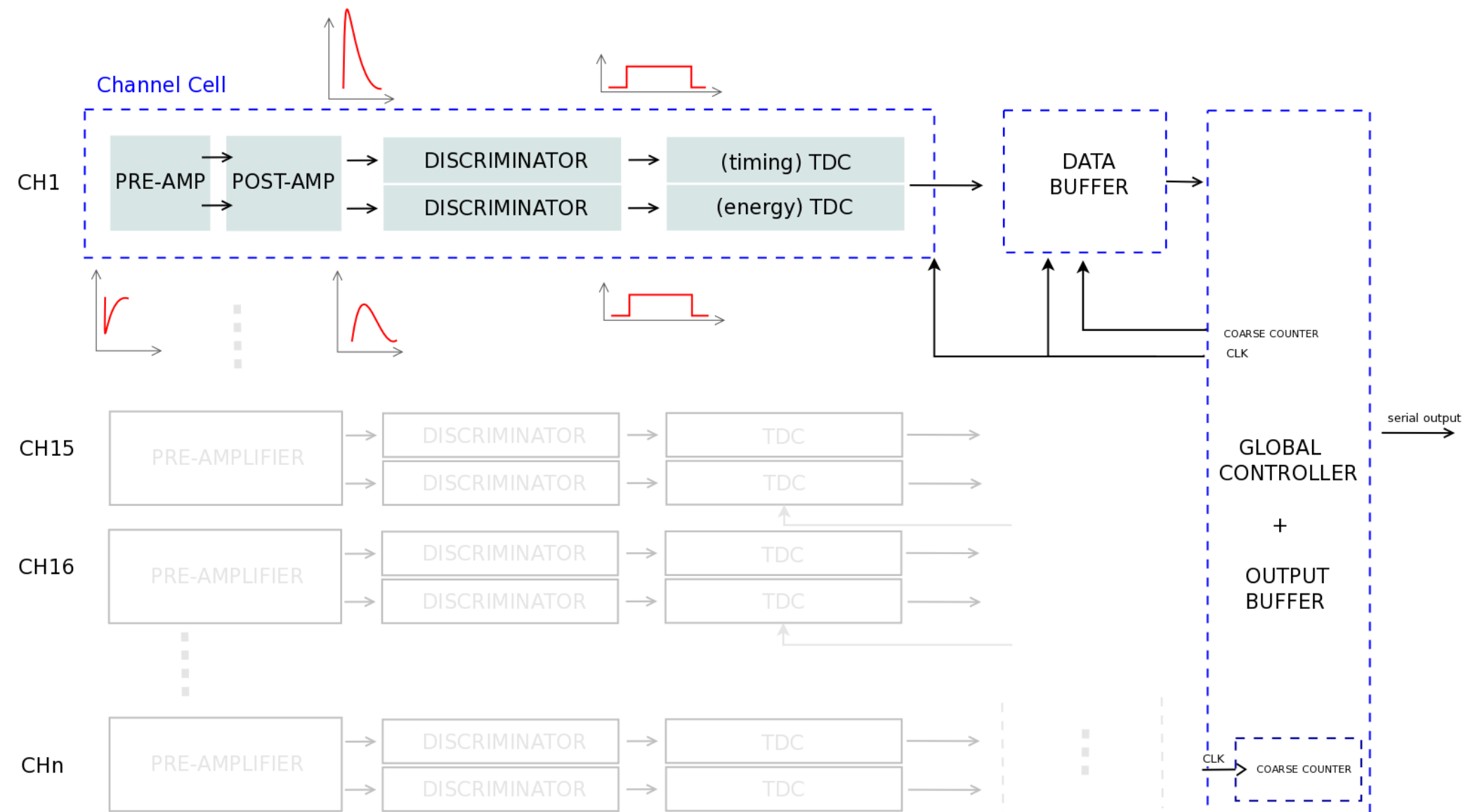
## TOFPET

| Parameter                            | Value                                  |
|--------------------------------------|----------------------------------------|
| Number of channels                   | 64                                     |
| Clock frequency                      | 80 – 160 MHz                           |
| <b>Dynamic range of input charge</b> | <b>300 pC</b>                          |
| SNR ( $Q_{in} = 100$ fC)             | > 20-25 dB                             |
| Amplifier noise (in total jitter)    | < 25 ps (FWHM)                         |
| <b>TDC time binning</b>              | <b>50 ps</b>                           |
| Coarse gain                          | $G_0, G_0/2, G_0/4$                    |
| Max. channel hit rate                | 100 kHz                                |
| Max. output data rate                | 320 Mb/s (640 w/ DDR)                  |
| Channel masking                      | programmable                           |
| <b>SiPM fine gain adjustment</b>     | <b>500 mV (5 bits)</b>                 |
| SiPM                                 | up to 320pF term. cap., 2MHz DCR       |
| Calibration BIST                     | internal gen. pulse, 6-bit prog. ampli |
| <b>Power</b>                         | <b>&lt; 10 mW per channel</b>          |

## MVD TDR

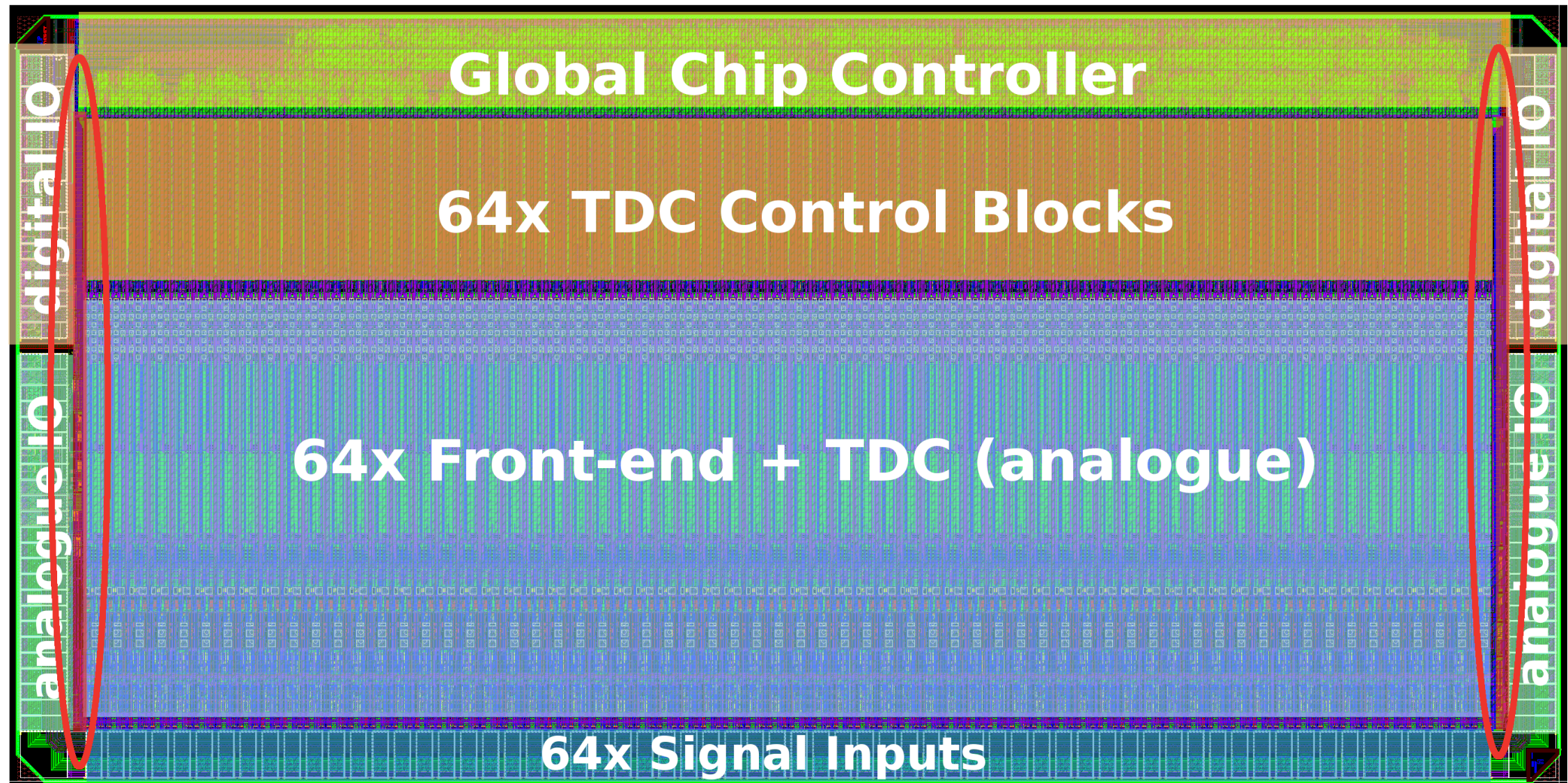
| Parameter                                     | Value                                                                                           | Remarks                                                                           |
|-----------------------------------------------|-------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| <b>Geometry</b>                               |                                                                                                 |                                                                                   |
| Width                                         | $\leq 8$ mm                                                                                     |                                                                                   |
| Depth                                         | $\leq 8$ mm                                                                                     |                                                                                   |
| Input pad pitch                               | $\approx 50$ $\mu$ m                                                                            |                                                                                   |
| Pad configuration                             | lateral pads occupied only for diagnostic functions, should be left unconnected for final setup |                                                                                   |
| Channels per front-end                        | $2^6 \dots 2^8$                                                                                 | default: 128 channels                                                             |
| <b>Input Compliance</b>                       |                                                                                                 |                                                                                   |
| Sensor capacitances,<br>Fully depleted sensor | $< 10$ pF<br>$< 50$ pF<br>$< 20$ pF                                                             | rect. short strips<br>rect. long strips (with ganging)<br>trapezoidal sensor      |
| Input polarity                                | either                                                                                          | selectable via slow control                                                       |
| Input ENC                                     | $< 800$ e <sup>-</sup><br>$< 1,000$ e <sup>-</sup>                                              | $C_{\text{sensor}} = 10$ pF<br>$C_{\text{sensor}} = 25$ pF                        |
| <b>Signal</b>                                 |                                                                                                 |                                                                                   |
| Dynamic range                                 | $240$ ke <sup>-</sup> ( $\approx 38.5$ fC)                                                      |                                                                                   |
| Min. SNR for MIPS                             | 12                                                                                              | 22,500 e <sup>-</sup> for MIPS in 300 $\mu$ m silicon, guaranteed within lifetime |
| Peaking time                                  | $\approx 5 \dots 25$ ns                                                                         | typical Si drift times                                                            |
| Digitisation resolution                       | $\geq 8$ bits                                                                                   |                                                                                   |
| <b>Power</b>                                  |                                                                                                 |                                                                                   |
| Overall power dissipation                     | < 1 W                                                                                           | assuming 128 channels per front-end                                               |
| <b>Dynamical</b>                              |                                                                                                 |                                                                                   |
| Trigger                                       | internally generated                                                                            | when charge pulse exceeds adjustable threshold value                              |
| Time stamp resolution                         | < 20 ns                                                                                         |                                                                                   |
| Dead time / ch                                | < 6 $\mu$ s                                                                                     | baseline restored to 1%                                                           |
| Overshoot recovery time / ch                  | < 25 $\mu$ s                                                                                    |                                                                                   |
| Average hit rates / ch                        |                                                                                                 | derived from simulations at a beam momentum of 15 GeV/c                           |
| (poissonian mean)                             |                                                                                                 |                                                                                   |
| Hot spots                                     | $9,000$ s <sup>-1</sup><br>$40,000$ s <sup>-1</sup>                                             | $\bar{p}p$<br>$\bar{p}Au$                                                         |
| Average occupancy                             | $6,000$ s <sup>-1</sup><br>$30,000$ s <sup>-1</sup>                                             | $\bar{p}p$<br>$\bar{p}Au$                                                         |
| <b>Interface</b>                              |                                                                                                 |                                                                                   |
| Slow control                                  | any                                                                                             | low pin count, e.g. I <sup>2</sup> C                                              |
| Data                                          | sparsified data                                                                                 |                                                                                   |

# TOFPET scheme



# TOFPET Layout

7.1 mm



Area:  $\sim 25\text{mm}^2$

# Hamming code

- Bit positions dividably by 2: parity bits
  - Rest: data bits
- Parity bits cover data bits, which have bit pos.  $2^p$  set

| Bit position      |    | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14  | 15  |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|-----|
| Encoded data bits |    | p1 | p2 | d1 | p4 | d2 | d3 | d4 | p8 | d5 | d6 | d7 | d8 | d9 | d10 | d11 |
| Parity bits       | p1 | X  |    | X  |    | X  |    | X  |    | X  |    | X  |    | X  |     | X   |
|                   | p2 |    | X  | X  |    |    | X  | X  |    |    | X  | X  |    |    | X   | X   |
|                   | p4 |    |    |    | X  | X  | X  | X  |    |    |    |    | X  | X  | X   | X   |
|                   | p8 |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X   | X   |