JÜLICH
FORSCHUNGSZENTRUM

panda

Status of the MVD Strip ASIC

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Outline

- Concept for MVD strip ASIC
  - Features of TOFPET ASIC
- Planned modifications
  - Current work
  - Radiation hardening
- Conclusion / Outlook

The MVD Strip ASIC…

- What to use for the MVD strip readout?

Existing ASIC	Modified existing ASIC	New development
+ (almost) no development – ASIC has to be available – specifications maybe not matched completely	+ reduced development + adjustable to needs – basis has to be available – specifications maybe exaggerated	+ matches needs + optimized for purpose – much development

The MVD Strip ASIC…

- What to use for the MVD strip readout?

Existing ASIC

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  develop
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no suitable ASIC found

Modified existing ASIC

+ reduced development
+ adjustable to needs
– basis has to be available
– specifications maybe exaggerated

New development

+ matches need
+ optimized
  purpos
– muc pment

not enough time / developers

TOFPET ASIC
as basis

The TOFPET ASIC

Combined TOF-PET (200 ps time resolution), ultrasound imaging and endoscopic biopsy

PET components:
- dSiPM/crystal endoscopic probe
- aSiPM/crystal external plate

Development by:
- LIP Lisbon
- INFN Torino

ENDO TOFPET US
Endoscopic TOFPET & Ultrasound

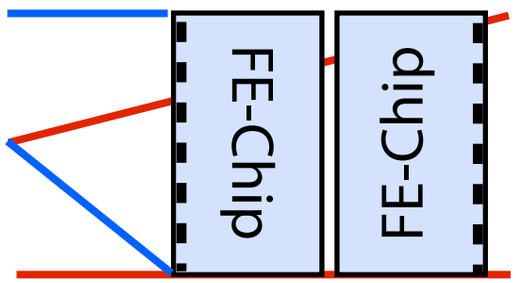
The TOFPET ASIC in detail

- Digitalization of signal with time of flight
  - high time resolution
  - low power consumption
- Only amplifier, capacitors and thresholds analogue
  - logic controls:
    - Charging, reset of capacitors
    - Threshold → timestamp
    - Common backend
  - flexible to adaptations

Parameter	TOFPET	MVD TDR
Number of channels	64	128
Channel pitch	102 µm	50, 65, 67 µm
Clock frequency	80-160 MHz	155,65 MHz
Power	8.7 mW/ch *	< 8 mW/ch
TDC time binning	50 ps	< 20 ns
Max. input hit rate	~ 300 kHz	40 kHz
Deadtime	~ 3 µs	< 6 µs

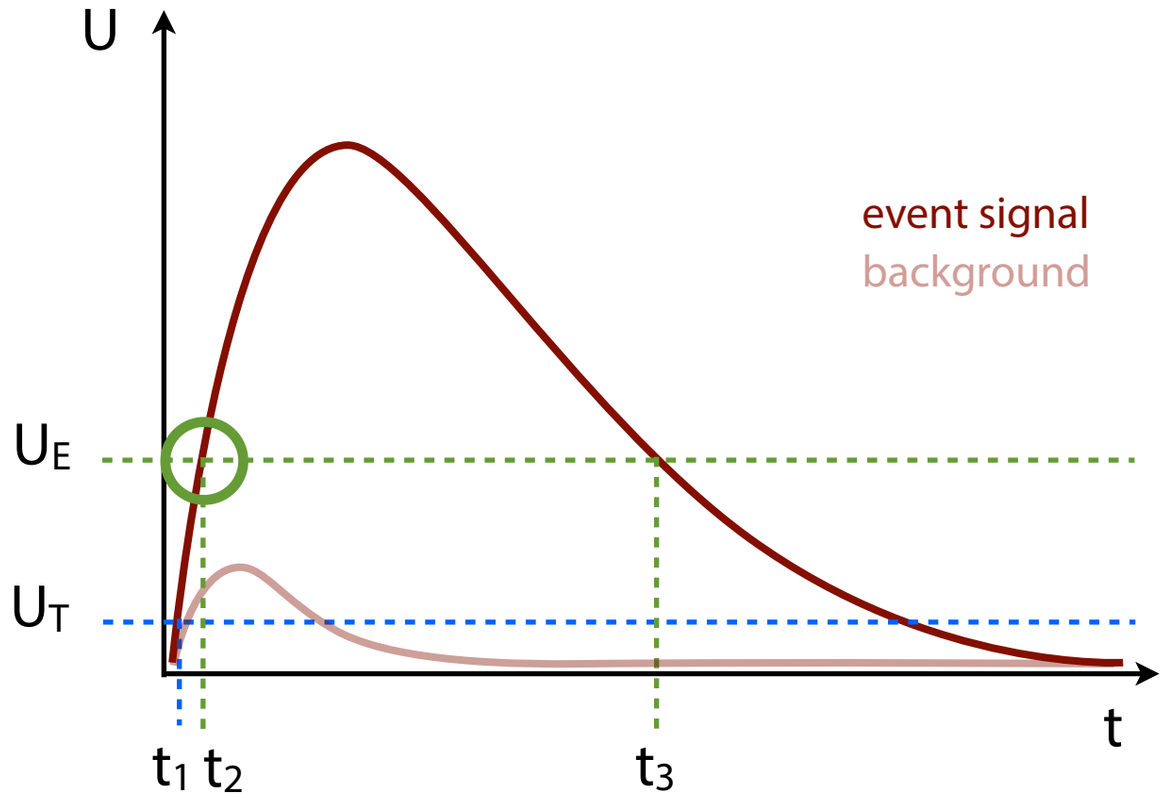
* powered two amplifiers per channel

Solution for higher channel pitch:

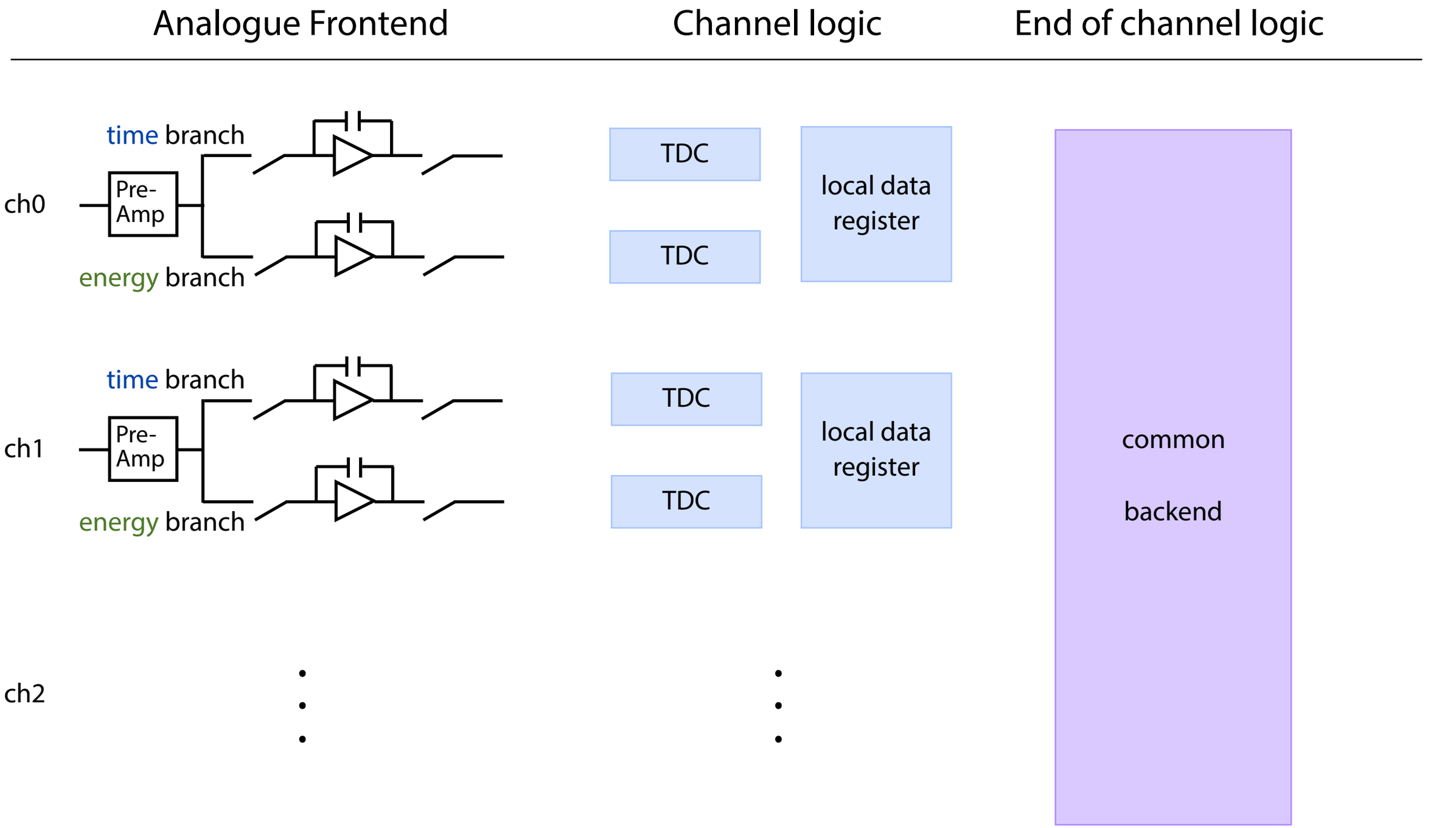


Function principle of TOFPET ASIC

- Two TDCs per channel
  - time and energy
    (low and high threshold)
  - energy trigger (t_2)
    validates time trigger (t_1)
- Charge with time-over-threshold
  - ToT meas.: $t_3 - t_1$
  - time binning: 50 ps



Structure for TOFPET ASIC



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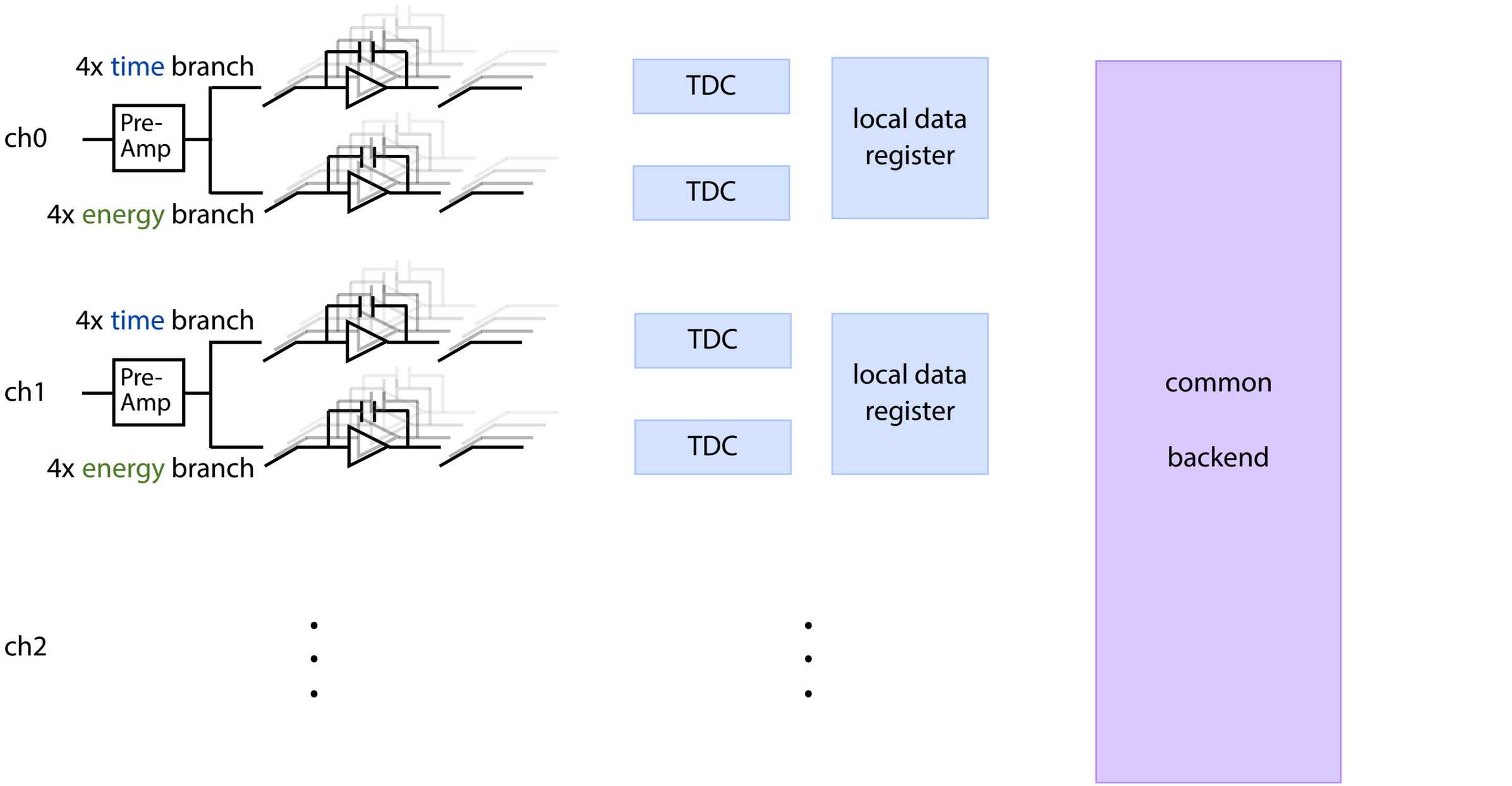


Planned modifications to MVD strip ASIC

- Improve general functionality
  - Bugs, recalibration of capacitors, placement of digital part, …

constantly ongoing

- Radiation hardening
  - Protect logic from single event upsets

TDC ctrl: almost
Backend: next

- Change technology (IBM 130 nm → UMC 110 nm)
  - Supported by Europractice
  - Cost effective

next step

- Adapt resolution and rate capability
  - Reduce clock speed (→ saves power)
  - Reduce time resolution (→ less data)

future

Types of radiation damage

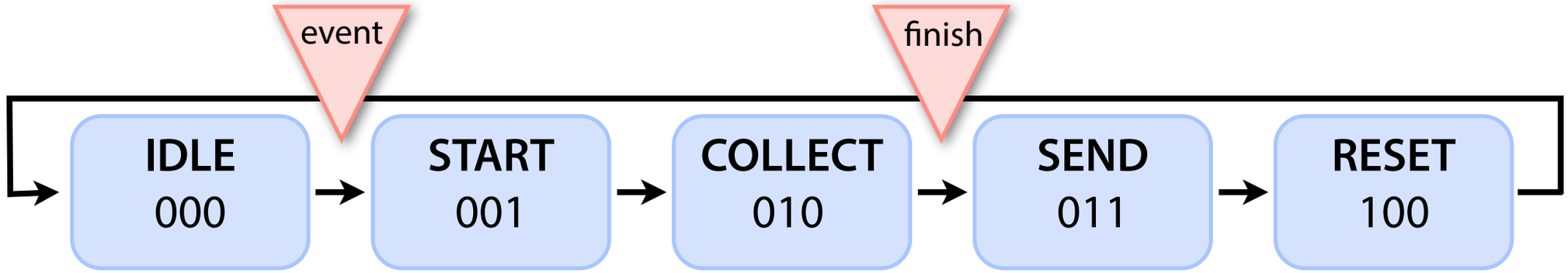
- Charge deposition in electronics can lead to:

- Hard errors
  - Destruction of gates
  - Permanent damage

- Soft errors
  - Effect only temporary
  - Single Event Upset (SEU)
    - Change a value inside a flip flop (buffer)

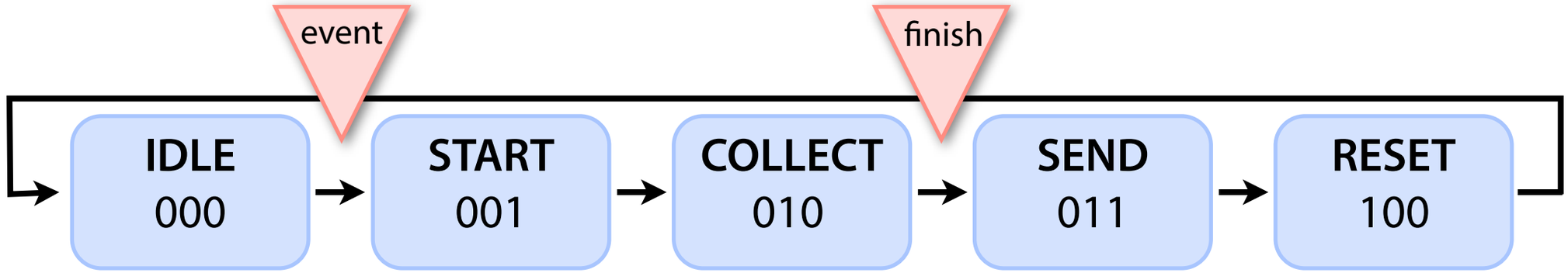
Single Event Upset

- *Example:* a fictional readout control
- Normal operation



Single Event Upset

- *Example:* a fictional readout control
- Radiation environment



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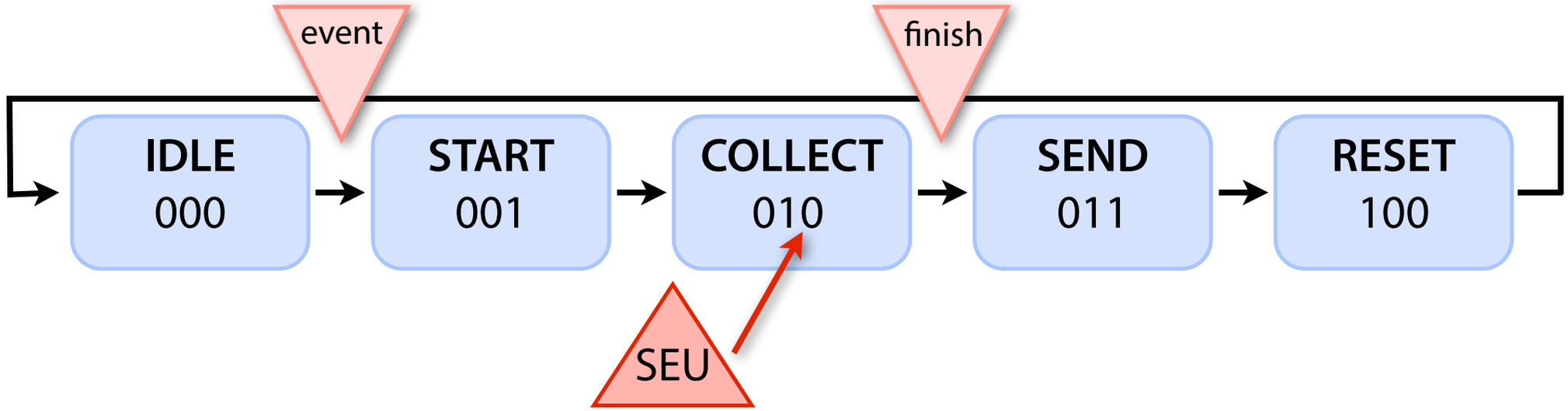

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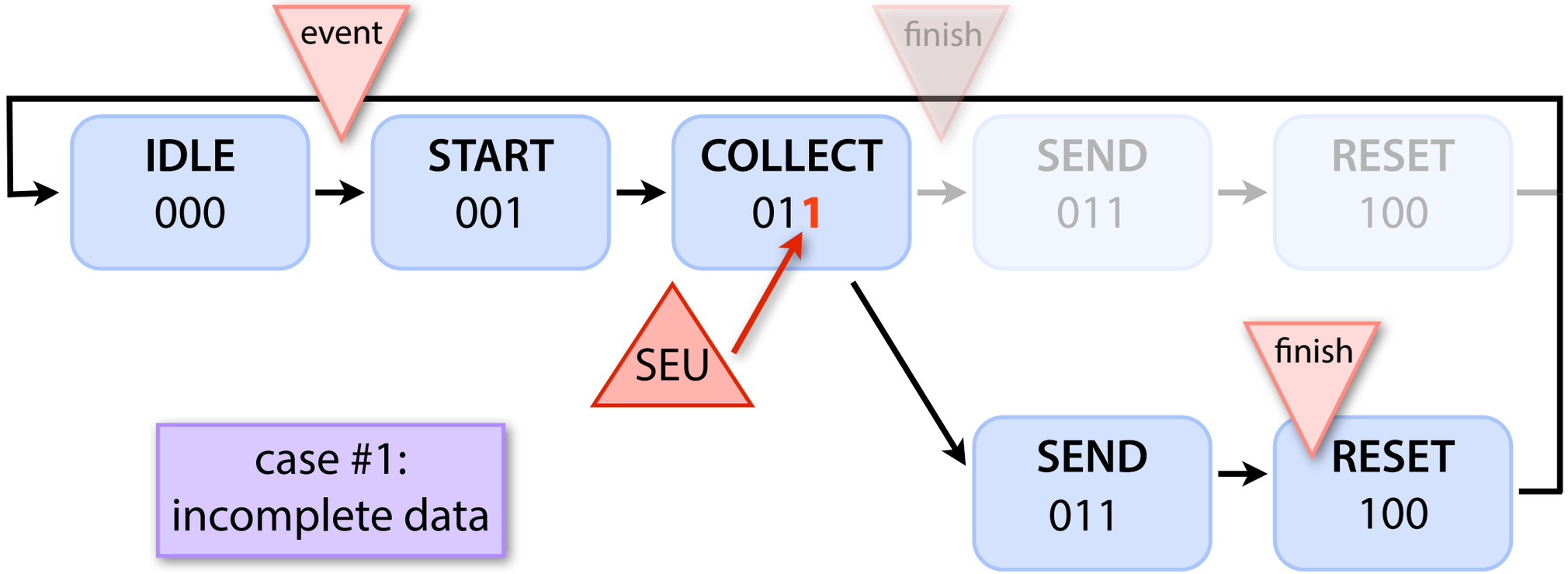

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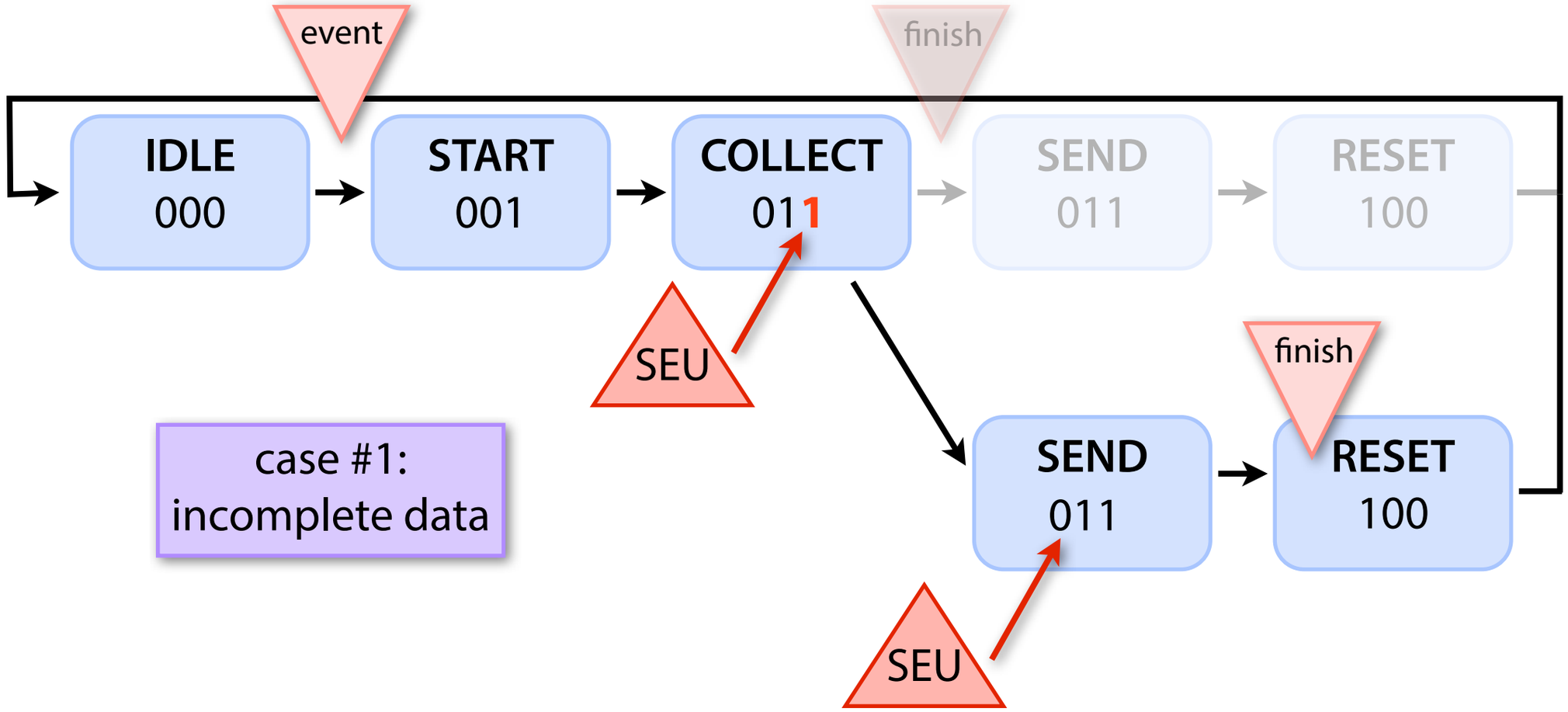

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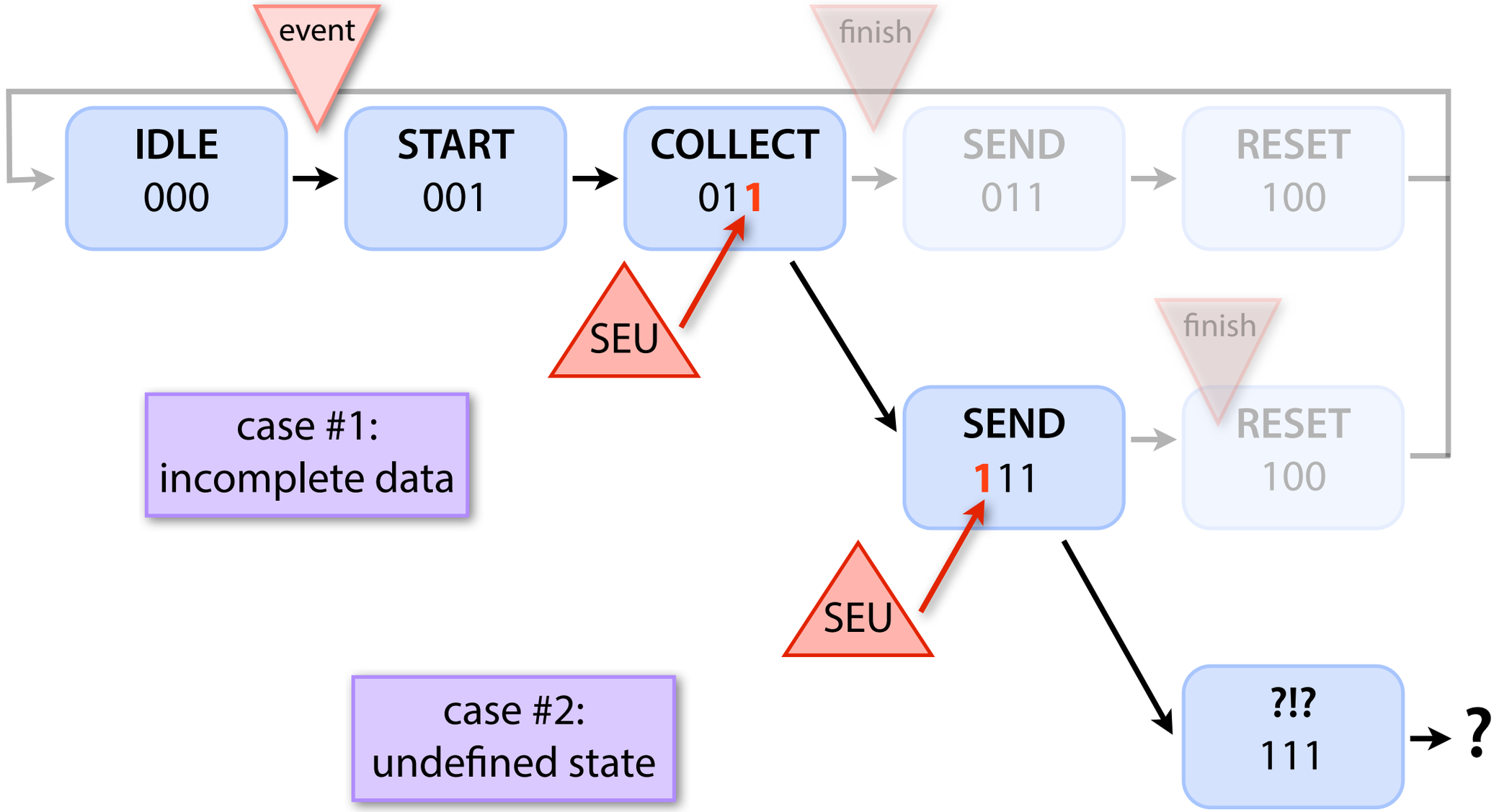
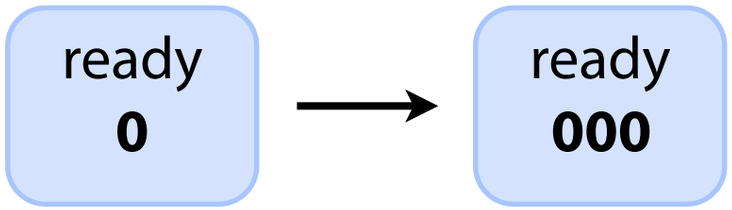


Prevent logic freeze

- Single bit:
  - Triple Mode Redundancy (TMR)



MVD Strip ASIC
Single bit FF: 140
TMR protected: 30

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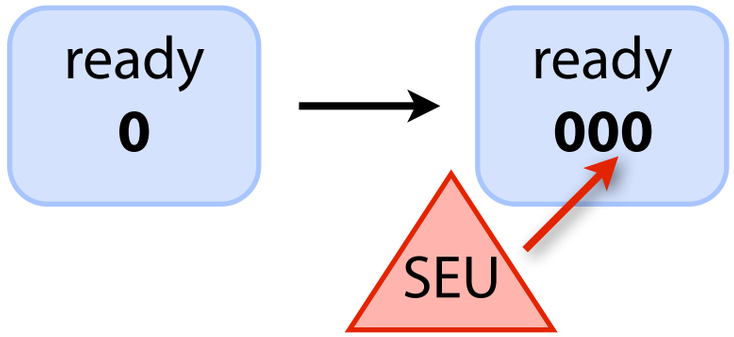

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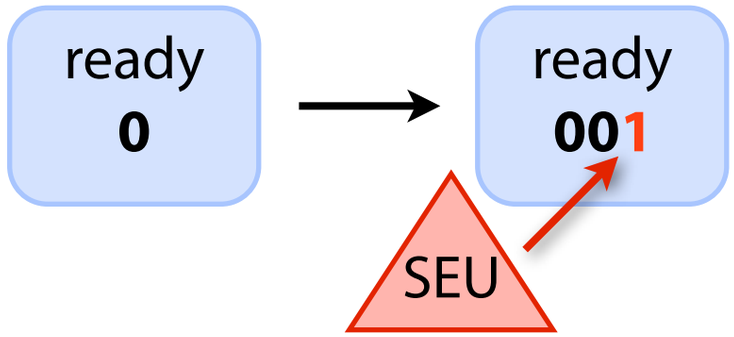

majority still says **0**

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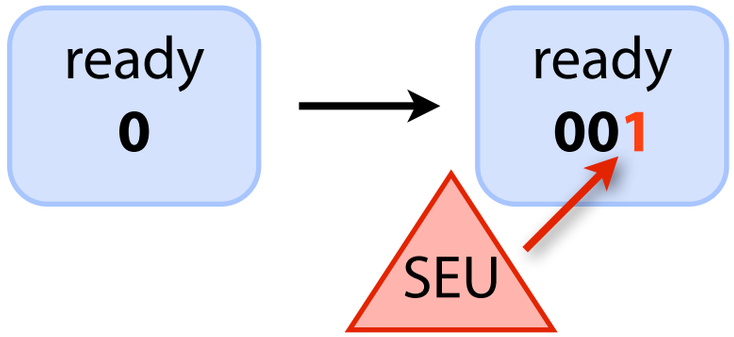

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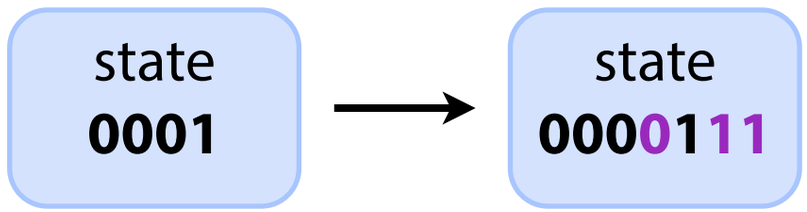
MVD Strip ASIC

Single bit FF:	140
TMR protected:	30

- Multiple bits (e.g. state machine):
  - Hamming encoded states



  - additional parity bits to detect and correct SEU

MVD Strip ASIC

Multiple bit FF:	320
Hamming protected:	133
(state machines:	100)

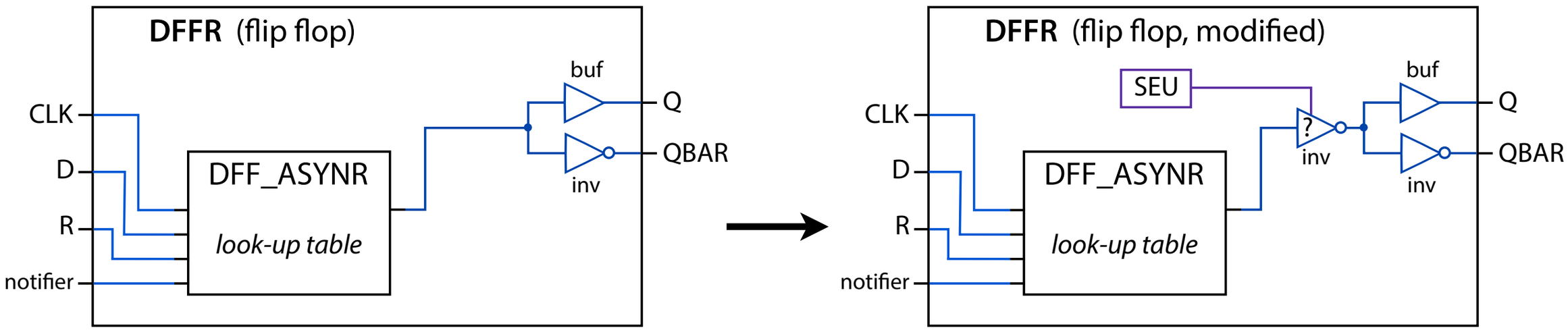
Detect corrupted data

- Protection of data inside the chip too expensive (area, power)
  - 5 times 10 bit timestamp buffers per channel
    - Hamming encoding: 20 additional bits + correction logic
- Detection of SEU desirable
  - Simple check: parity bit
    - even # of 1: parity 0
    - odd # of 1: parity 1
  - SEU: mismatch between data & parity
  - Implementation easy (xor) and small

data	→	data + parity
000101	→	000101**0**
001101	→	001101**1**

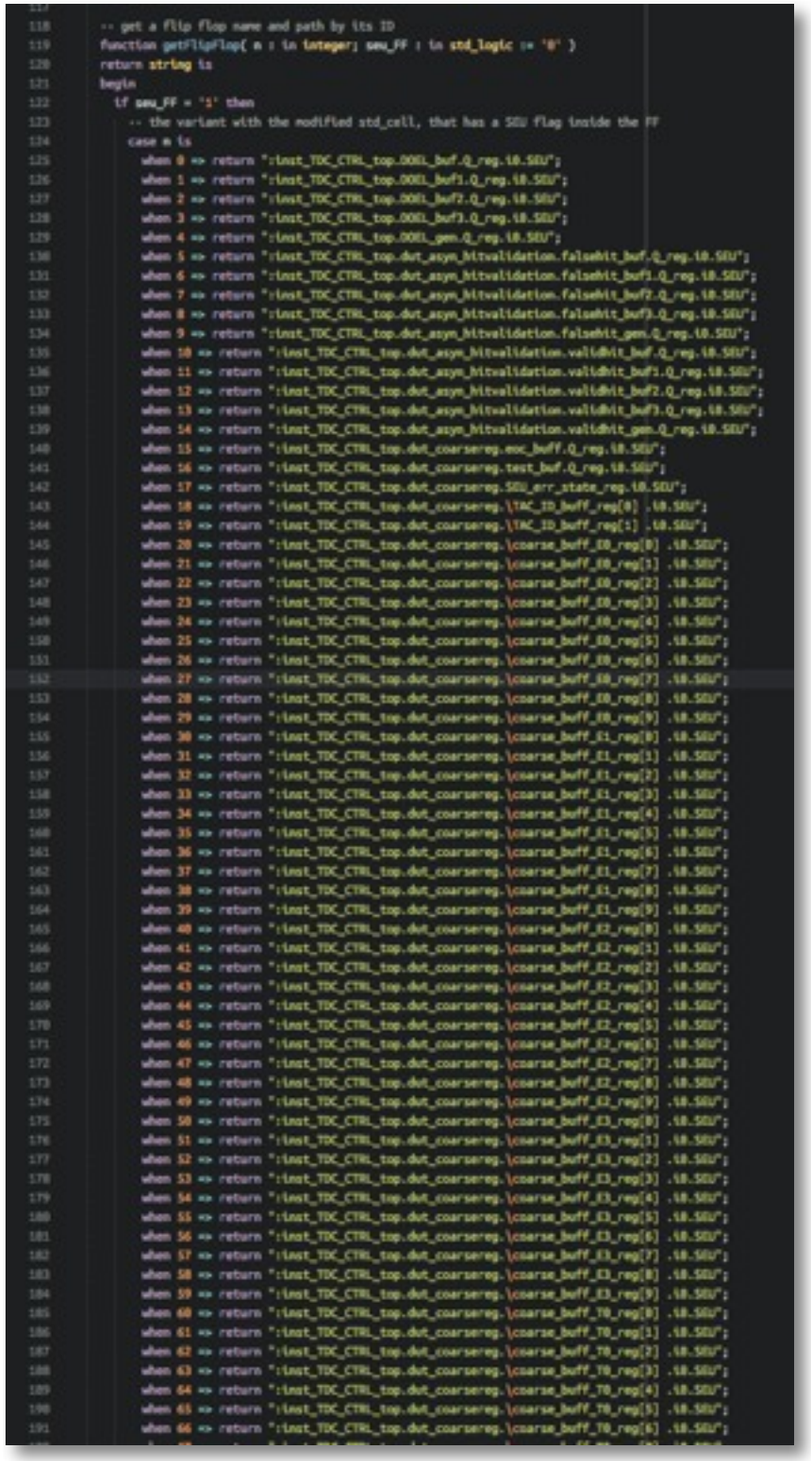
Simulate SEU

- Step 1: Ability to simulate a SEU
  - Functions of development environment »Cadence«
    - `nc_force`: forces a signal inside the logic to a given value
    - `nc_release`: releases a previous force
  - Problem: flip flop in simulation without internal memory
    - Flipped value in input wire
    - Modified standard cell library



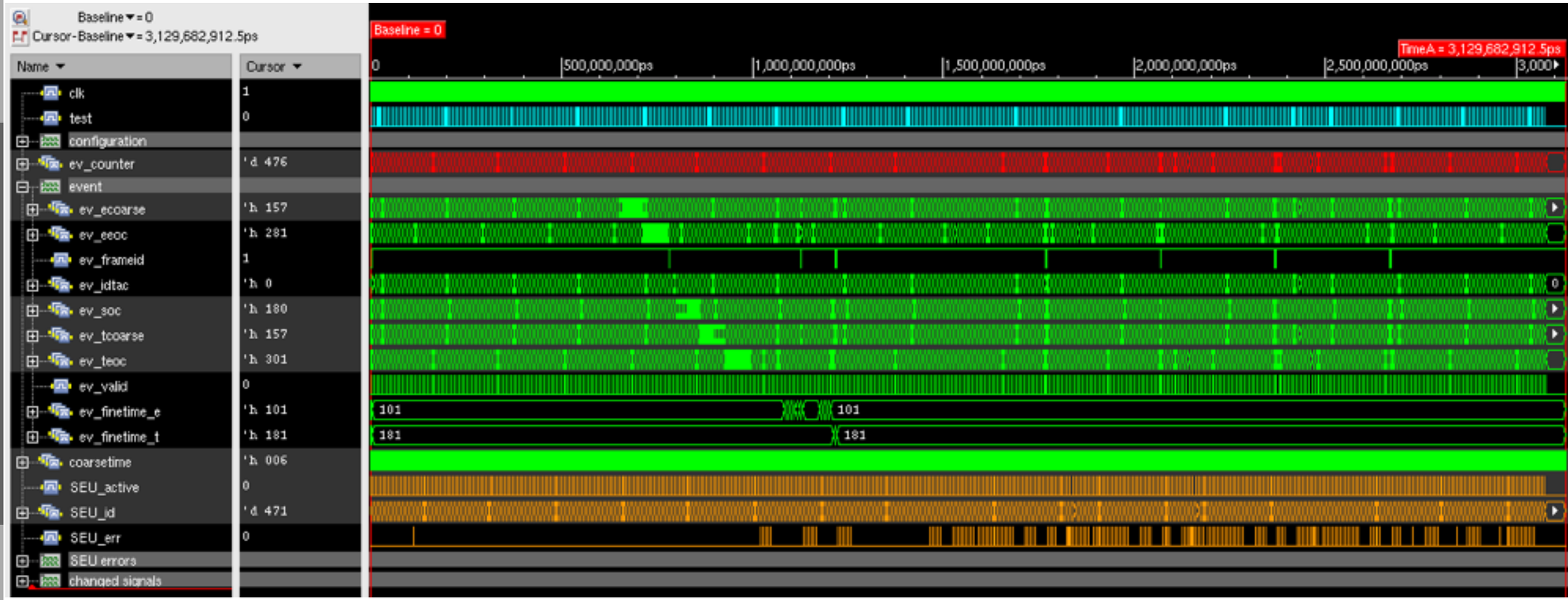
Simulate SEU in project

- Step 2: Check all flip flops
  - Which flip flops are critical? (besides state machines)
  - Tool to generate list of flip flops
    - Input: design after synthesis
    - Python parser filters input
  - Implementation easy to use
    - Include generated file
    - One command generates the SEU:
      `sim_SEU_FF( ID, clk, clk_period );`
  - Found 24 critical flip flops



Result of SEU tests

- Test of all 460 flip flops:



- No logic freeze
- Only corrupted data (→ parity bit)

Name of MVD strip ASIC

- But how should we name it?

- My suggestion:

  PASTA – **Pa**nda **St**rip **A**SIC

- Robert‘s suggestion:

  STRATOS – **St**rip **A**SIC **To**rino **S**olution

- Other ideas?

Conclusion / Outlook

- TOFPET ASIC as basic for MVD strip readout
- Modification in progress
  - Radiation hardening almost complete
  - Switch to different technology soon
- Further modifications for PANDA needs
  - Save more power and data
- We need a name…

Conclusion / Outlook

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- Modification in progress
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  - Switch to different technology soon
- Further modifications for PANDA needs
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- We need a name…

Thank you!

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Backup

Pamareter comparison

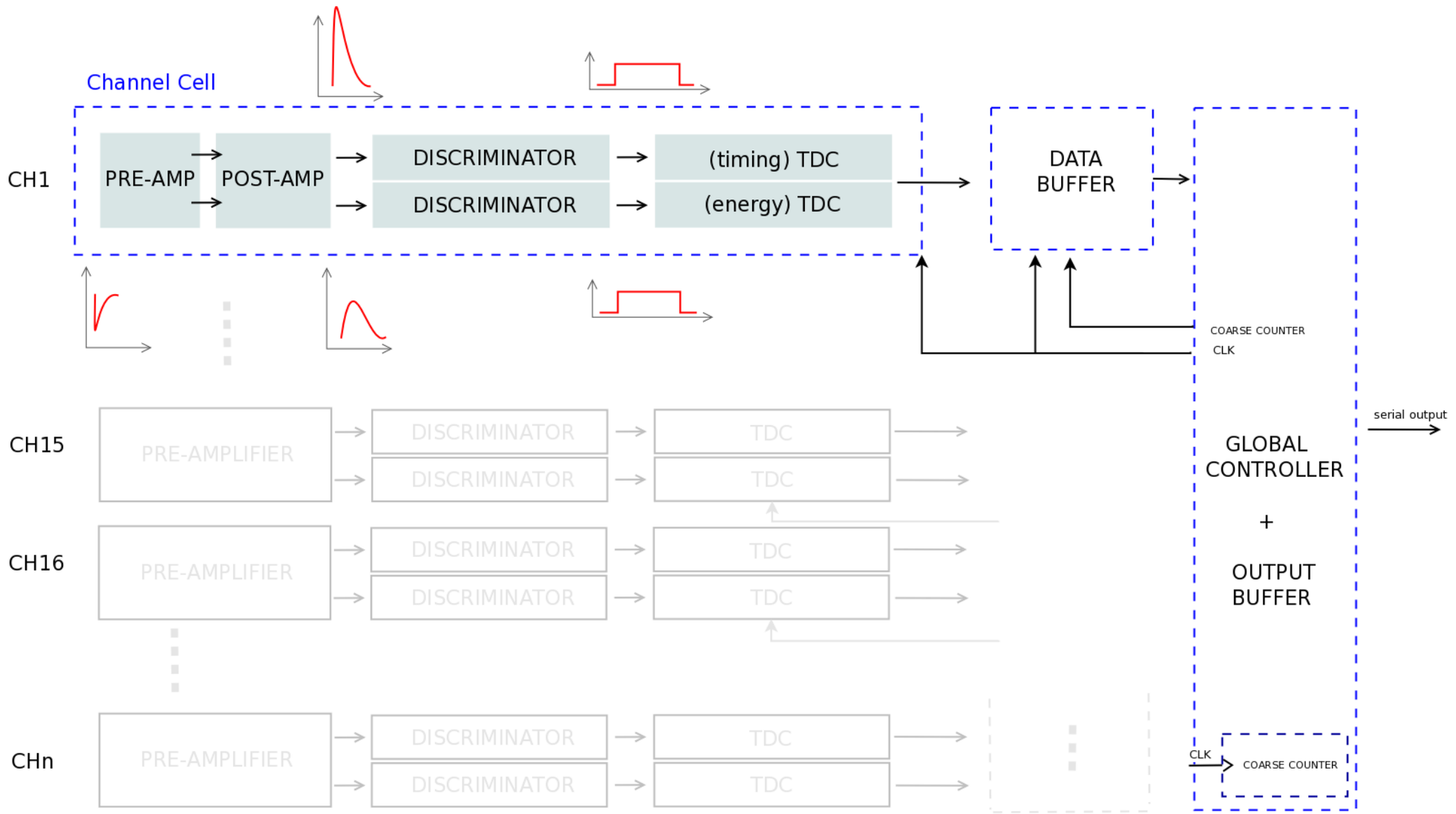
TOFPET

Parameter	Value
Number of channels	64
Clock frequency	80 – 160 MHz
Dynamic range of input charge	**300 pC**
SNR (Q_{in} = 100 fC)	> 20-25 dB
Amplifier noise (in total jitter)	< 25 ps (FWHM)
TDC time binning	**50 ps**
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. channel hit rate	100 kHz
Max. output data rate	320 Mb/s (640 w/ DDR)
Channel masking	programmable
SiPM fine gain adjustment	**500 mV (5 bits)**
SiPM	up to 320pF term. cap., 2MHz DCR
Calibration BIST	internal gen. pulse, 6-bit prog. ampli
Power	**< 10 mW per channel**

MVD TDR

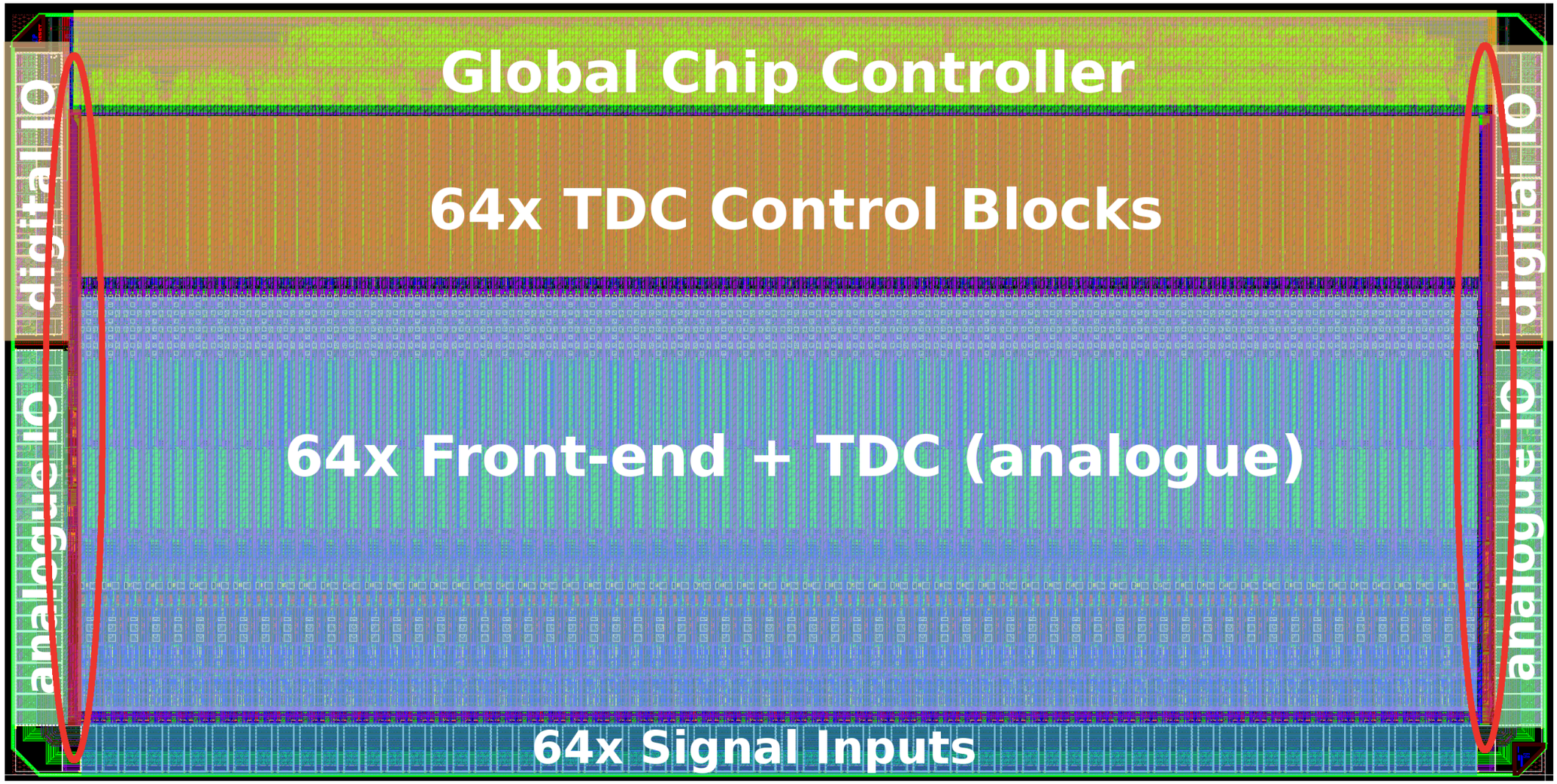
Parameter	Value	Remarks
Geometry		
Width	≤ 8 mm	
Depth	≤ 8 mm	
Input pad pitch	≈ 50 µm	
Pad configuration	lateral pads occupied only for diagnostic functions, should be left unconnected for final setup	
Channels per front-end	$2^6 \ldots 2^8$	default: 128 channels
Input Compliance		
Sensor capacitances, Fully depleted sensor		
	< 10 pF	rect. short strips
	< 50 pF	rect. long strips (with ganging)
	< 20 pF	trapezoidal sensor
Input polarity	either	selectable via slow control
Input ENC	< 800 e^-	$C_{sensor} = 10$ pF
	< 1,000 e^-	$C_{sensor} = 25$ pF
Signal		
Fynamic range	240 ke$^-$ (≈38.5 fC)	
Min. SNR for MIPS	12	22,500 e^- for MIPs in 300 µm silicon, guaranteed within lifetime
Peaking time	≈ 5 . . . 25 ns	typical Si drift times
Digitisation resolution	≥ 8 bits	
Power		
Overall power dissipation	< 1 W	assuming 128 channels per front-end
Dynamical		
Trigger	internally generated	when charge pulse exceeds adjustable threshold value
Time stamp resolution	< 20 ns	
Dead time / ch	< 6 µs	baseline restored to 1%
Overshoot recovery time / ch	< 25 µs	
Average hit rates / ch		derived from simulations at a beam momentum of 15 GeV/c
(poissonian mean)		
Hot spots	9,000 s^{-1}	$\bar{p}p$
	40,000 s^{-1}	$\bar{p}Au$
Average occupancy	6,000 s^{-1}	$\bar{p}p$
	30,000 s^{-1}	$\bar{p}Au$
Interface		
Slow control	any	low pin count, e.g. I^2C
Data	sparsified data	

TOFPET scheme



TOFPET Layout

7.1 mm



3.5 mm

Area: ~ 25mm²

Hamming code

- Bit positions dividably by 2: parity bits
  - Rest: data bits
- Parity bits cover data bits, which have bit pos. 2^p set

Bit position		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Encoded data bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8	d9	d10	d11
Parity bits	p1	X		X		X		X		X		X		X		X
	p2		X	X			X	X			X	X			X	X
	p4				X	X	X	X					X	X	X	X
	p8								X	X	X	X	X	X	X	X