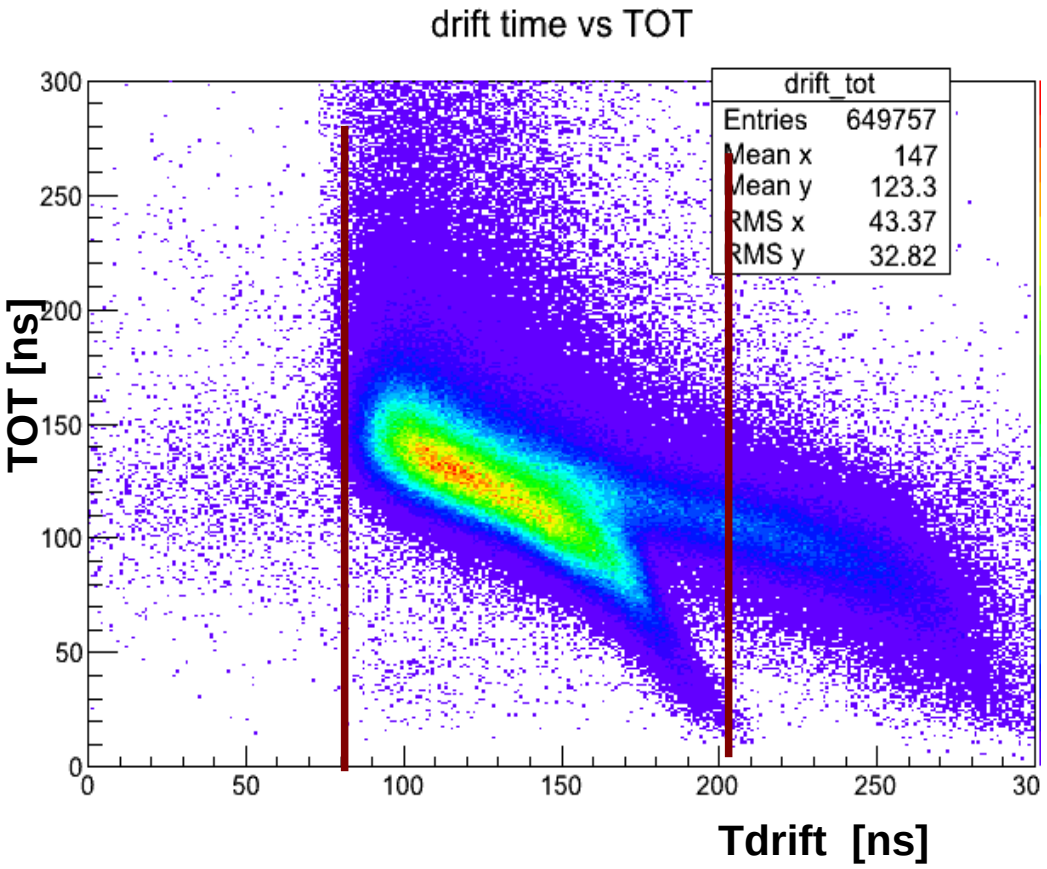
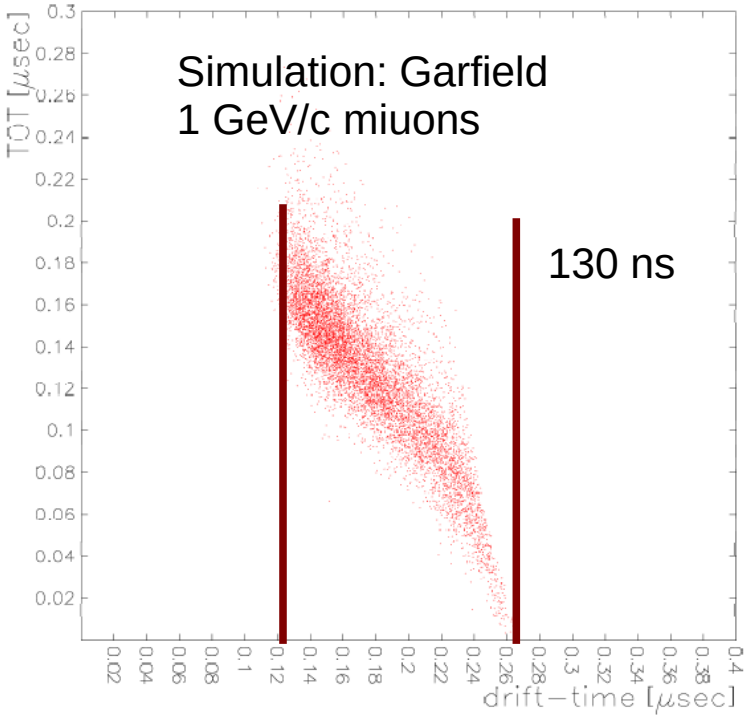
STRAWS READOUT STATUS REPORT

Grzegorz Korcyl – Jagiellonian University 2013

General issue



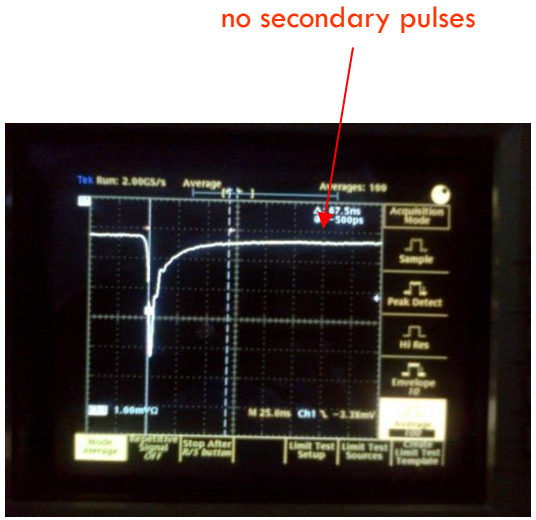


The problem: „second leg" structure in TDrift>130 ns !!

Investigations

- ## Secondary emission from cathode

  Excluded by observation of 55Fe pulses
  directly from a straw tube , HV up to 1900 V
  (no trace of pulses delayed by 130 ns (drift time))



- ## Cross talk between straws

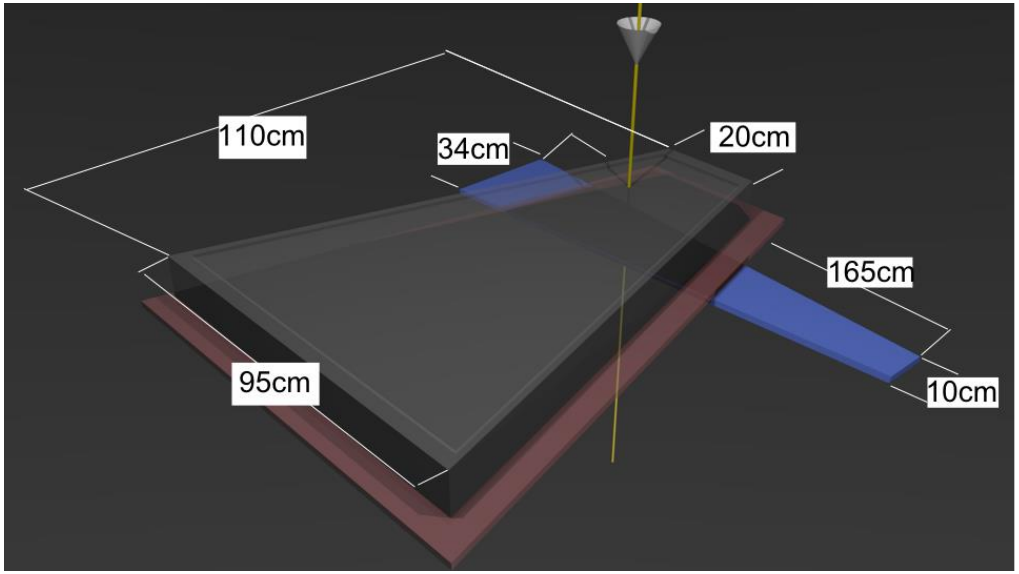
  Excluded – no cross talk pulses observed on a straw tube
  with turned off HV placed directly near straw tubes
  with HV on and irradiated with 55Fe

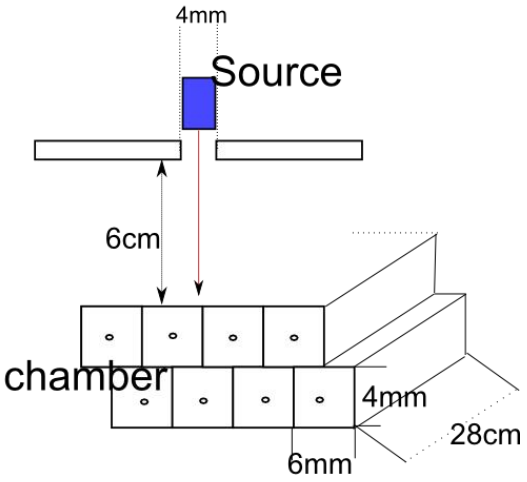
- ## ??

  Further search is needed

ASIC with MDC

- Setup



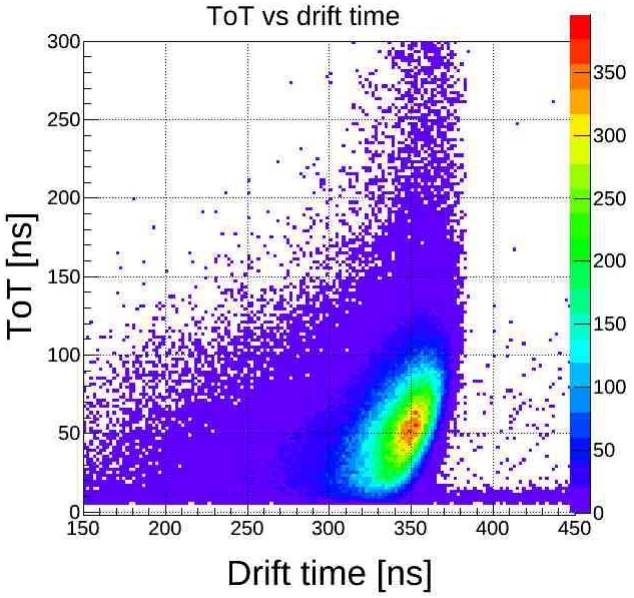


- Data has been taken with Sr source and MDCII chamber
- Gas mixture: 70% Ar, 30% CO2

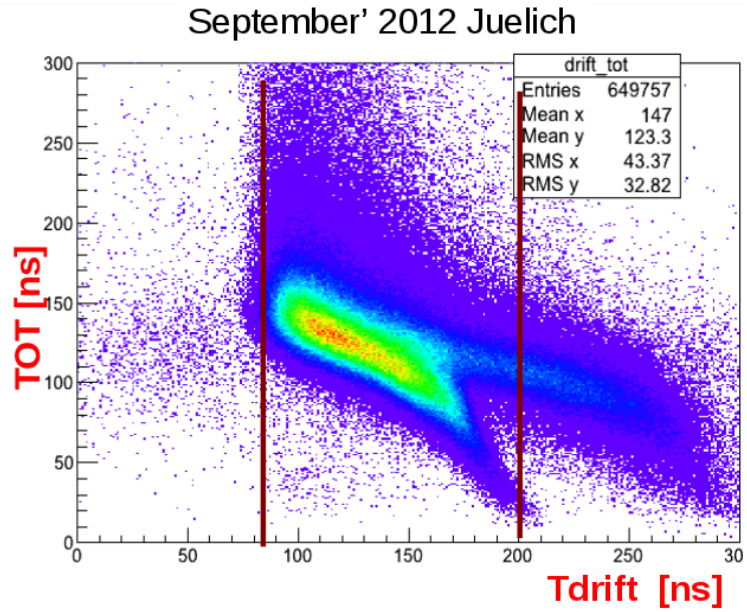
ASIC with MDC

Paweł Strzempek

- TOT vs Drift Time Comparison



Example of tot vs drift time spectrum measured with MDC



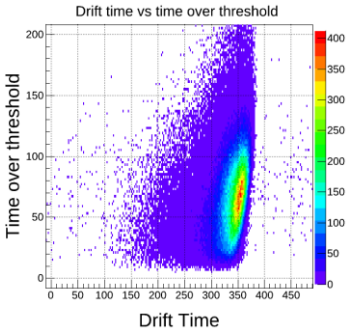
Example of tot vs drift time spectrum measured with straws at Juelich

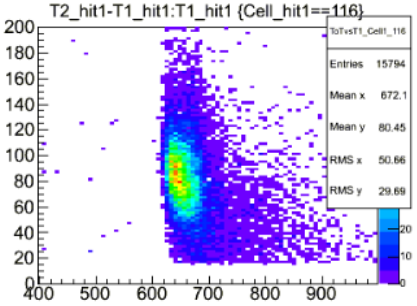
ASIC with MDC

Paweł Strzempek

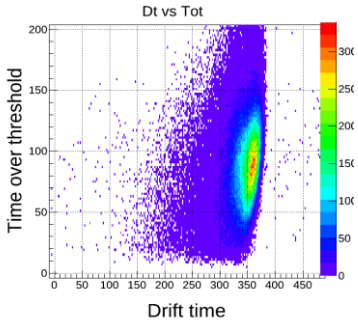
- Cracow ASIC vs ASD8 Comparison (different chamber)

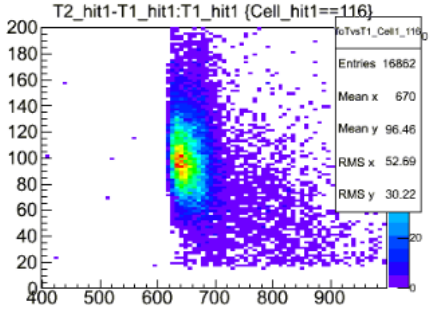
1700 V

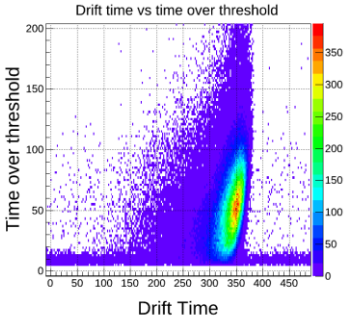


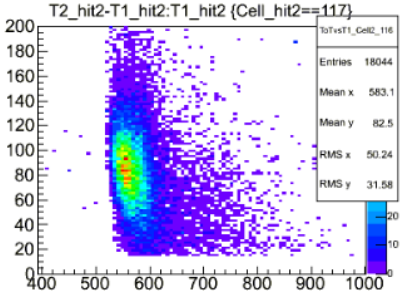


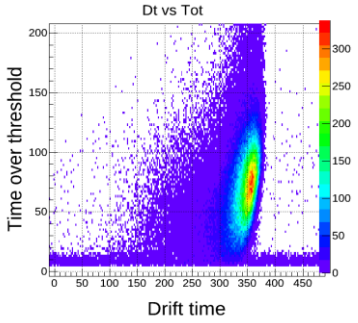
1750 V

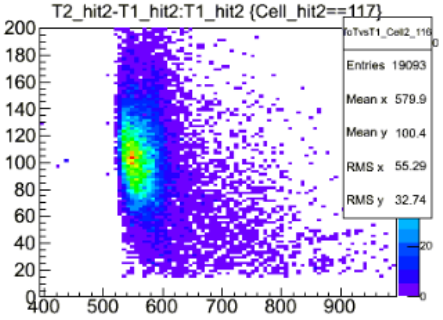










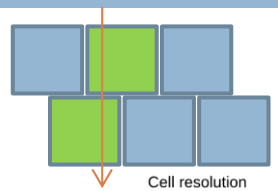


ASIC ASD8 ASIC ASD8

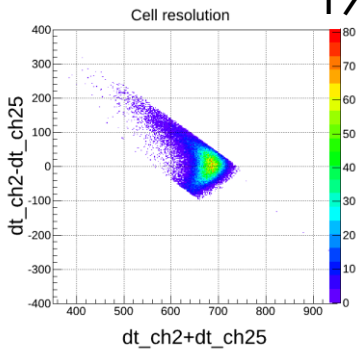
ASIC with MDC

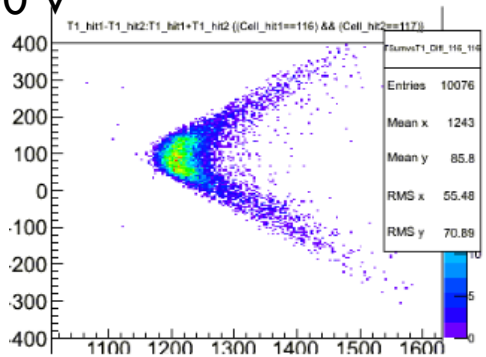
Paweł Strzempek

- Resolution comparison

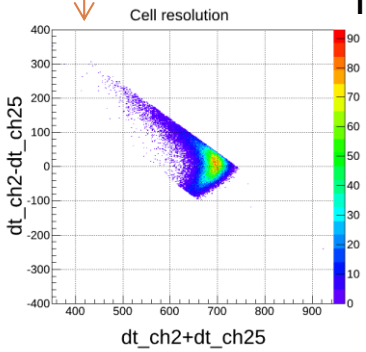


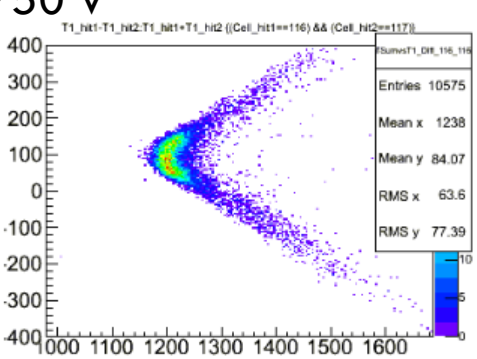
1700 V

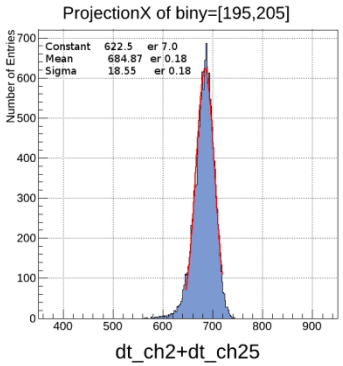


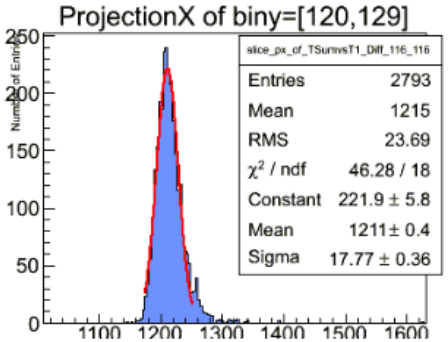


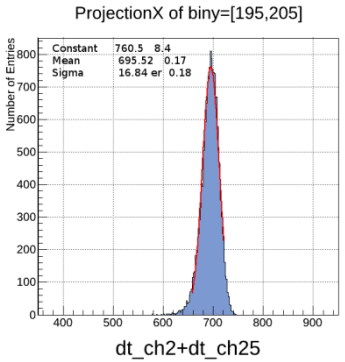
1750 V

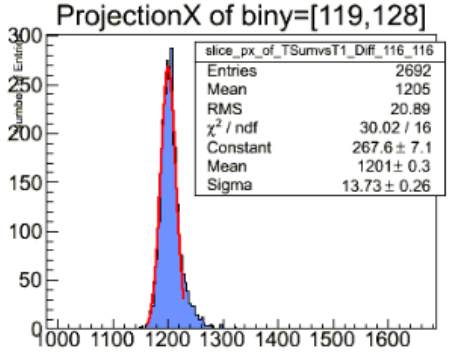












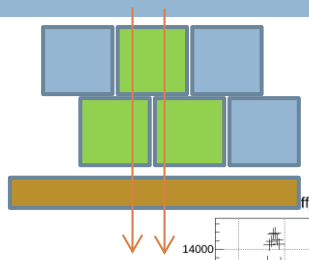
σ = 18.55 ± 0.18[ns] σ = 17.77 ± 0.36[ns] σ = 16.84 ± 0.18[ns] σ = 13.37 ± 0.26[ns]

ASIC ASD8 ASIC ASD8

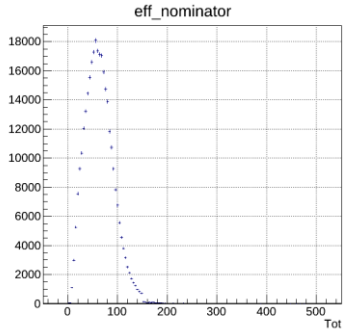
ASIC with MDC

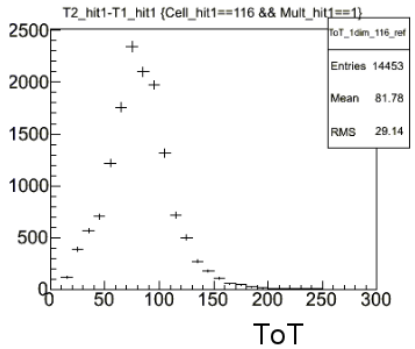
Paweł Strzempek

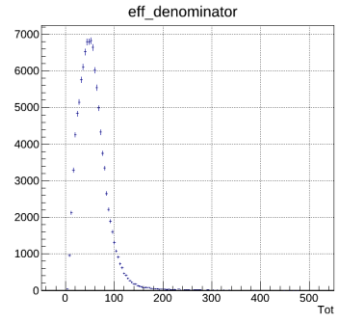
- Efficiency comparison

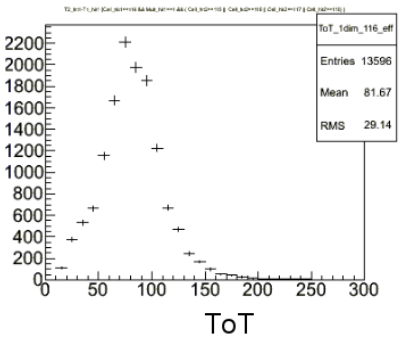


1700 V









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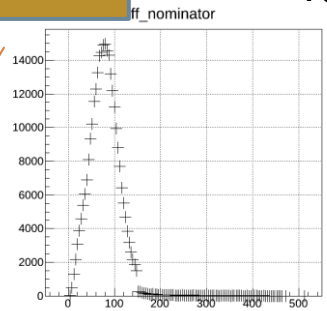
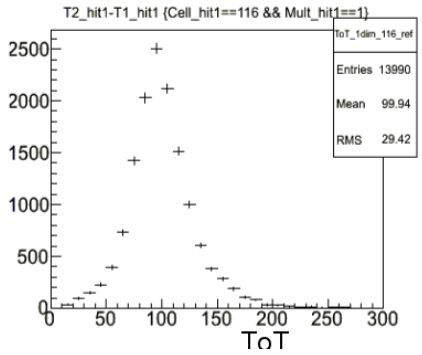
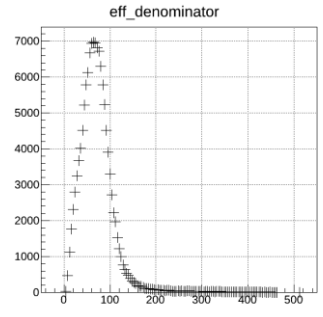
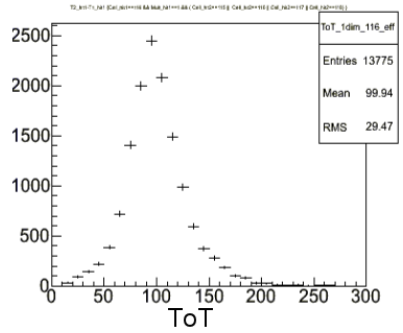








Efficiency: 26%

ASIC

Efficiency: near 100%

ASD8

Efficiency: 35%

ASIC

Efficiency: 100%

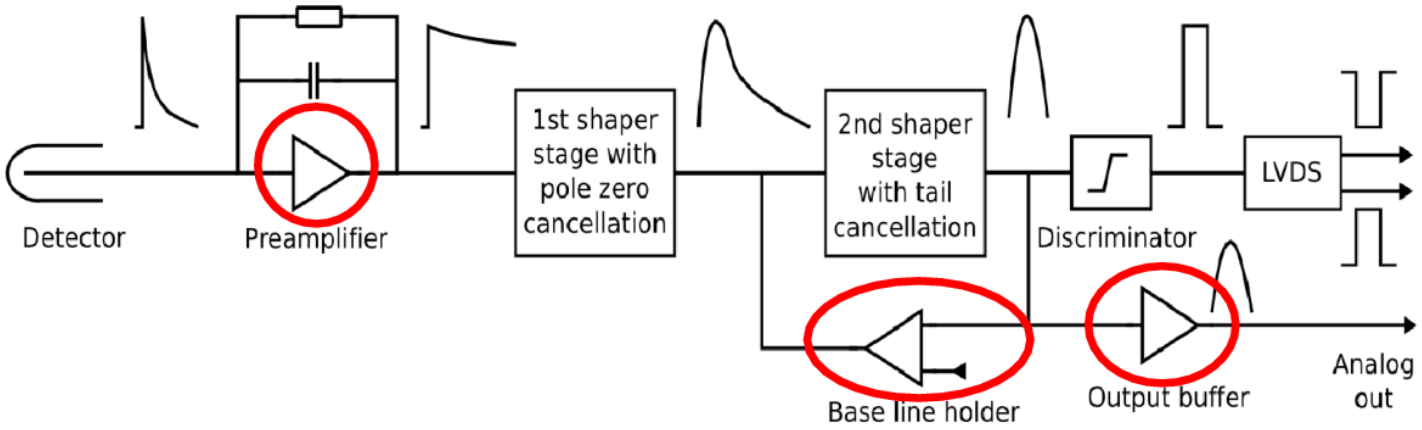
ASD8

ASIC with MDC

- Conclusions:
  - We get worse time resolution due to multiple scattering. Lower efficiency for Panda FEE was due to too high thresholds. However we don't want to improve efficiency by increasing HV but rather by noise reduction (better grounding etc.)
  - Low efficiency means that with given voltage threshold was set too high
  - Repeat the measurements with cosmic rays

ASIC v2 development

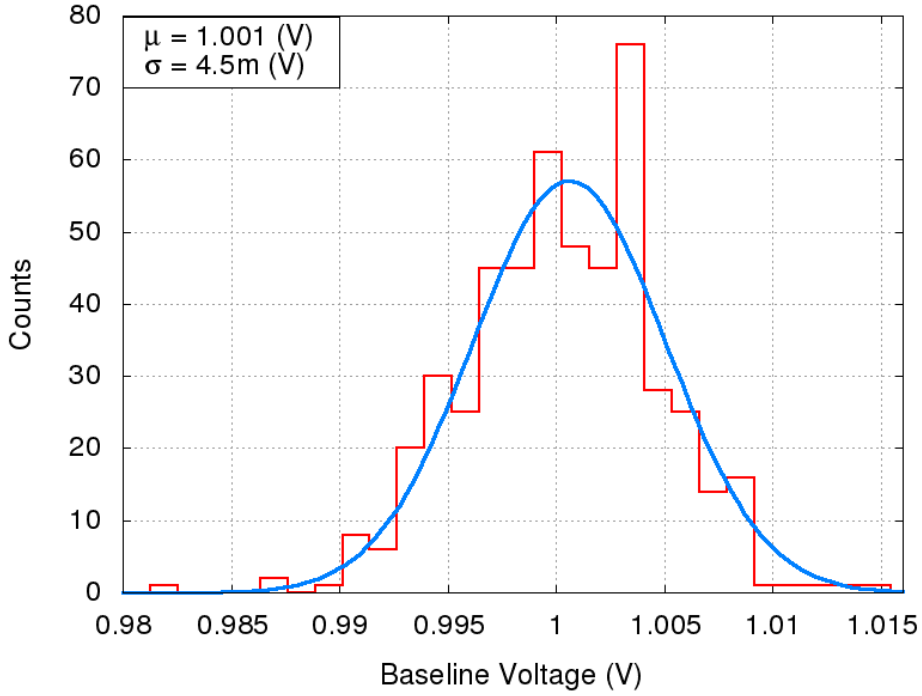
- Main goals



  - Preamplifier:
    - Speed augmentation
    - Saturation prevention
  - Diminuation of the shaping time
  - Minimalization of the base line dispertion
  - Analog buffer:
    - Augmentation of dynamic range
    - Equalization of DC level to the base line
    - Work with larger capacity load

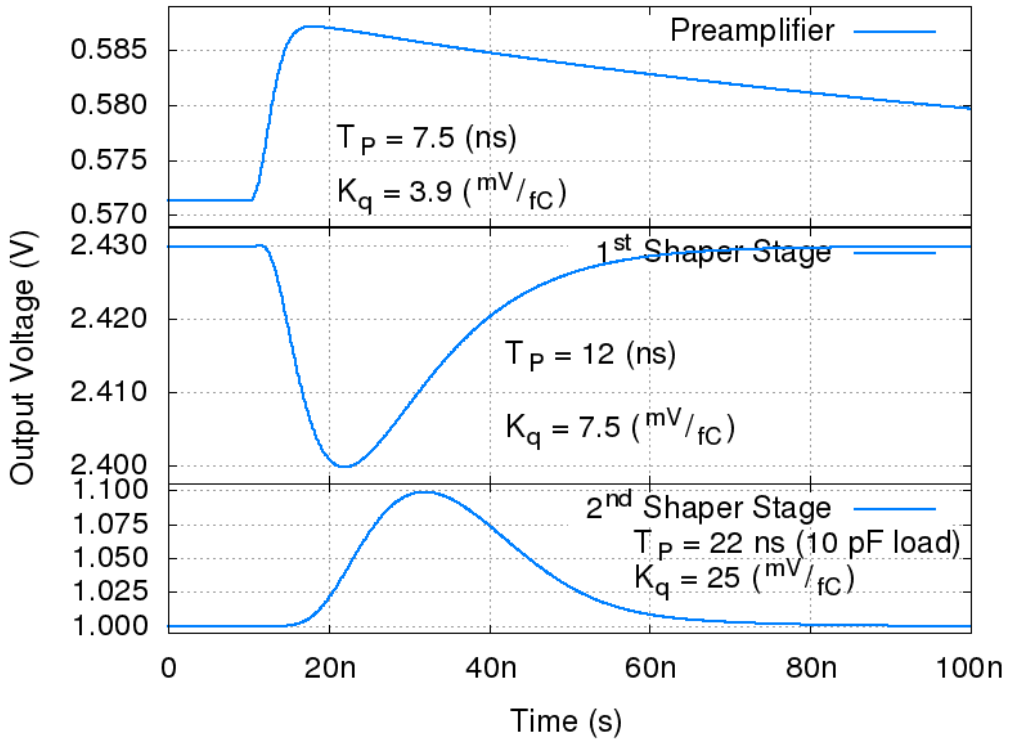
ASIC v2 development

- Early stage simulations
  - Basle line dispertion



ASIC v2 development

- Early stage simulation
  - Response times



- 2nd shaper stage – wrong load applied

ASIC v2 development

Dominik Przyborowski

- Development summary:
  - Optimalization of the preamplifier
  - Faster first shaper
  - Optimalization of the second shaper toghether with its output level
  - DACs added to trim the thresholds for the discriminator
  - Submission in October

Summary

- „Second leg” issue still not solved – ongoing investigations
- Cracow ASIC tested with MDC and compared to ASD8
- ASIC v2 in development by Dominic – early simulations, submission in October
- Early tests of TRB3 as TDC for ASIC