@ELSA INSIGHT

DOGMA @Bonn

7.05.2025

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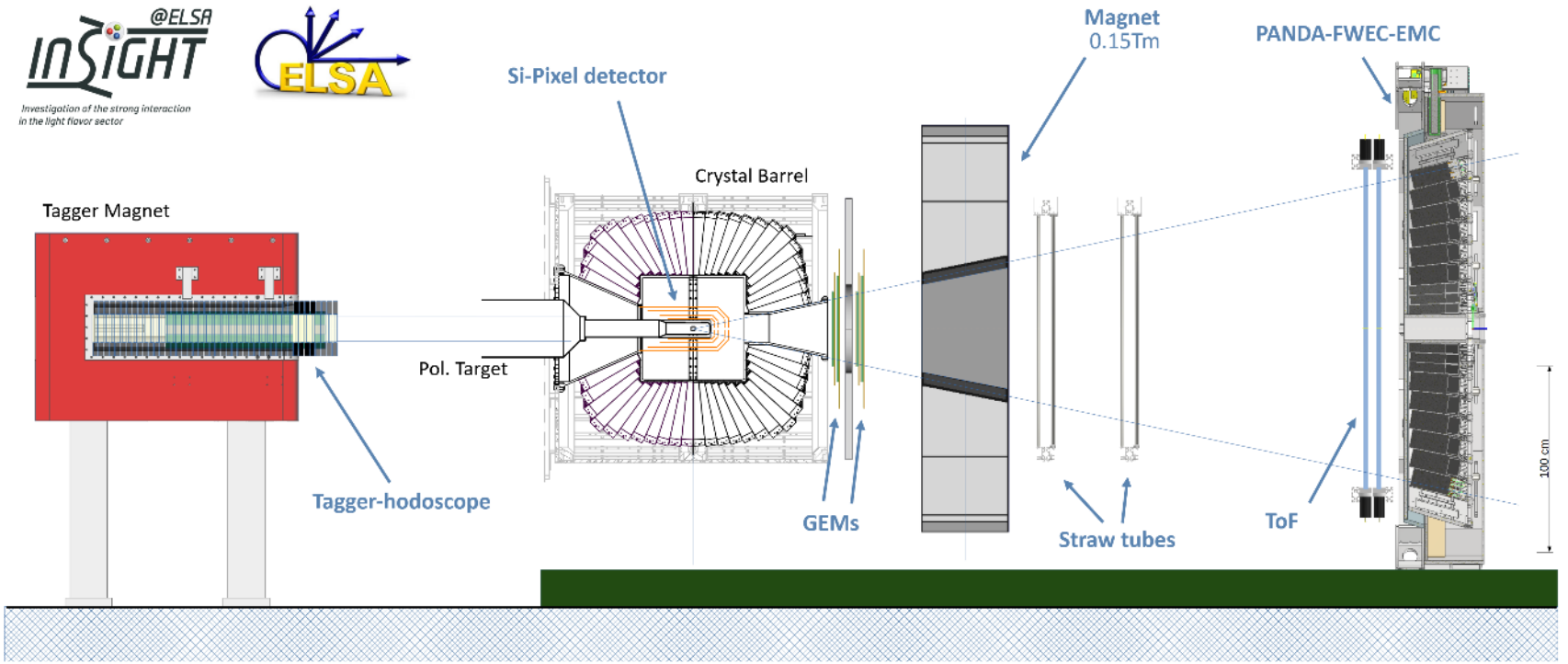
INSIGHT a new experiment at ELSA

Experiment will be a major upgrade of the CBELSA/TAPS-experiment



New detectors will be FPGA-based readout systems

→ CB-ELSA DAQ needs further improvements to integrate new systems

Starting point

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Existing detectors

- Crystal Barrel
- Adapted PANDA-SADC based on Kintex 7 (energy readout)
- Spartan 6 based VME board (time readout, cluster finder)

Other detectors entering

- Straws (PANDA)
  - Existing Frontends (PASTTREC ASIC)
  - Digitizing platform (TRB5 TDR)
- FWEC-EMC (PANDA)
  - Existing PANDA-SADC (Kintex 7 based)
- GEMs (Amber)
  - Frontend with LVDS outputs/interface
- Pixel (Belle 2, OBELIX chip)
  - Data IO via LVDS

- TOF
- Tagger (improved timing)

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1. Test-setup using DOGMA-TDC

2. INSIGHT-DAQ Trigger-/Time-Distribution via DOGMA

Starting point – ToF developments

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Look for a new TDC

Keeping in mind: number of different readout platforms in the experiment should be small

Two ideas:

- Test TRB5 to use the same as straws → contact with M. Traxler => DOGMA
- Porting existing exp. TDC-VHDL to Kintex 7 for PANDA LVDS-DC (based on PANDA-SADC)

Goal

- ToF - Measuring time of flight with high precision
- overall resolution $\sigma \sim$ 100-110ps

→

- Current experiment TDCs binning of 40ps not good enough

→ Need for a high resolution TDC for the ToF detector (with ToT) and tagger

→ Use DOGMA in our ToF-development setup

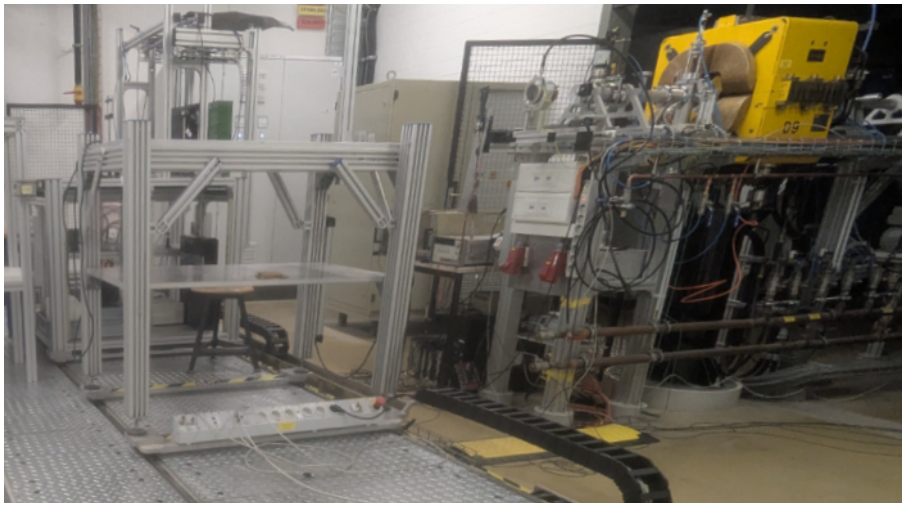
ToF setup for beam test @ELSA using DOGMA

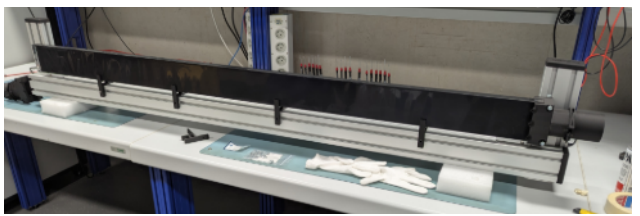
Testing of ToF prototype bars with beam in an experiment-like environment

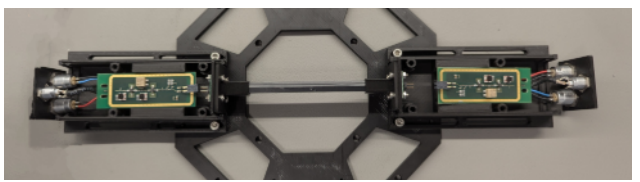
Using TDC (DiRICH5d2) with

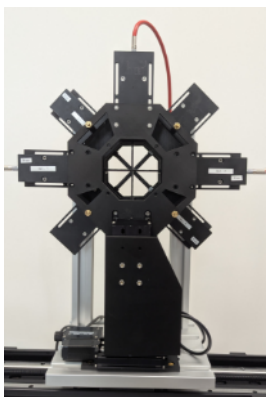
- ToF Prototype bars (EJ-204)
  PMT readout (~1-2V pulse height)
- Startdetector (EJ-232)
  SIPM readout (~0.7-1.4V pulse height)
- Test situation
  - Readout by 1 TDC
  - Distributed readout by 2 TDC
    → influence of time syncing
    (performance of Dogma)

→ Test timing performance of new ToF bars



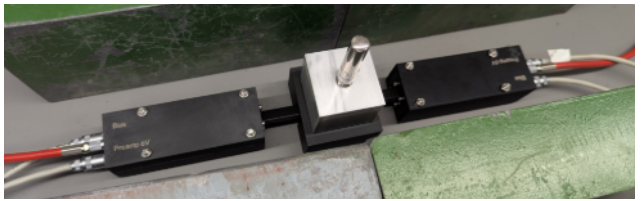


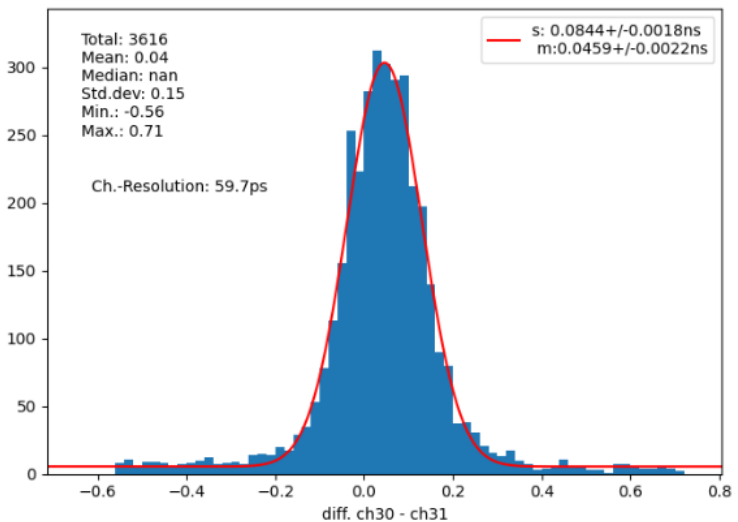


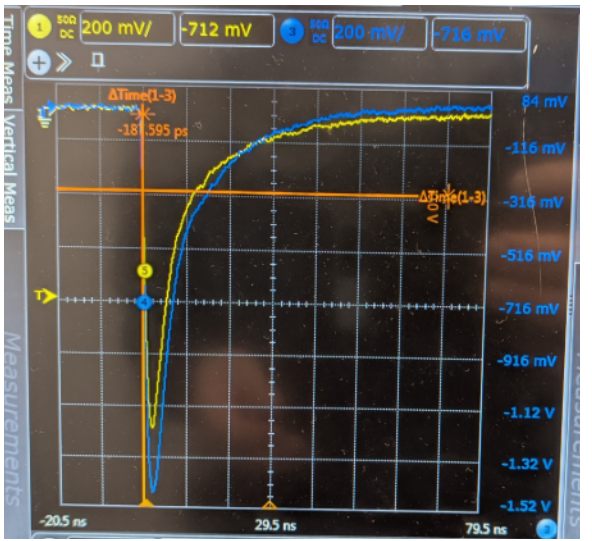


Startdetector – SIPM readout

First test with Sr^{90} source







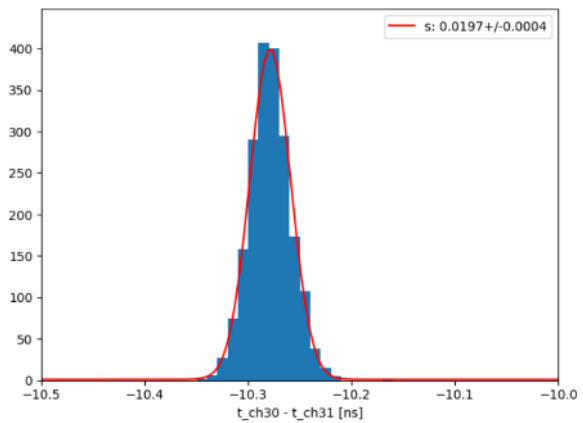
Successful adapting SIPM-Preamp out to TDC input, using reduced gain!
→ still not optimal/problematic in case of high rates

DOG resolution – Test pulser

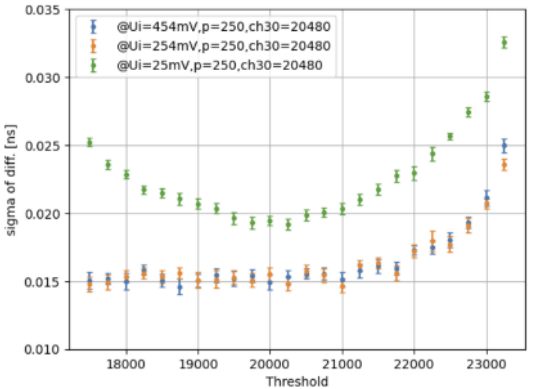
Fed signal of wave generator into 2 DOG inputs

Reduced gain on input to minimal value

@25mV, threshold ~20000



Threshold-Scans



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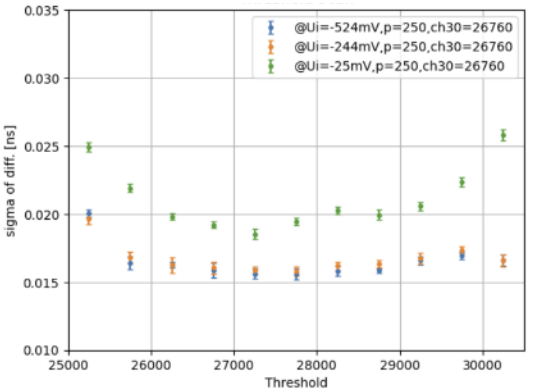

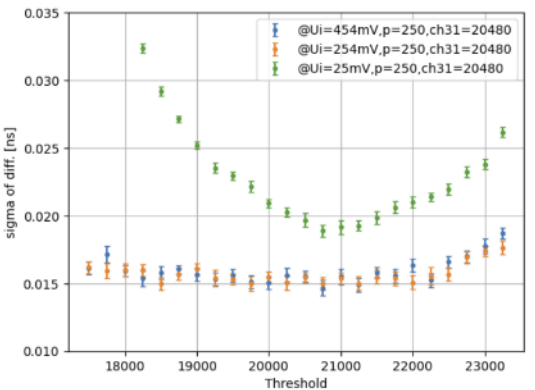

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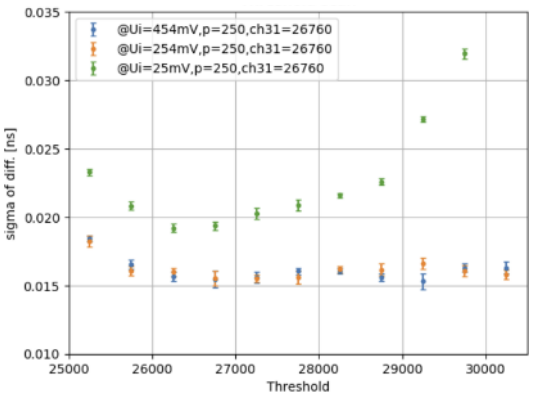
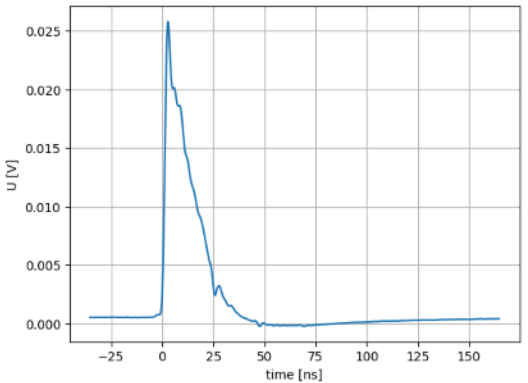
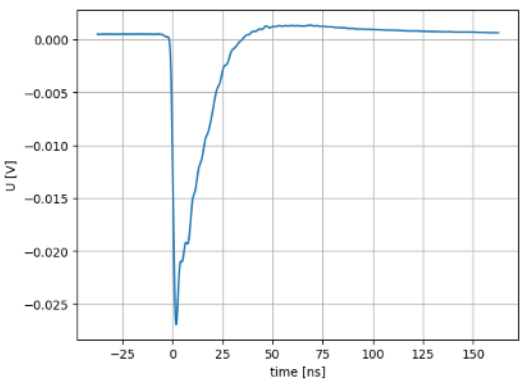


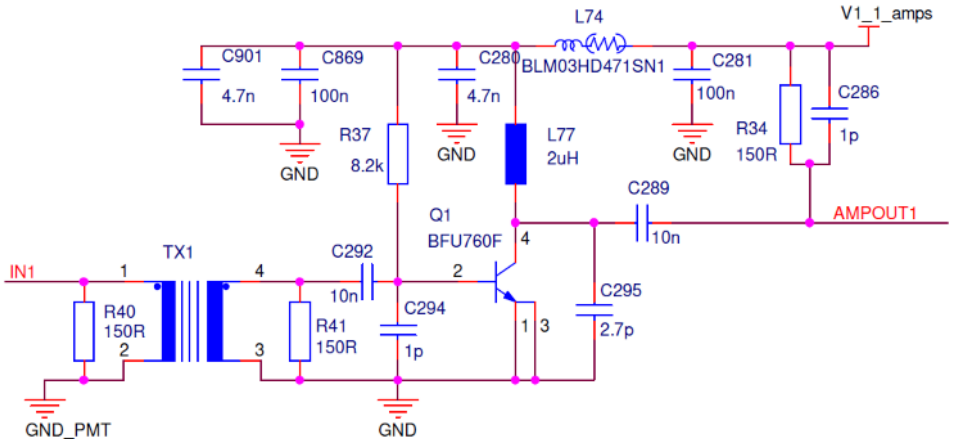
Pos. input pulse

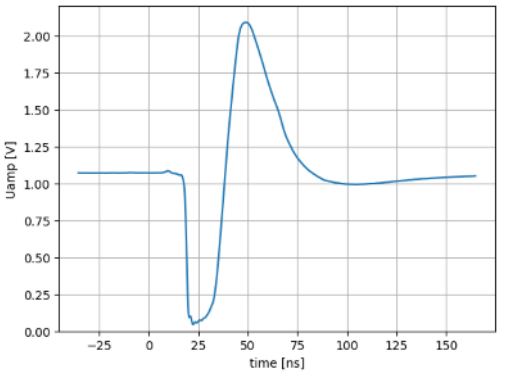
Neg. input pulse

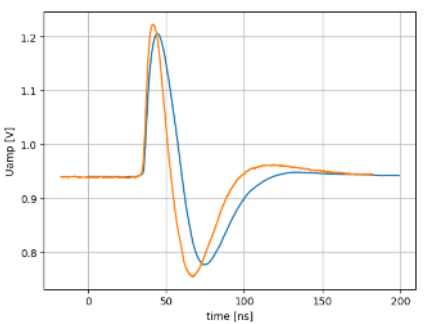
DOG (DiRICH5d2)-Input stage

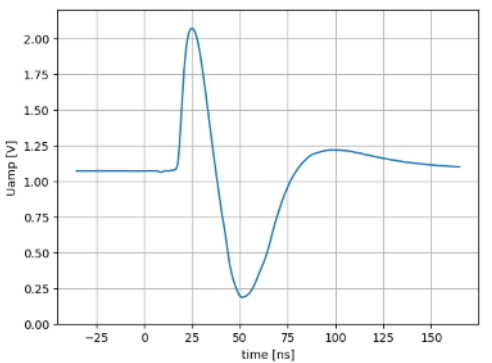












Blue:
simulation LTSpice

Output waveform in case of high rates not optimal → problematic

Current status – towards beam tests

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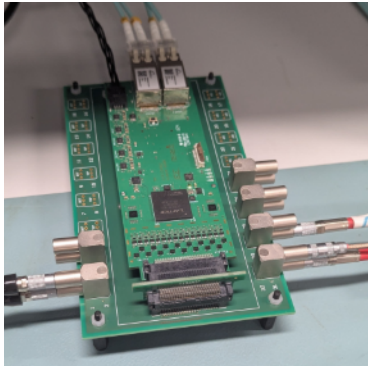
General developments

To handle data more basic (python based):

- Simple data receiver – dump data to disk
  - Up to 100MB/s possible
- Classes for data handling
  - Calibration
  - Analysis

Built break out board



→ Developments can be used by others

Start-detector for testsetup

- SIPM-Preamp adapted for TDC DiRICH5d2 input
- Reached time res. of σ ~ 60ps with Sr^{90} source

TODOs:

Test with electrons >2GeV energy at ELSA

- Setup in test area
- First tests in June
- Bar input adaption

Use a 2nd TDC for testing time sync mechanism

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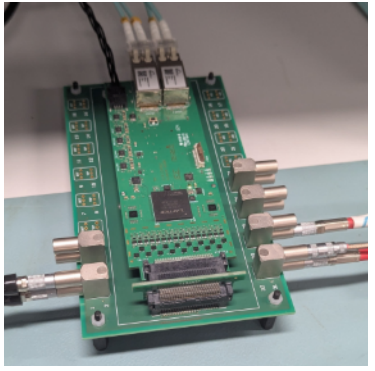

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Change topic → DAQ

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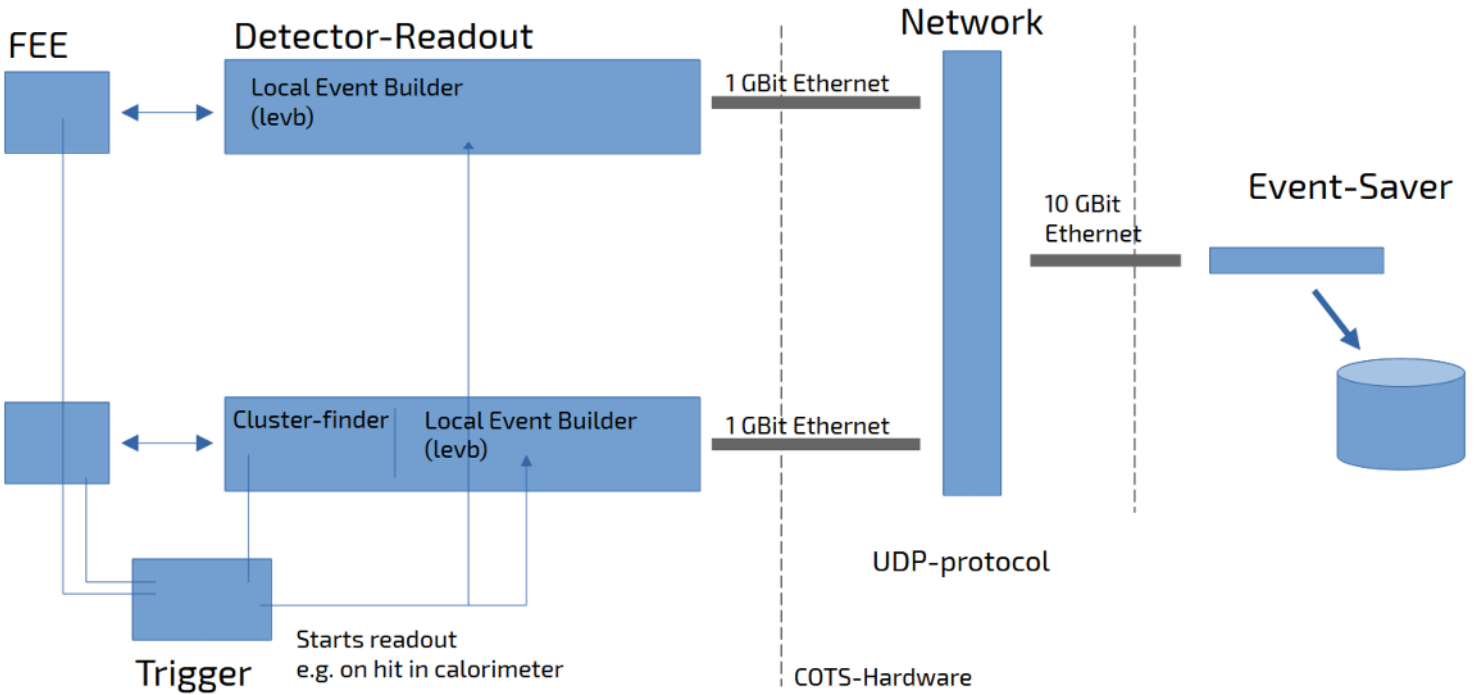
Current CBELSA/TAPS-DAQ structure



Features:
- VME based readout
- triggered
- data transport via UDP
- push architecture

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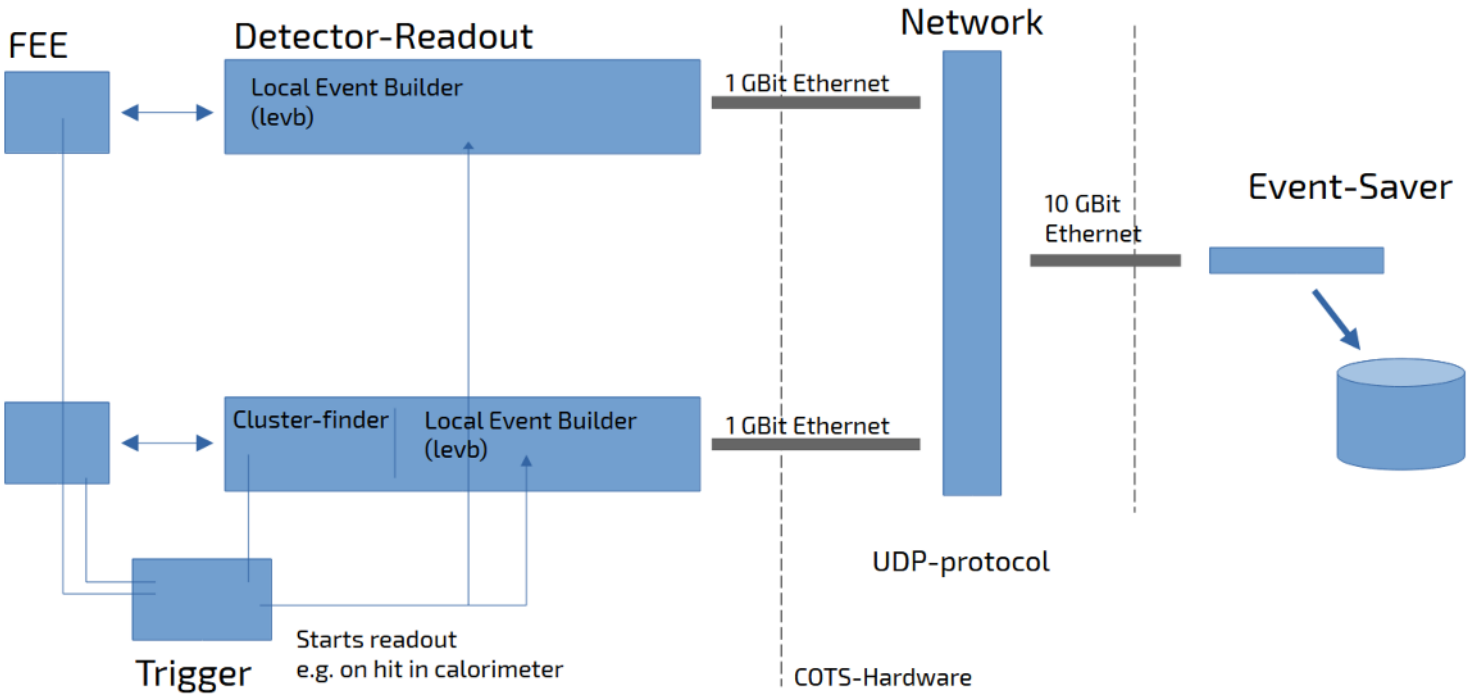

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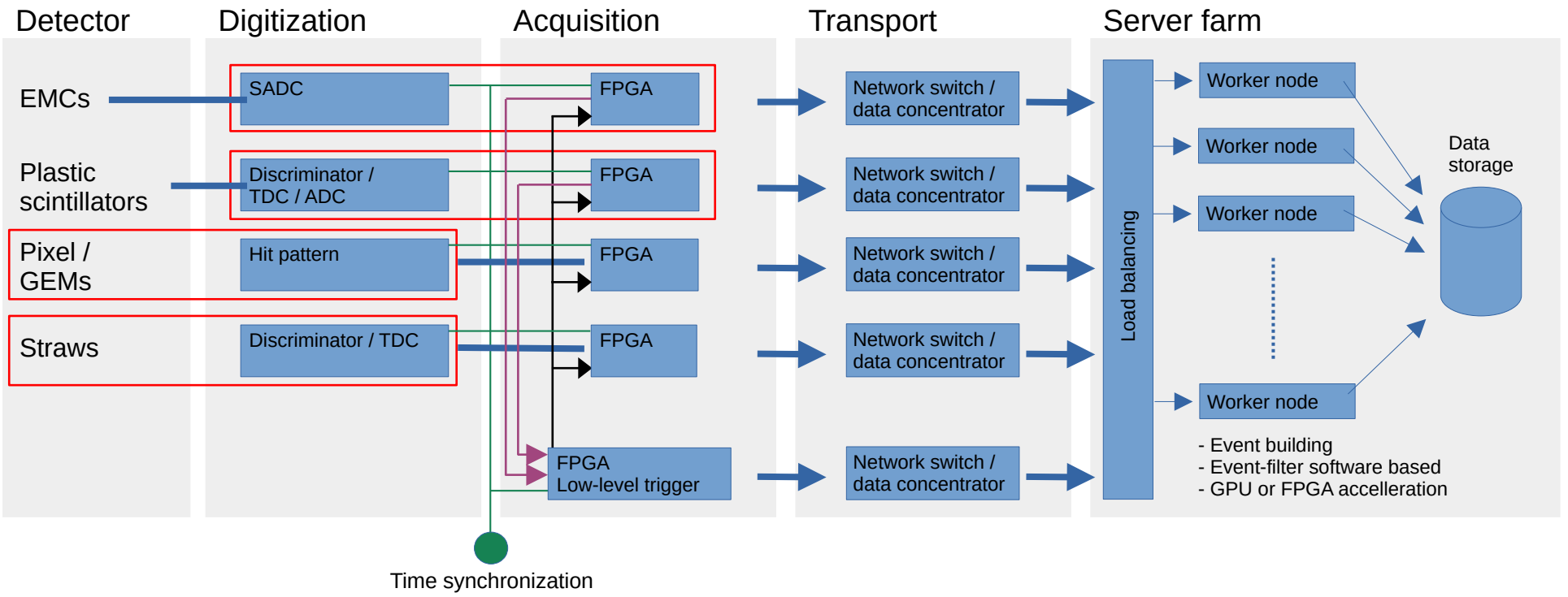
→ looks like DOGMA principle

Future DAQ of INSIGHT



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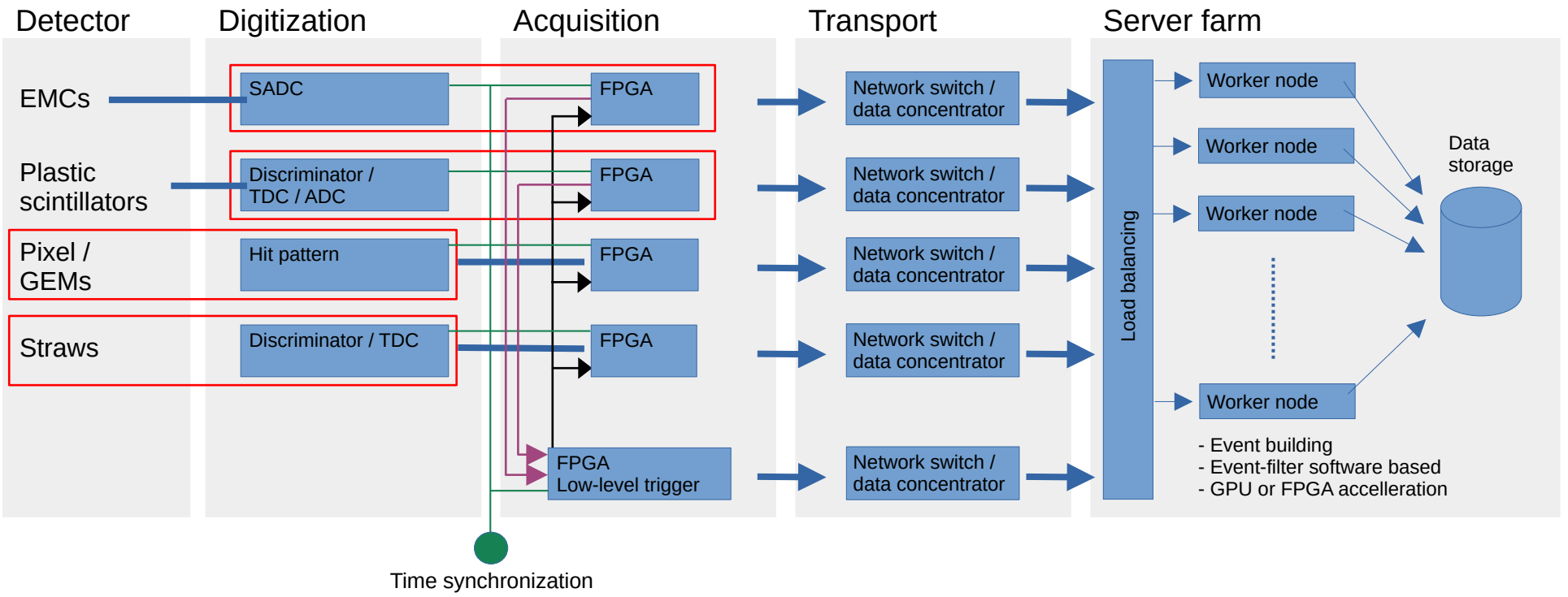

→ DOGMA-Hub sync may serve as time/(trigger) system

INSIGHT DAQ Platform

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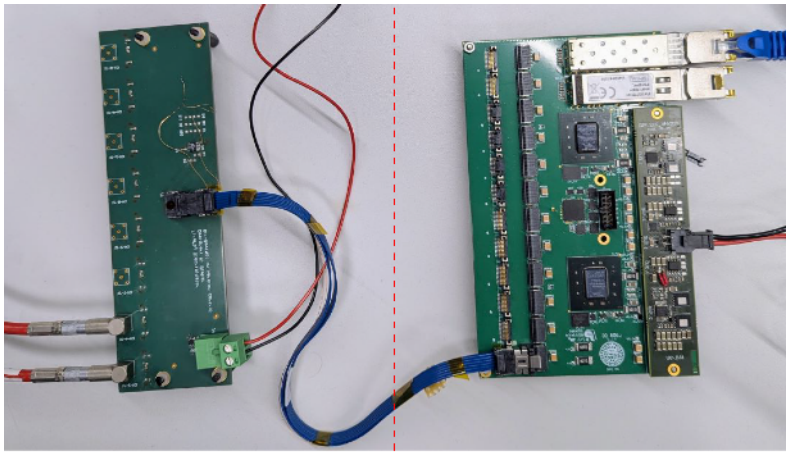
Goals

- Keep DAQ system as homogeneous as possible
- Separate Digitization and DAQ domains

Prototype (LVDS-DC)

- Based on SADC hardware
  - 2 x Kintex7 FPGAs
  - 2 x Gigabit Ethernet (SFP)
- Up to 72 LVDS channels per FPGA
- Share firmware framework with SADC

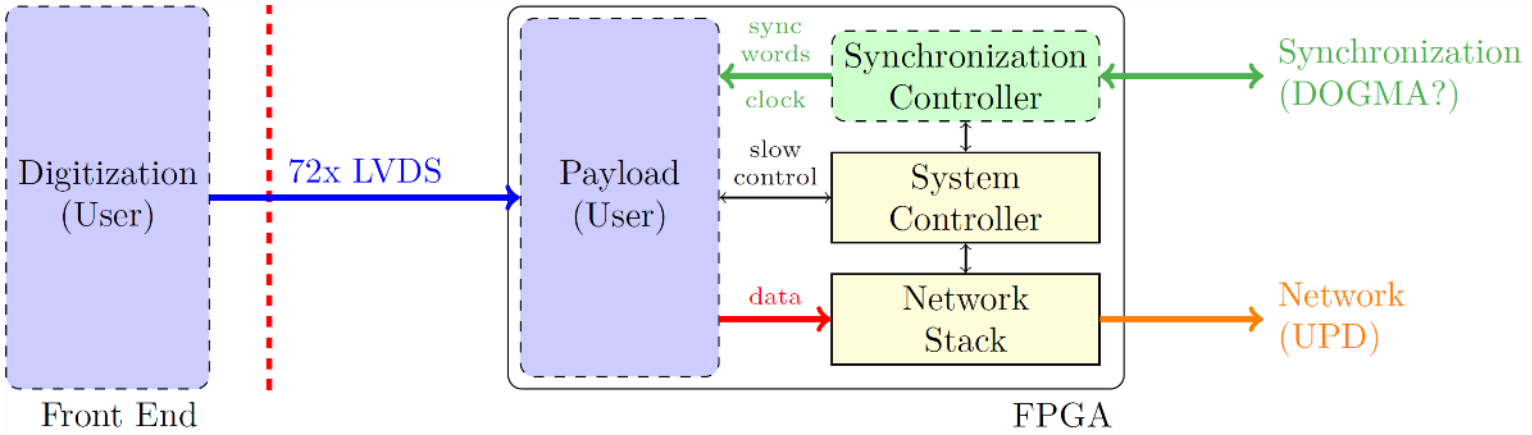


PANDA LVDS-DC

CB-SADC

PANDA-SADC

DAQ Firmware Architecture



- Focus on code reuse and maintainability
- Define clear interfaces
- Framework provides common functionality
  - Network Stack (UDP/IP Link)
  - Slow Control / Configuration
  - Time and Trigger distribution (to be implemented)

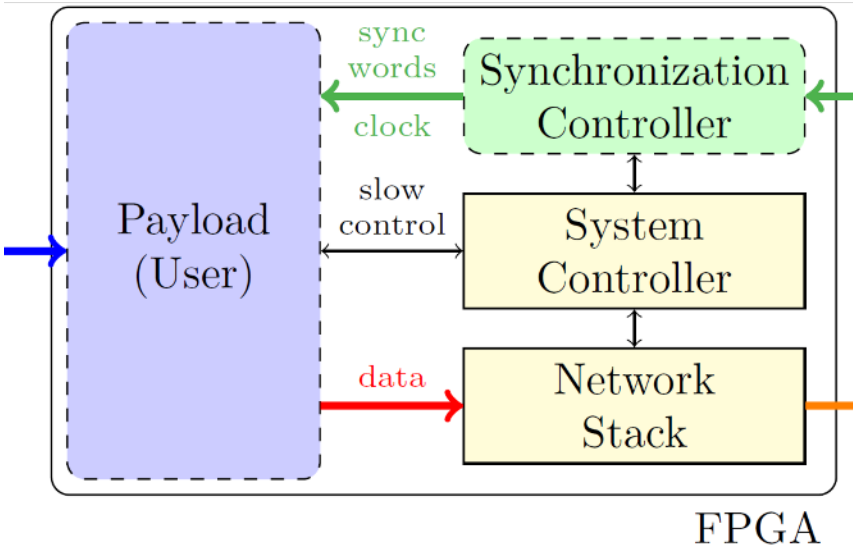
- Sub detector-specific payloads
  - SADC (CB and PANDA-FWEC)
  - TDL-TDC (Reference implementation for LVDS-DC)
  - Many more possible

Summary

- Continuing to use / evaluate DOGMA in the ToF test setup

- DOGMA seems promising candidate for overall timing distribution at INSIGHT
  → However, thorough evaluation needed

- Need to ensure
  - Integrability
    - Works with existing hardware?
    - Firmware open for modifications?
  - Scalability
    - Number of Synchronization links?
    - Cascading of DOGMA hubs?
  - Performance



- Interest to collaborate and contribute to DOGMA development

- Timing / synchronisation of INSIGHT detectors = important issue to be solved