FSD, NCAL, VETO

DAQ Systems

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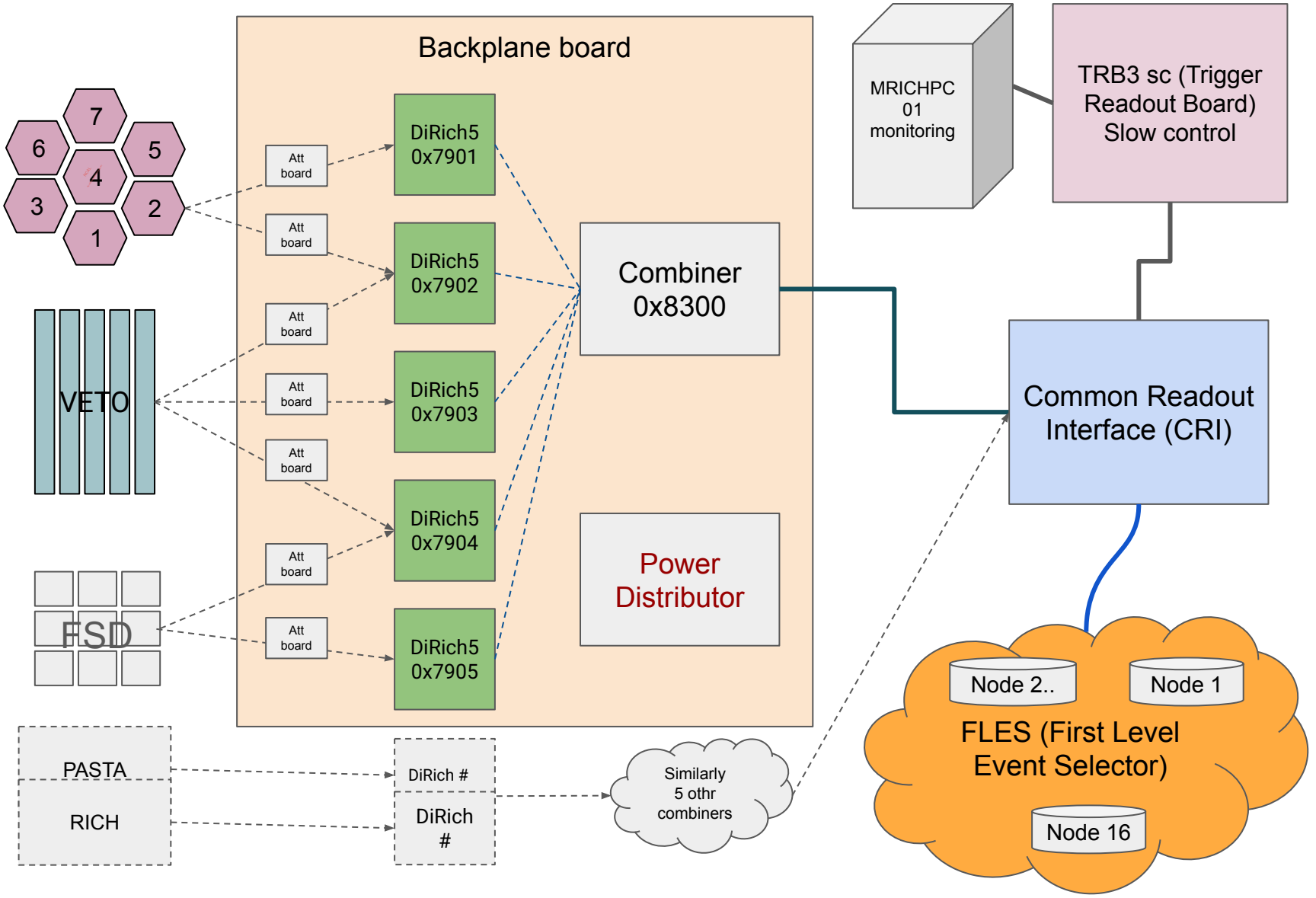
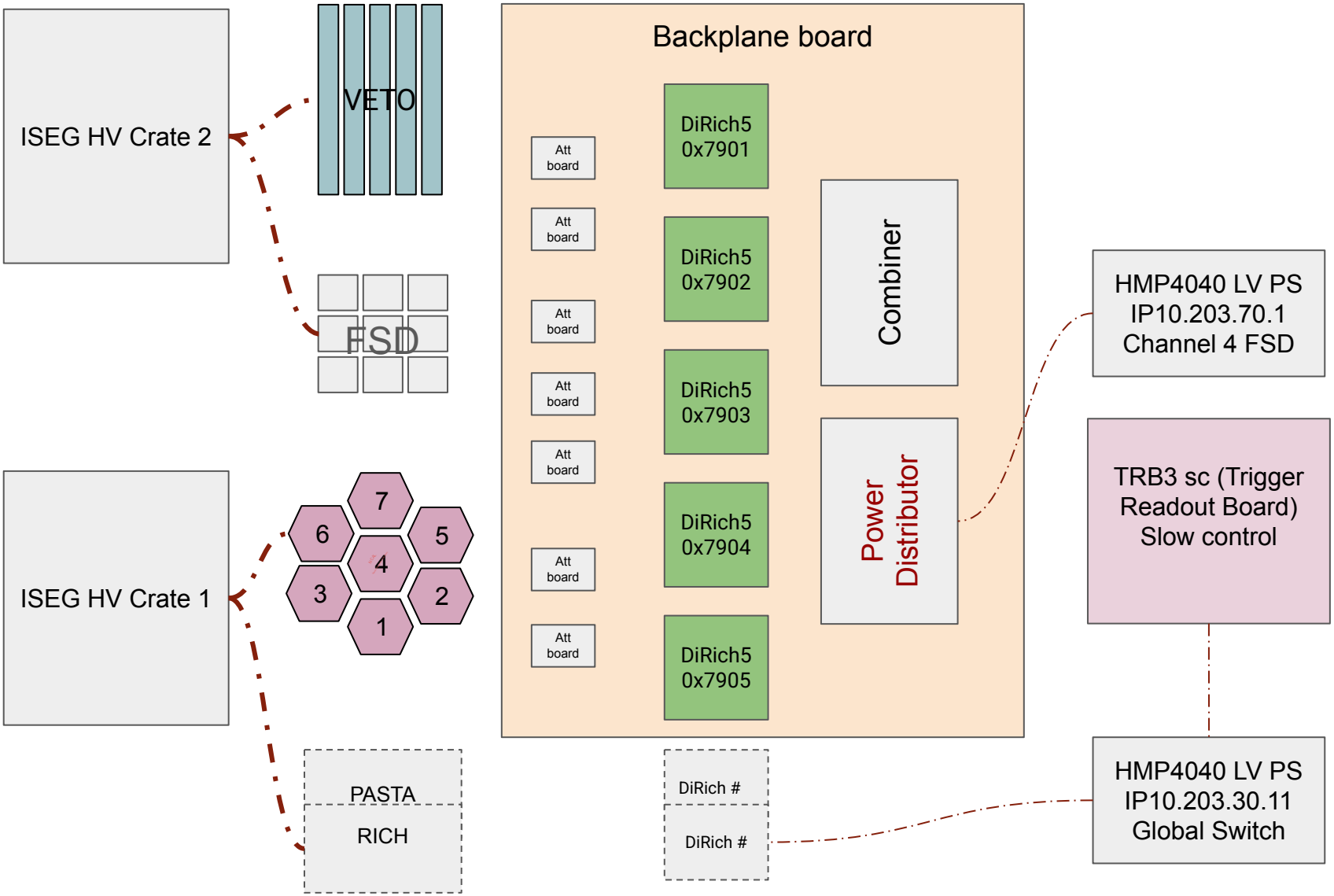
FSD, NCAL, VETO DAQ Flowchart



FSD, NCAL, VETO HV / LW Power



Mappings

FSD, NCAL, Veto: HV & Dirich configuration

All Dirich Thresholds are set -50mV, All HV are negative polarity

Detektor	Channel	HV line / addr / ch	DIRICH Module	Adapter Input#	DIRICH Channel	Att. Factor	HV Value
	1	0 / 3 / 9	0x7902	7	25 / 27	~ 100	
	2	0 / 3 / 10	0x7901	6	21 / 23	~ 100	
	3	0 / 3 / 11	0x7901	3	09 / 11	~ 100	
	4	0 / 3 / 12	0x7902	6	21 / 23	~ 100	
	5	0 / 3 / 13	0x7901	4	13 / 15	~ 100	
	6	0 / 3 / 15	0x7902	3	09 / 11	~ 100	
	7	0 / 3 / 15	0x7902	4	13 / 15	~ 100	
	NCAL is on Crate 1 - "big"						
	Veto is on Crate 2 - "small" in the cave						
	A1	0 / 0 / 1	0x7904	4	13 / 15	~ 10	
	B1	0 / 1 / 1	0x7904	6	21 / 23	~ 10	
	A2	0 / 0 / 2	0x7903	2	05 / 07	~ 50	
	B2	0 / 1 / 2	0x7904	7	25 / 27	~ 10	
	A3	0 / 0 / 3	0x7903	3	09 / 11	~ 50	
	B3	0 / 1 / 3	0x7903	8	29 / 31	~ 50	
	A4	0 / 0 / 4	0x7904	8	29 / 31	~ 10	
	B4	0 / 1 / 4	0x7902	5	17 / 19	~ 100	
	A5	0 / 0 / 5	0x7903	5	17 / 19	~ 50	
	B5	0 / 1 / 5	0x7902	2	05 / 07	~ 100	

FSD
beam direction

#	1x1	1x2	1x3
DIRICH ADDR	0x7905	0x7905	0x7905
Dirich ch	3/1	5/7	11/9
ATTENUATOR	2.2k - 1k	2.2k - 1k	2.2k - 1k
Voltage	-1150	-1150	-1150
HV Channel	Crate 2, module 0, CH 6	Crate 2, module 0, CH 6	Crate 2, module 0, CH 6

#	2x1	2x2	2x3
DIRICH ADDR	0x7905	0x7905	0x7905
Dirich ch	13/15	17/19	21/23
ATTENUATOR	2.2k - 1k	2.2k - 1k	2.2k - 1k
Voltage	-1000	-1000	-1000
HV Channel	Crate 2, module 0, CH 7	Crate 2, module 0, CH 7	Crate 2, module 0, CH 7

#	3x1	3x2	3x3
DIRICH ADDR	0x7905	0x7905	0x7903
Dirich ch	25/27	29/31	23/21
ATTENUATOR	2.2k - 1k	2.2k - 1k	4.7k - 1.5k
Voltage	-1100	-1100	-1100
HV Channel	Crate 2, module 1, CH 6	Crate 2, module 1, CH 6	Crate 2, module 1, CH 6

	ISEG Board	ISEG IP Add:	Channel numbers:	crate module address
HV crate 1 (RICH)	3:7400041	10.203.0.74	ch a0,a1,a2,a3,a4,a5	u300,u301,u302,u304,u305,u306
HV crate 1 (NCAL)	3:7400041	10.203.0.74	a9,a10,a11,a12,a13,a14,a15 (ncal)	u303,u307,u308,u309,u310,u311,u312,u313,u314,u315
HV crate 2 FSD, Veto	0:7400121 0:7400122	10.203.70.2	kein script	

Note: There are two versions of NCAL and Vetos , this document belongs to the one in mCBM cave

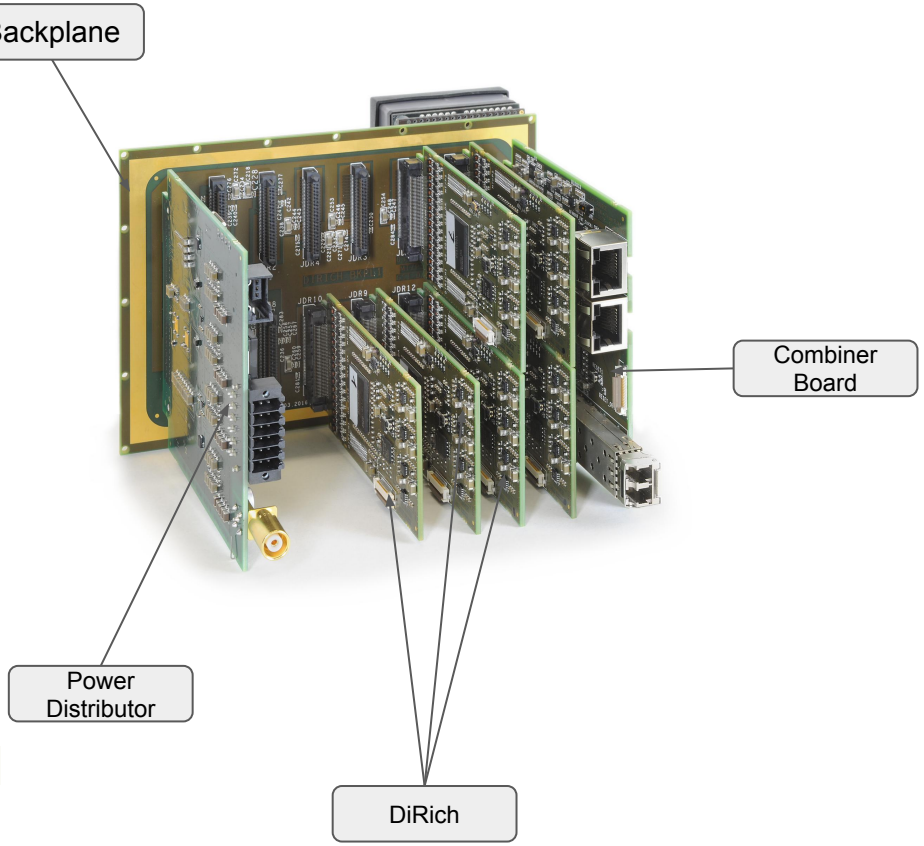
DiRICH - Full Module

And here it is, the complete module for the Hades and CBM RICH detectors: 6 64-channel MC-PMTs and all electronics for read-out

- The backplane (10x15cm) holds all components. 14 layers in the PCB route all analog and digital signals as well as power
- The power module regulates all necessary supply voltages and provides the HV connection
- The concentrator module connects to the central DAQ and provides trigger and slow-control to all read-out modules
- The DiRich front-end module with in-FPGA TDC and the analog preamplifier stage, see two posts below

An extensive description of the features can be found on a poster, presented at TWEPP 2016.

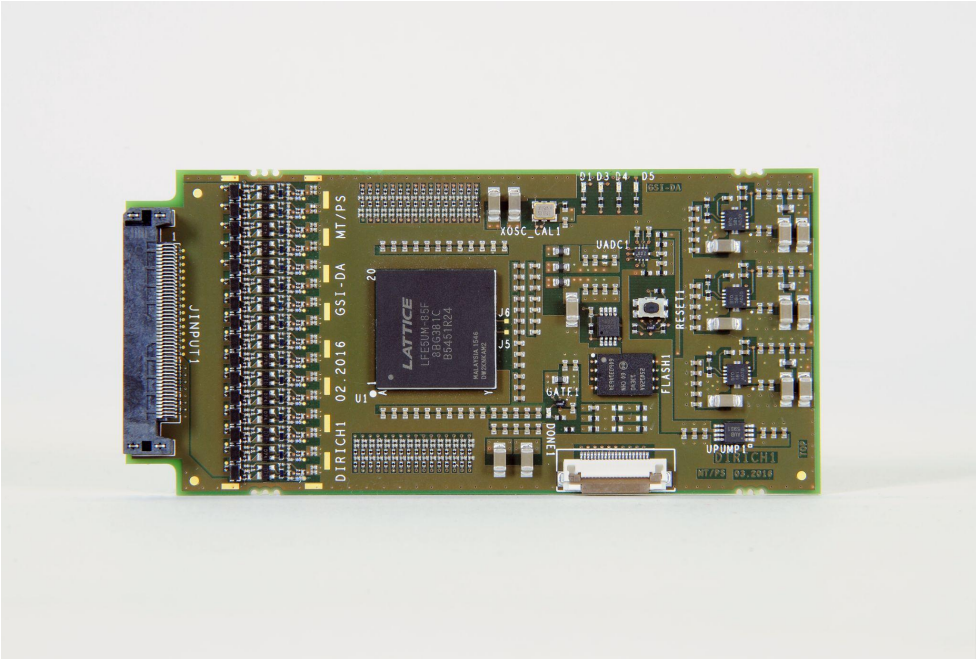
Photo: Gabi Otto, GSI



DiRich

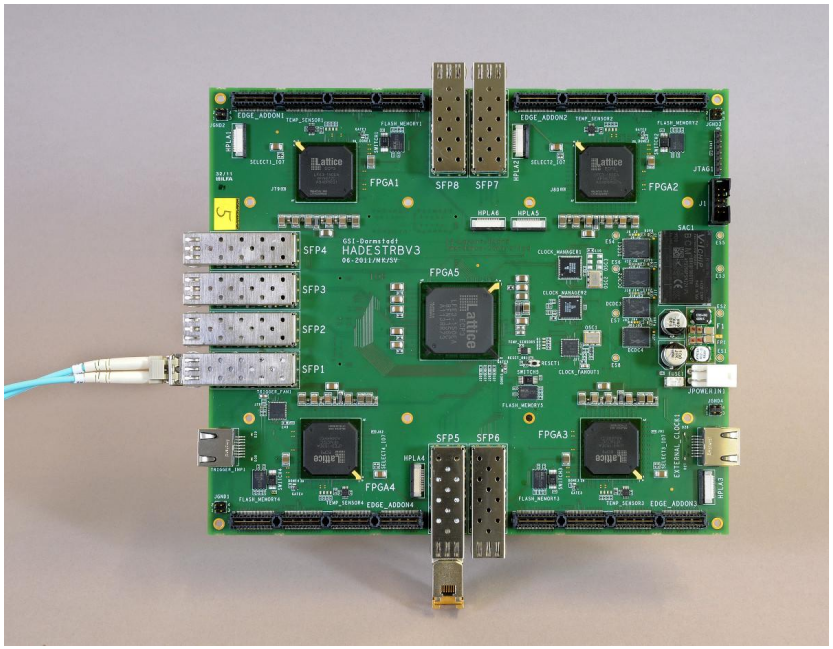
The DiRich board serves as a data acquisition platform that interfaces with photon detectors, collecting and digitizing signal information. It performs time measurement using Time-to-Digital Converters (TDCs) to accurately record signal arrival times. The board then transmits the processed timing data to the TRB3 system for synchronization and event building.

1. 32 channels
2. galvanic isolation of PMT to FEE (transformer)
3. ~factor 30 gain amplifier, 12mW
4. individual threshold for each discriminator
5. TDC with ~10ps intrinsic time precision (ToT measurement)
6. data acquisition system included (TRBNet)
7. data is sent out on the same connector
8. only one connector for everything => cable-free system



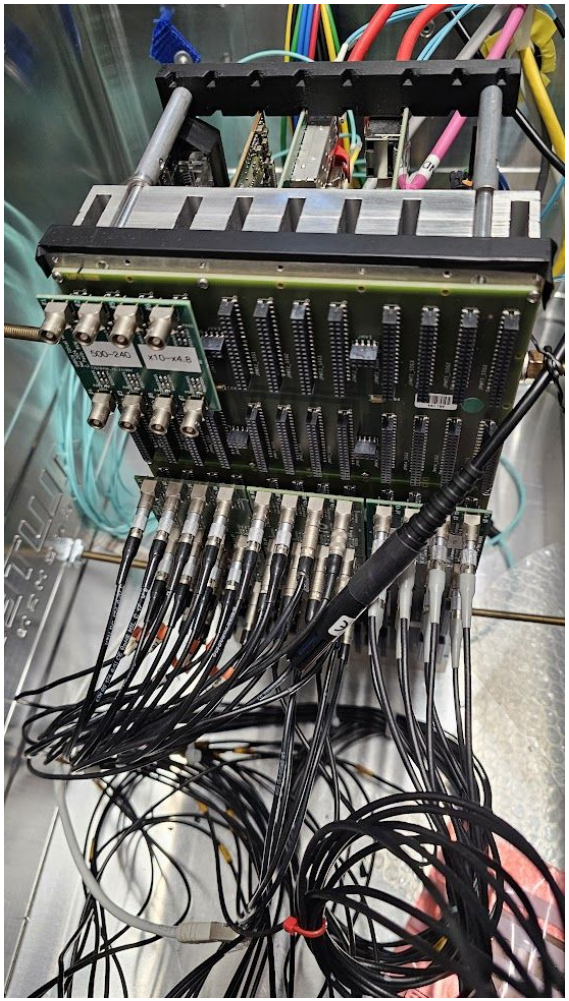
TRB3 - Trigger and Readout Board

In the DiRich scheme for CBM, the TRB3 serves as the central trigger and data acquisition platform. It generates timing signals, collects data from the DiRich detectors, and synchronizes the data streams. The TRB3 aggregates the data into coherent events and transmits them to the Eventbuilder for further processing. It also manages system control, monitoring, and error detection, ensuring smooth operation during experiments.



The TRB3 FPGA platform. (Image: G. Otto, GSI)

Box of Pandora



mCBM Cave