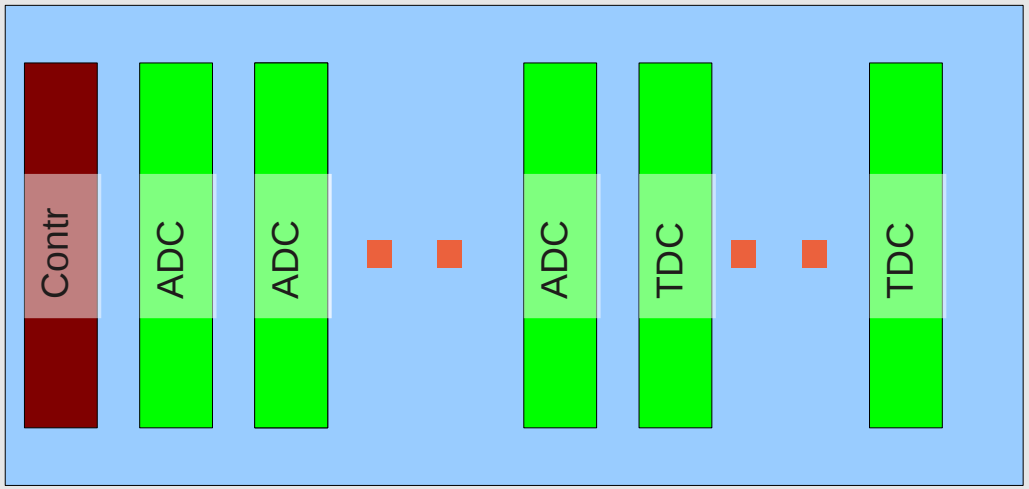
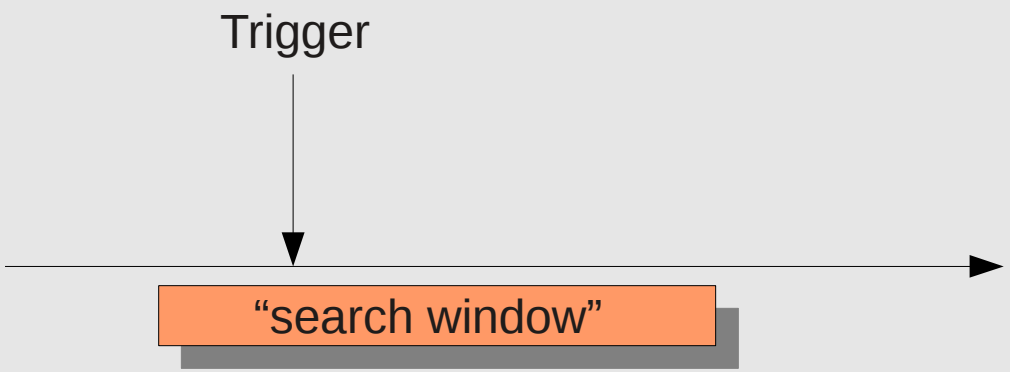
Overview

- DAQ for dE/dx tests
- Sampling ADC overview
- “free running” parameter extraction, triggerless data output, SODA
- Needed time sampling frequency
- Readout structure

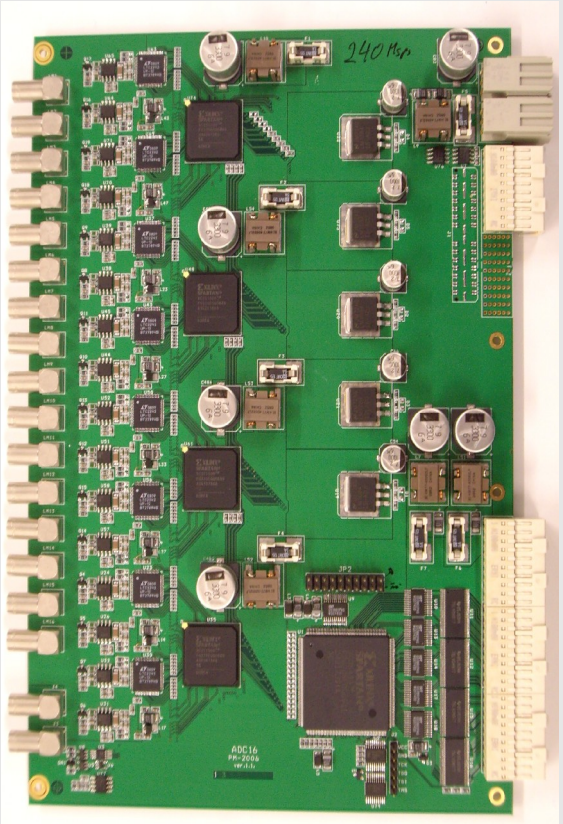
DAQ for dE/dx tests





- LVD Crate 80MHz bus
- 15 slots
- Controller with optical link
- SIS1100 as receiver in PC
- ADC + TDC
- ADC – 80/160/240 MHz
- TDC – F1/GPX
- Digitalisation free running 8us history window
- Parameter extraction after receiving trigger

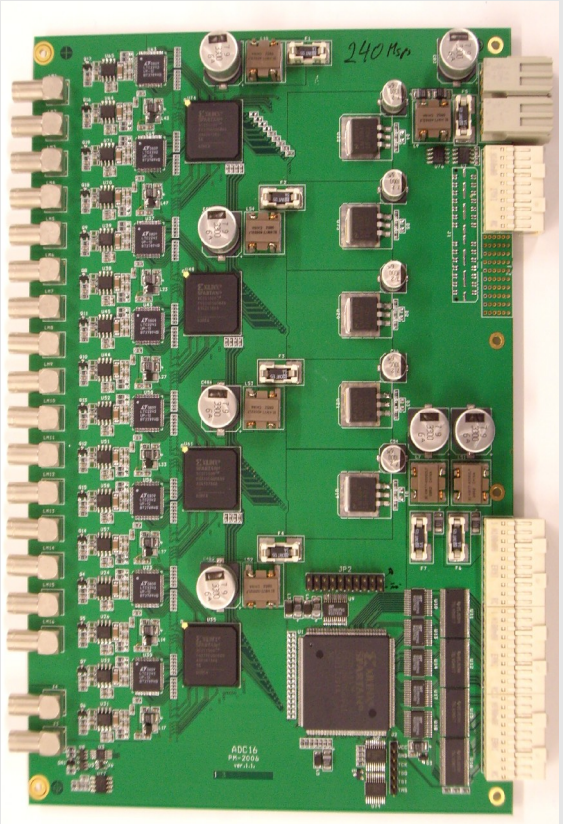
SAMPLING ADC



allrounder

egg-laying wool-milk-sow

SAMPLING ADC

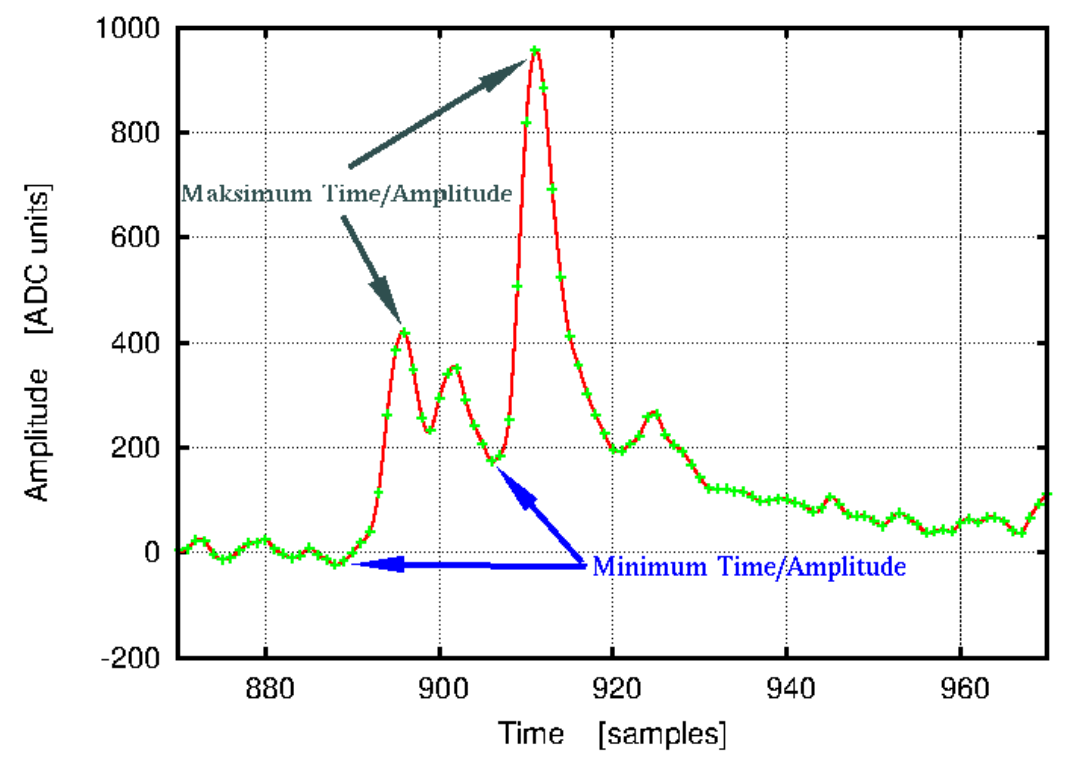


- 4x4 channels
- 240 MHz sampling rate
- 12 bit ADC (+/- 0.6V)
- Free running 8us history window
- Almost all settings per channel

Different functions in one module

- ADC
- TDC
- QDC
- Scaler
- Coincidence logic – self trigger
- Intelligent scope
- “running” baseline correction
- Digital input filter

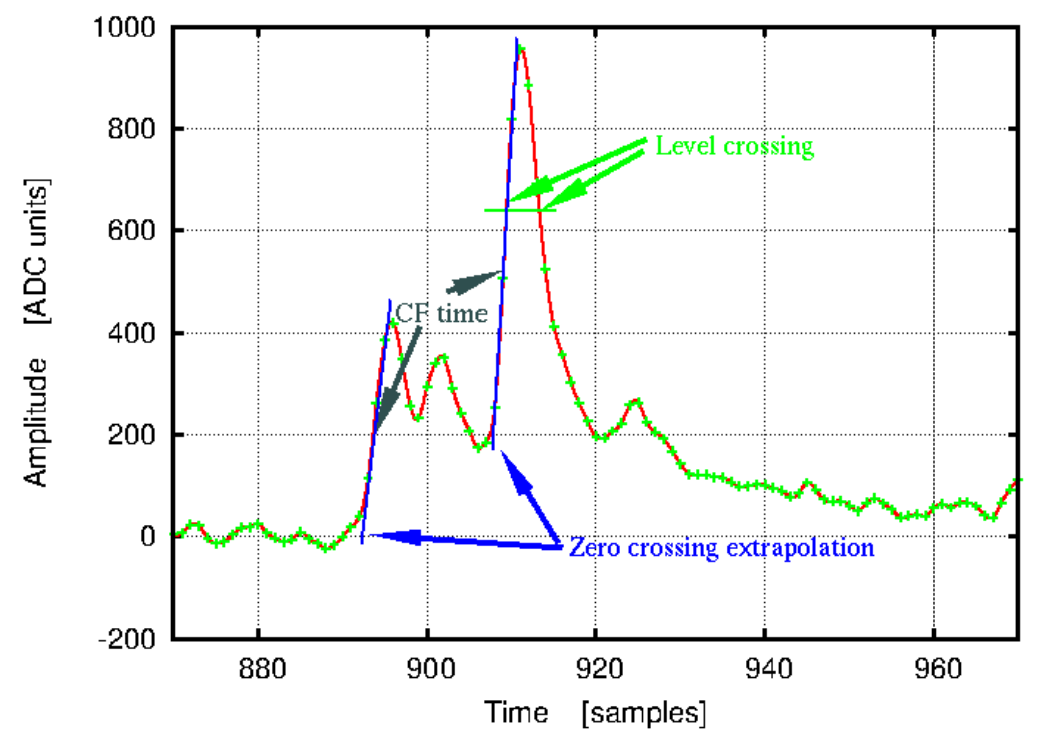
SAMPLING ADC - ADC



From FPGA signal analysis:

- Amp. and time of min
-
- amp and time of max
- pile-up detection
- Signal rise time

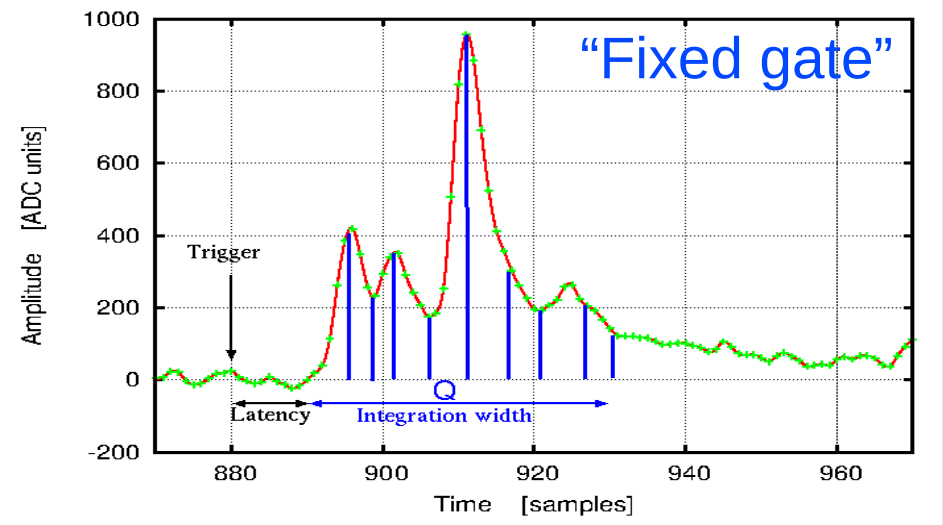
SAMPLING ADC - TDC

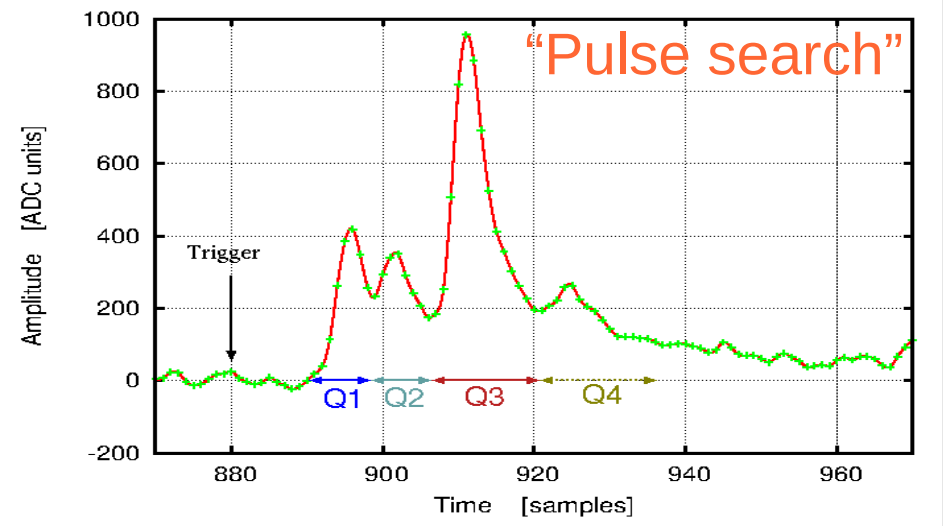


Times in 1/16 of "sampling bin" (ca. 0.26 ns)

- digital constant fraction
- zero crossing extrapolation
- level crossing (with min. width)
- min,max

SAMPLING ADC - QDC





"Fixed gate" – "standard" QDC mode

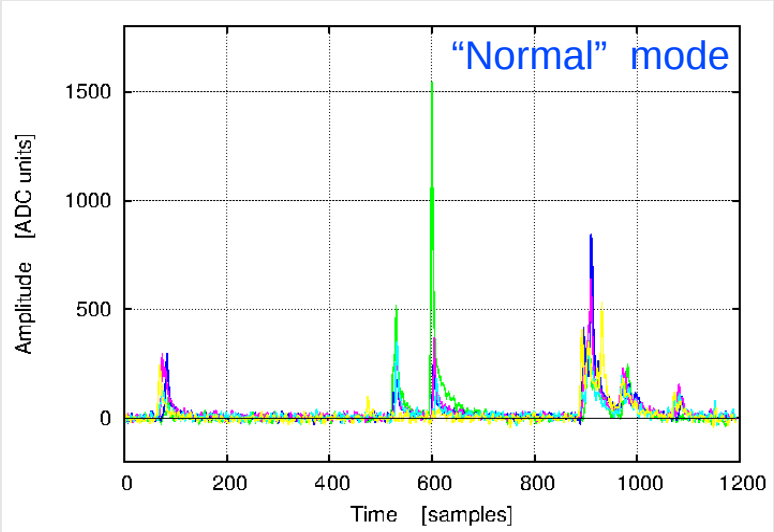
- "Q"
- Max ,grav. center, time, amp
- begin, end amp.

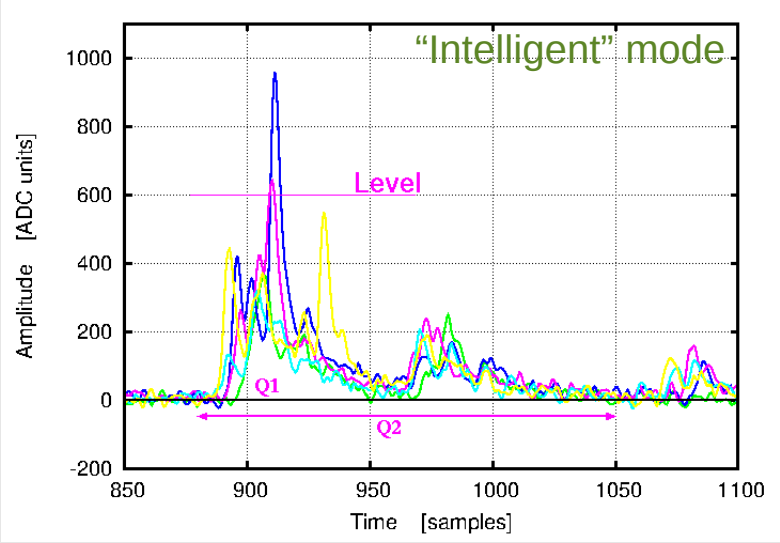
"Pulse search" QDC

- "Q" for each pulse (different modes, pile-up detection)
- "Q" for cluster (normal and delayed) for "straw" signal integration (and phoswich detectors)

"fixed gate" and "pulse search" windows can be set independent for each of 4 input groups

SAMPLING ADC - Scope





"Normal" scope mode

raw data from <= 8us search window before or after trigger

"Intelligent" scope mode

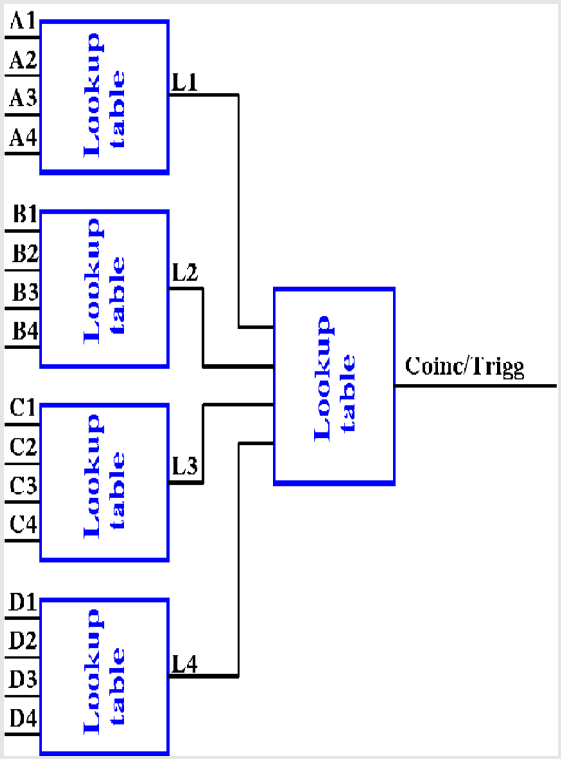
raw data from search window triggered by

- "fixed" Q
- cluster Q
- two different level crossing
- pulse existence

selected per channel by lookup table

Test mode - raw data synchronous or synchronous with selected time intervals

SAMPLING ADC – self trigger



Independent set for every channel

- logic level (+width) – also used for scaler
- delay
- length

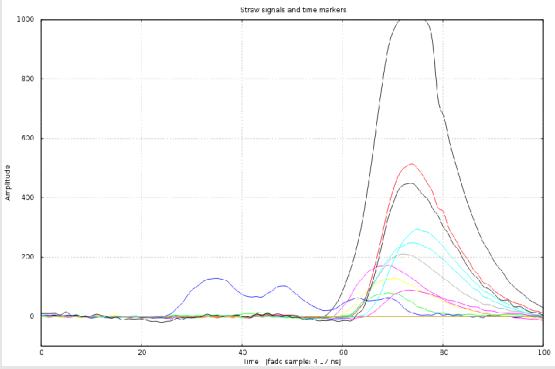
Coincidence set by lookup table for each Block (A,B,C,D)

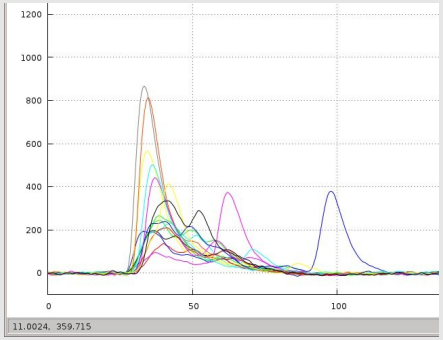
Logic outputs (L1,L2,L3,L4) can be again combined by lookup table

Coinc/Trigg can be used for synchronous trigger on all modules in crate (ADC+TDC) (self trigger)

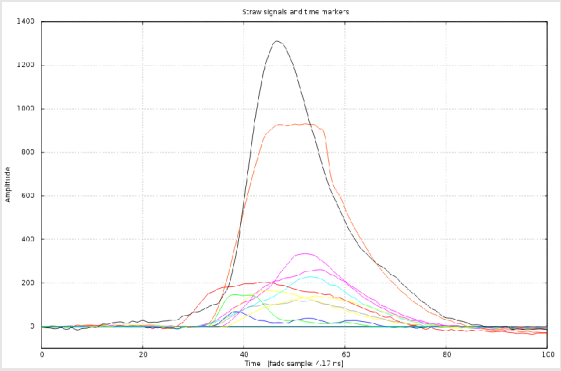
Why SAMPLING ADC

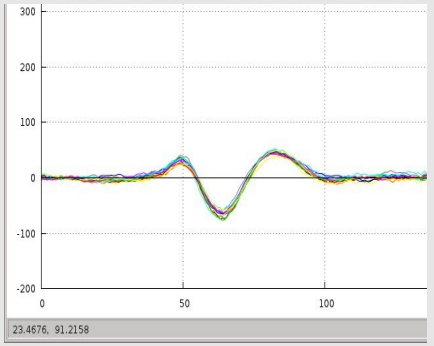
Pile-up's



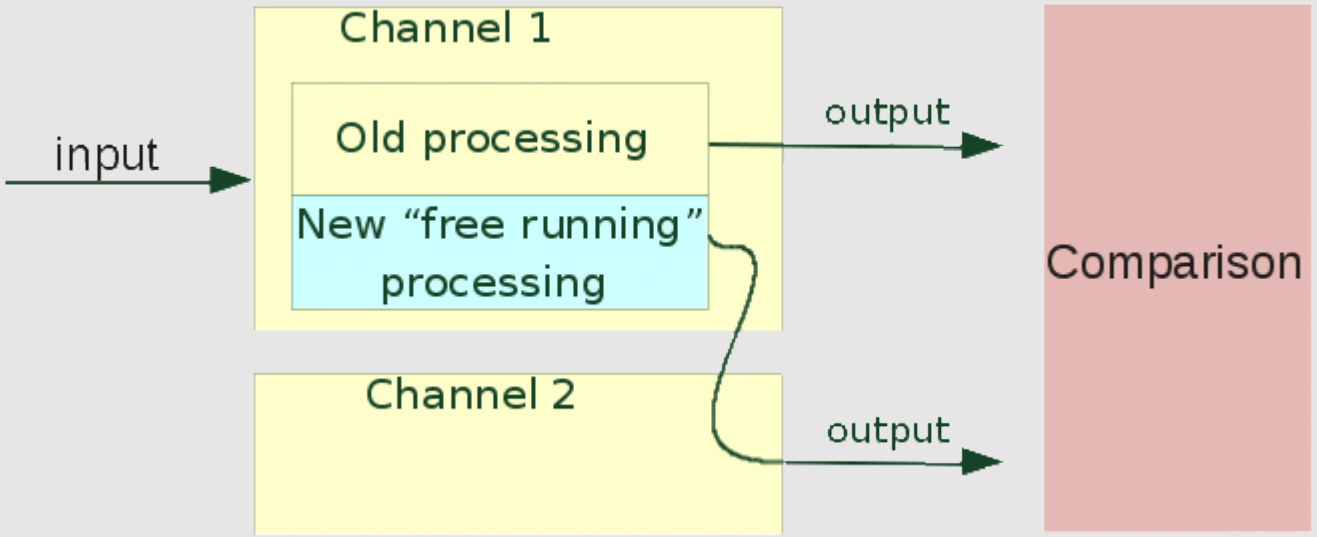


Overrange ,cross talk



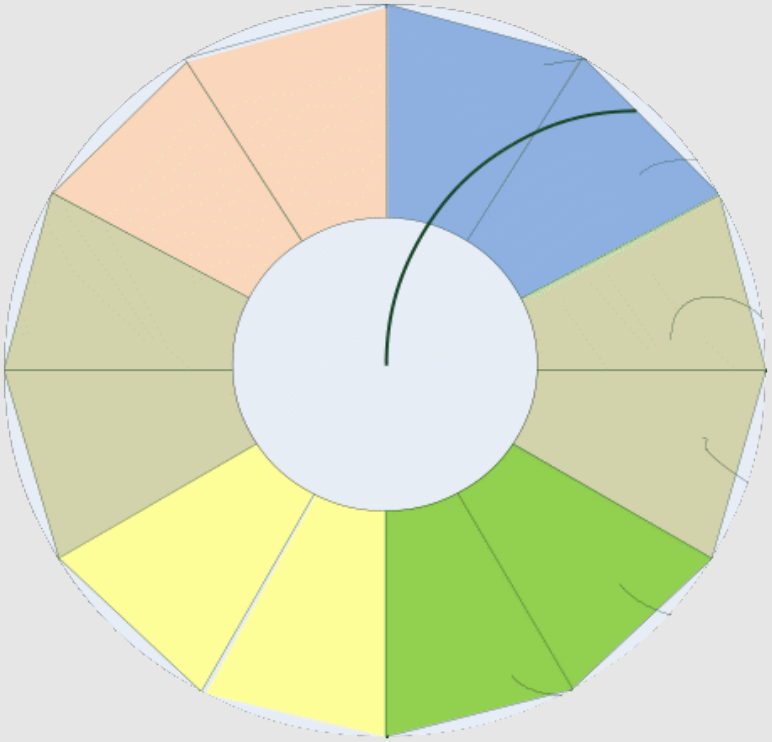


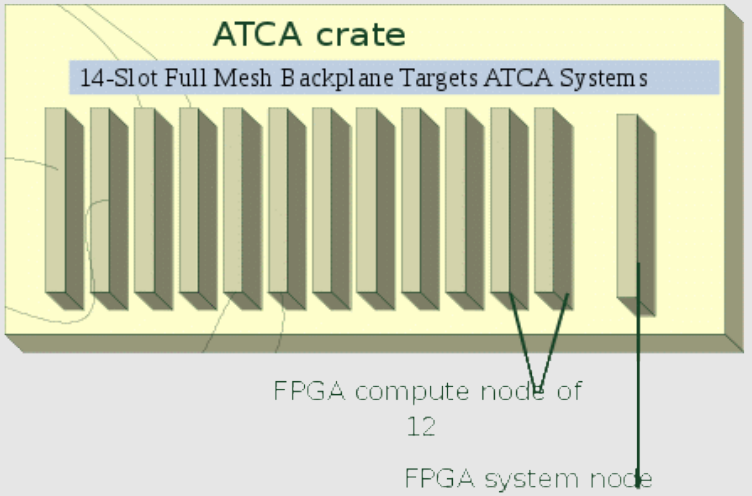
“free running” extension



Needed sampling frequency

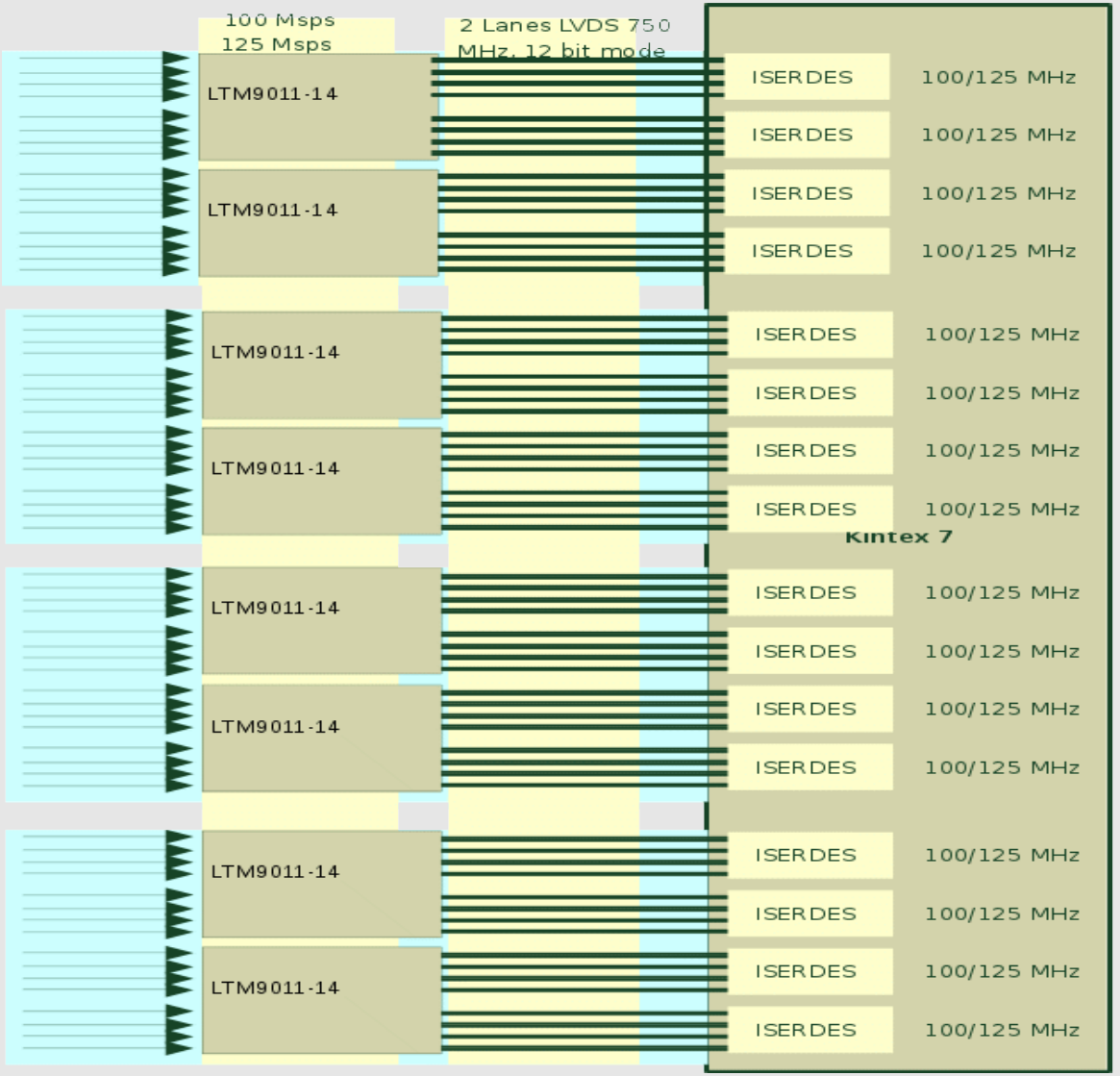
Readout structure





Power supply pro ATCA board: ADC LTM9011: 0,1W/ Ch.à400x0,1= 40 W;
FPGA Kintex max 12Wà12x11=132 W
Preis/channel 30..40 €

Readout structure



Readout structure