Results of the 2012 Juelich STT-FEE tests

Forschungszentrum Juelich,

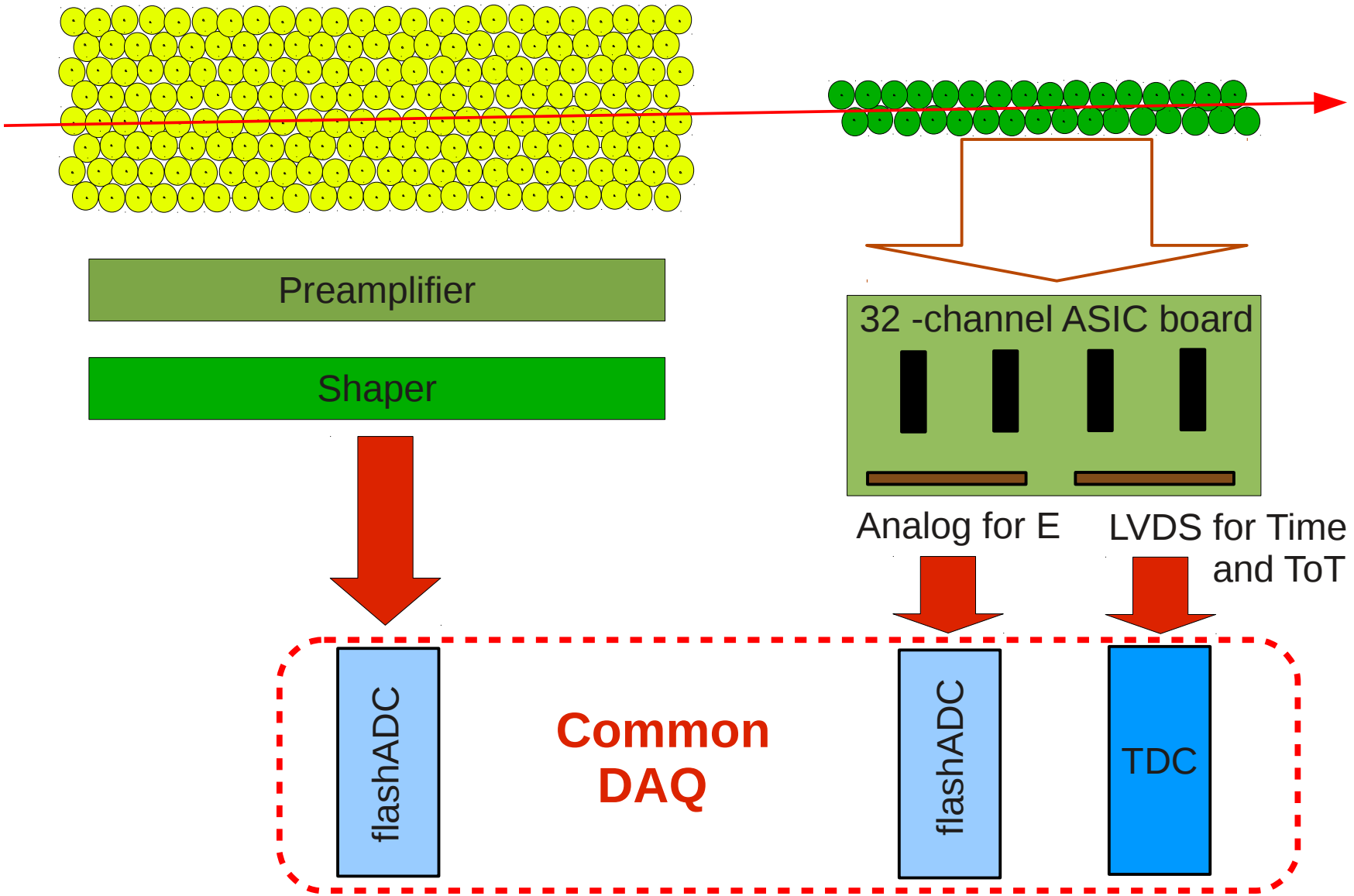
IFJ PAN Kraków,

AGH Kraków,

IF UJ Kraków,

…….

Two types of FEE have been tested



Discreet electronics – shaping amplifiers

Signal booster

16-channel charge preamplifier:

- **input impedance adjusted to straw impedance;**
- **2 stages:**
  - **integration amplifier,**
  - **voltage amplifier (gain factor 4).**

Shaper

16 channel shaping amplifier:

- **differential input amplifier (gain 1.4);**
- **signal tail cancellation;**
- **three integration stages;**
- **baseline restoration circuit at last integration stage.**

Total gain of each channel of whole system: 2.3 mV/fC
Noise level (peak-to-peak): 2 fC

Intermediate signal transmission: concentric cable up to 5 m long

8 prototypes installed and tested at proton beam together with PANDA STT Prototype. Available integration constants τ : 6-, 15-, 33-, 73-, 165 ns.

Search for optimal integration time of the system allowing simultaneous precise measurement of time and energy.

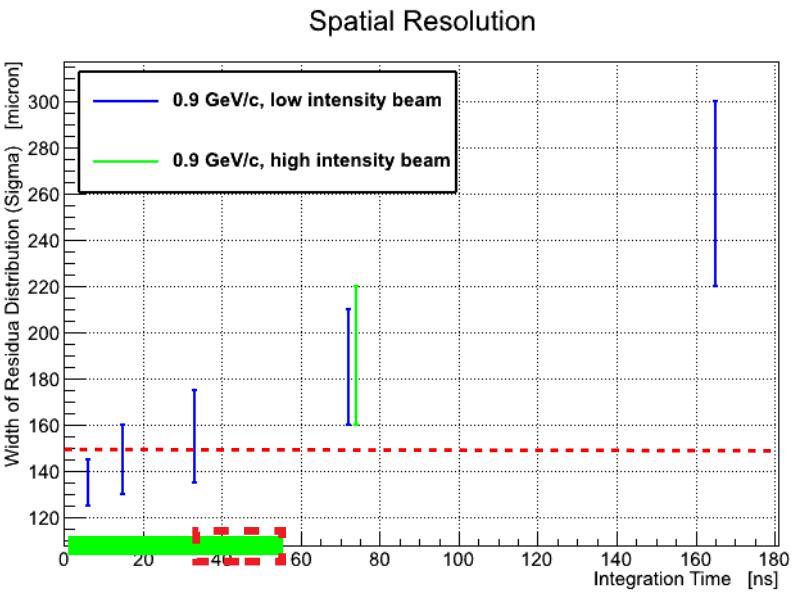
Short summary for discreet electronics

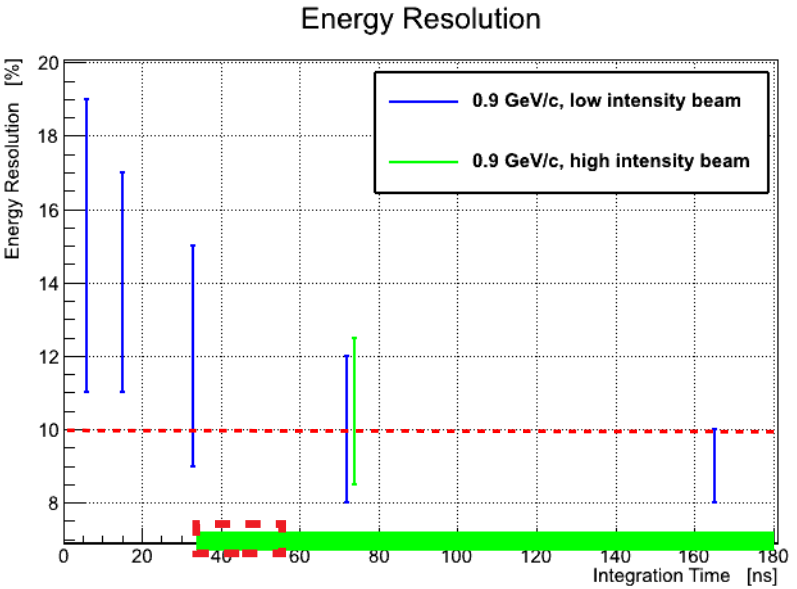
Advantages :

1. Feasibility of simultaneous measurement of track position as well as particle energy loss with precision demanded for PANDA STT (spatial resolution < 150 micron) (energy loss resolution < 10 %) is proved. (After careful signal shape analysis).

2. Obtained results are consistent with previous tests done with the use of current amplifier .

3. Both baseline stabilization as well as the tail cancellation are fulfilled by the present prototype of electronics.



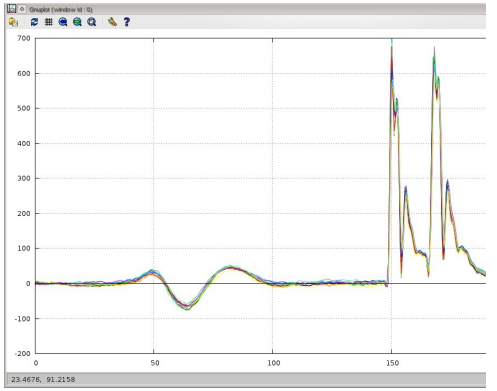


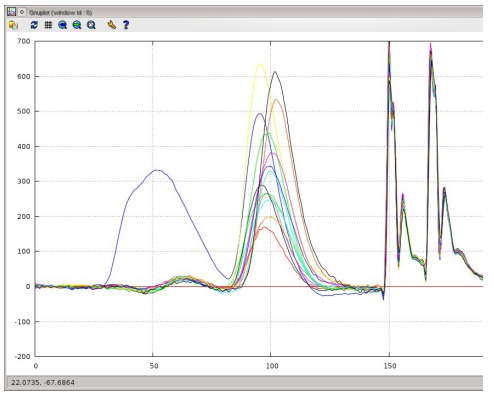
Short summary for discreet electronics

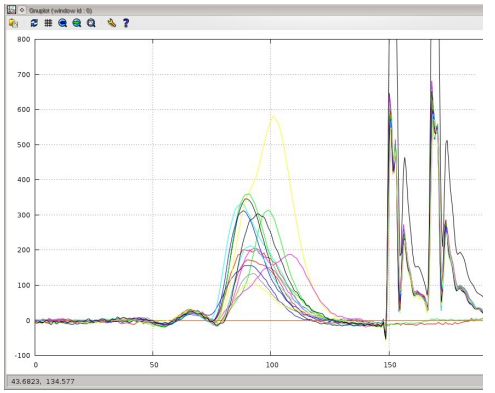
Disdvantages :

1. Observed cross-talk in electronics. Needs to be corrected in the design of the possible next prototype.

2. Preshaping stage of the booster amplifier needs to be shifted to the main shaper in order to simplify the preamp and reduce its dimensions.

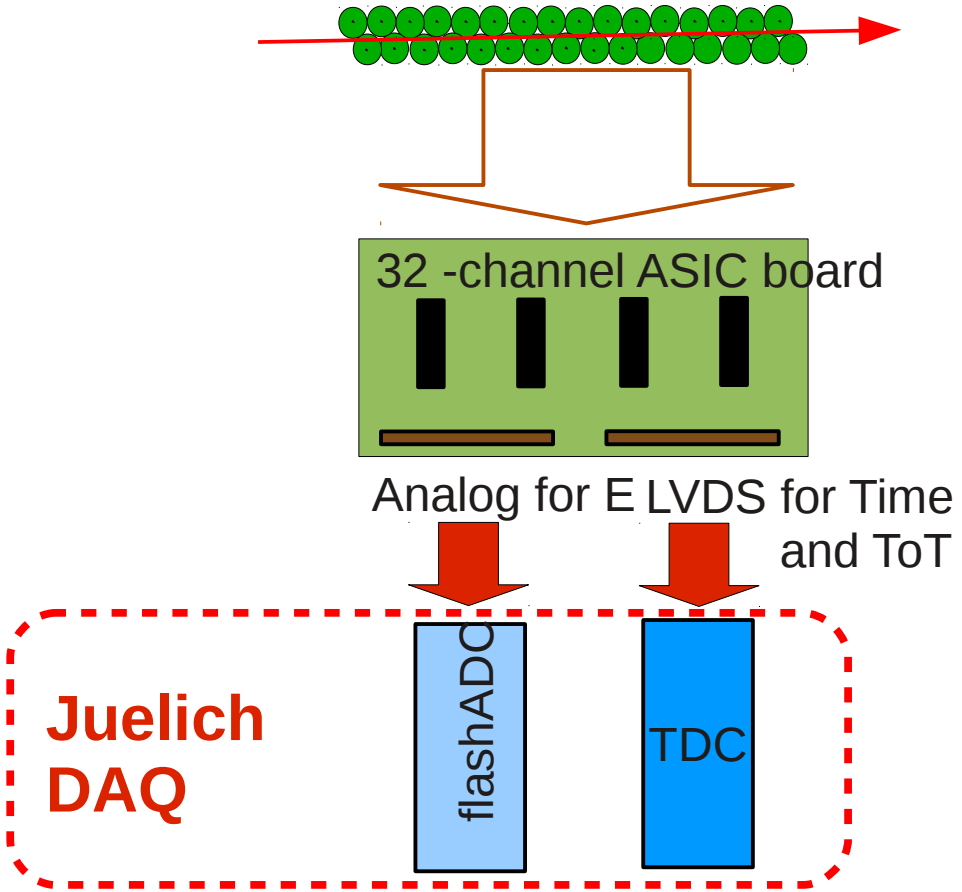






Test of ASIC

ASIC performance @ 900 MeV/c and 600 MeV/c
Beam intensity 100 – 500 kHz/straw
Data collected in fADC + TDC



Problems with efficiency and position resolution

p_beam = 600 MeV/c

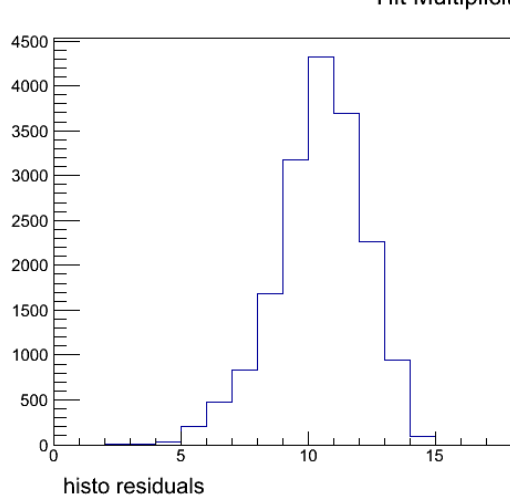
Low efficiency ?

Why ?

Previous test shown almost 100 % detection efficiency of straws+FFE

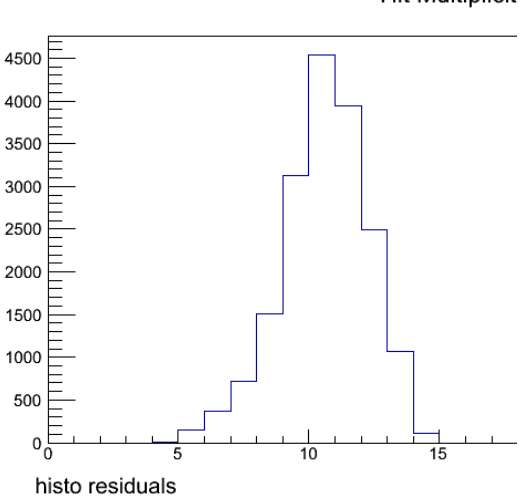
Residua distribution worse than expected !

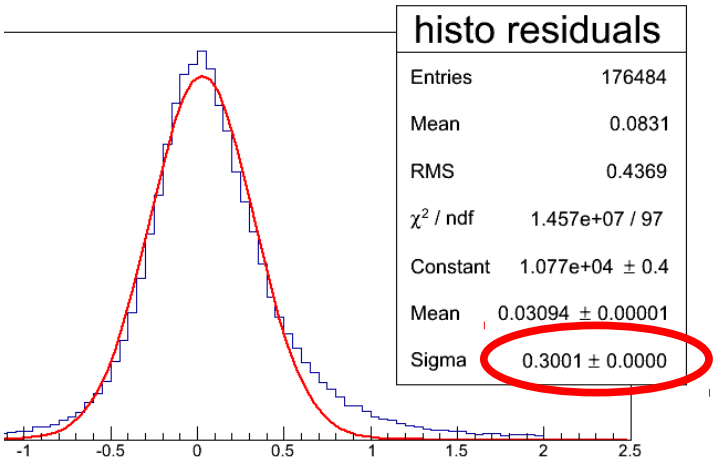
Time from TDC

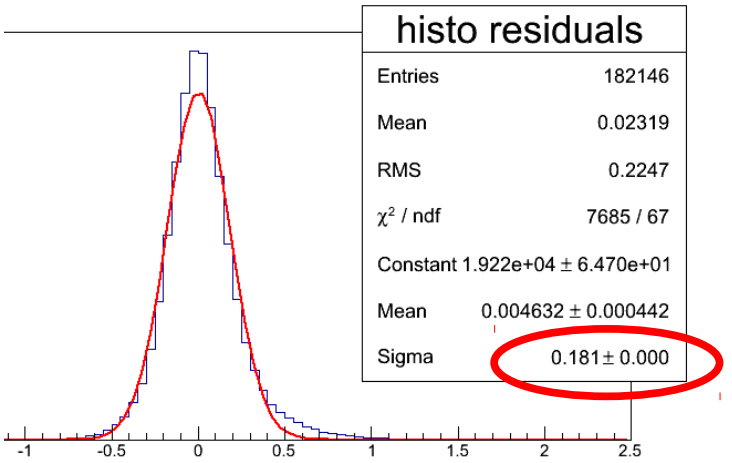


Expected maximum ~ 15-16

Time from fADC

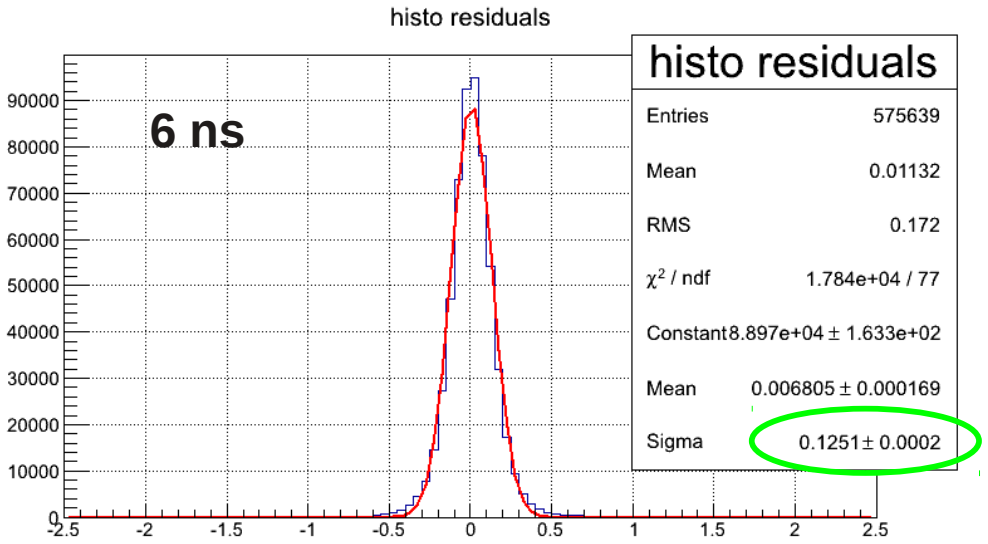


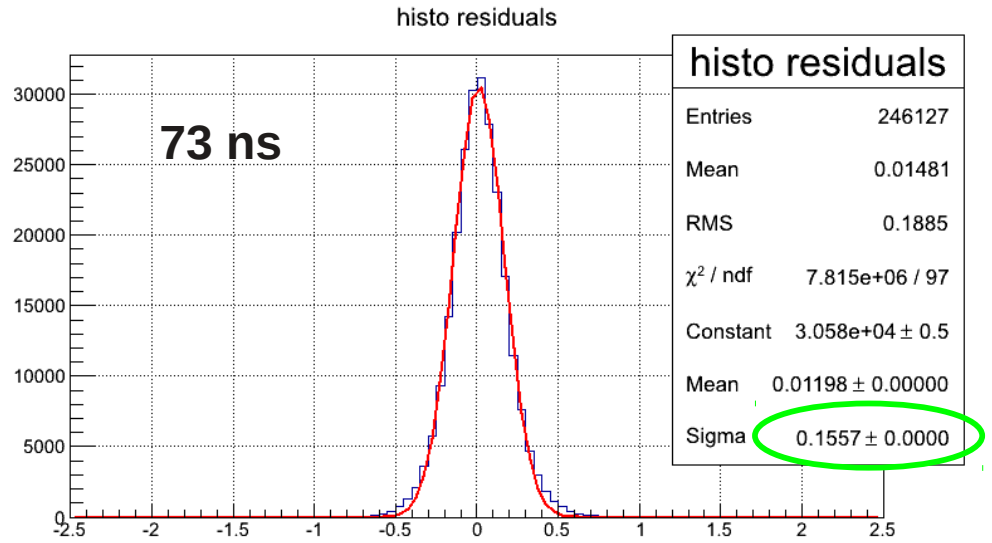




Compare: results for shaping amplifier

Results of position resolution are not biased with the deficiencies of calibration and tracking method since for shaping amplifier, with exactly the same calibration and tracking the results are decent.

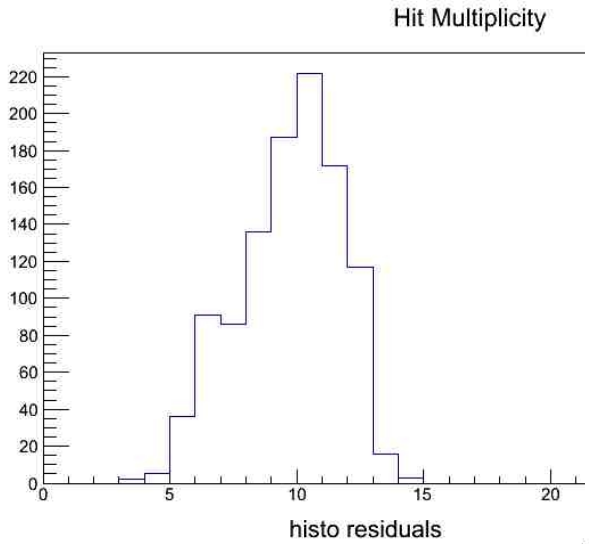


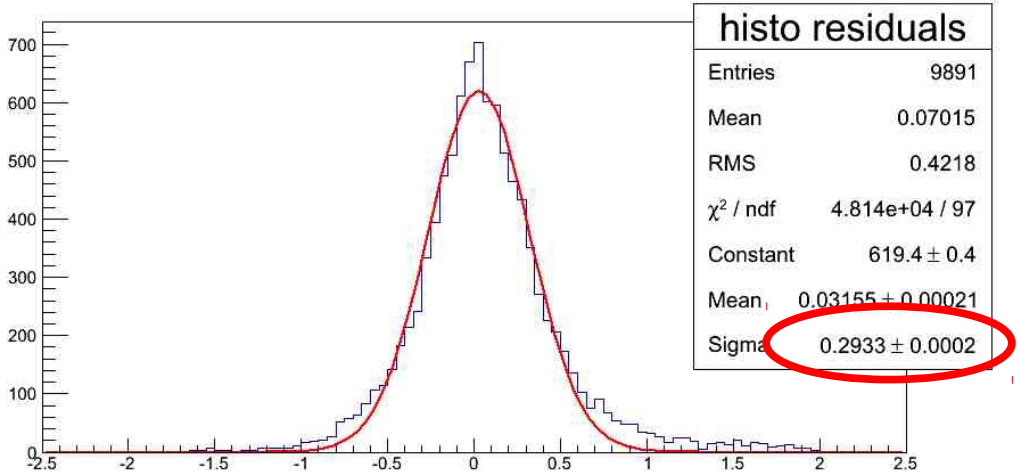


Problems with efficiency and position resolution

p_beam = 900 MeV/c

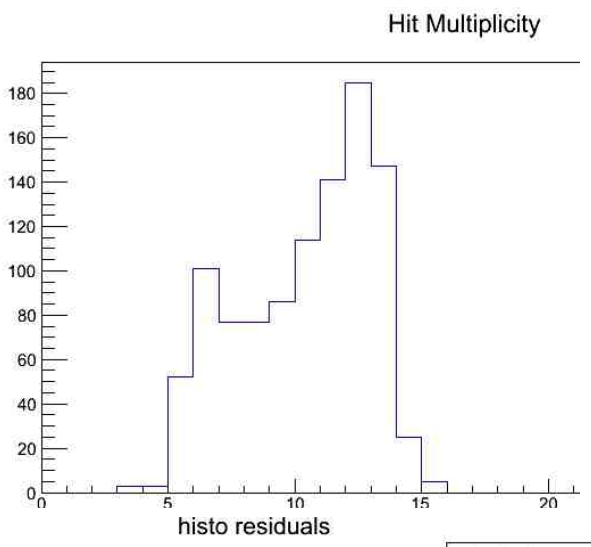
Time from TDC

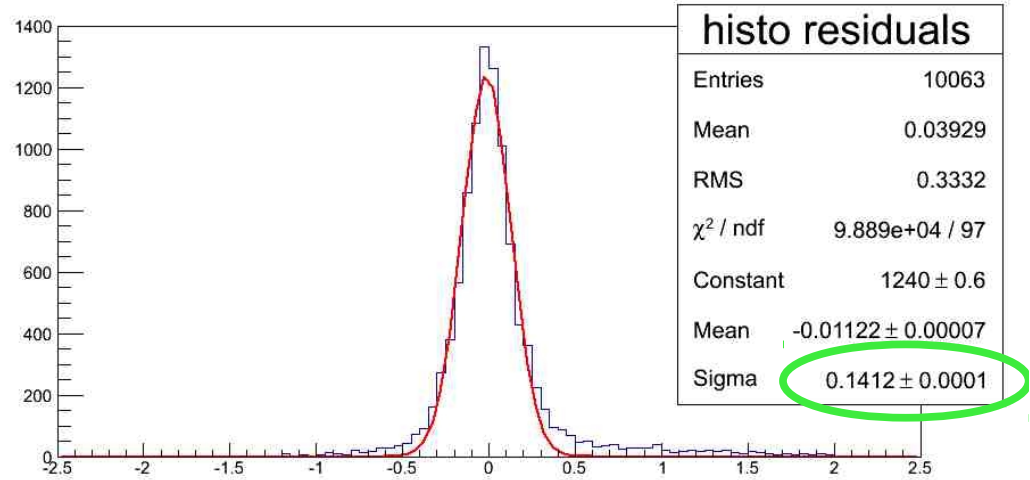




No improvement !

Time from fADC





Improvement !

Possible reason of problems

Significant variation of gain (?), threshold (?) or baseline position (?) over individual channels of ASIC ?

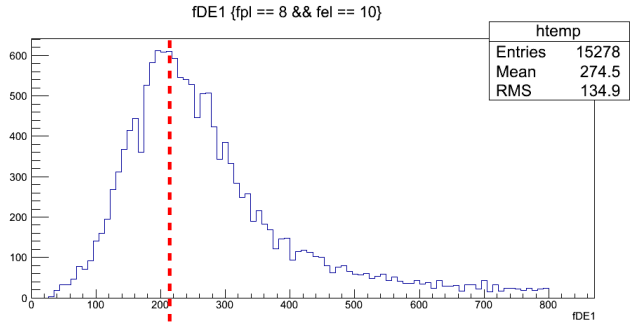
Layer1

Limited dynamic range of ASIC : fluctuations in amplitudes over channels cause significant drop of efficiency ?

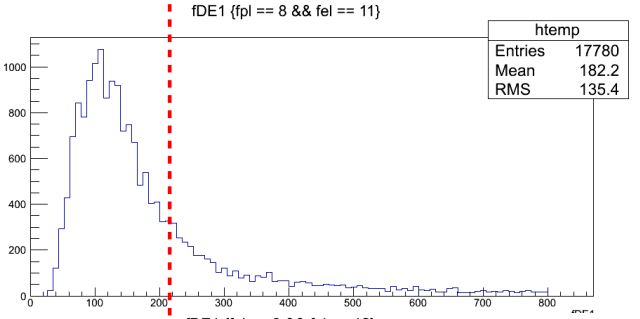
Problems with discriminator of ASIC ?

Channels of the lower amplitudes are subject to stronger walk error which can not be compensated offline.

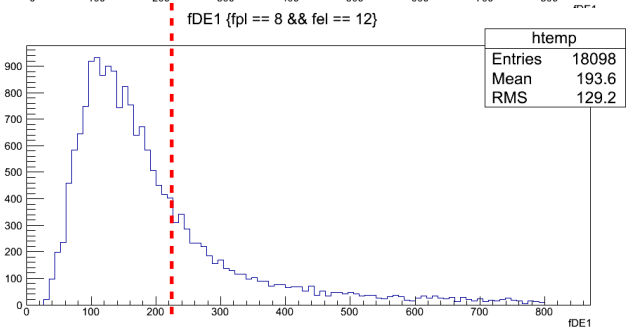
Straw 10



Straw 11



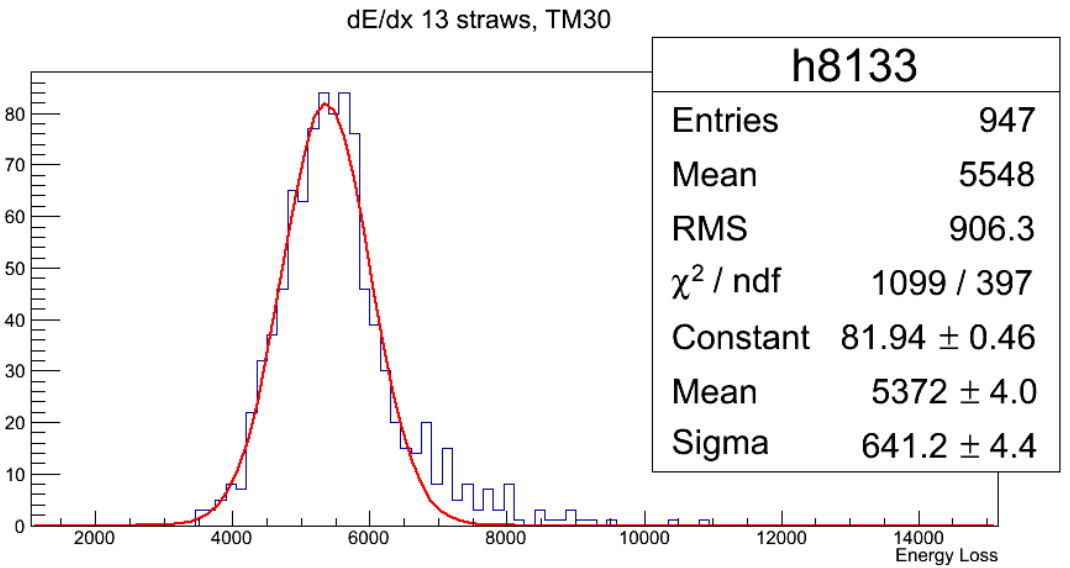
Straw 12



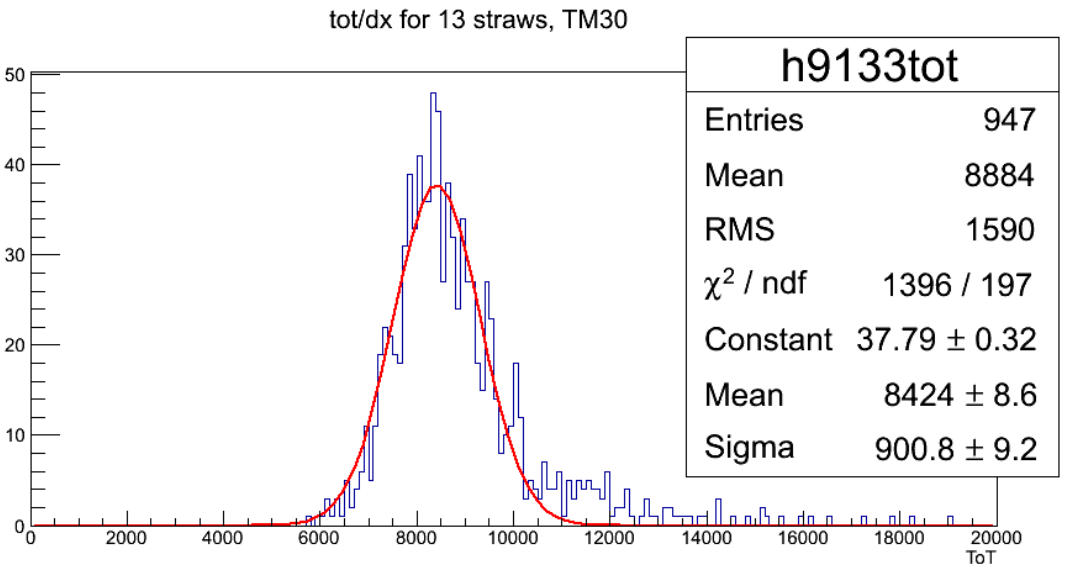
Energy loss and ToT

Integration of analog signals from ASIC.

Expected ~ 11 %



13 +- 1 %



12 +- 1 %

Conclusions

Unexpected problems with efficiency and timing resolution of ASIC discovered.

Results confirmed by two independent analysis (J.B. & K.P.).

(Manual) analysis of analog signals of ASIC has shown that efficiency and position resolution can be improved.

Energy resolution derived from integration of analog signals from ASIC is worse the expected.

Reasons have to be identified and avoided in the next iteration of ASIC prototype.

Backup slides

STT FEE test at COSY proton beam during September FAIR week

Time: **21-23 0.9.2012**

Available beam momenta: **2.0 GeV/c, 0.9 GeV/c**

Beam intensities: **30 - 100 kHz (low intensity)**
1 – 2 MHz (high intensity)

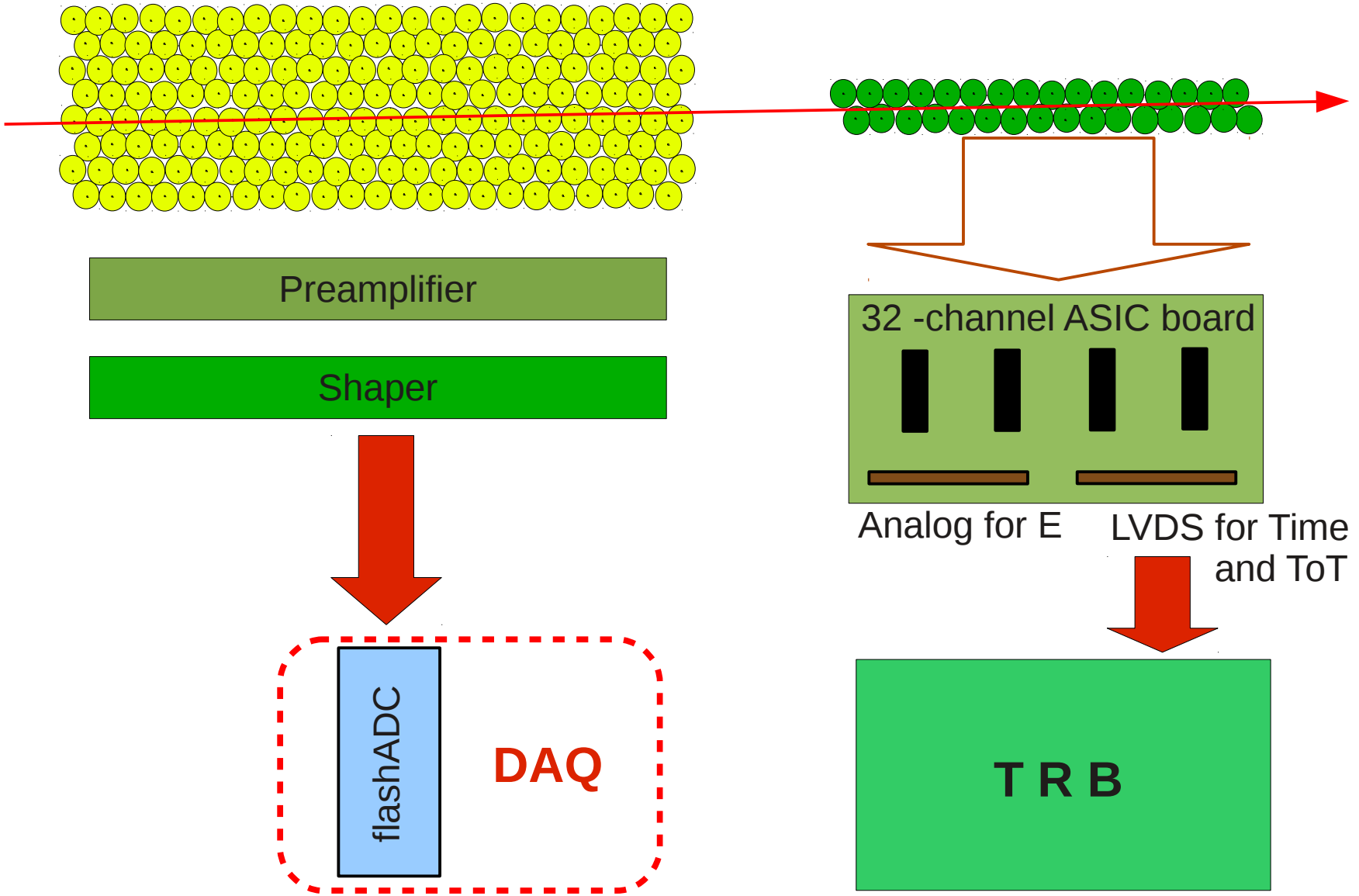
1. ASIC – specialized, programmable chip allowing for tail cancellation and baseline restoration:
   - time information (digital) (+ Time over Threshold → energy)
   - energy information (analog)

AGH University + Jagellonian University Kraków (Poland)

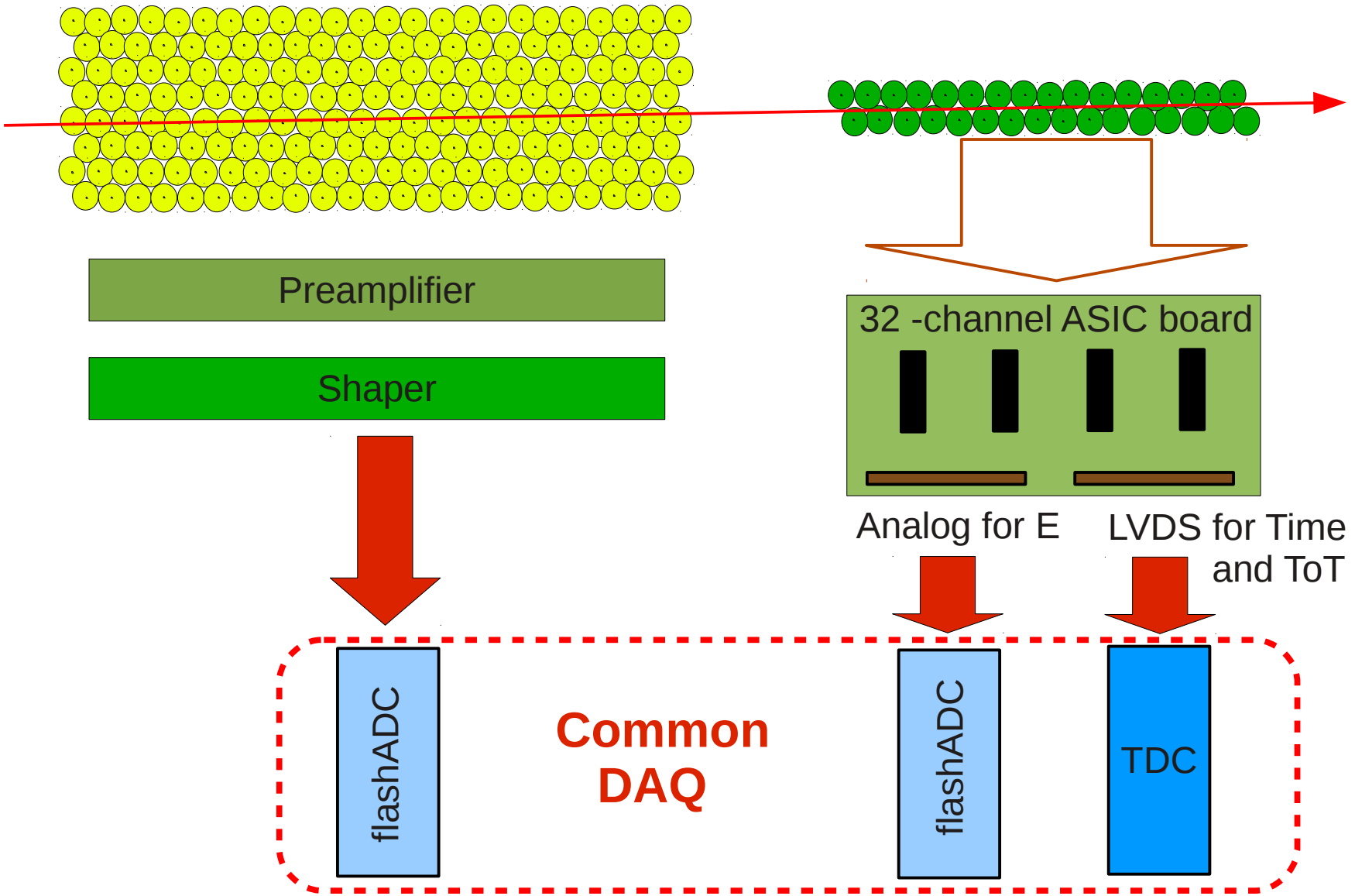
2. Signal booster + Shaper + FPGA-FlashADC; fixed optimal integration time, tail cancellation, baseline restoration:
   - time information (from FPGA discriminators)
   - energy information (from FPGA amplitude search procedure)

FZ Juelich (Germany) + INP PAN Kraków (Poland)

STT FEE test at COSY proton beam during September FAIR week



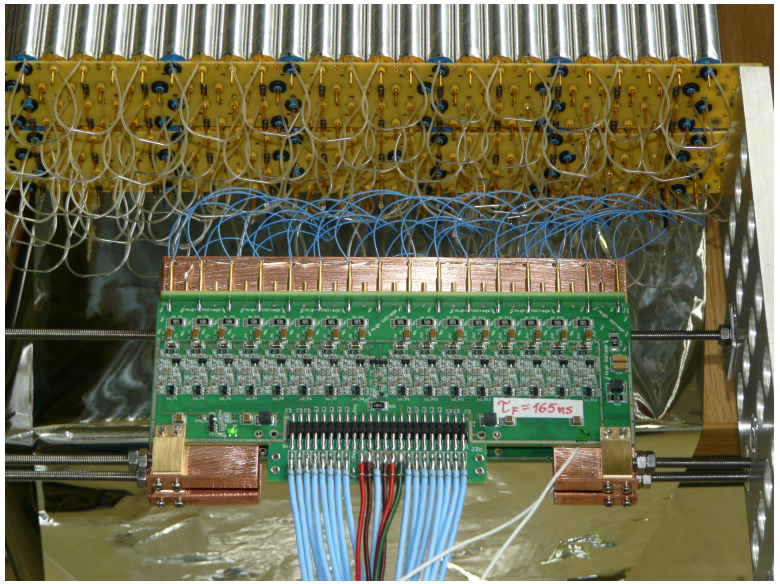
STT FEE test at COSY proton beam during September FAIR week



Optional readout electronics for PANDA STT

Signal booster

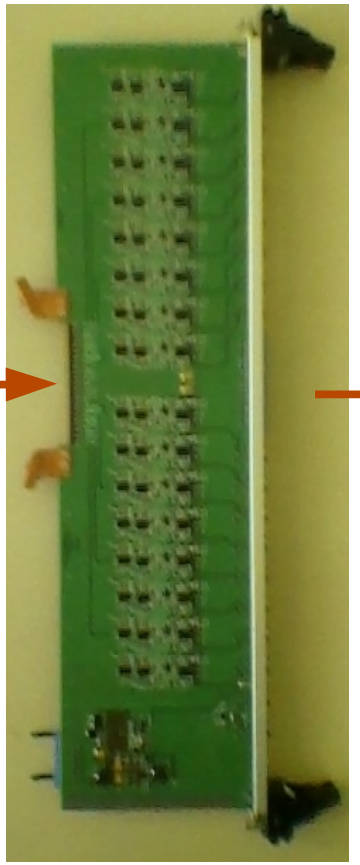
Low power charge sensitive preamplifier (installed at detector)



up to 5 m

Shaper

Tail cancellation & BLR

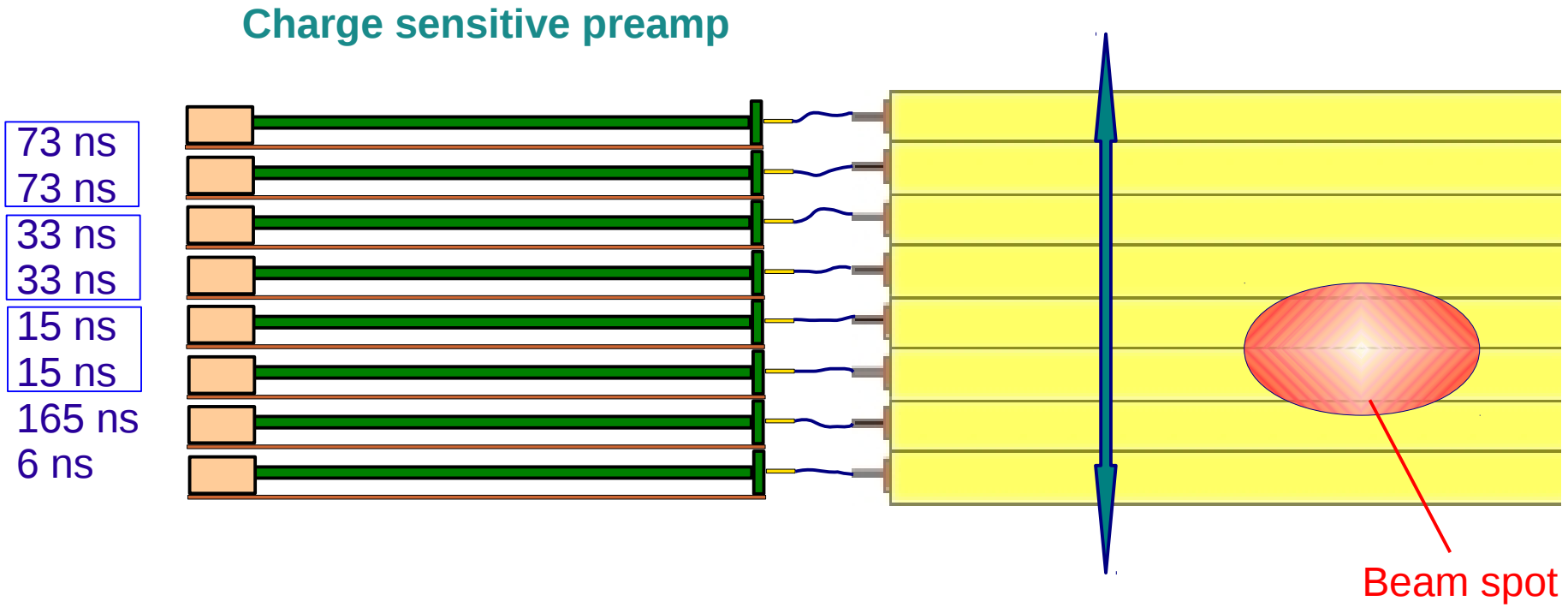


FPGA flashADC

Time

Energy

Testing of various integration times



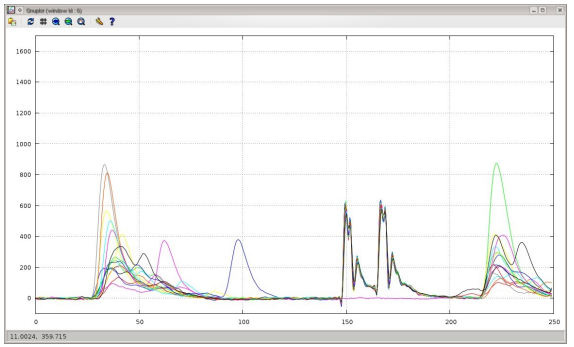
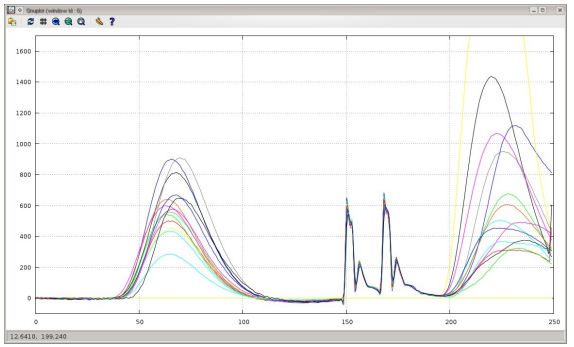
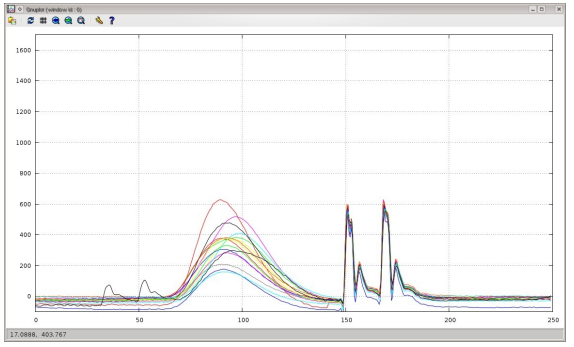
Tracking and analysis of data sets for different time constants

→ time resolution

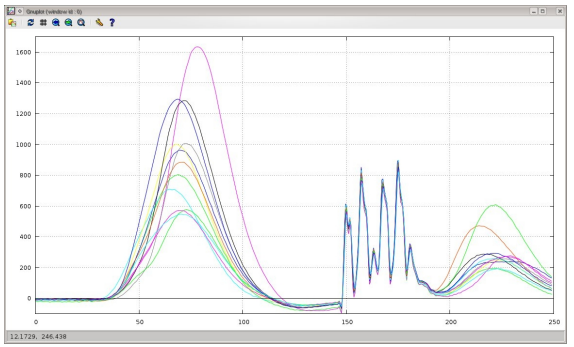
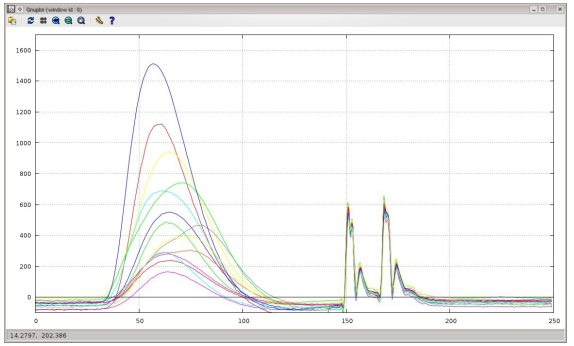
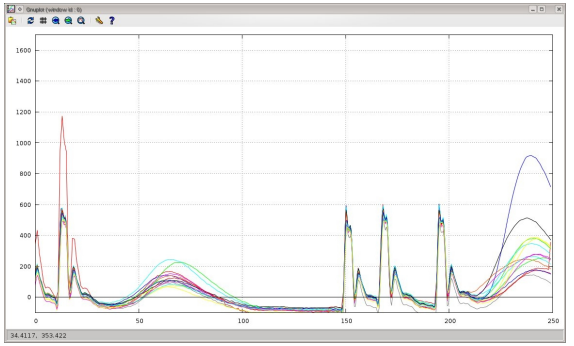
→ energy resolution

Stability of baseline

Low beam intensity

High beam intensity

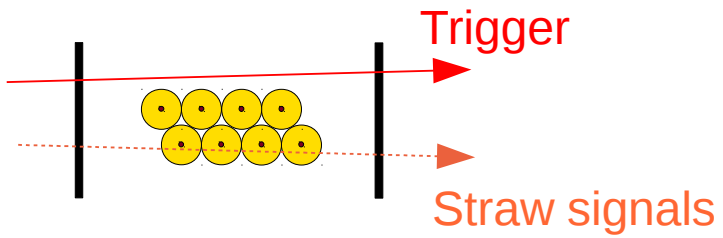
Both for low beam intensity as well as for high beam intensity there are few percent of events with shifted baseline. This effect comes from baseline determination in fQDC. Correction of the baseline is usually possible and easy.

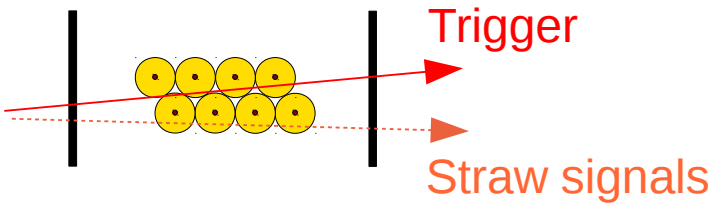
K. Pysz

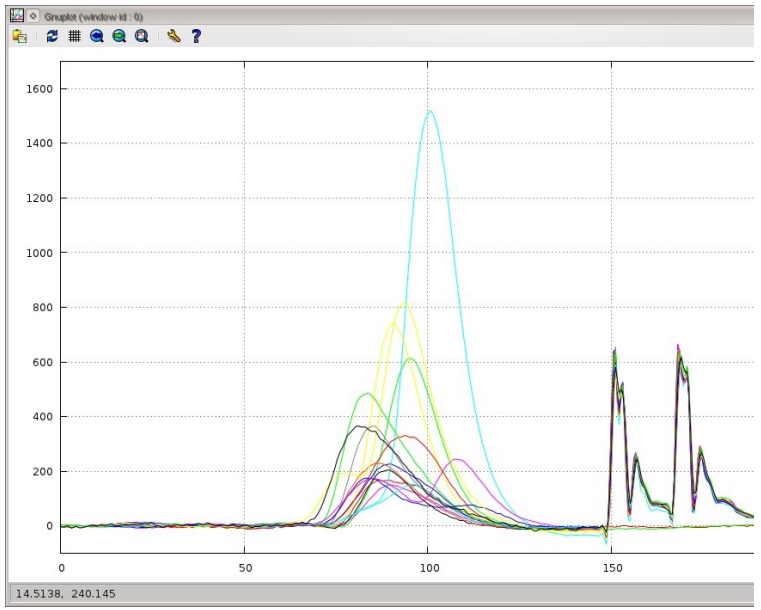
Unfavorable phenomenons

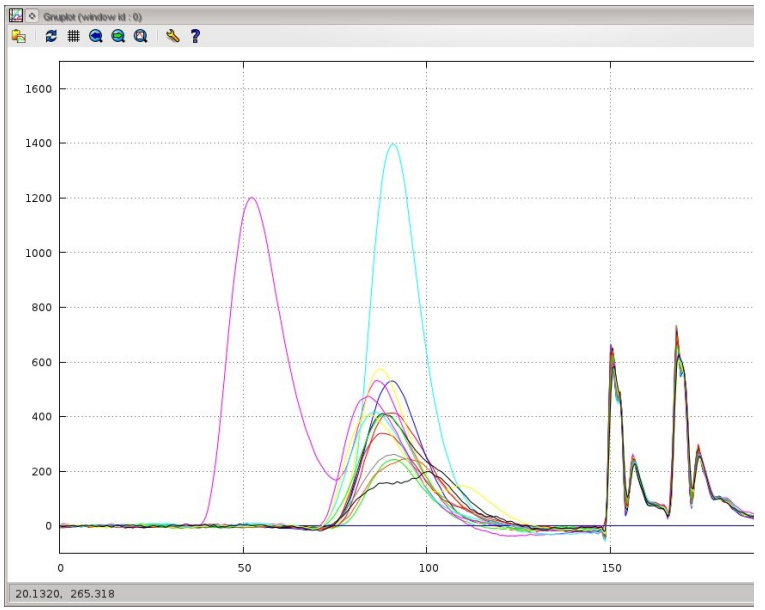
1. Pile-up in trigger:

The same event but time difference





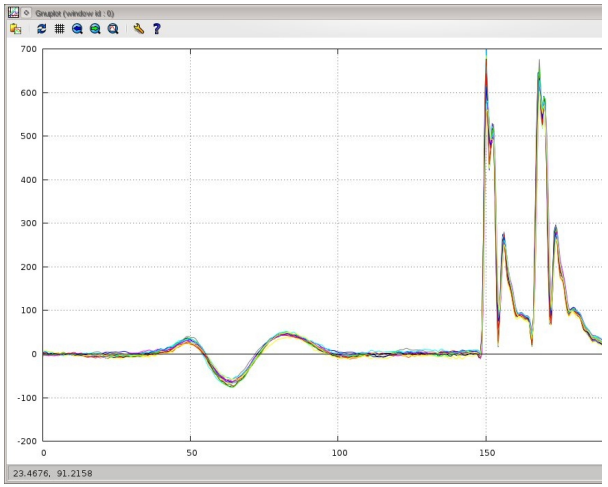


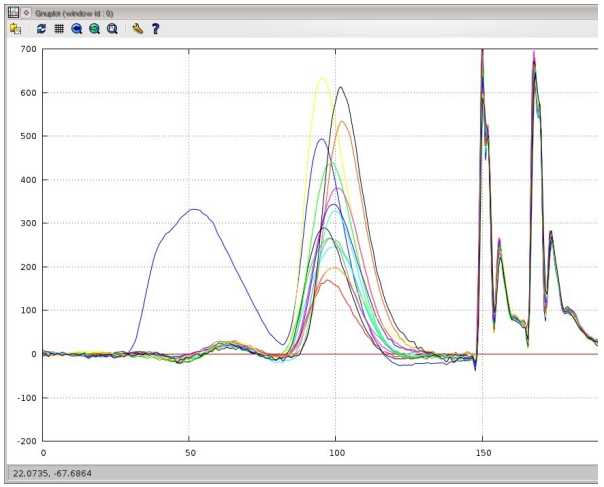


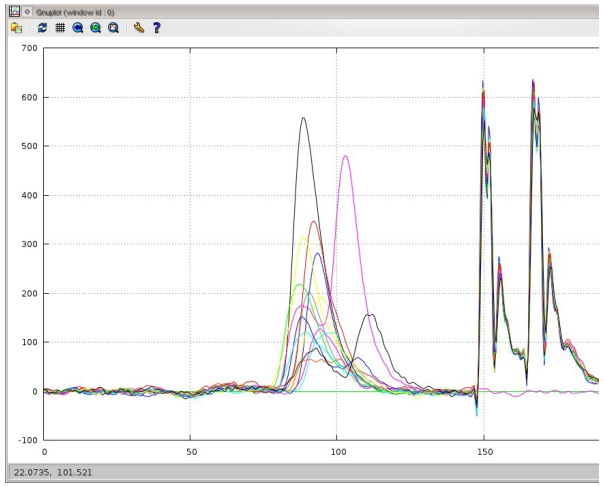
Only fraction of incorrect events can be rejected by proper condition in data sorting or by tracking.

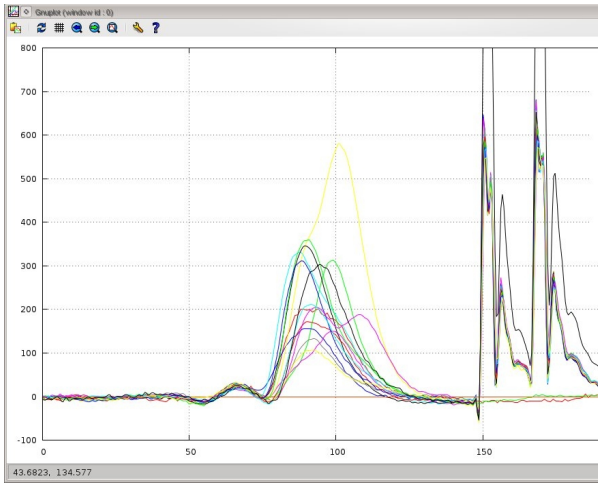
Unfavorable phenomenons

2. Cross-talk in electronics : Timing deteriorated – delay in drift time







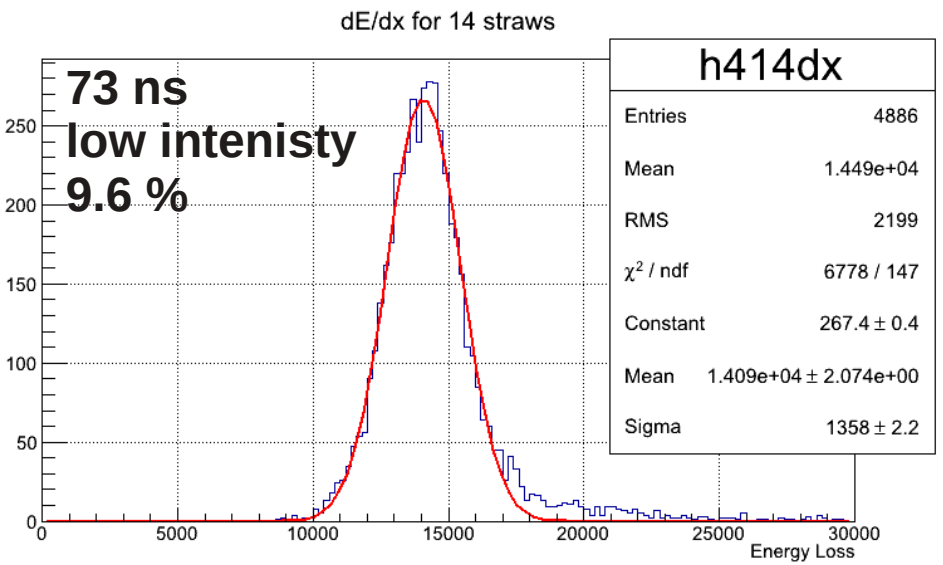


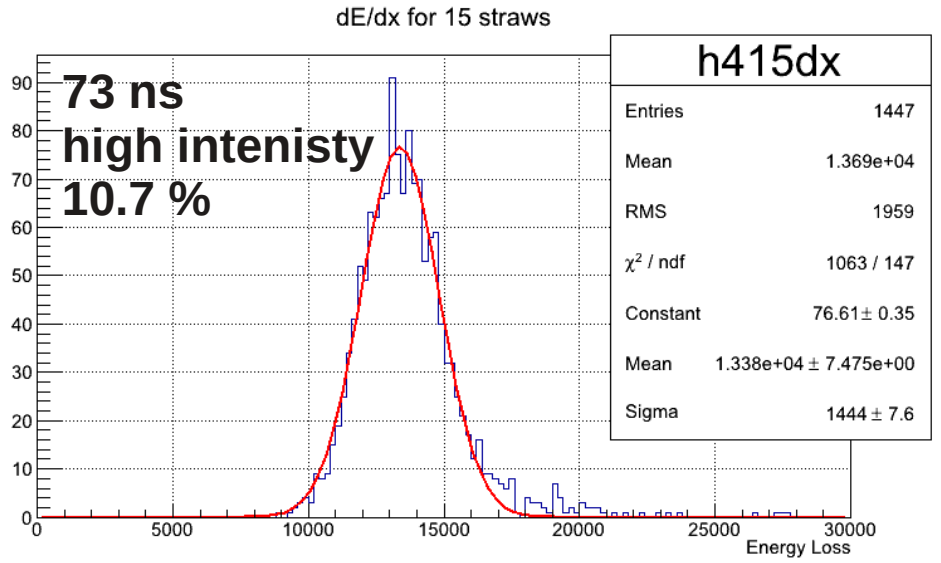
To some extent events with cross-talk can be rejected in data sorting.

Energy- and position resolution

6 ns

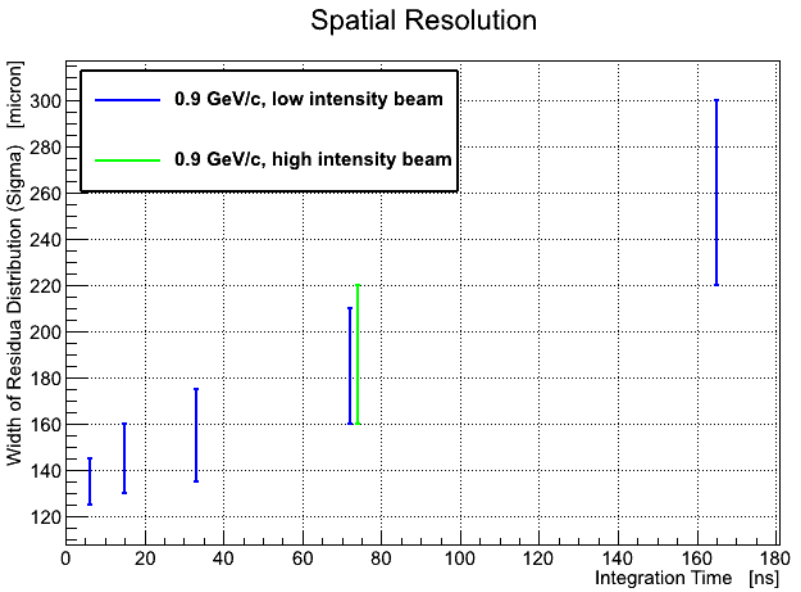
73 ns

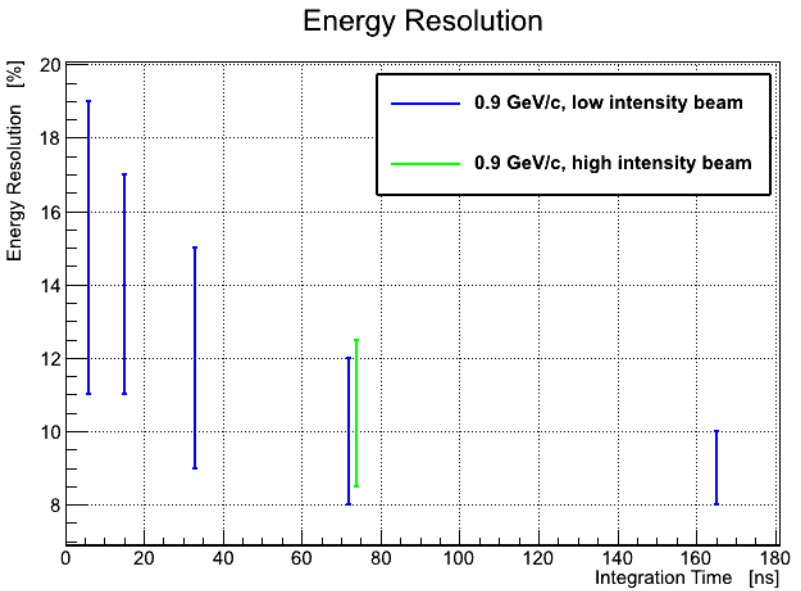




Spatial- and Energy resolution

Spreads of obtained results origin from various gas amplification, threshold levels, discriminator type, track length, ….



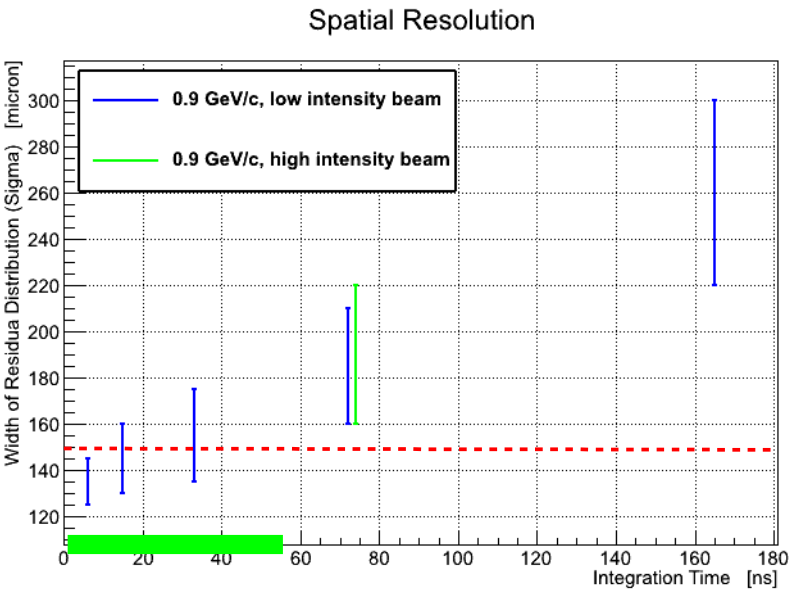


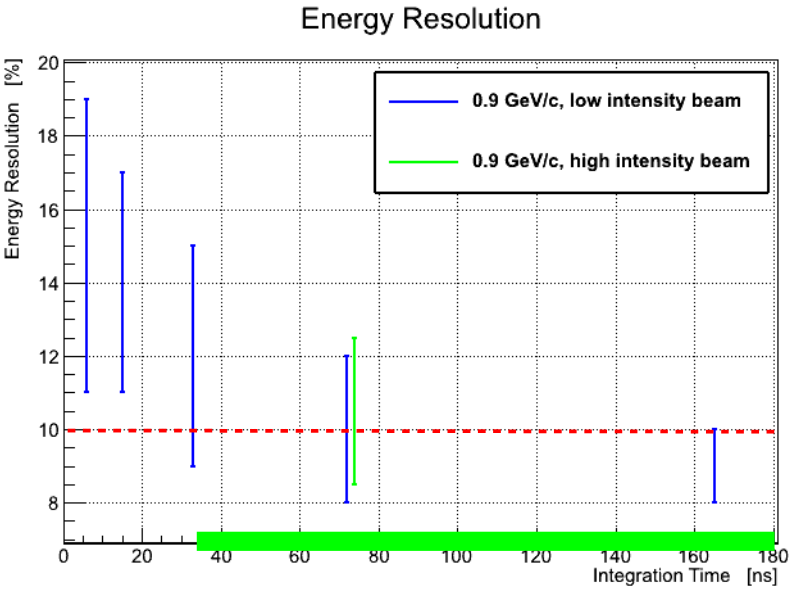
Spatial- and Energy resolution

Spreads of obtained results origin from various gas amplification, threshold levels, discriminator type, track length, ….

Demanded spatial resolution: < 150 µm

Demanded energy resolution: < 10 %



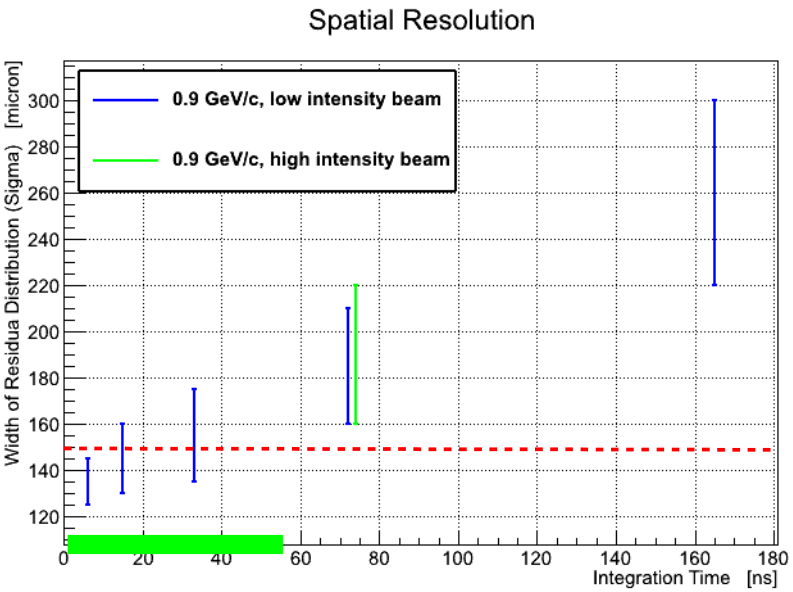


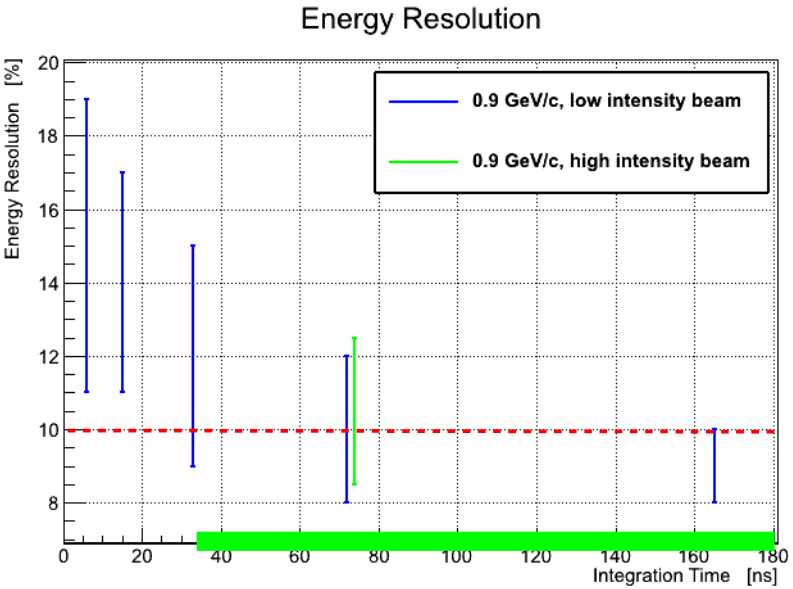
Spatial- and Energy resolution

Spreads of obtained results origin from various gas amplification, threshold levels, discriminator type, track length, ….

Demanded spatial resolution: < 150 µm

Demanded energy resolution: < 10 %





Conclusions

1. Front End Electronics consisting of charge preamplifier and shaping amplifier (with BLR and tail cancellation) followed by FPGA flashADC was tested with the low and high intensity proton beam at COSY.

2. Straw tube signals were integrated with the mean of integration time of 6 ns – 165 ns.

3. With a careful signal shape analysis the feasibility of simultaneous measurement of track position as well as particle energy loss with precision demanded for PANDA STT (spatial resolution < 150 micron) and energy loss (resolution < 10 %) is proved.

4. The best energy loss resolution for 0.9 GeV/c (8 %) is consistent with results obtained in the previous tests for current amplifier (8 % @ 1,0 GeV/c).

5. Sufficient energy resolution with signal integration over less then 70 ns is consistent with results obtained in the previous tests for current amplifier.

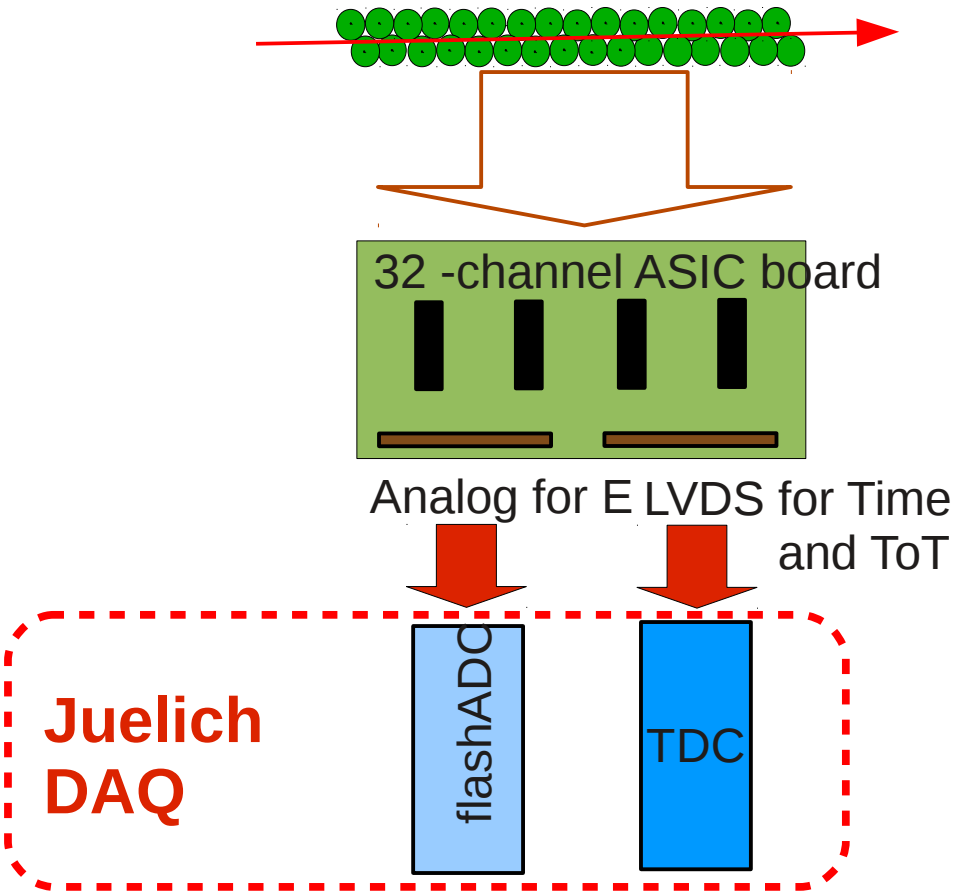
6. Spatial resolution behavior is reasonable.

7. Observed cross talk has to be avoided in the next iteration of shaping electronics.

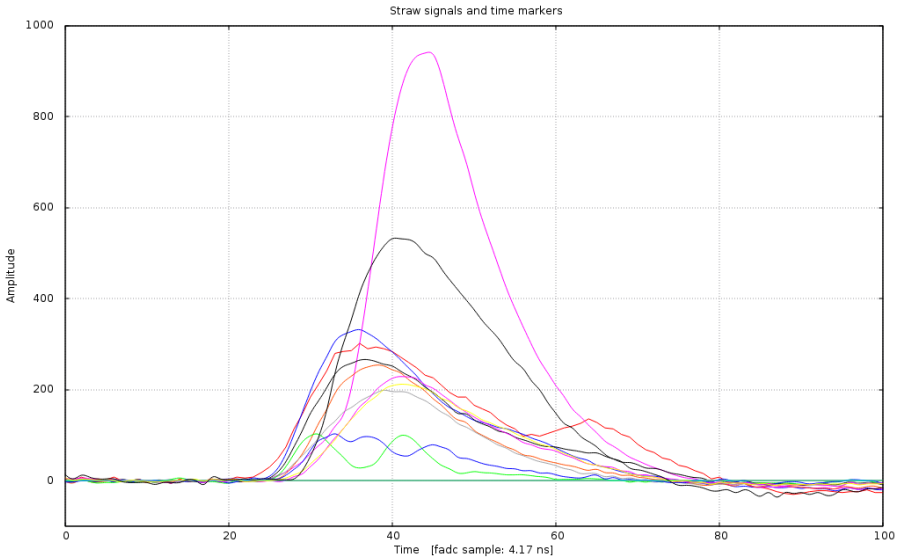
8. Both baseline stabilization as well as the tail cancelation are fulfilled by the present prototype of electronics.

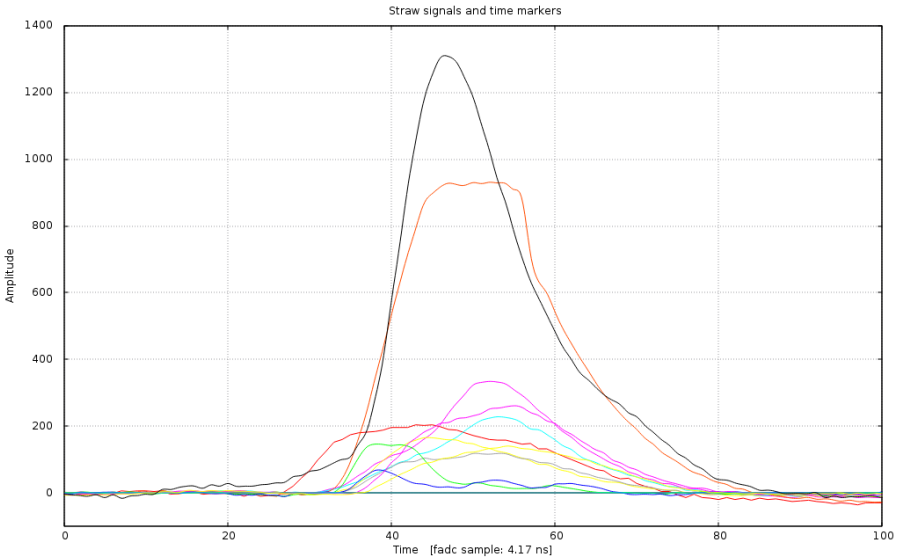
Few words about ASIC

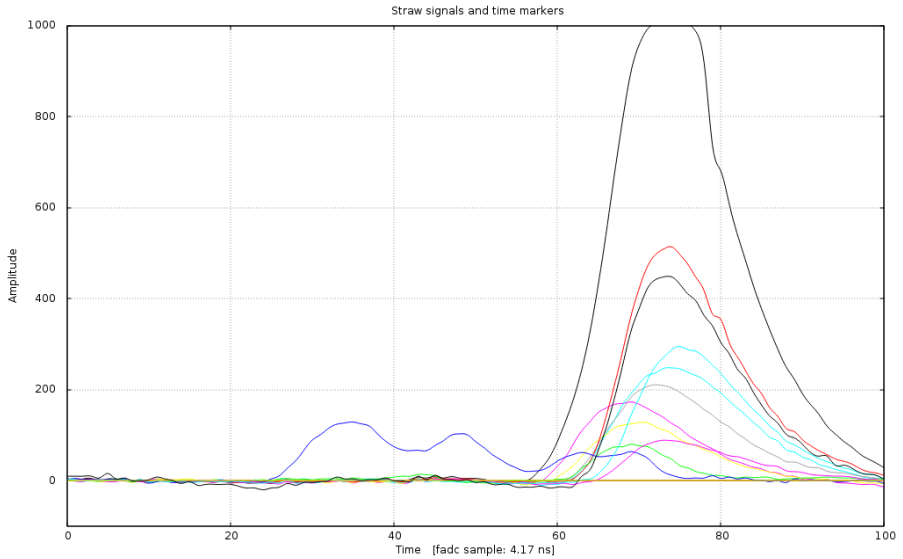
ASIC performance @ 900 MeV/c and low beam intensity
Data collected in fADC+TDC

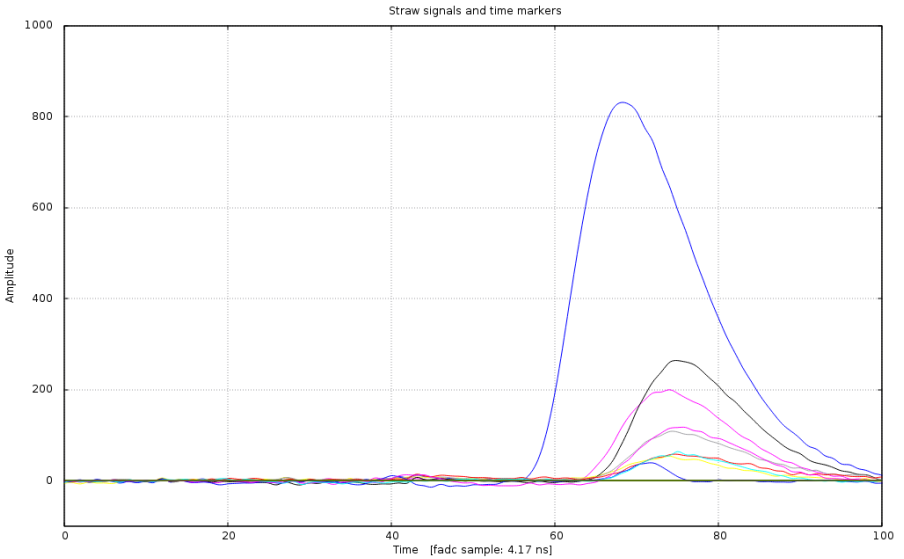


ASIC analog signals (FlashADC)







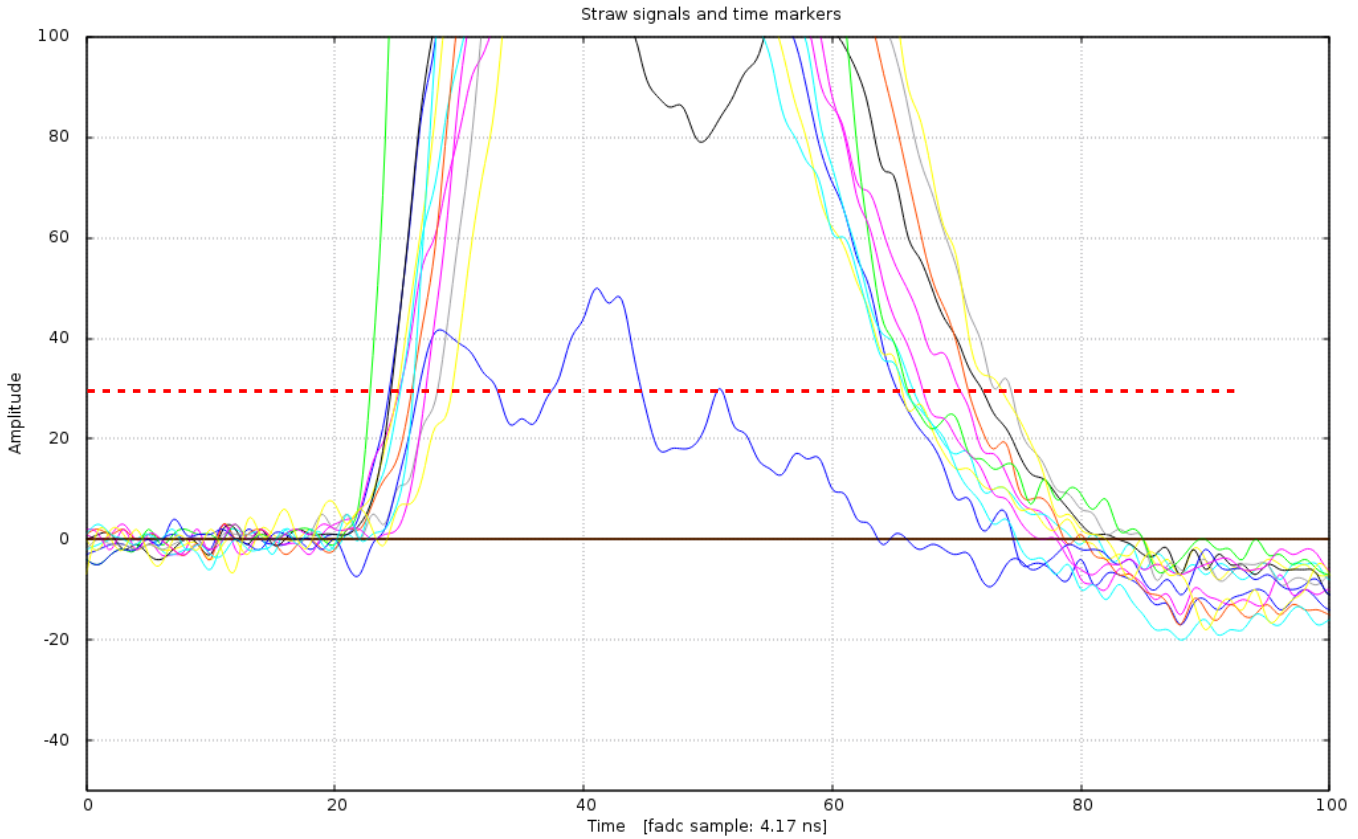


K. Pysz

Time information from ASIC

Timing for analog signals:

Leading Edge Discriminator

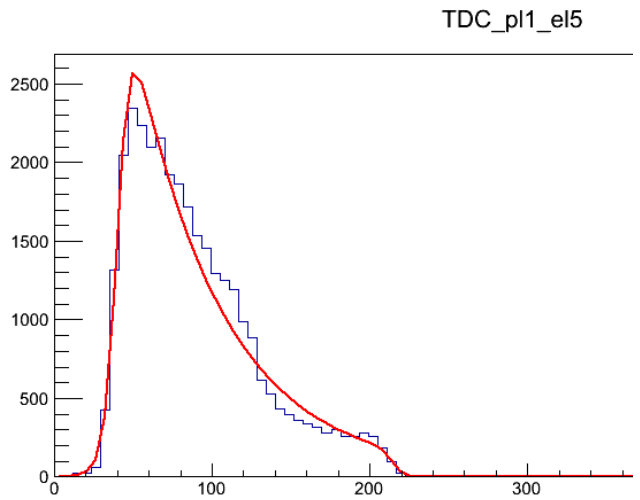


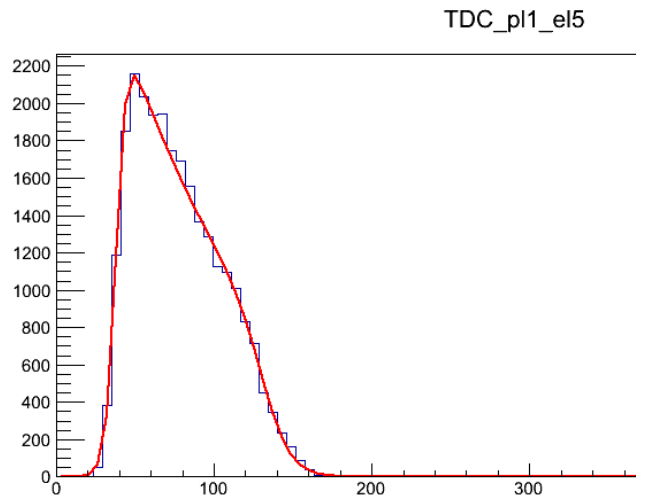
Drift time spectra

2 layers

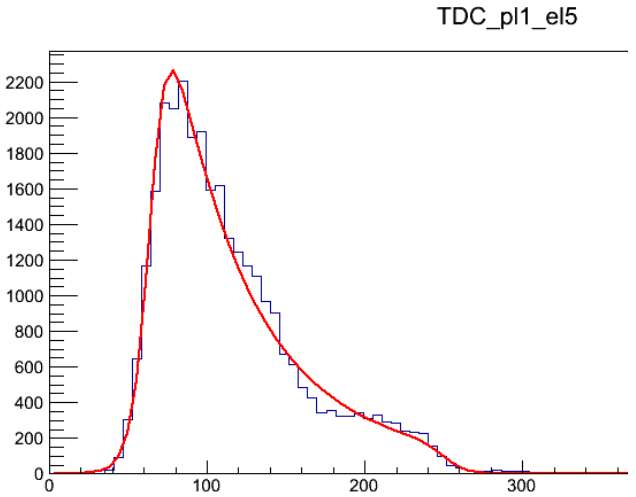
1 layer

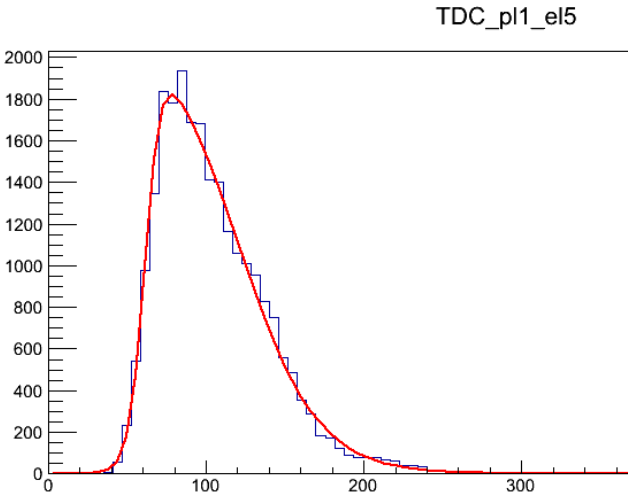
fADC





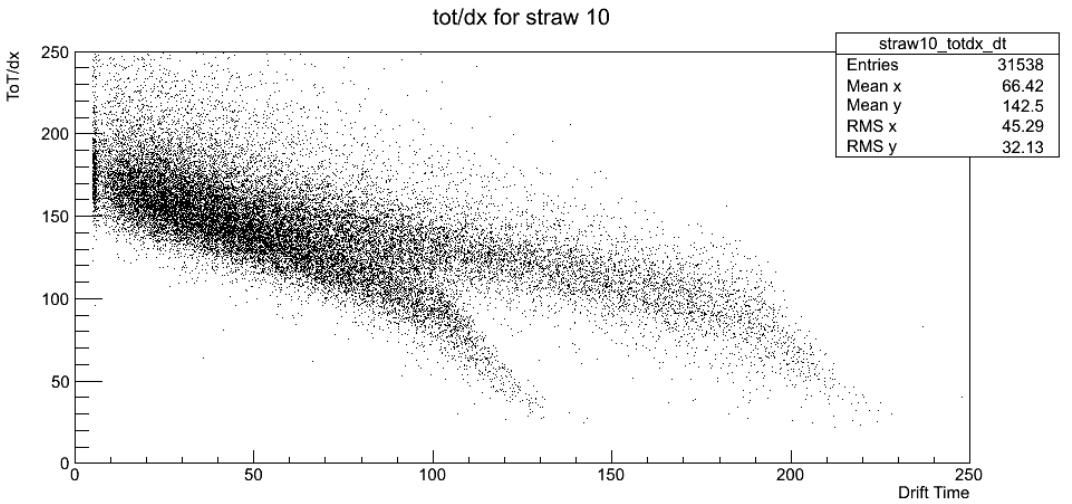
TDC



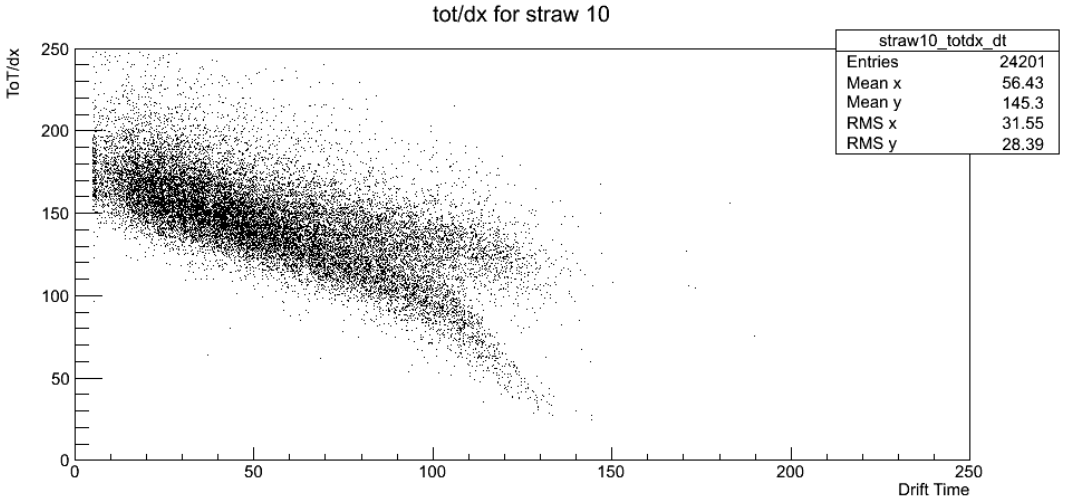


Problem of the drift time spectra

2 layers



1 layer



Extended tail in the drift time spectra originates predominantly from pile-up in trigger and should be suppressed after tracking.

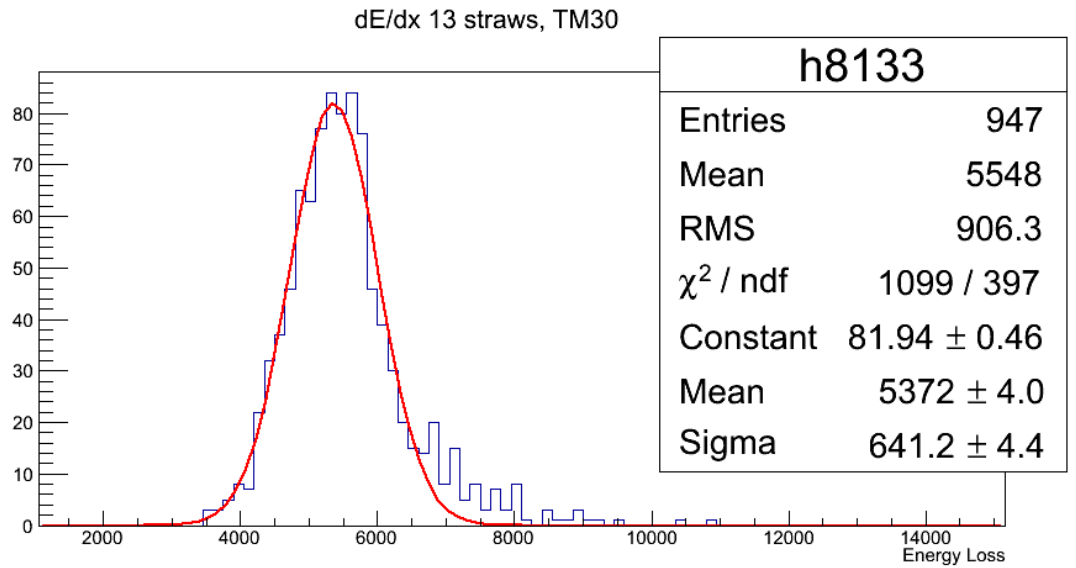
K. Pysz

Tracking with ASIC

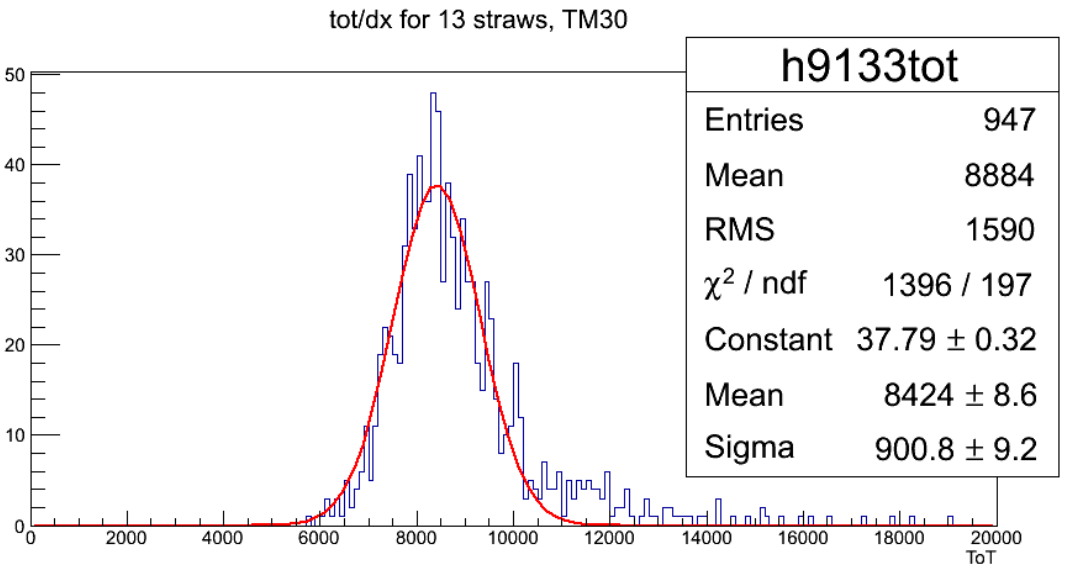
Time from TDC

Time from fADC

Energy loss and ToT



13 +- 1 %



12 +- 1 %

Thank you !

Aim: selection of the optimal integration time of the shaper allowing for required timing resolution as well for sufficient energy resolution

Available shapers

τ: Proper work up to:

6 ns	(6 MHz),
15 ns	(4 MHz),
33 ns	(3 MHz),
73 ns	(2 MHz)'
165 ns	(1.3 MHz)

FPGA Const. Fraction Disc.: ~ 1 ns