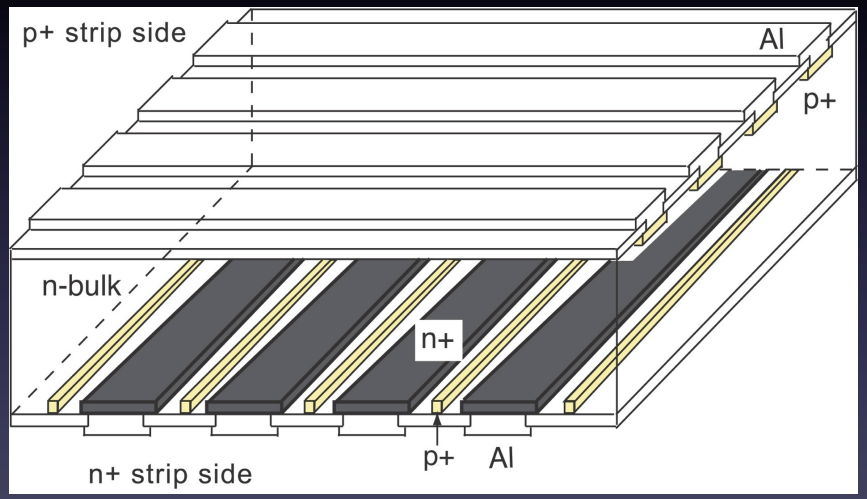
Updates on the front-end electronics for the microstrip sensors of the MVD

MVD meeting, Alba 29 April 2013

INFN-Sezione di Torino

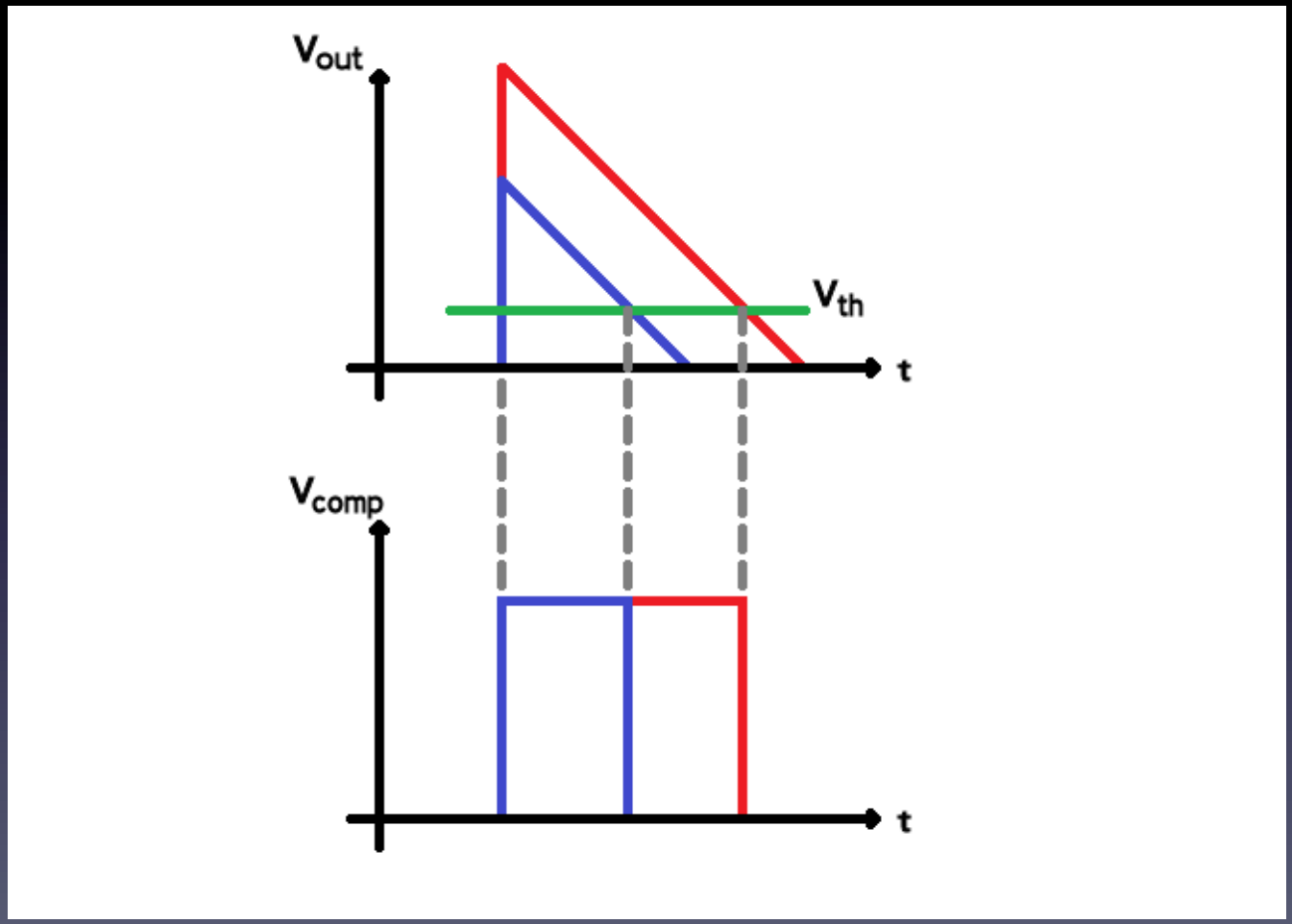
Speaker: Valentino Di Pietro

Microstrip Sensors requirements

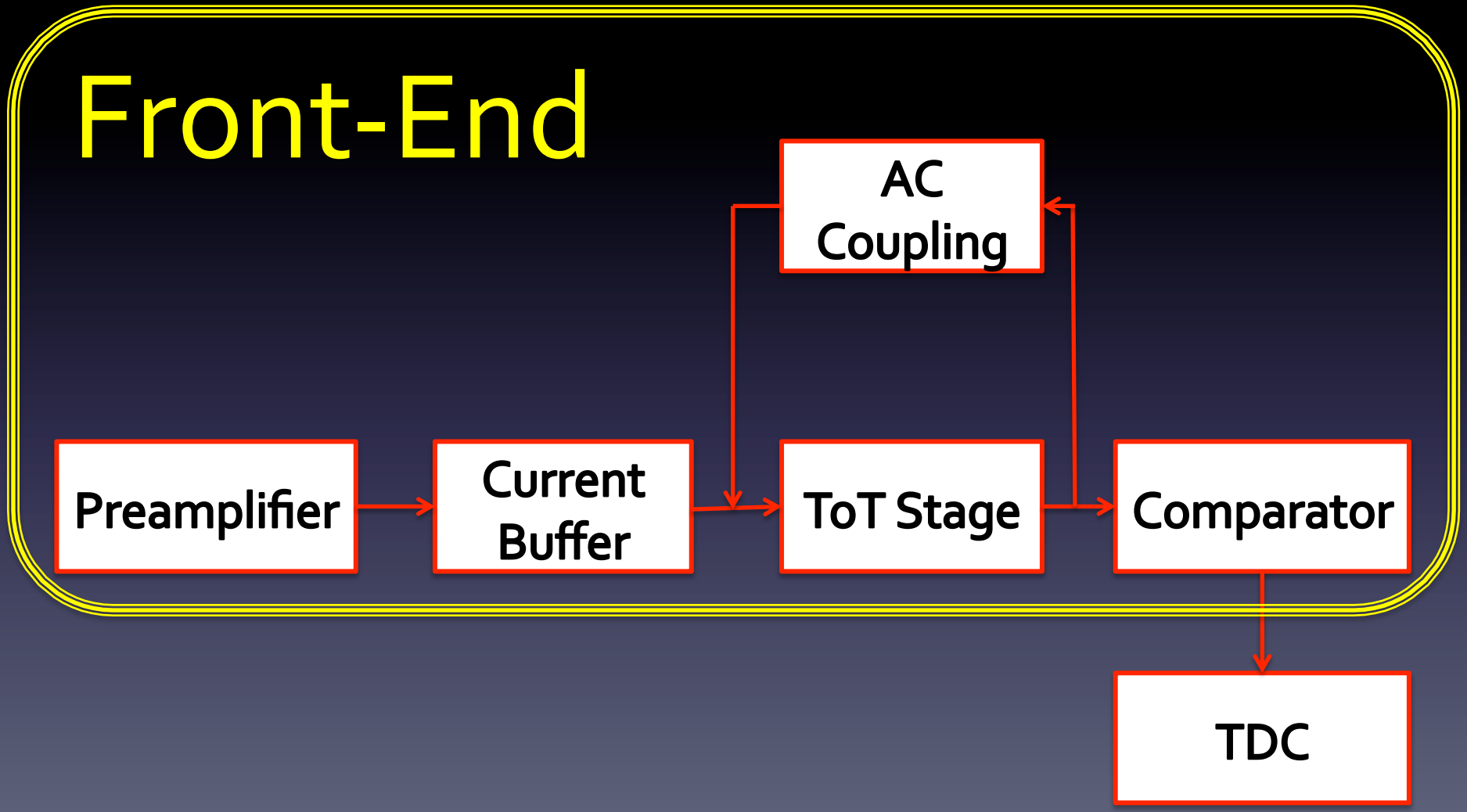


- Specifications
  - Length ~ 8-10 cm
  - Width ~ 60-80 μm
  - Pitch ~ 100 μm
  - C_{det} ~ 5-30 pF
- Goals
  - Dynamic range ~ 9 bits
  - Noise < 2000 e^-
  - Power consumption ≤ 4 mW/ch

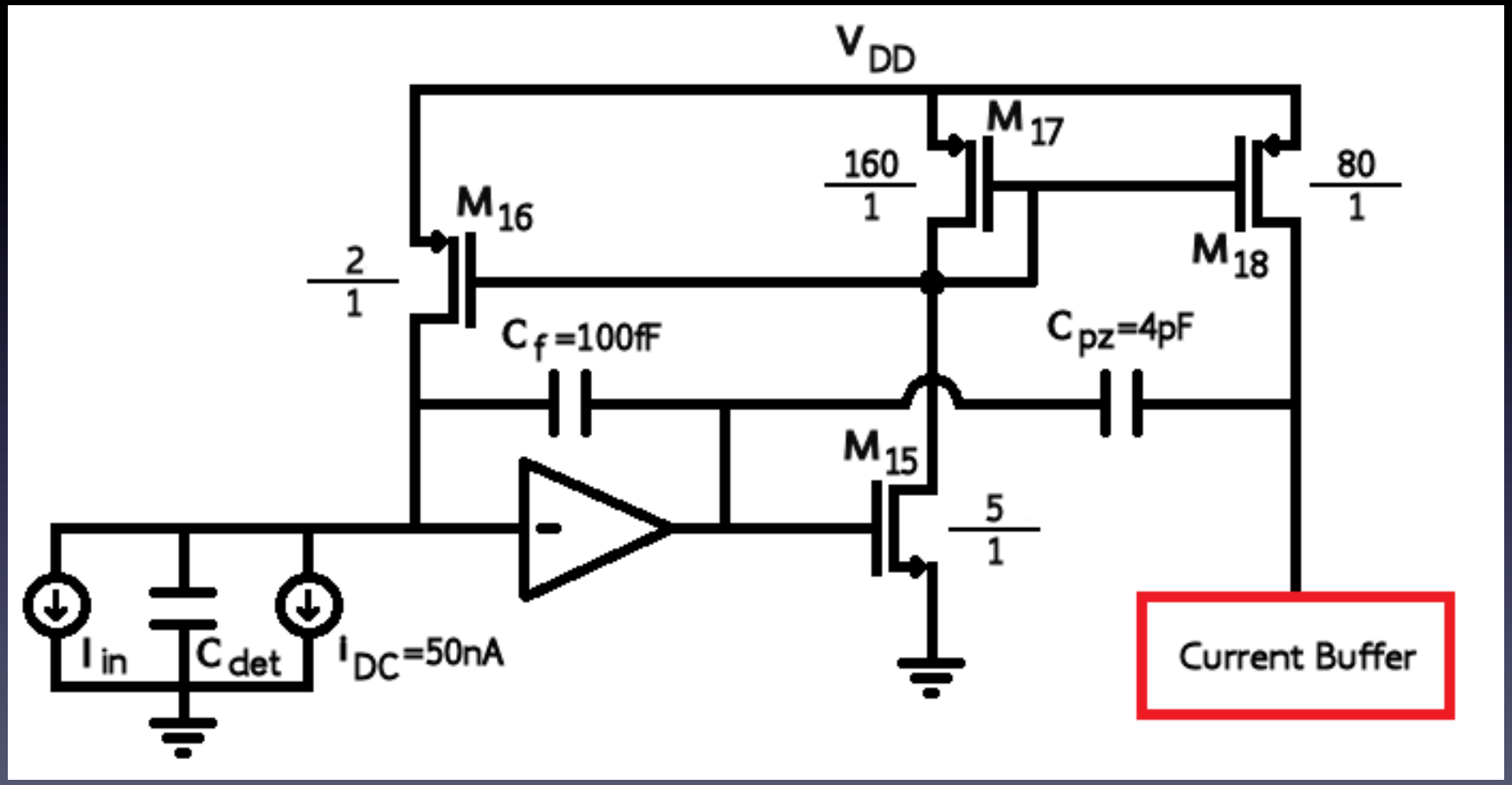
ToT technique



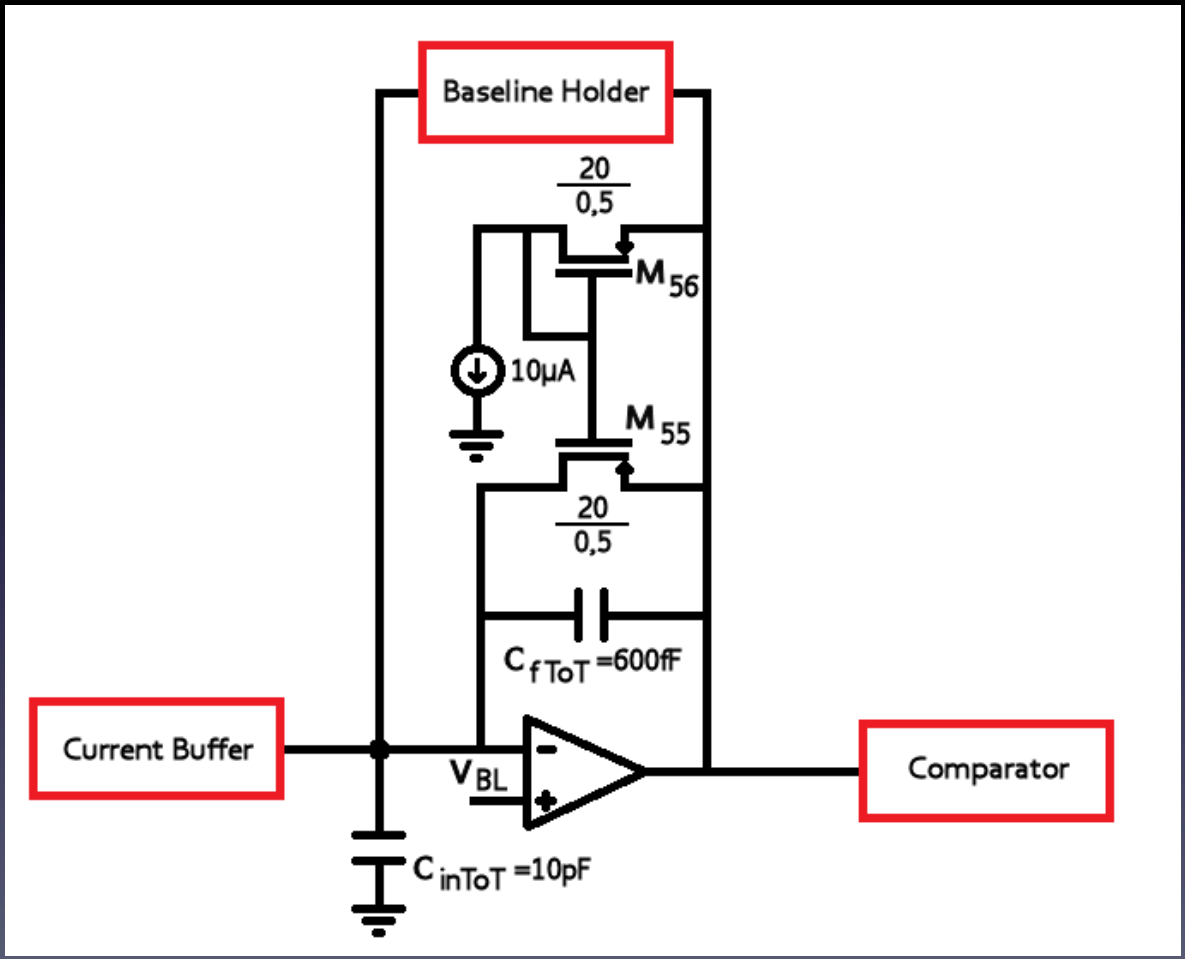
Implemented input stage



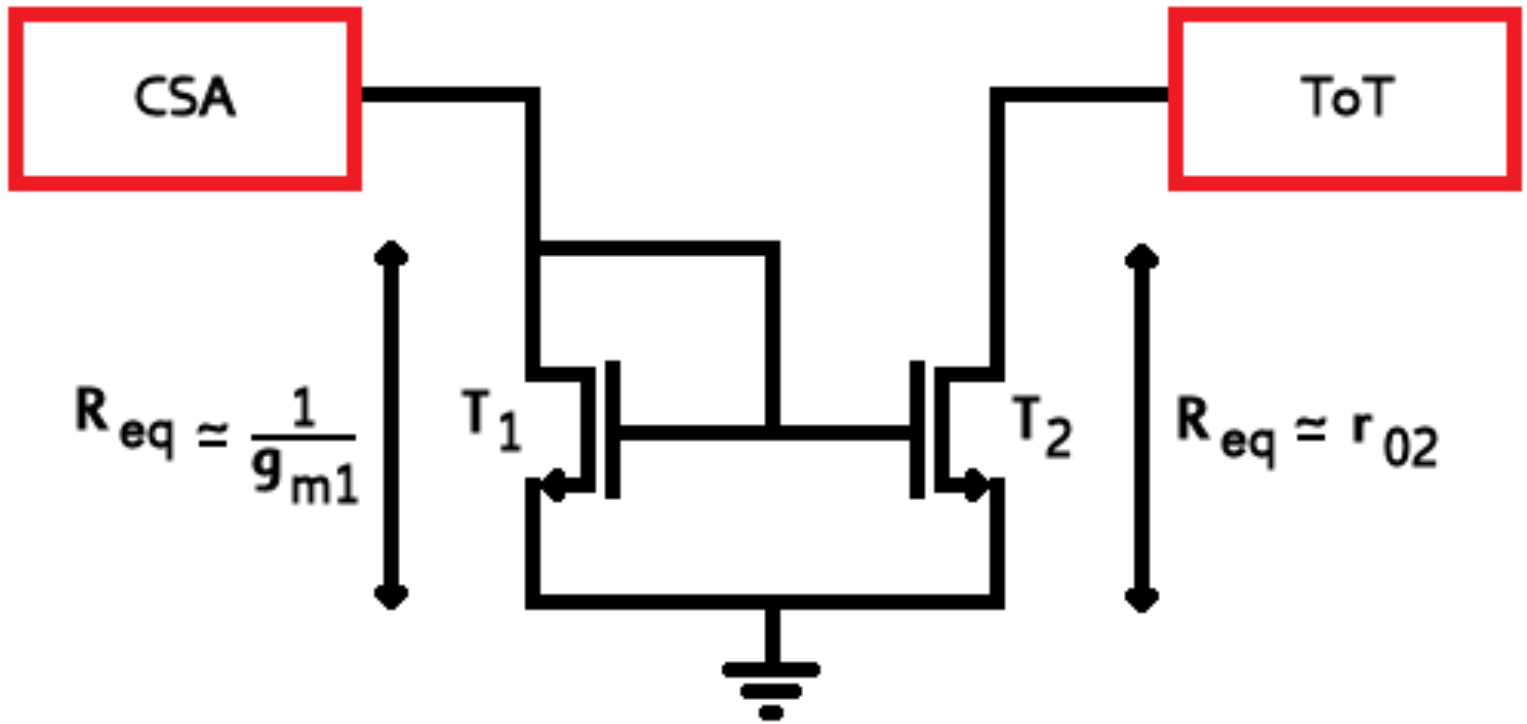
Implemented FE Stage: CSA



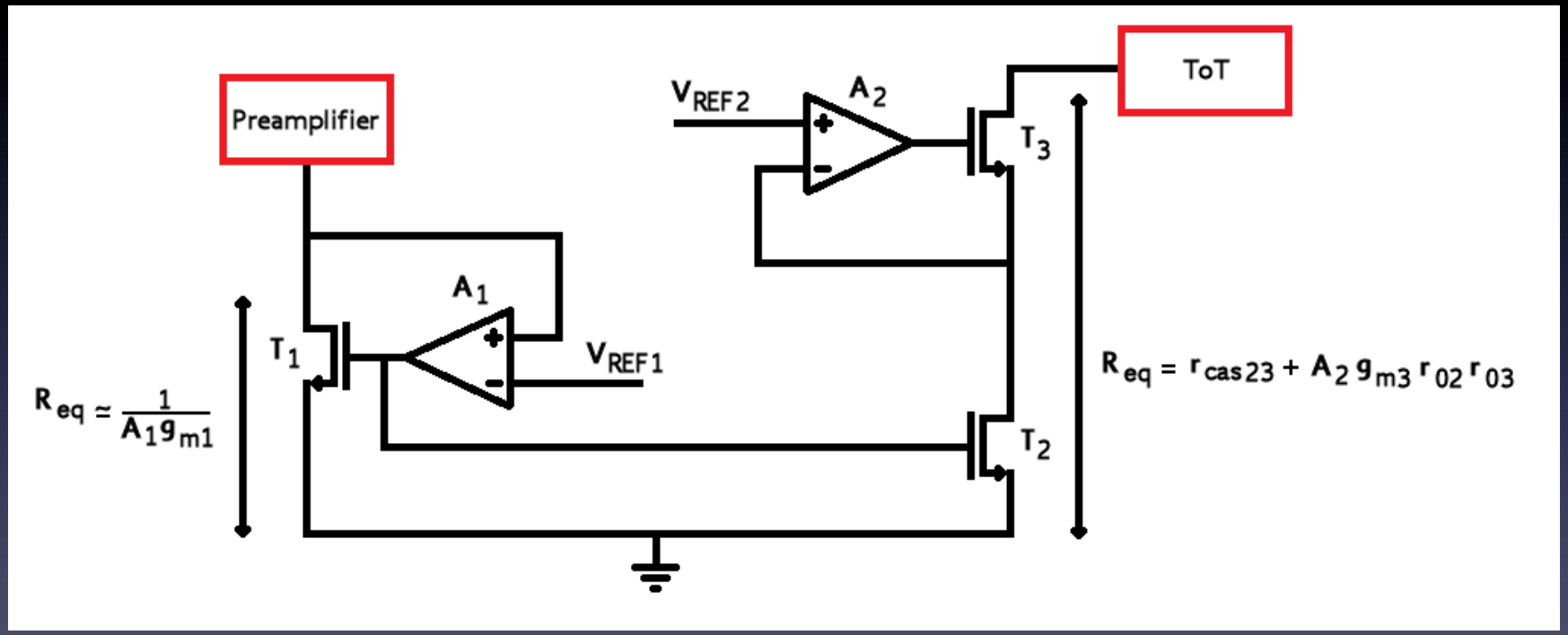
Implemented FE stage: ToT Stage



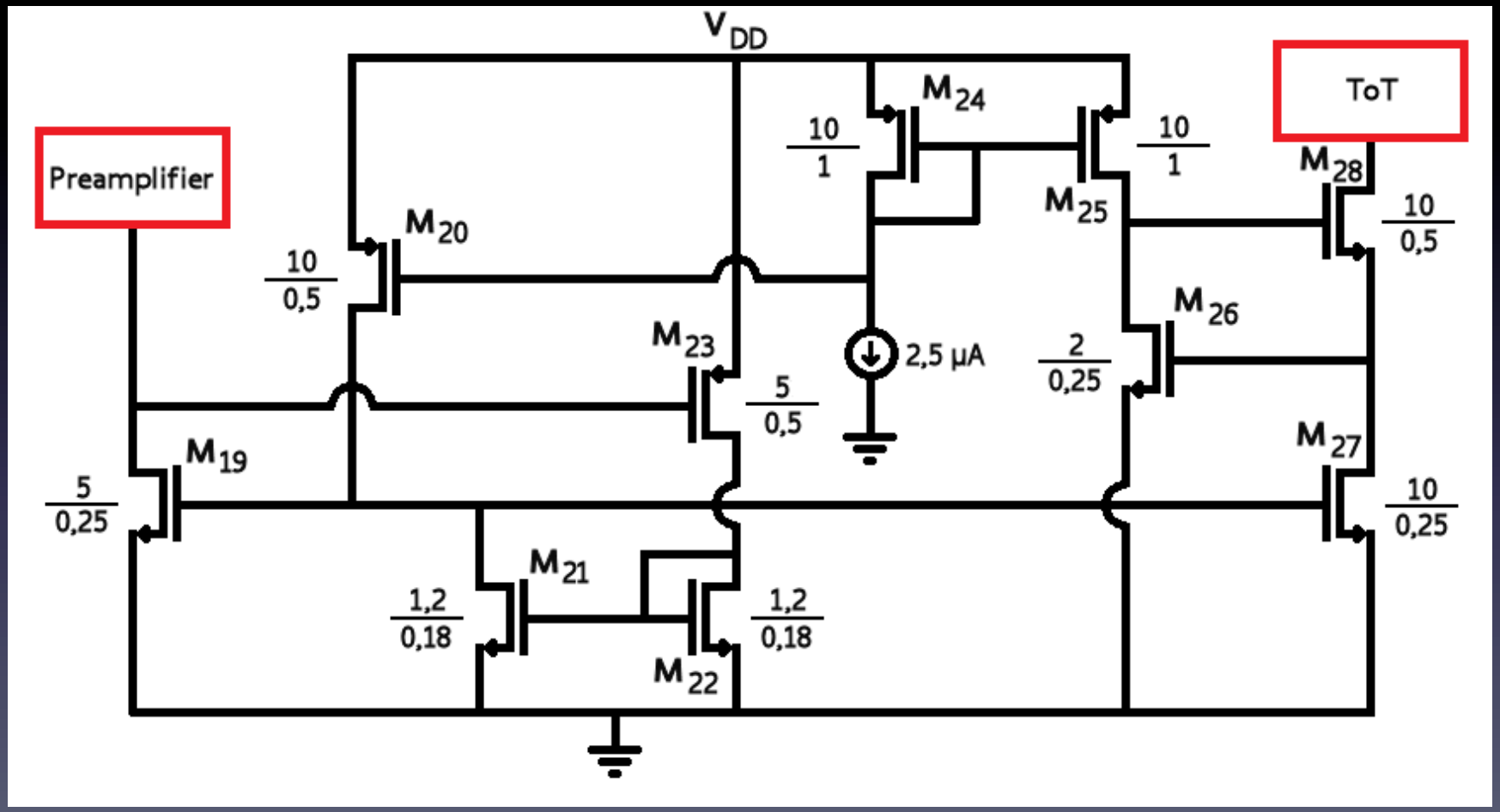
Current Buffer



Current Buffer with g_m-boosting

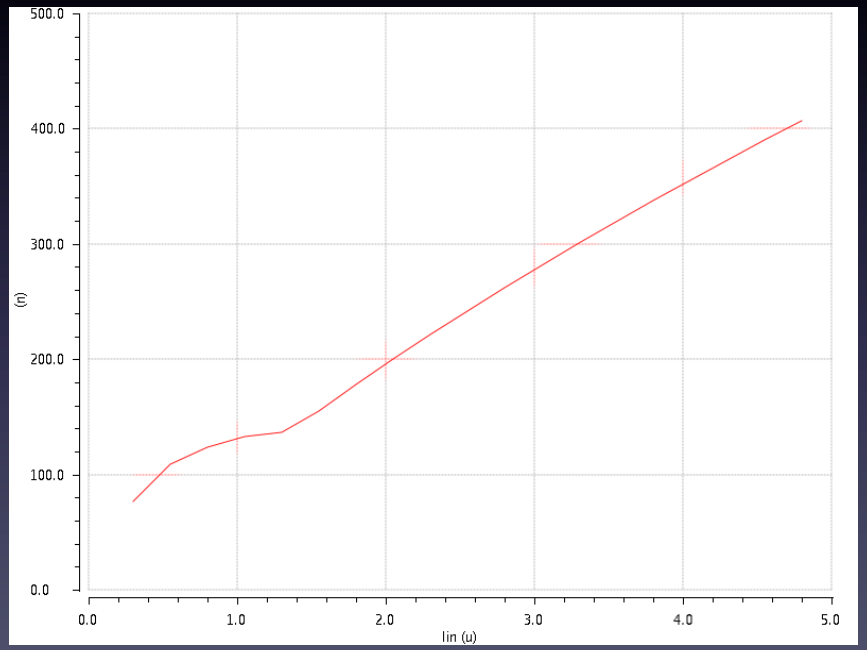


Implemented FE stage: Current Buffer

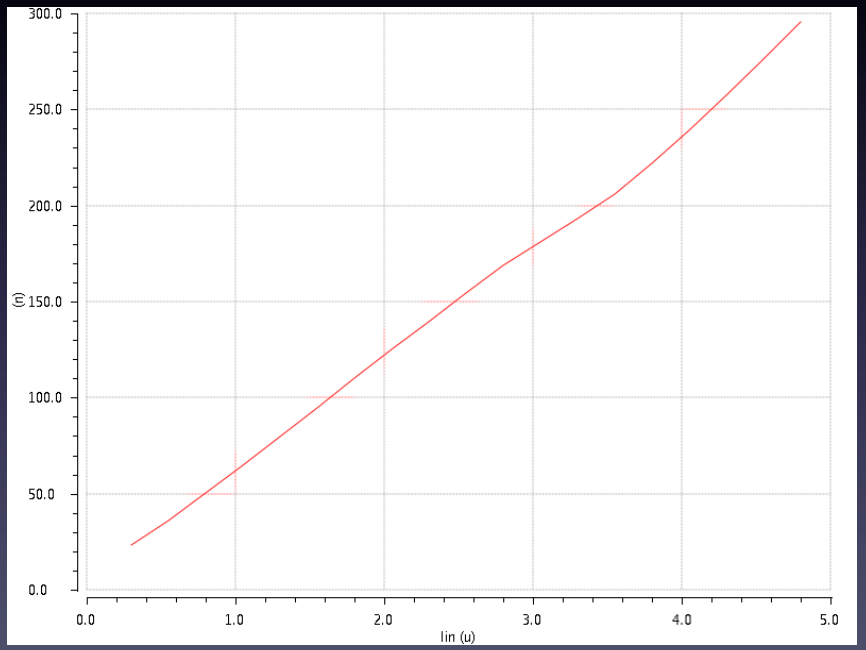


Simulations: Current Buffer

Without g_m-boosting

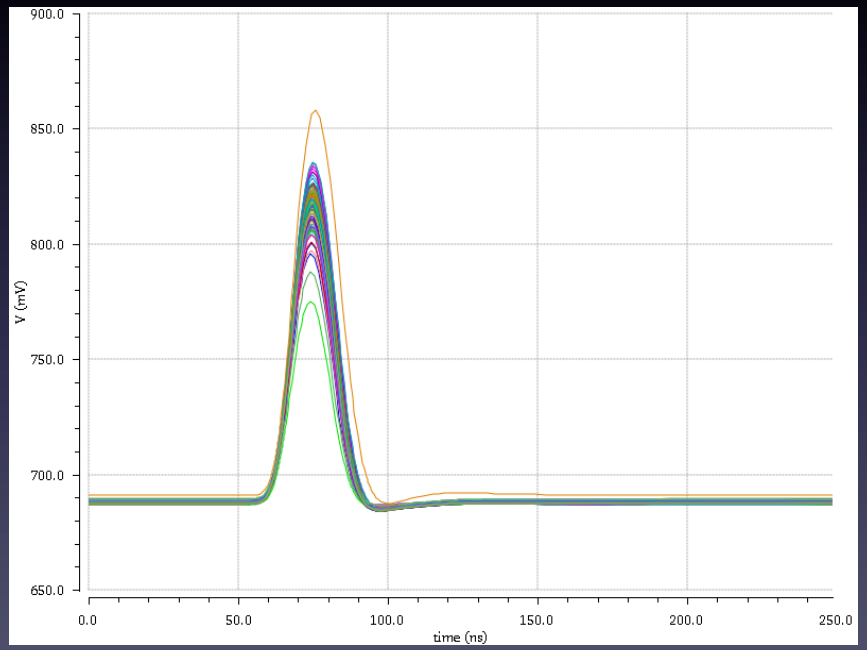


With g_m-boosting

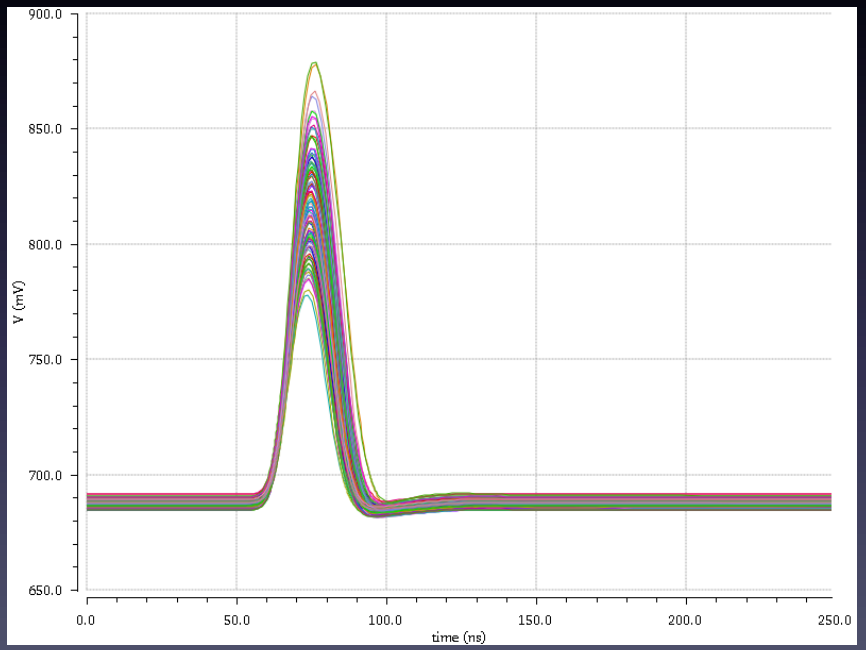


Simulations: Monte Carlo (1)

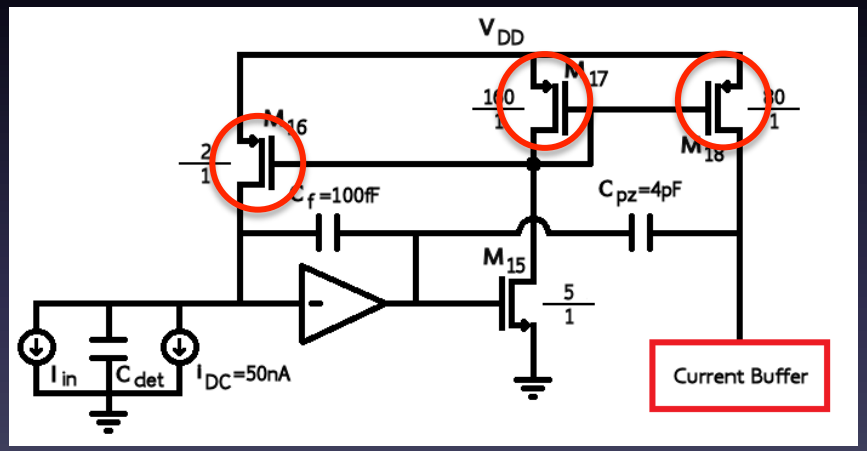
Process variations

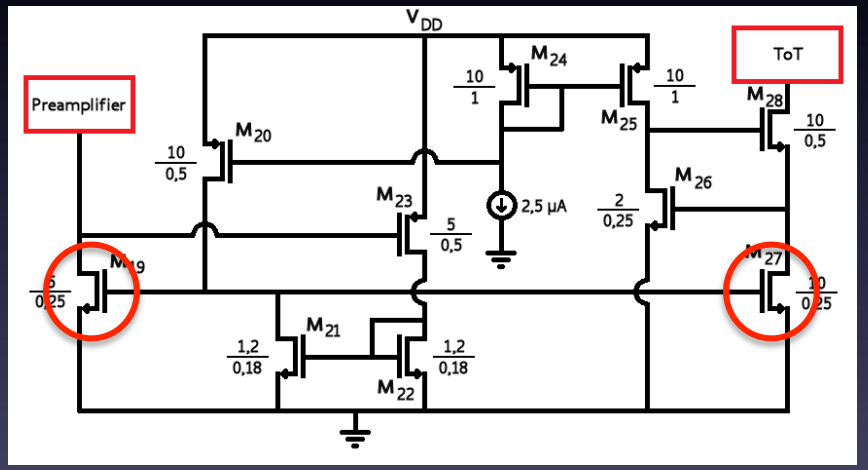


Mismatch variations



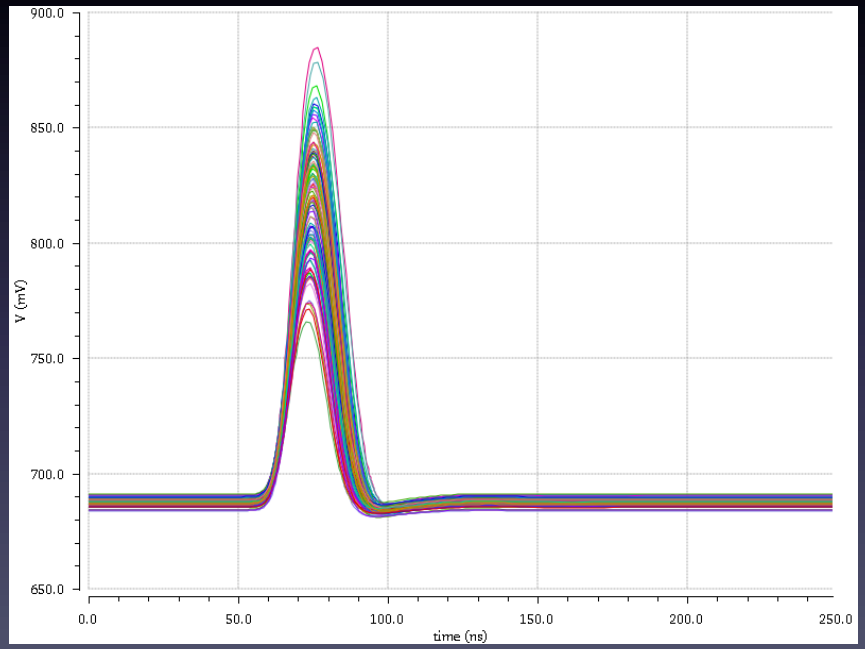
Simulations: Monte Carlo (2)



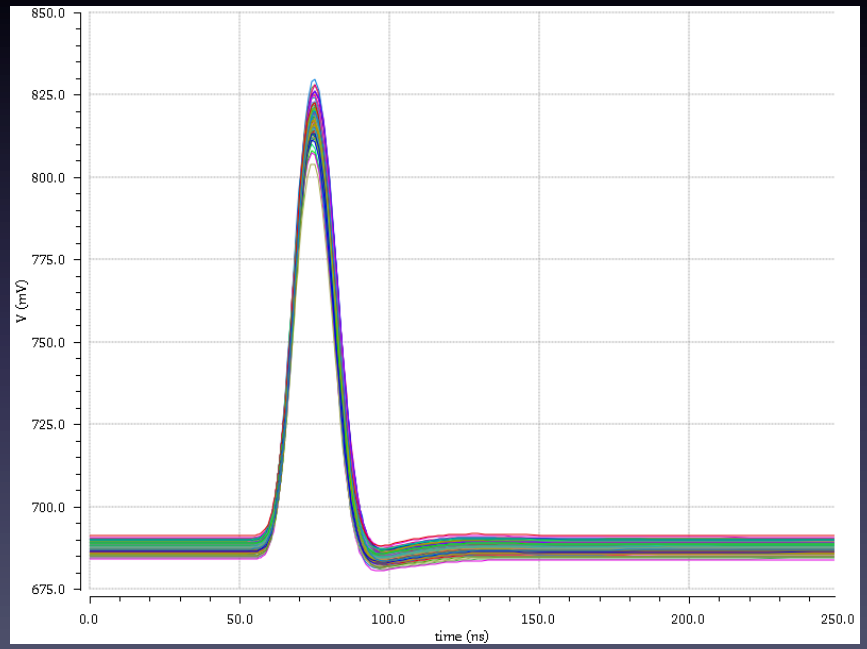


Simulations: Monte Carlo (3)

MC without input biasing current mirror

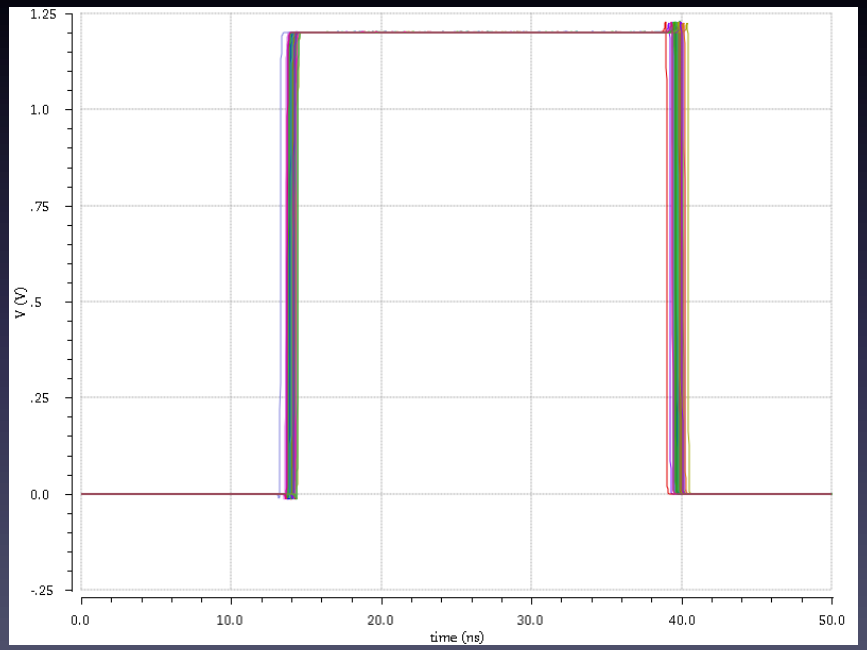


MC without current buffer current mirror



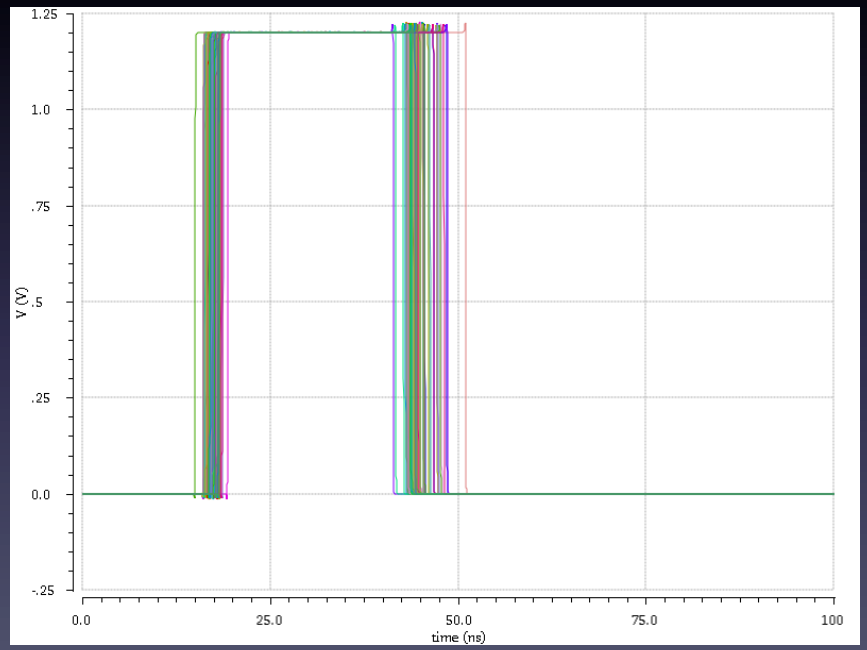
Simulations: Jitter

C_{det} = 5 pF



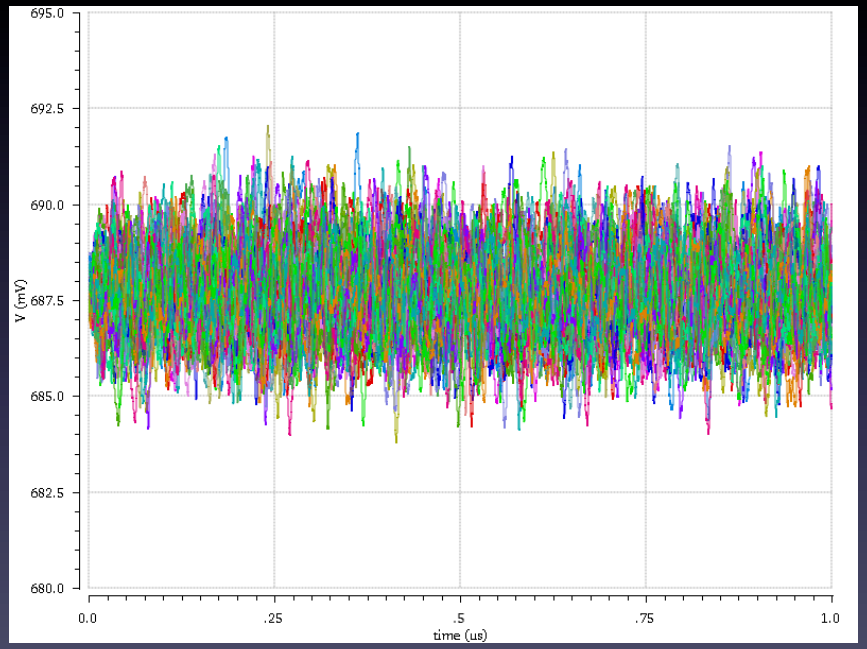
σ_t ~ 300 ps

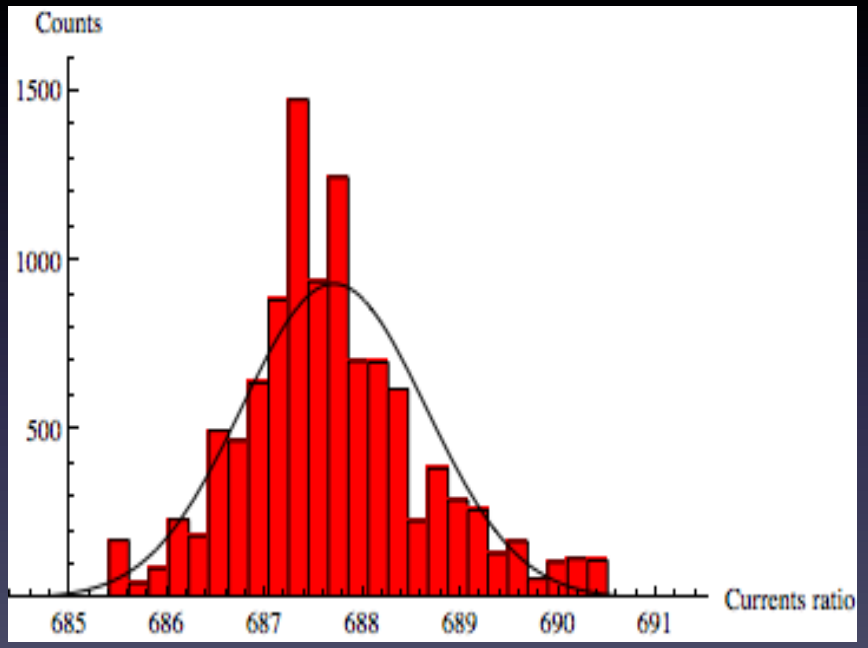
C_{det} = 30 pF



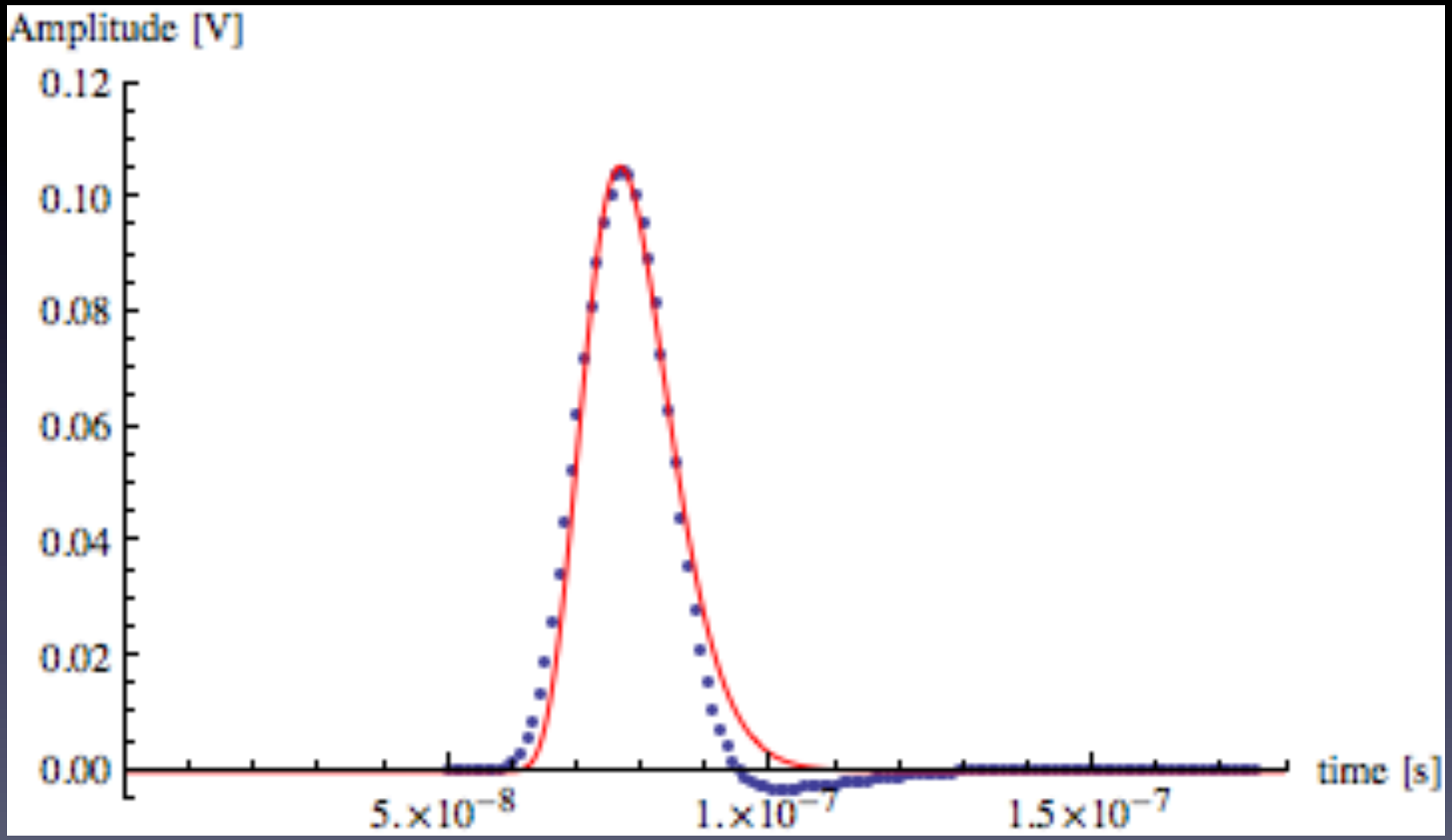
σ_t ~ 1.5 ns

Simulations: Noise (1)

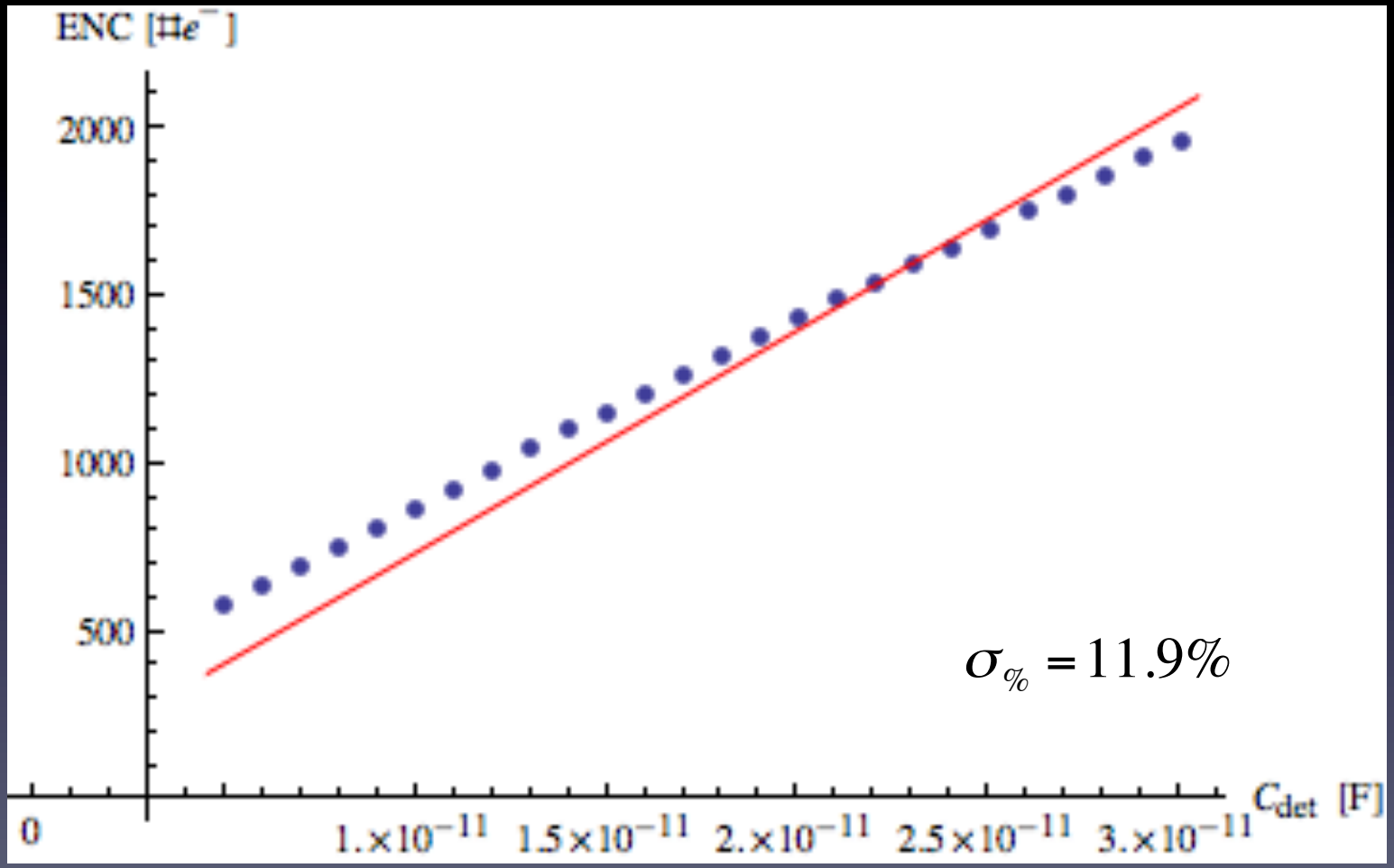




Simulations: Noise (2)



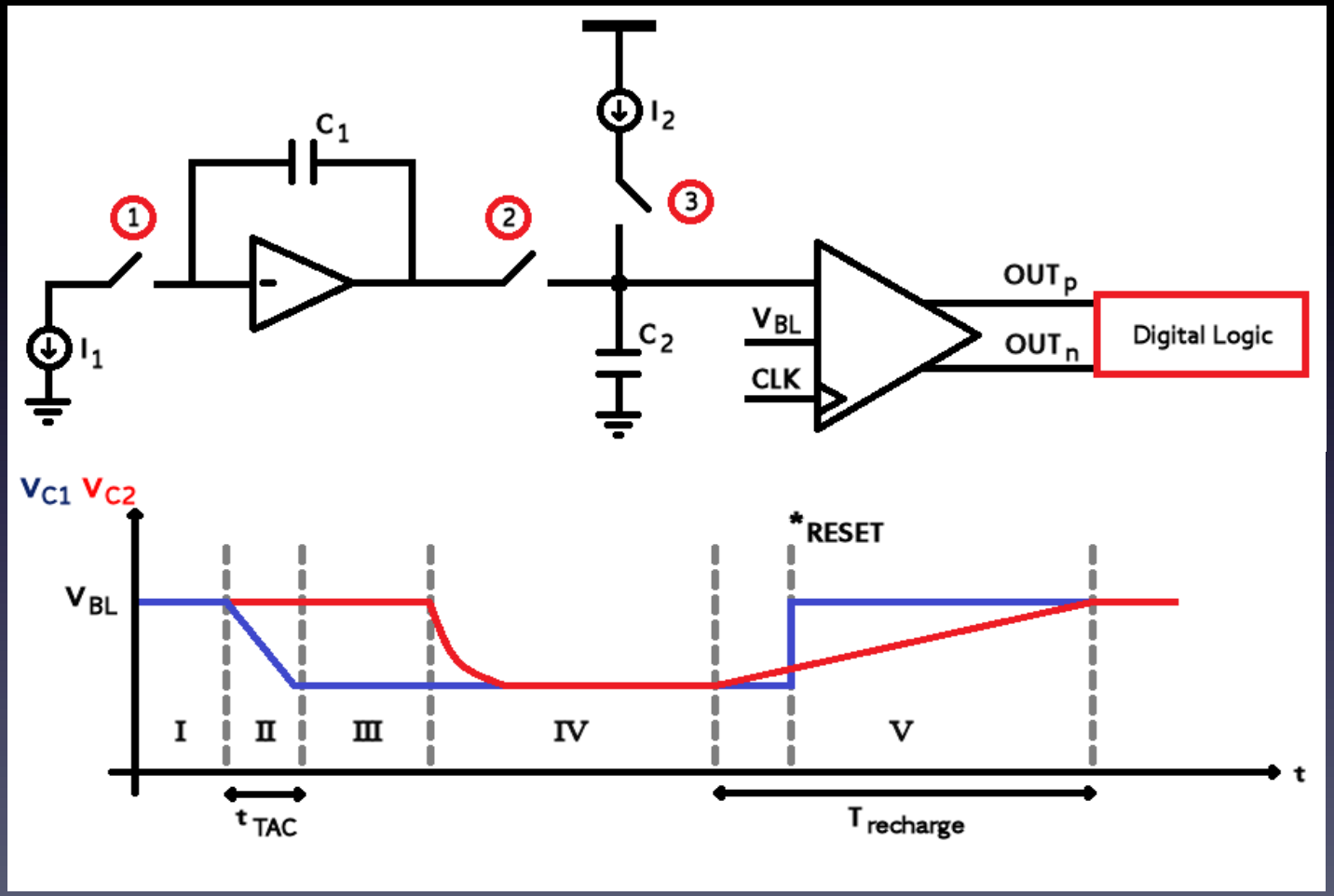
Simulations: Noise (3)



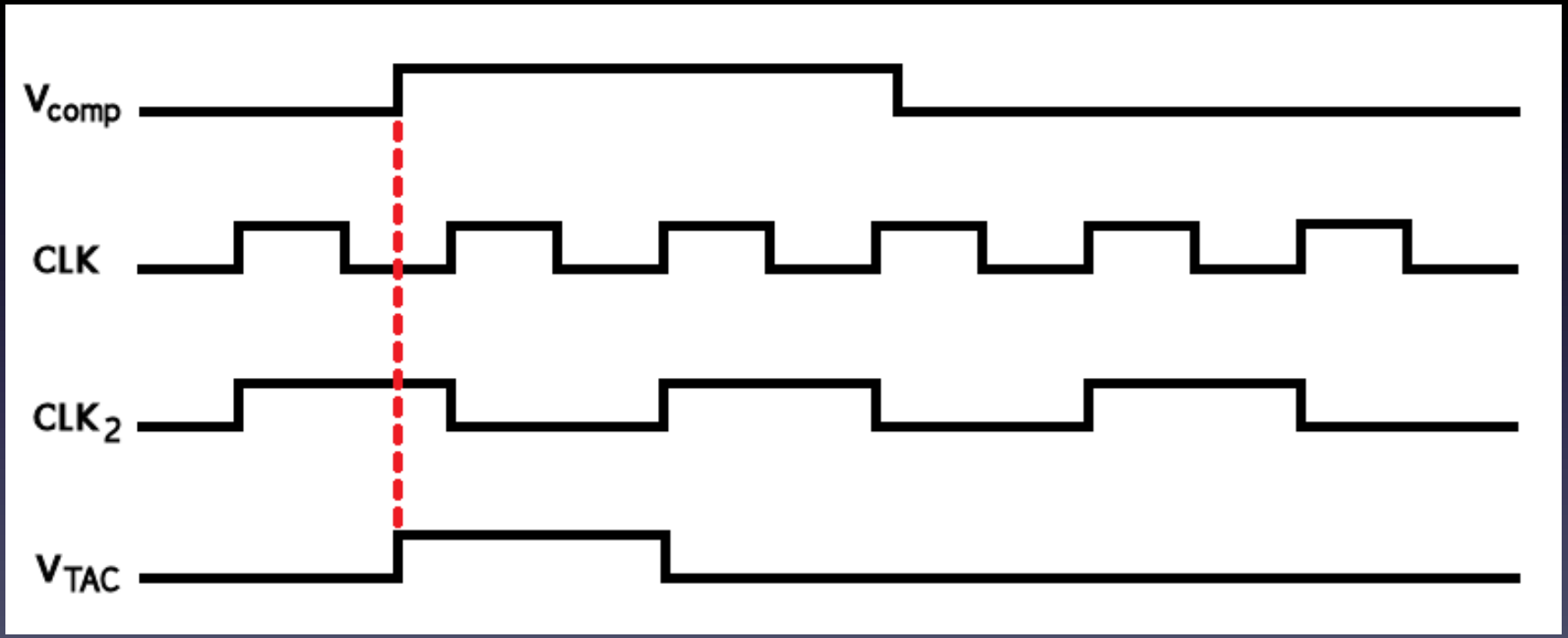
TDC Introduction

- Accurate time measuring (binning ~ 100 ps)
- Prototype under testing
- Study the implementation with a new cheaper 0.11 μm technology

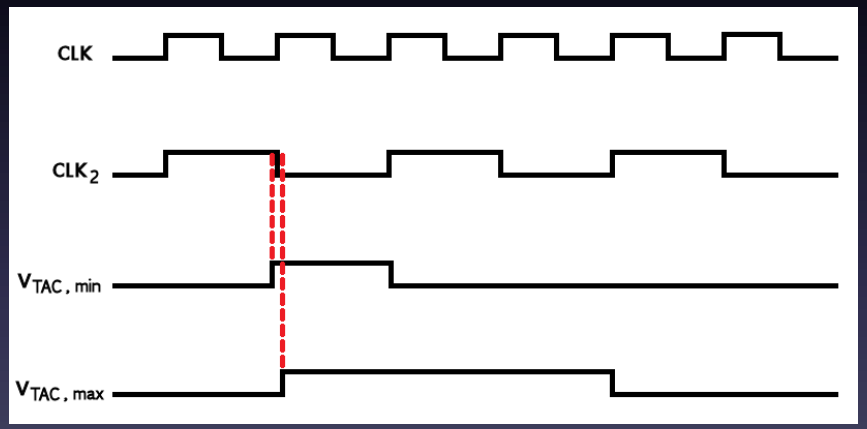
TDC Implementation



TDC Principles (1)



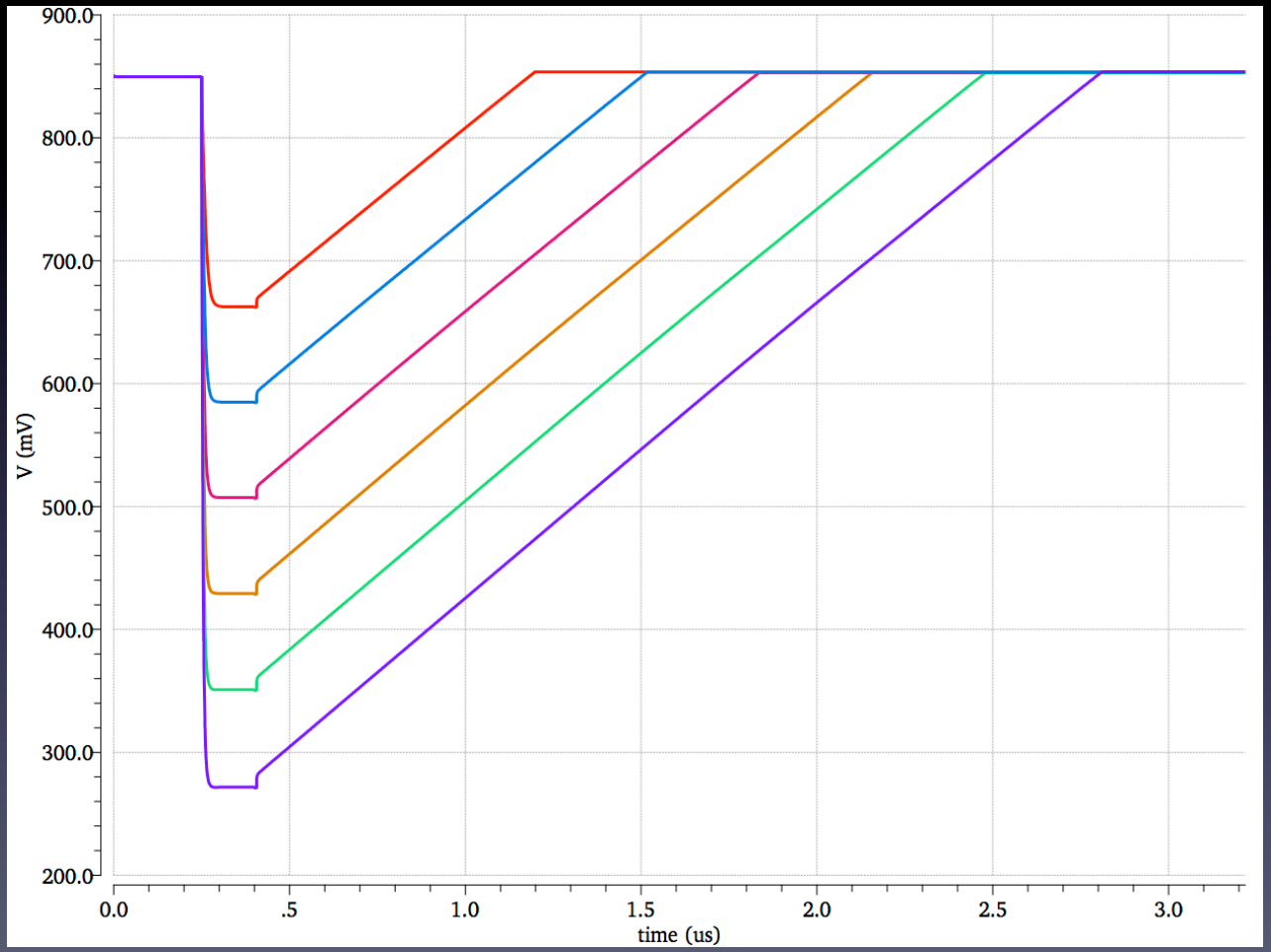
TDC Principles (2)



- $T_{CLK} < t_{TAC} < 3\,T_{CLK}$
- Binning ~ 50 ps

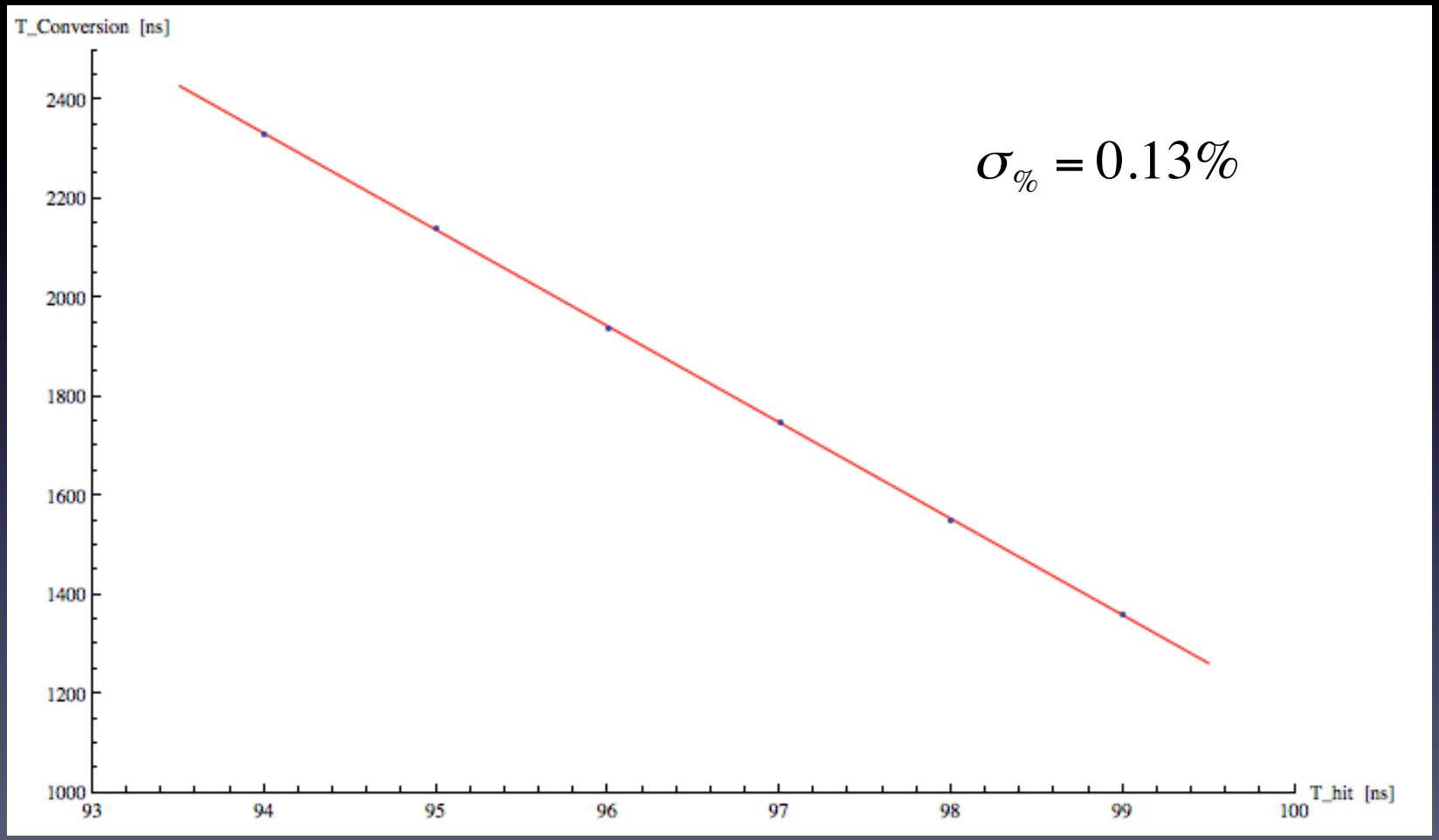
$$T_r = \frac{I_1}{I_2}\frac{C_2}{C_1}t_{TAC}$$

Simulations: TDC Linearity (1)



Simulations by Alberto Riccardi

Simulations: TDC Linearity (2)



Simulations by Alberto Riccardi

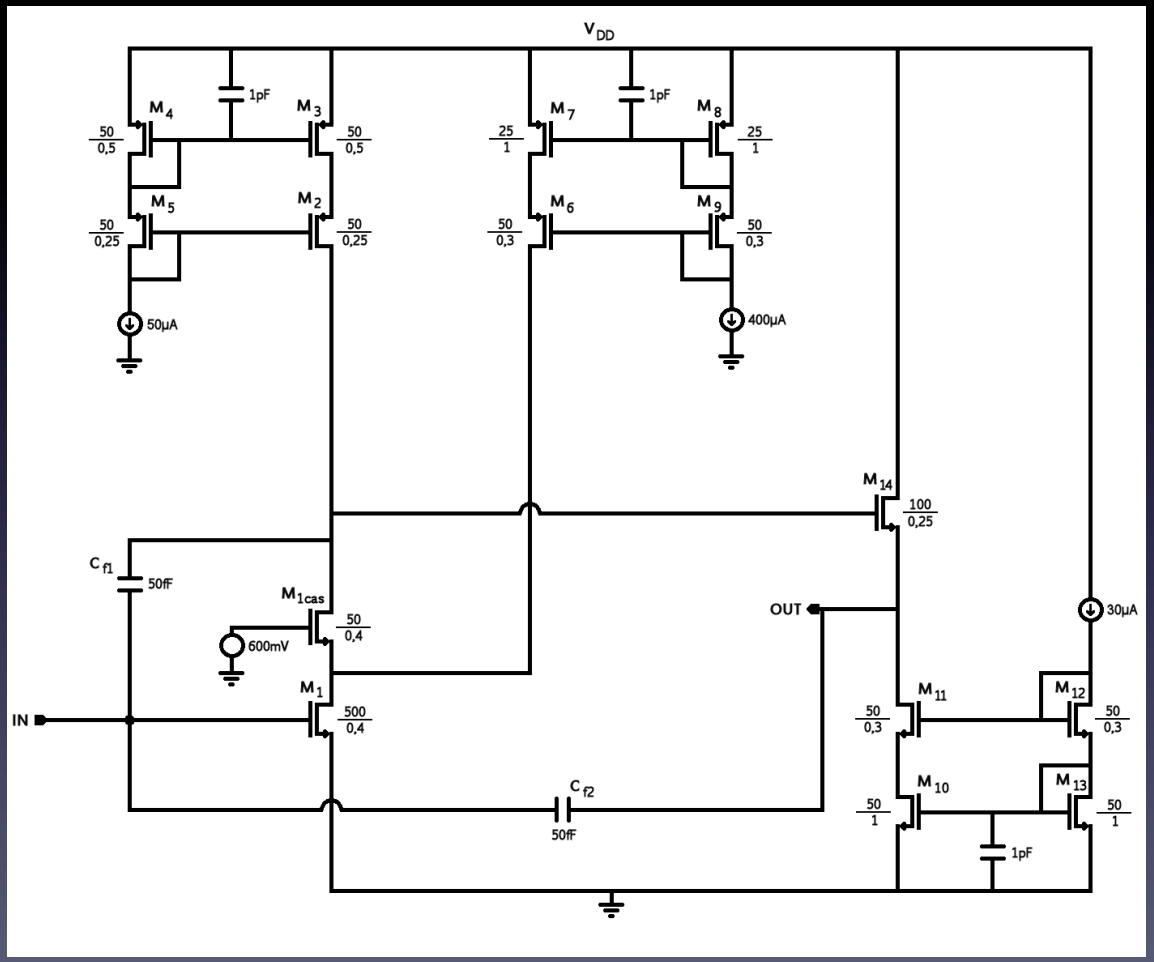
Conclusions and perspectives

- Matching between electronics and physics simulations
- Improvement of the ToT stage output linearity
- Topology adjustment to process signals of both polarities
- Improvement of the TDC flexibility
- Combined simulations FE+TDC
- Layout design

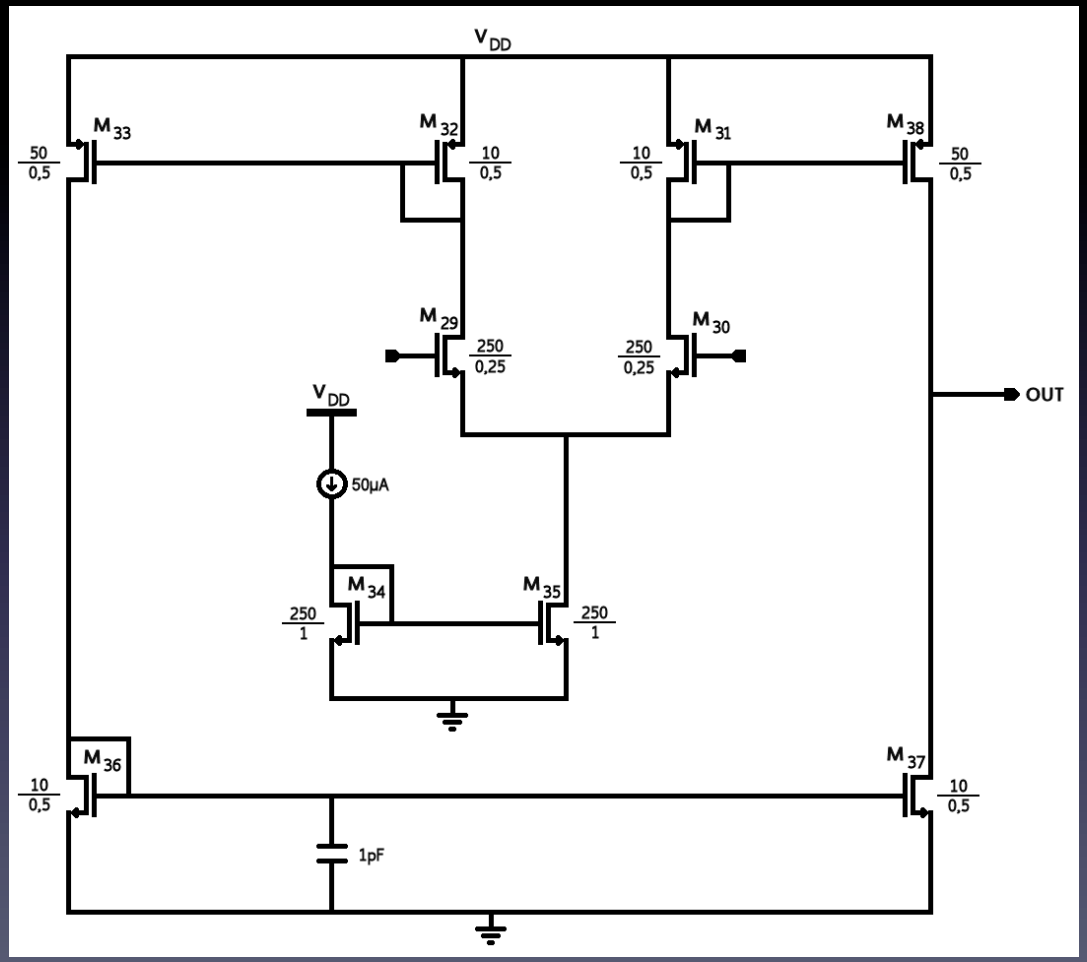

Thank you for your
kind attention

Backup Slides

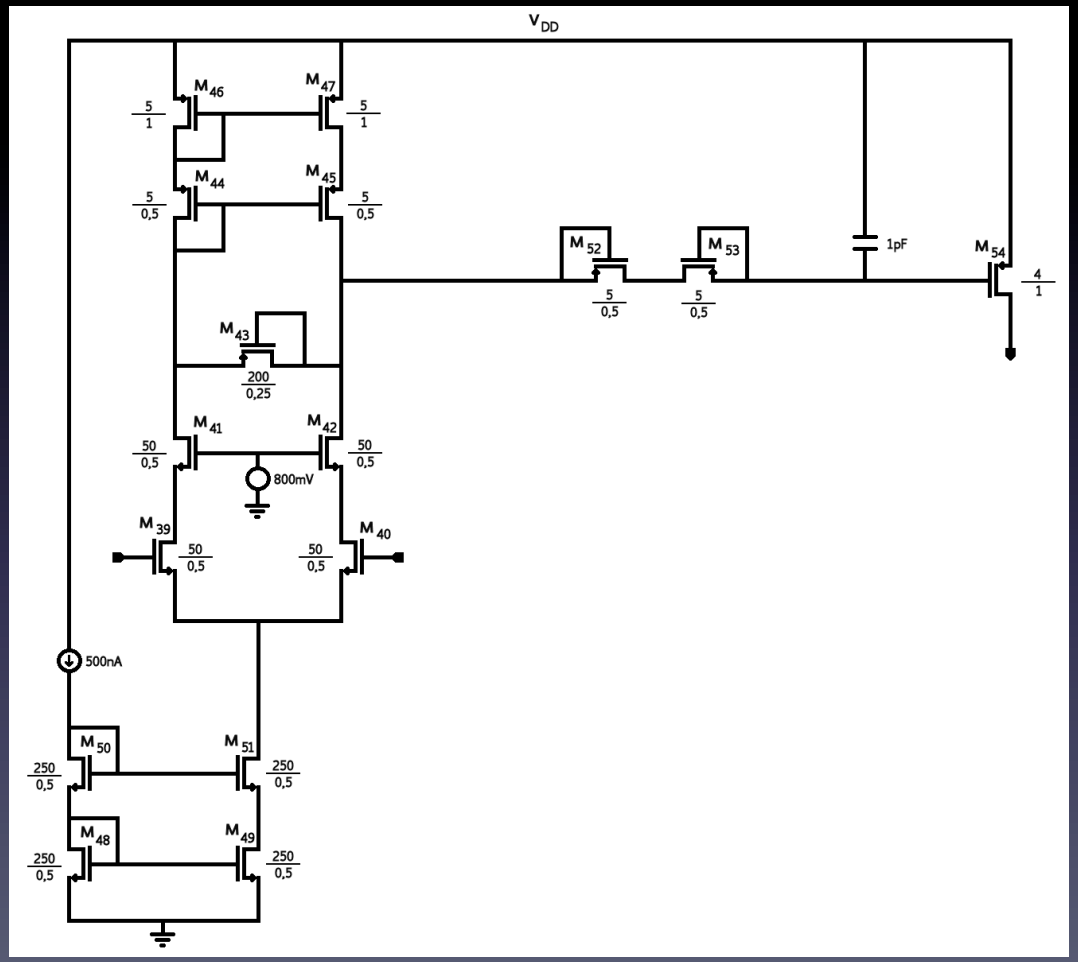
CSA schematic



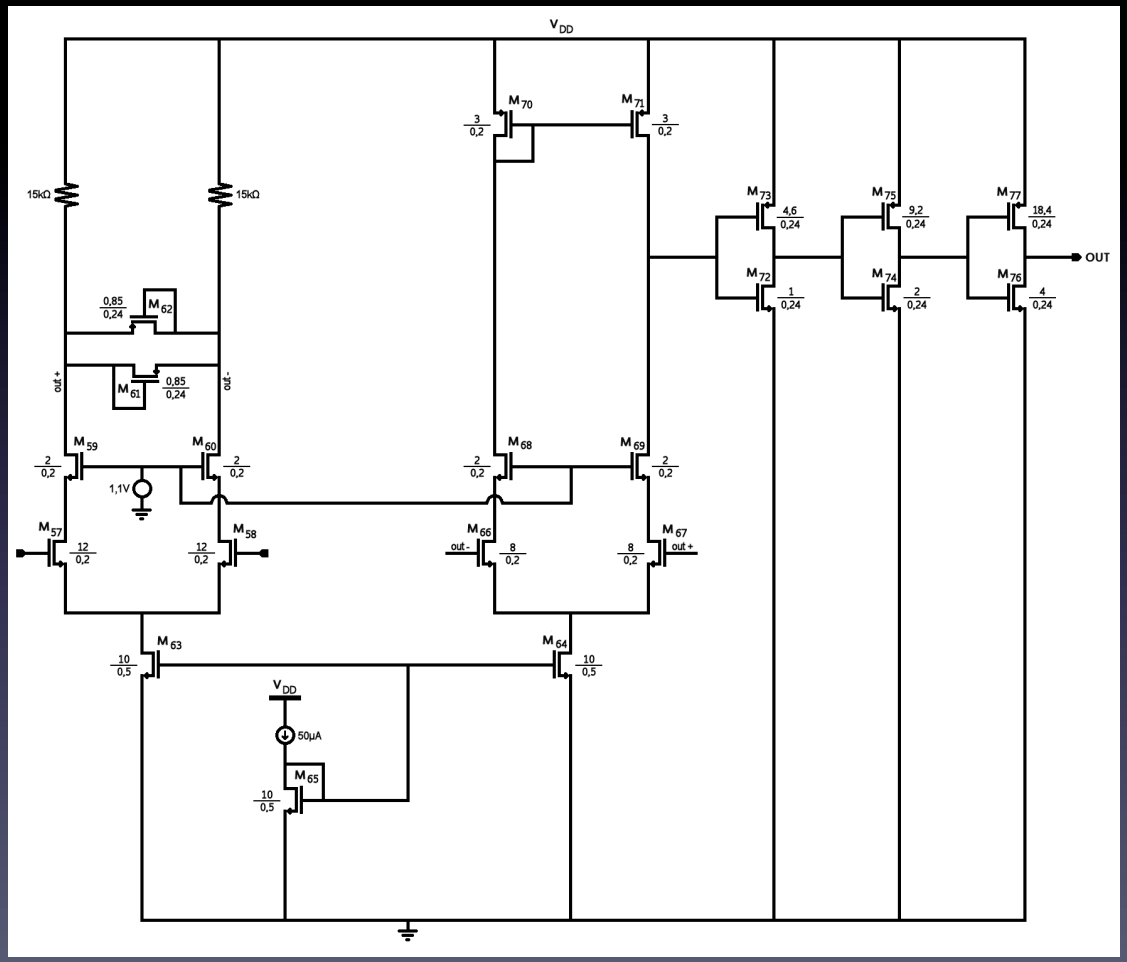
ToT Amplifier schematic



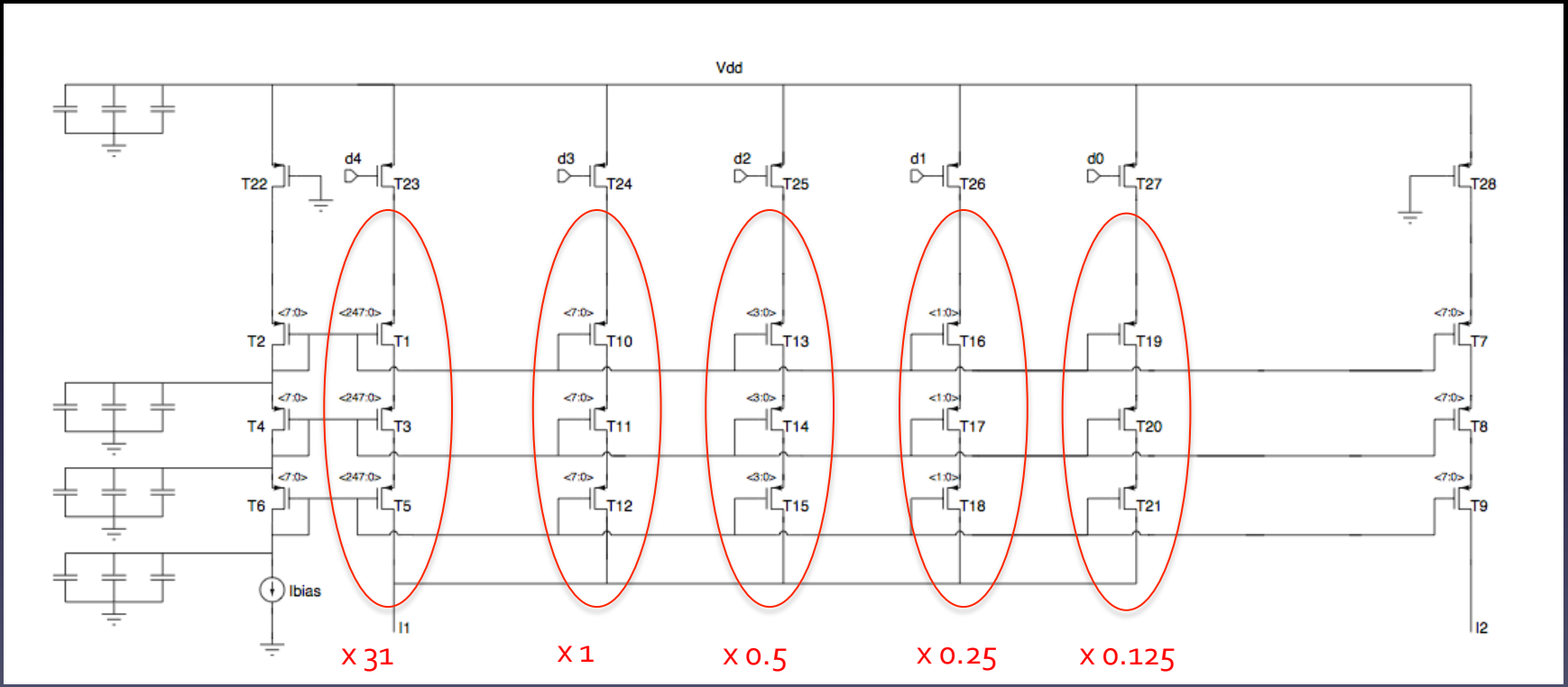
Baseline Holder schematic



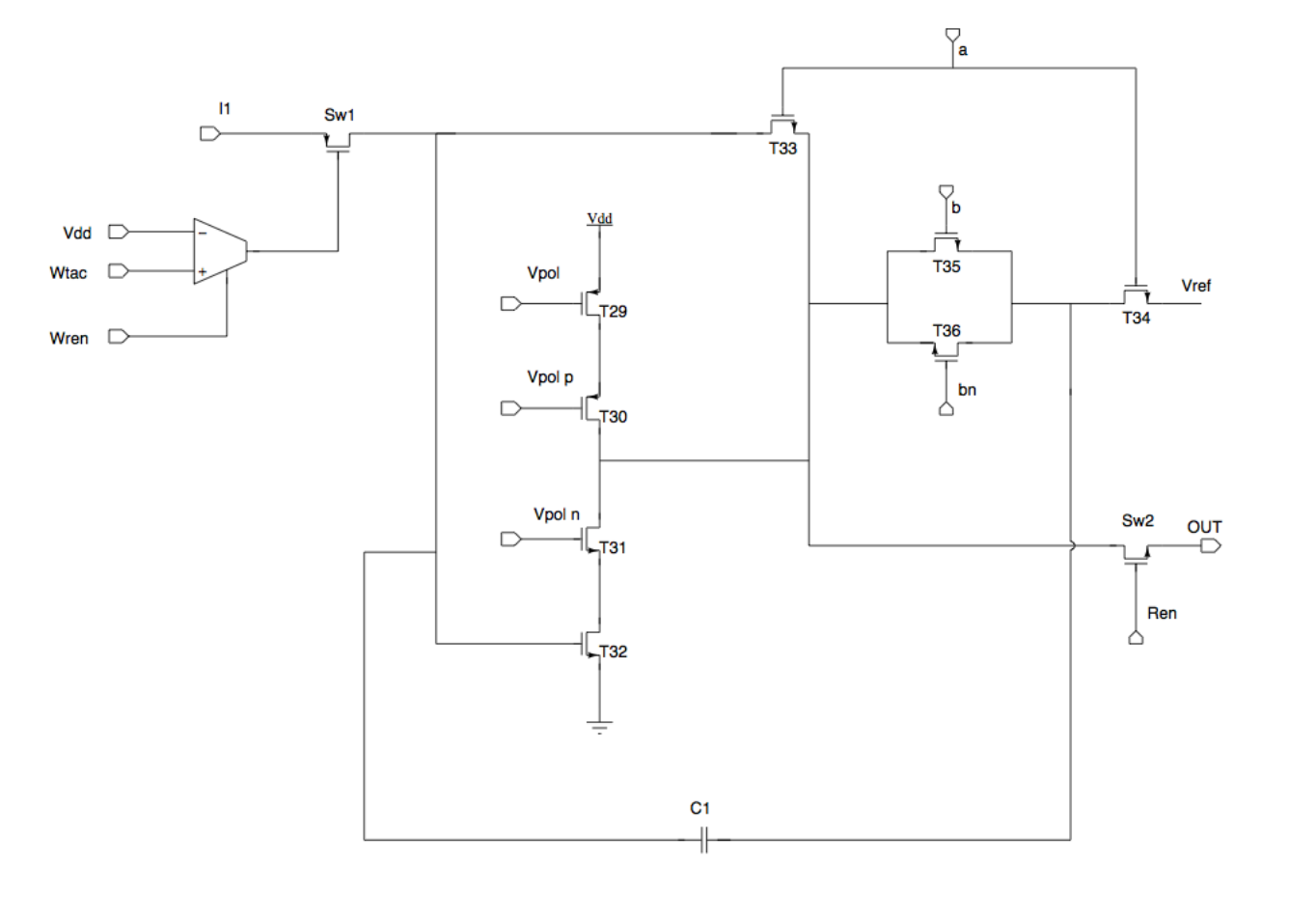
Comparator schematic



Current Source



Time to Amplitude Converter



Implemented pole-zero cancellation

- $$\left(R_f\right)_{eq} = \frac{v_{preamp}}{I_f} = \left(\frac{g_{m17}}{g_{m16}}\right) \cdot \frac{1}{g_{m15}}$$
- $$\left(R_x\right)_{eq} = \frac{v_{out}}{I_{out}} = \left(\frac{g_{m17}}{g_{m18}}\right) \cdot \frac{1}{g_{m15}}$$
- $$\frac{g_{m17}}{g_{m16}} = 80$$
- $$\frac{g_{m17}}{g_{m18}} = 2$$

$$\frac{\left(R_f\right)_{eq}}{\left(R_x\right)_{eq}} = \frac{C_{pz}}{C_f} = 40$$

Simulations: FE performances

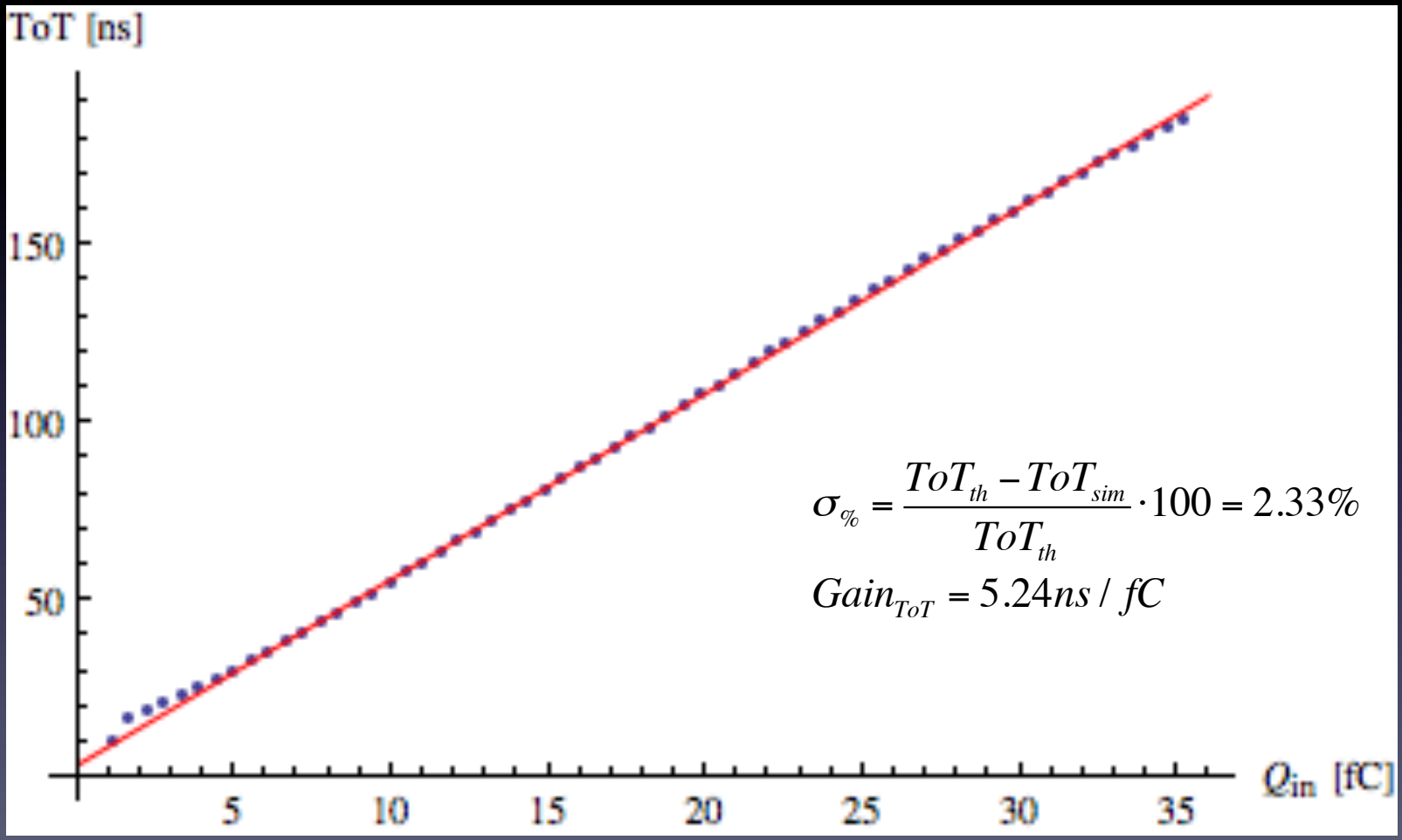
C_{det} = 5 pF

- ToT stage gain ~ 32 mV/fC
- SNR (Q_{in} = 4 fC) ~ 117

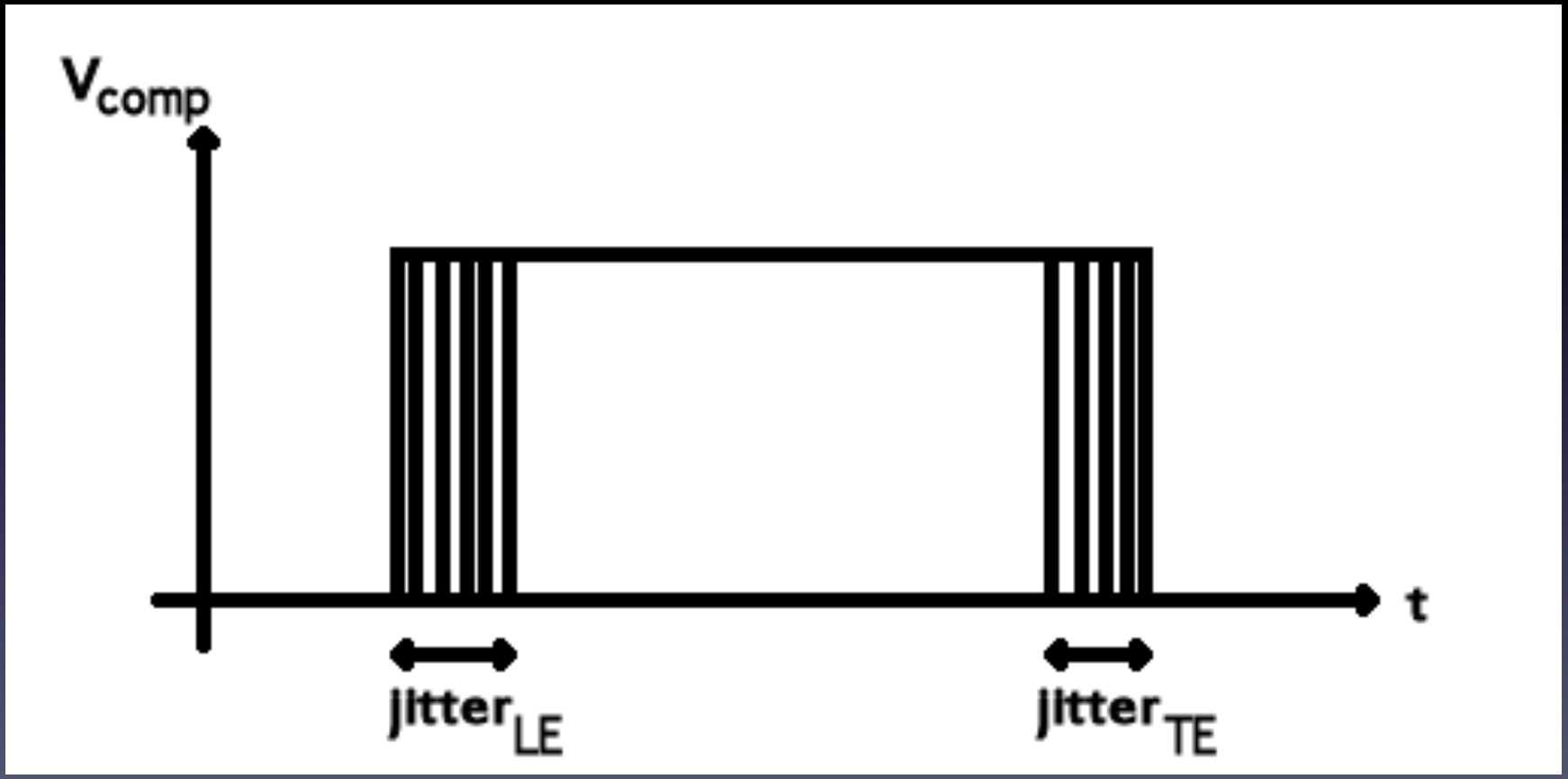
C_{det} = 30 pF

- ToT stage gain ~ 19 mV/fC
- SNR (Q_{in} = 4 fC) ~ 26

Simulations: Linearity

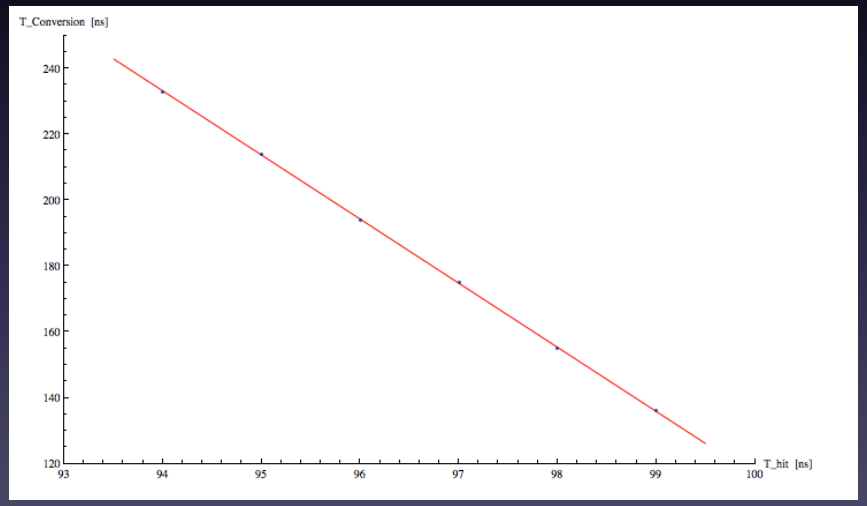


Simulations: Jitter (1)

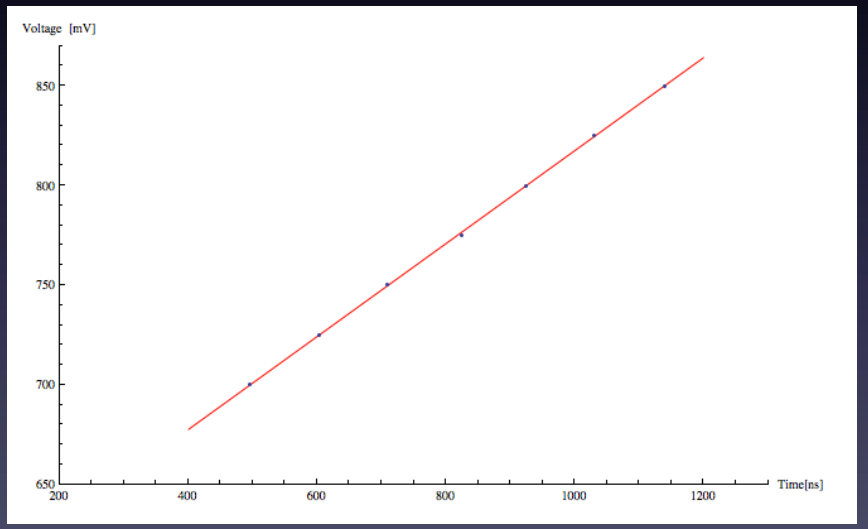


TDC Linearity

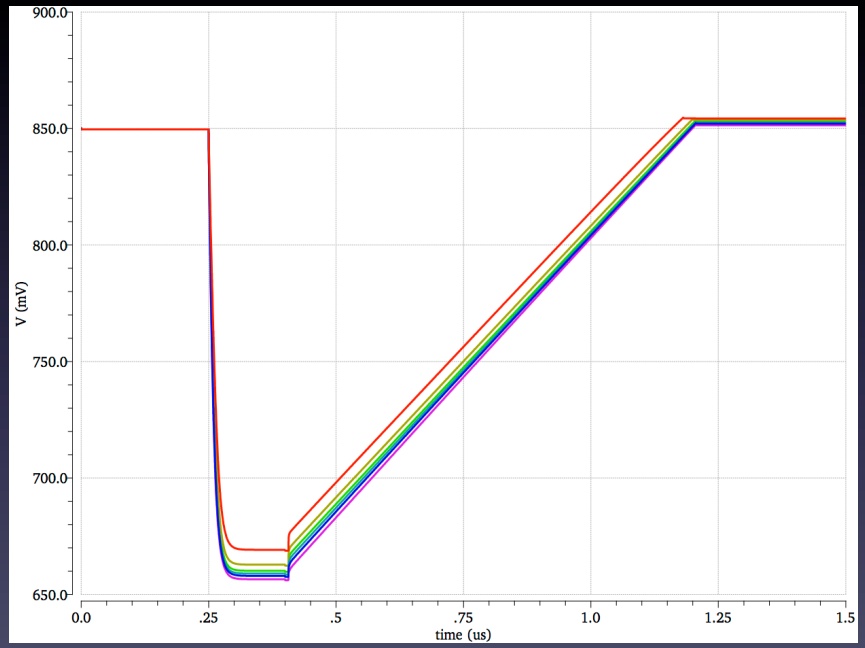
Discharging phase



Recharging phase

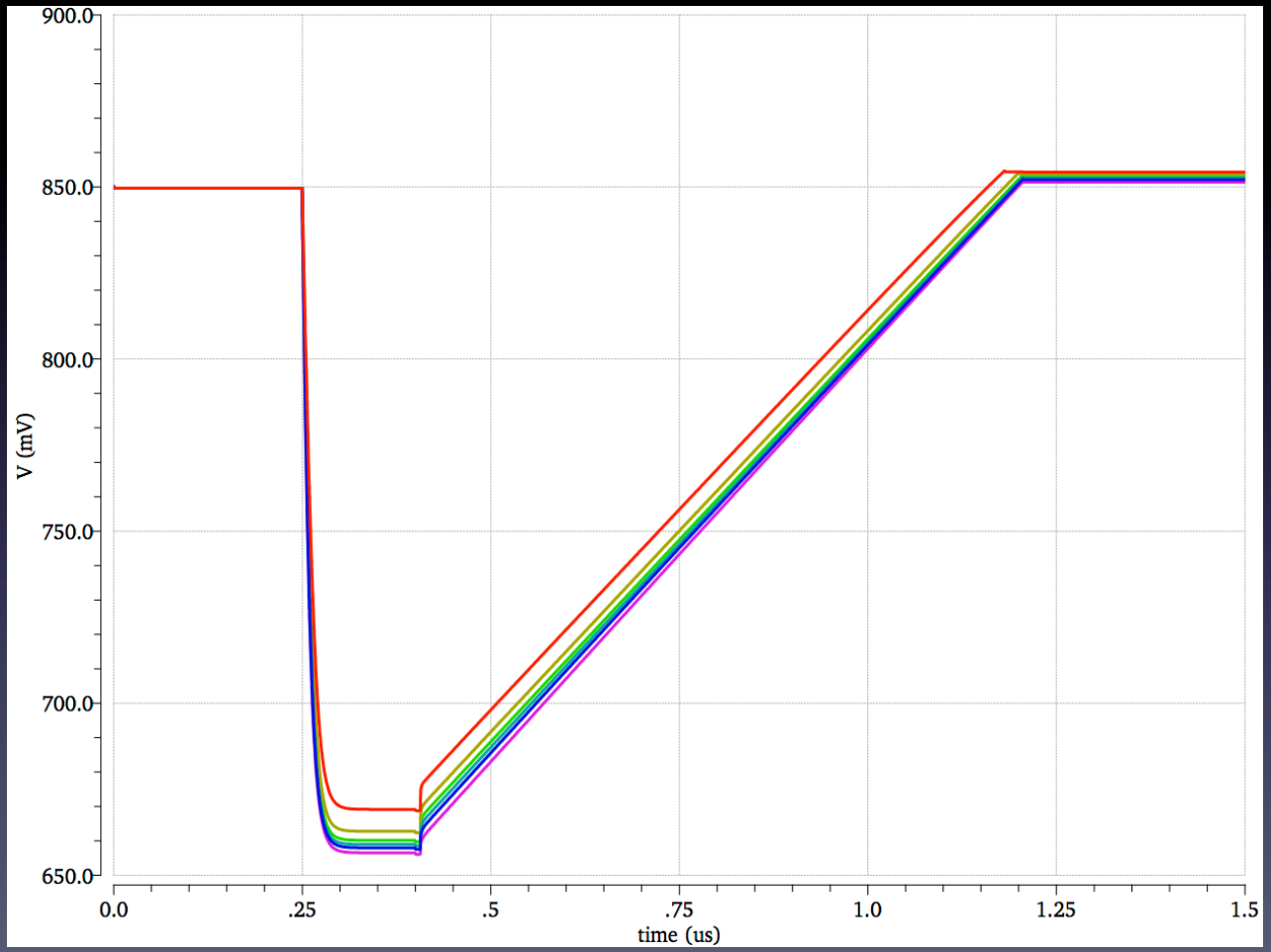


Simulations: Temperature variations

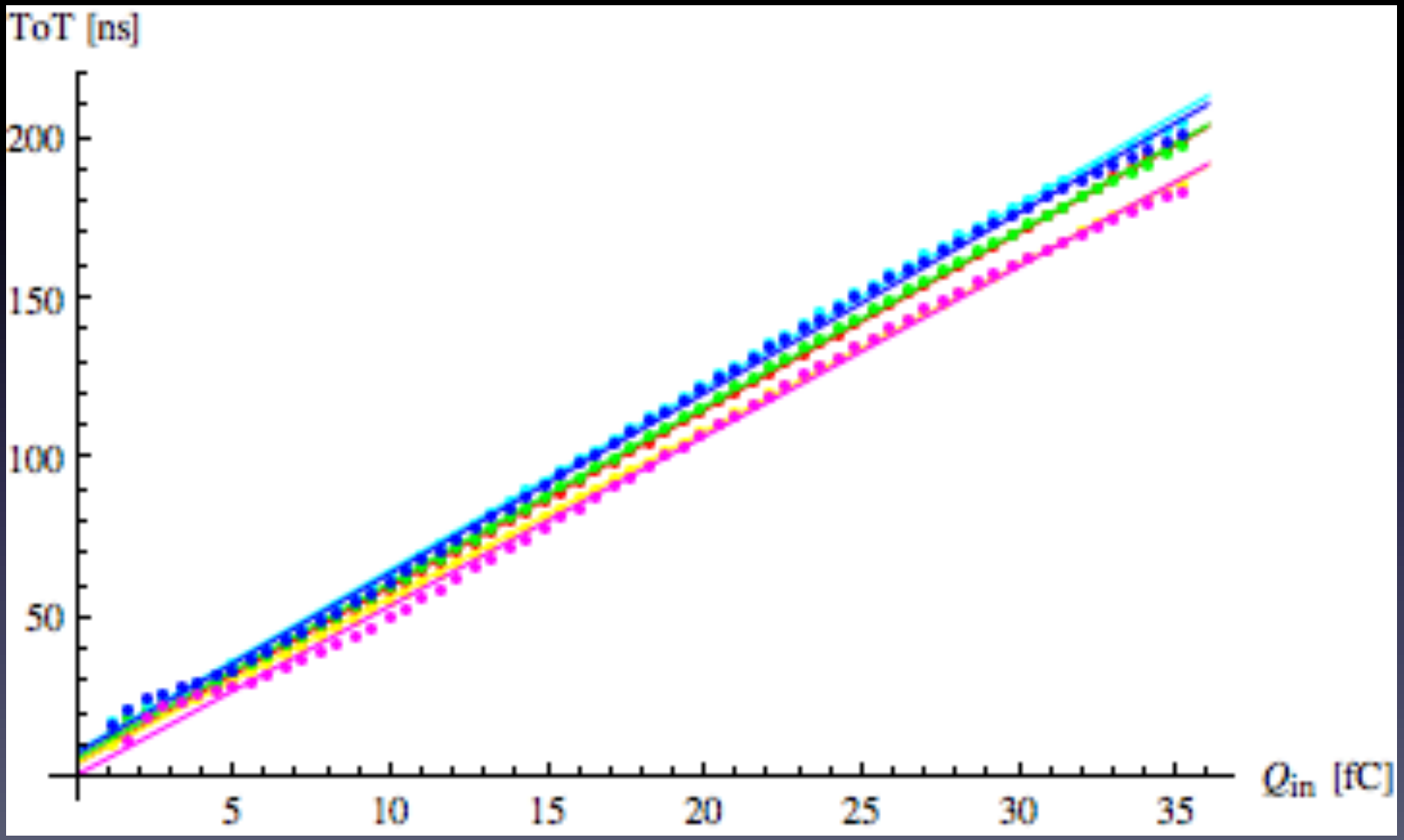


Temperature [°C]	Time of conversion
0	0010111101
25	0011000000
50	0011000001
75	0011000001
100	0011000001
125	0011000001

TDC Temperature variations

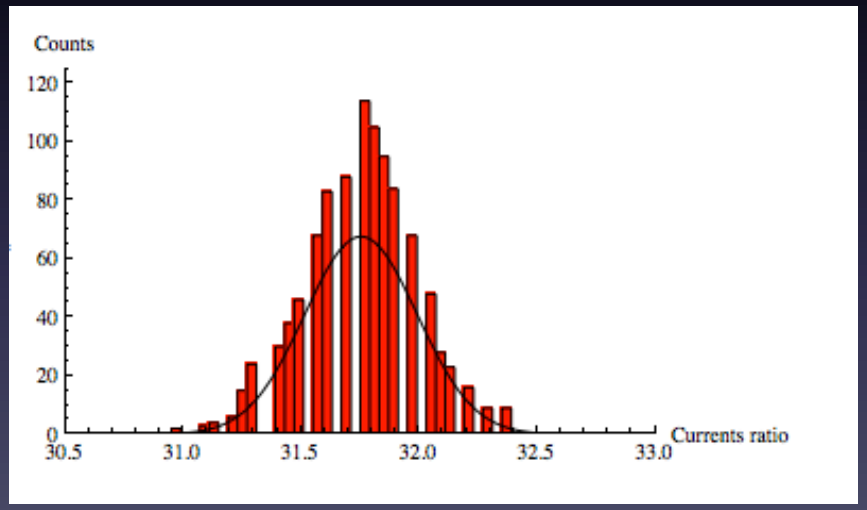


FE Temperature variations



A vs B Technologies

A Technology



B Technology