SODAnet on Kintex 7

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Differences to earlier Xilinx

- Reference: Virtex5 implementation by Peter Schakel et al. (uses one GTP/GTX, reset until expected data arrive)
- 7-Series: GBTs bundled by four (“Quad”)
- Individual channel PLLs + one (lower jitter) Quad PLL
- GTP (Artix) — GTX (Kintex) - GTH (Virtex) —— GTZ (Virtex)
- Logic ressources similar within 7 family, also most others (DSP, IO, clock)
- High-level SODAnet code (Jan Michel, for Lattice FPGA) could be synthesized and simulated with Xilinx ISE

RX schema

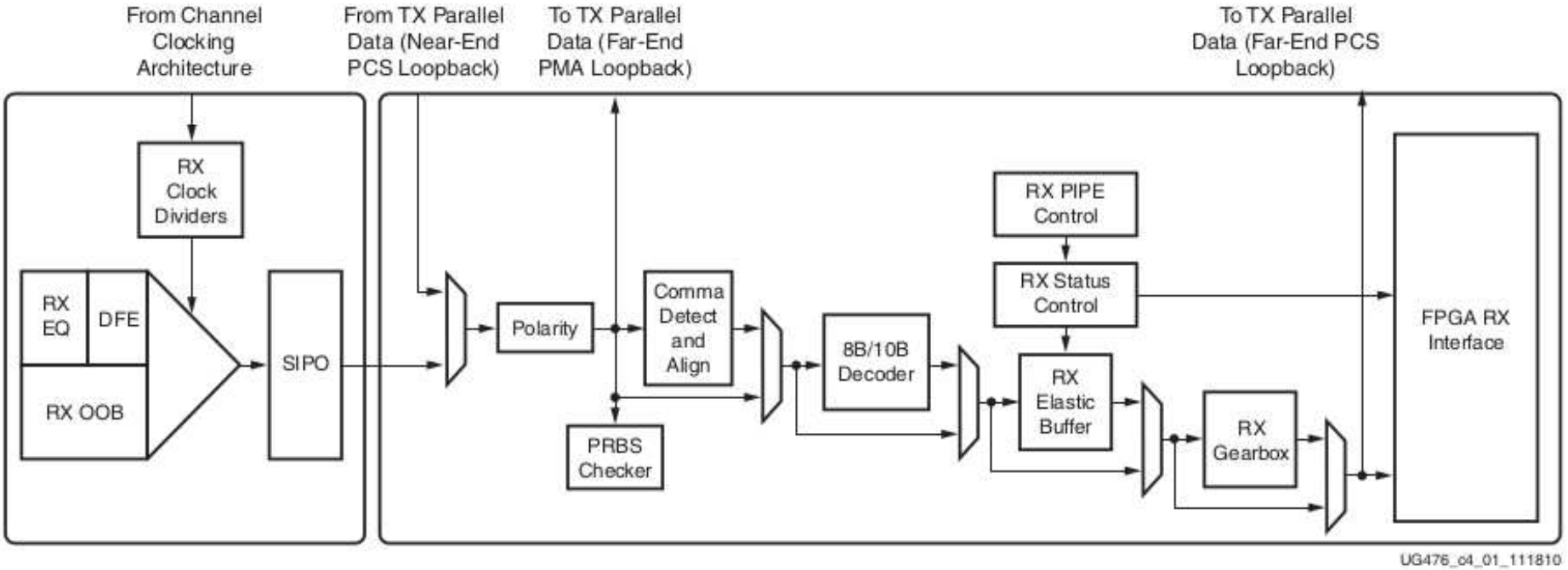

Figure 4-1: **GTX/GTH Transceiver RX Block Diagram**

Control of Byte Alignment

- New in 7-Series GTX: COMMA_ALIGN_LATENCY
- Access via DRP, 7 bits
- Also available on Artix GTP and Virtex7 GTH
- Possibilities:
  1. don't change alignment, use value to compensate
  2. use RXSLIDE with RXSLIDE_MODE=PMA (?)
  3. reset as before
- might allow to simplify pattern check, use builtin comma detection
- supposedly close to Lattice version (Jan Michel)

Open Questions, Outlook

- Clocking, Availability of usable oscillators on boards – Line rates?
- RXSLIDE useful? If yes, why not used before, eg. on Virtex 5? (Would make things more deterministic, avoid resets.)
- “Vivado” toolchain?
- Connection to GBTX (MVD) protocol