The TOFPET chip: a time based readout for radiation detectors

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PANDA FEE/DAQ WORKSHOP - 28-30/4/2013 - ALBA

Outline

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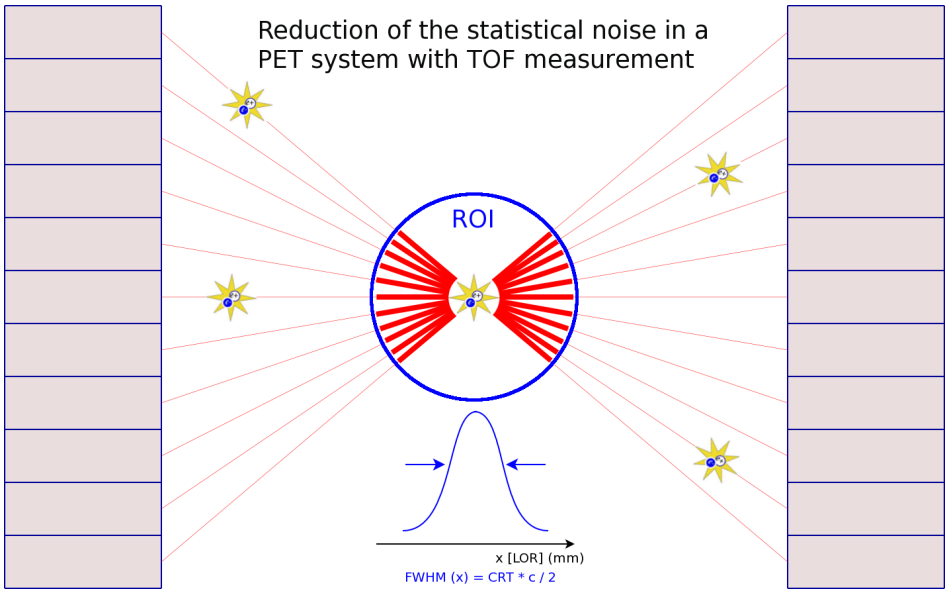
Motivation for Time-of-Flight measurements in PET



↪ A 200 ps coincidence resolving time (CRT) confines the annihilation coordinate to a 3 cm segment along the LOR.

- This measurement can identify, with an error $\Delta x = \Delta t \cdot \frac{c}{2}$, the position of the annihilation along the chord that defines the travel path of the back-to-back photons
  - spatial resolution is the same
  - **background rejection is significantly improved**
- Consequently achieving:
  - **Higher SNR of the reconstructed image,**
  - **Shorter exam time, or**
  - **Reduced injected dose of radiopharmaceutical**

EndoTOFPET-US FP7: Endoscopic PET and Ultrasound

Combined TOF-PET (200 ps time resolution), ultrasound imaging and endoscopic biopsy

PET components:
- dSiPM/crystal endoscopic probe
- aSiPM/crystal external plate

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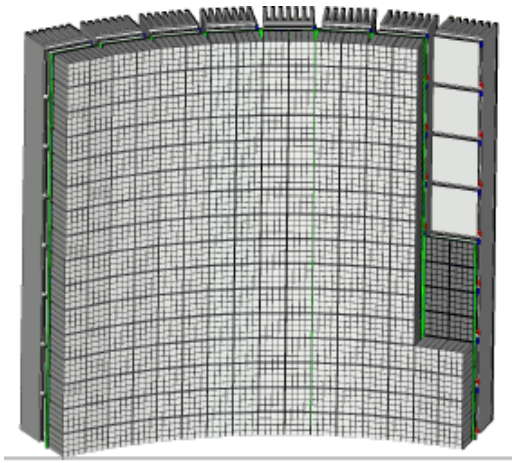
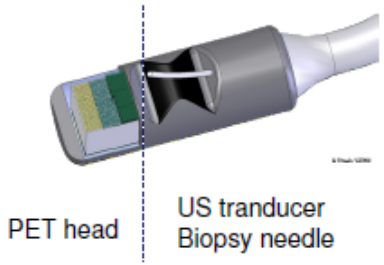
Readout ICs for Time-of-Flight PET

Combined **TOF-PET (200 ps coincidence resolving time resolution)**, ultrasound imaging and endoscopic biopsy



External PET plate



Endoscopic probe

- Extraction of TOF information: Need to trigger the time-of-arrival of the first photoelectron(s) to reduce the effect of the scintillation light statistics
- Endoscopic probe PET: crystals and SPAD array (TU Delft)
- External PET plate: crystals, SiPMs and custom ICs:
  - STiC2 (Univ. Heidelberg): digital-based TDC
  - **TOFPET-ASIC (LIP/INFN): analogue-based TDC**

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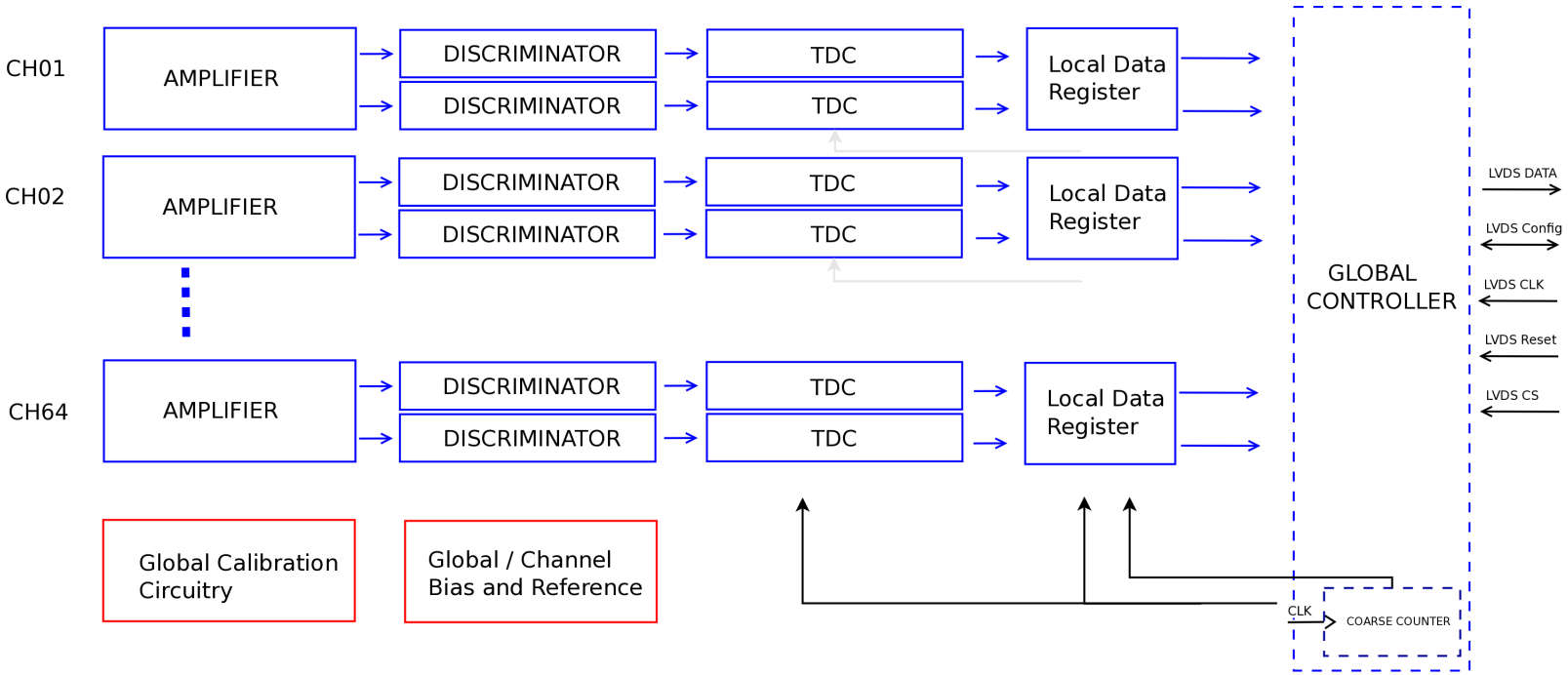
Features of an ASIC for SiPM readout in PET applications

Parameter	Value
Number of channels	64
Clock frequency	$80 - 160$ MHz
Dynamic range of input charge	**300 pC**
SNR ($Q_{in} = 100$ fC)	$>$ 20-25 dB
Amplifier noise (in total jitter)	$<$ 25 ps (FWHM)
TDC time binning	**50 ps**
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. channel hit rate	100 kHz
Max. output data rate	320 Mb/s (640 w/ DDR)
Channel masking	programmable
SiPM fine gain adjustment	**500 mV (5 bits)**
SiPM	up to 320pF term. cap., 2MHz DCR
Calibration BIST	internal gen. pulse, 6-bit prog. amplitude
Power	**$<$ 10 mW per channel**

Outline

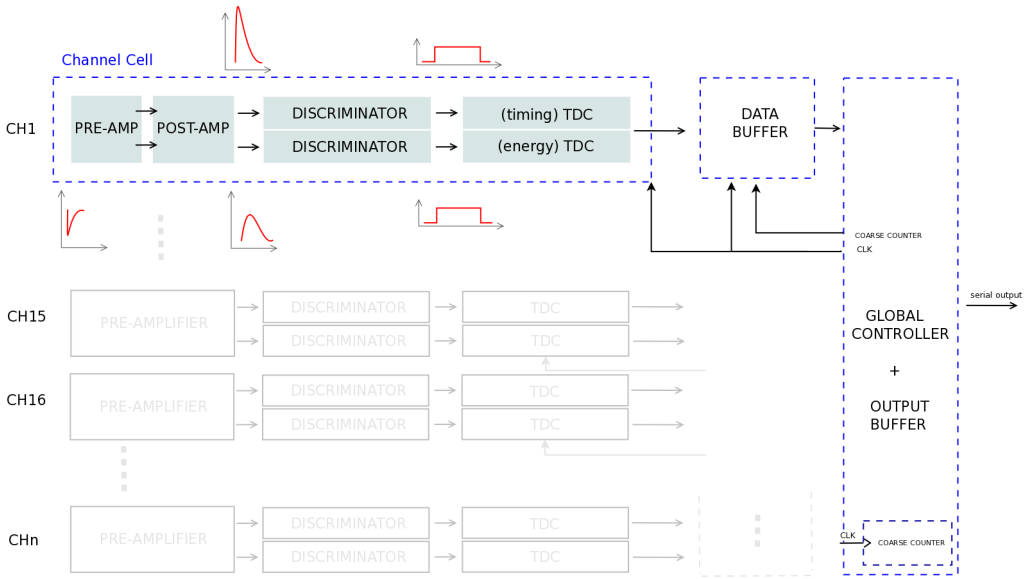
Overview of the chip architecture

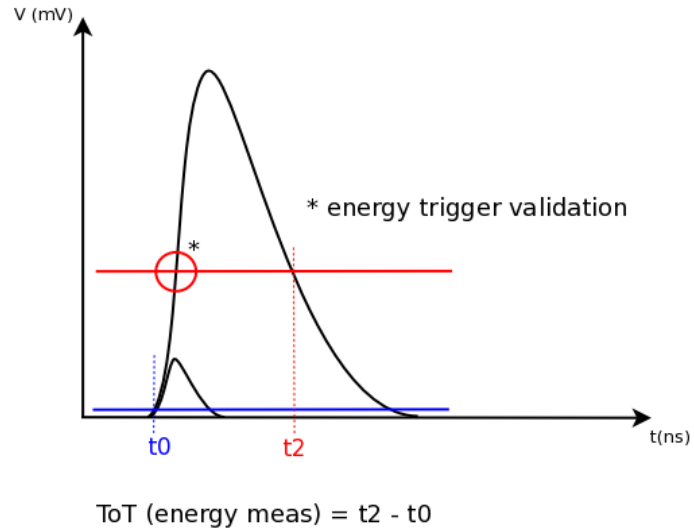
The TOFPET ASIC consists of a 64-channel analogue block, calibration circuitry, Golden-reference and Bias generators and a global controller.



- LVDS 10 MHz SPI configuration link for bias/channel setting
- LVDS 160-640 Mbps data output interface
- On-chip DACs and reference generators

Overview of the channel architecture

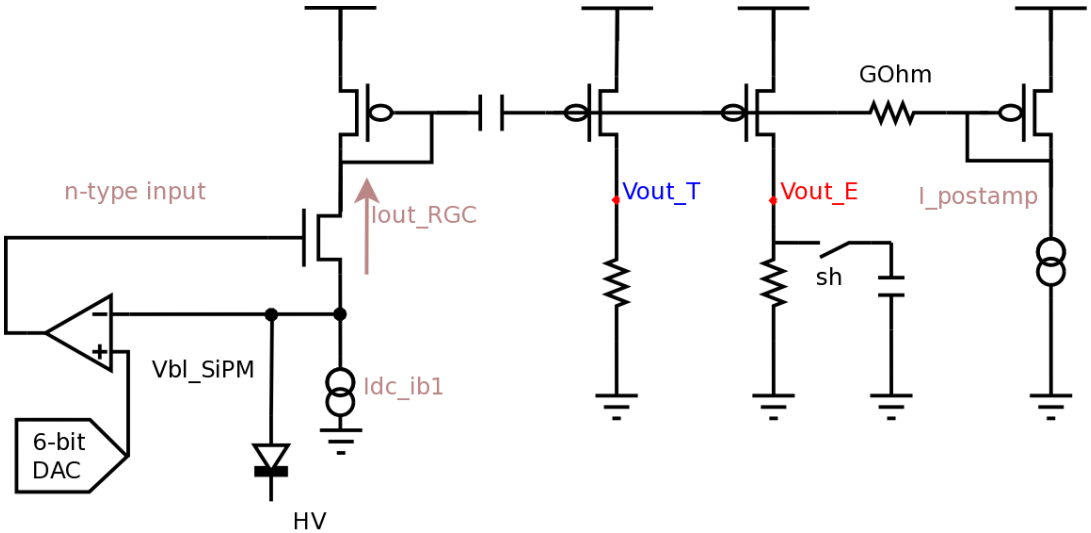


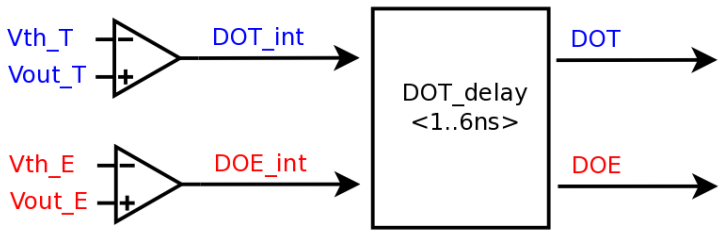


- Time and charge measurements with independent TDCs
- TDC time binning 50 ps (option 25 ps)
- Charge measured with Time-over-threshold

Front-End

- Low-Zin pre-amplifier, 2 independent TIA branches for Timing and Energy triggers
- Fine adjustment of the HV bias (6-bit over 500mV range) of the SiPM
- Selectable shaping function for Vout_E to avoid re-triggering and correct eventual loss of ToT vs. Qin monotonicity
- Selectable delay line for dark count filtering
- Usable for p-type or n-type (hole, electron collection) devices

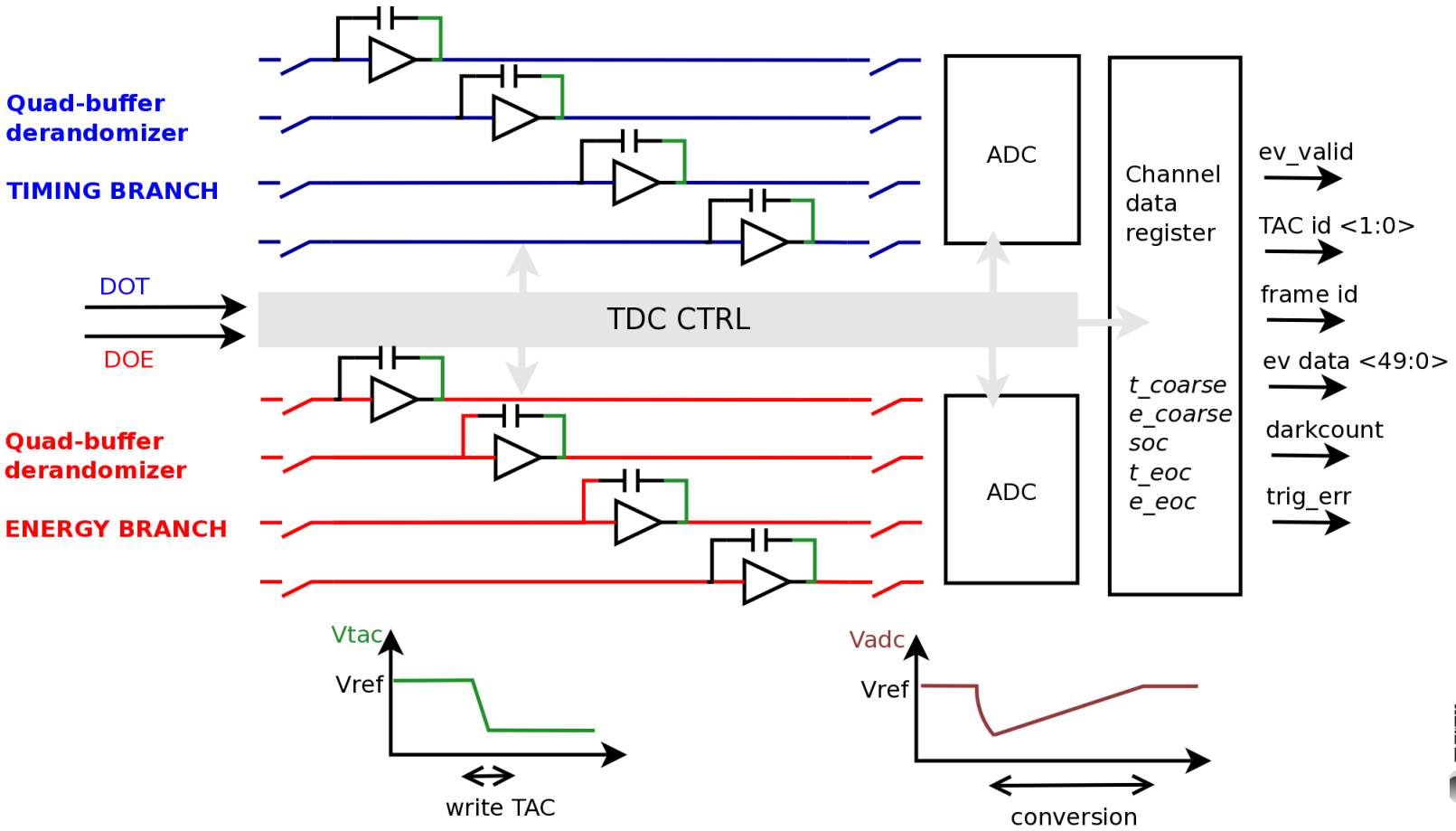




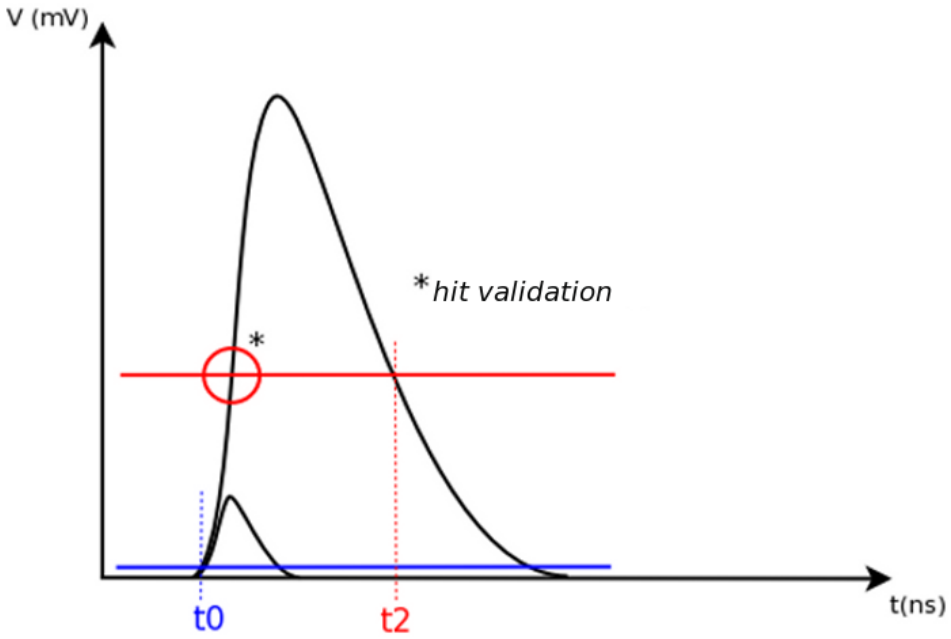
Time-to-Digital Converter

Analogue TDC with 50 ps time binning - based on Time-to-Amplitude Conversion [Stevens89, Rivetti09]

- TDC Control: switching, hit validation, buffer allocation, data reg.
- Time stamp: 10-bit master clock count + Fine time measurement

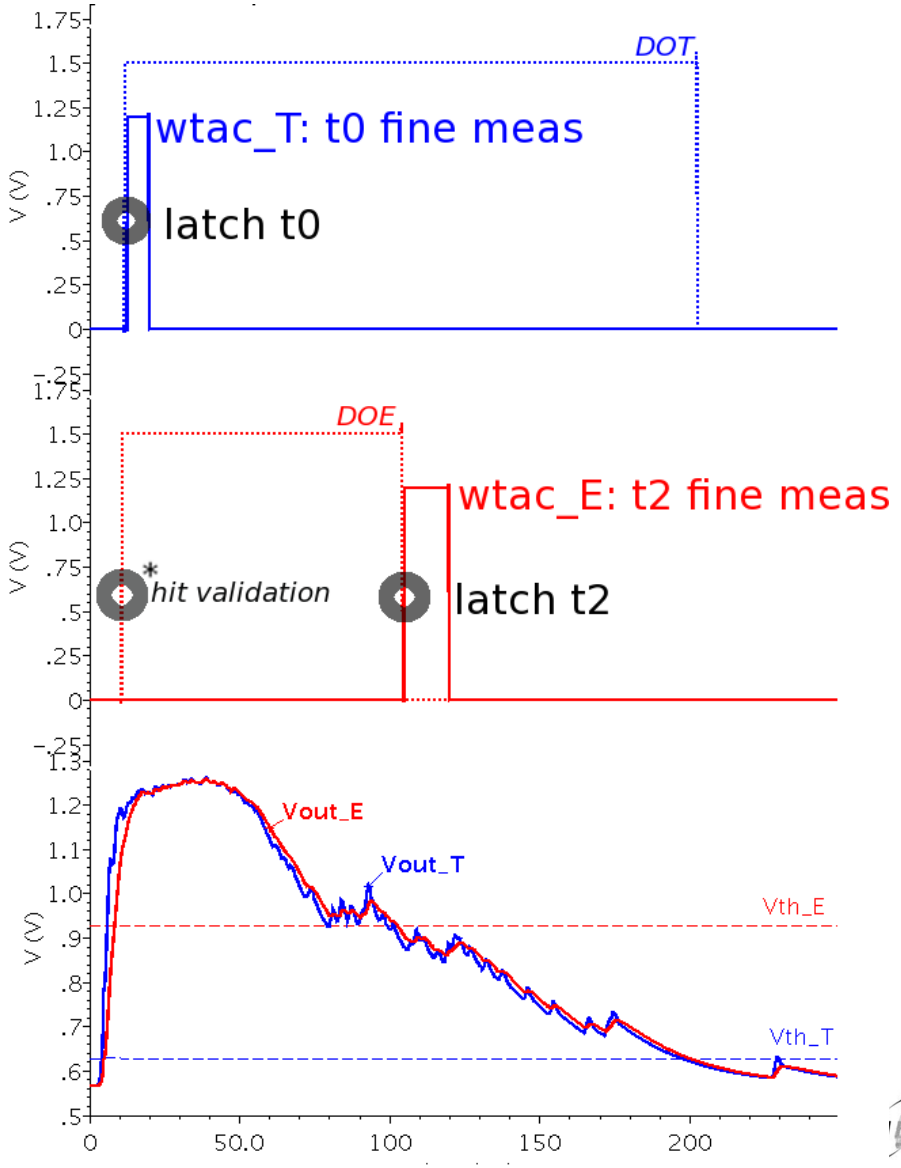


TDC operation for a valid event



ToT (energy meas) = t2 - t0

a)

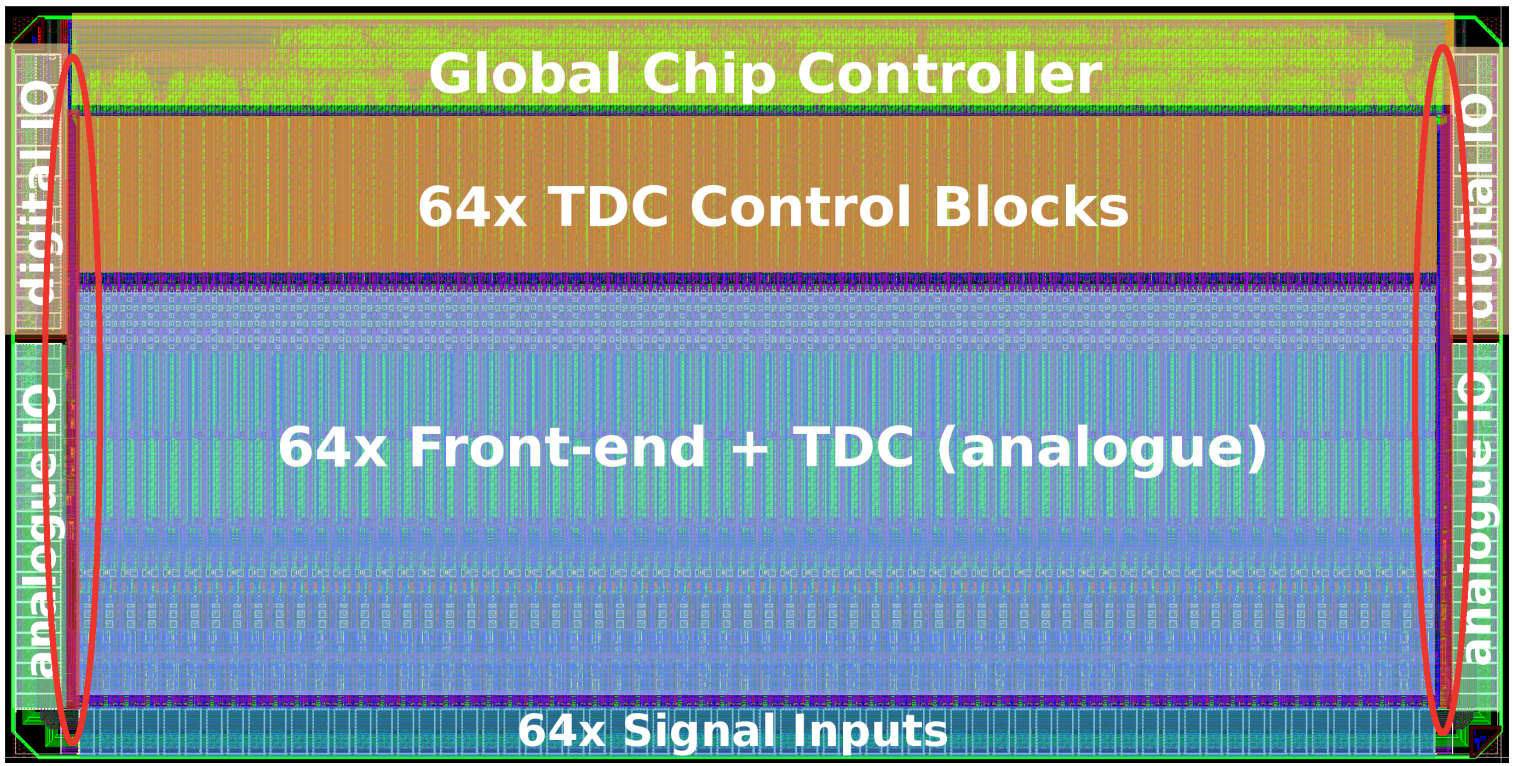


b)

Outline

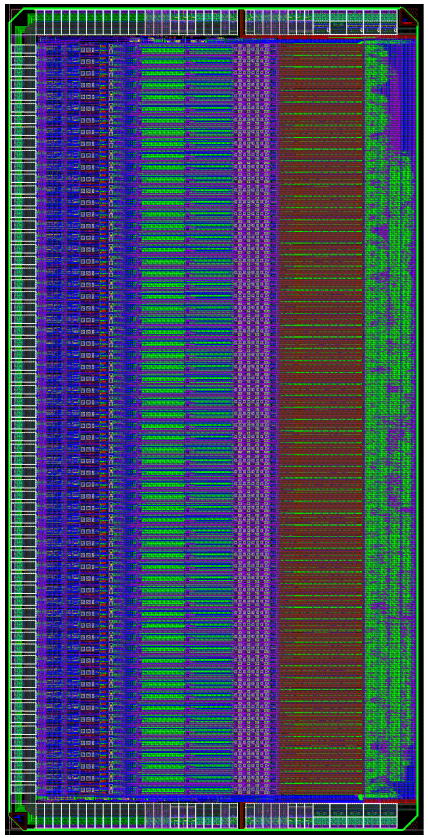
Floorplan of the 64-channel mixed-mode chip

- CMOS 130nm 25mm^2 64-channel ASIC
- Highlight shows the allocated area for bias and calibration circuitry.
- One pad-free edge to allow abutting two twin chips into a 128-channel BGA package.



Packaging of a 128-channel SiP

- The TOFPET ASIC has one pad-free edge
- That allows a second (rotated) chip to be abutted
- The compact 7x7 mm SiP can be packaged into a BGA



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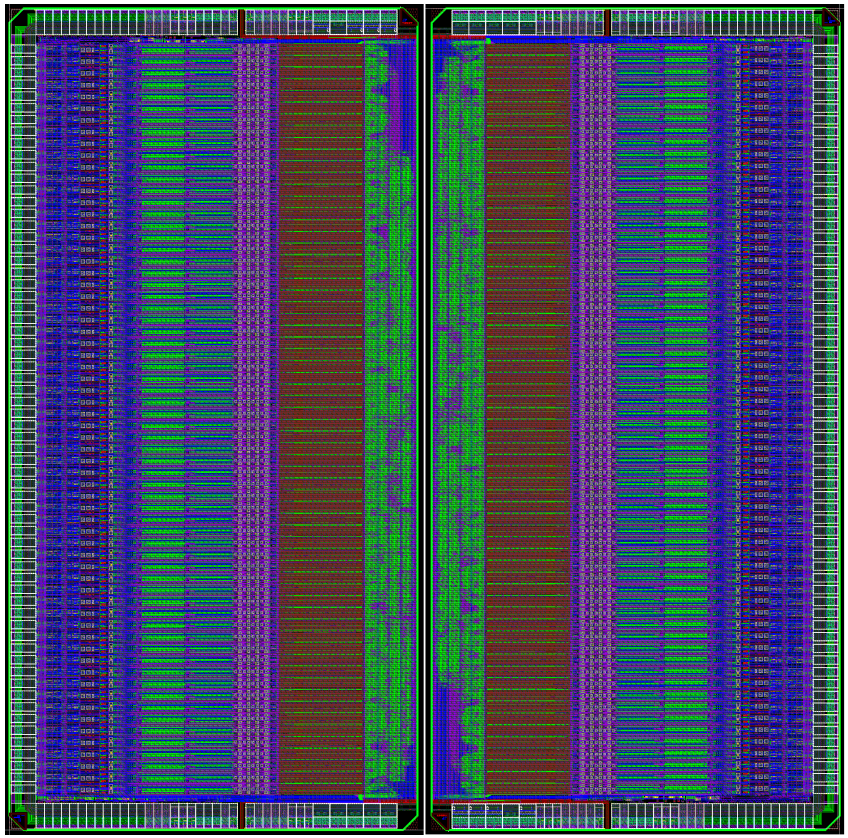

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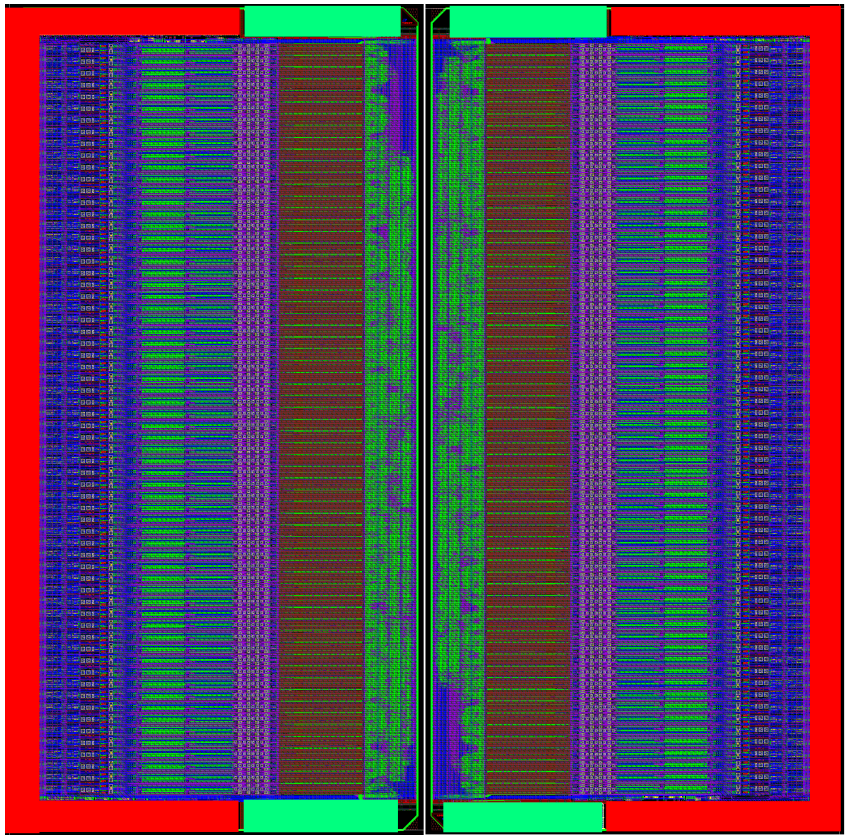

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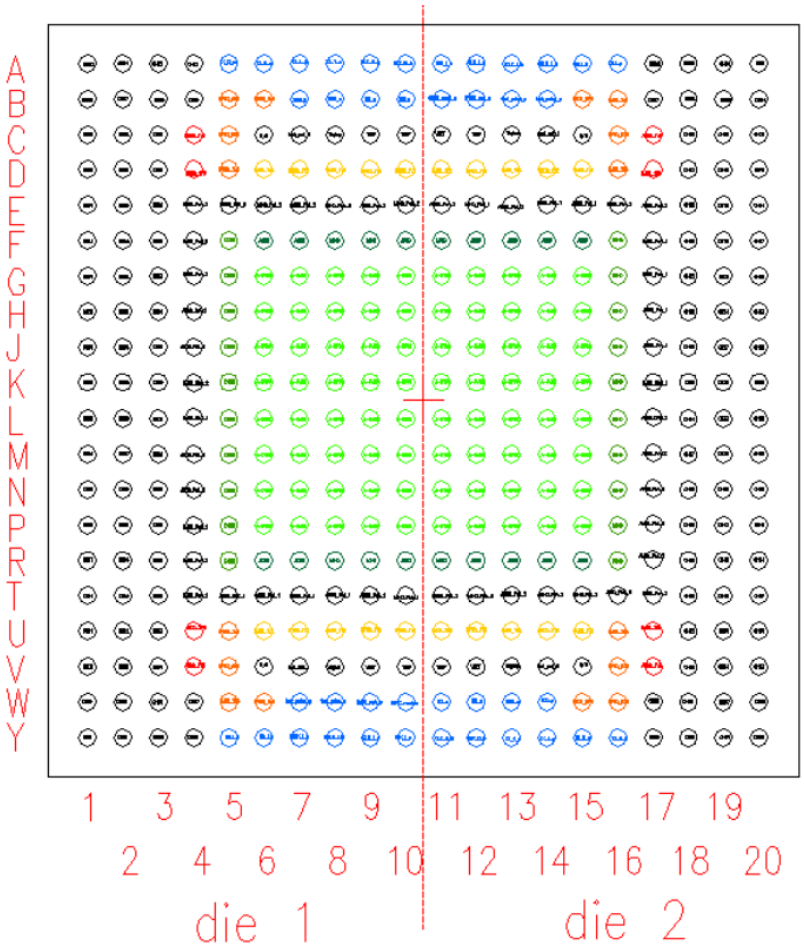
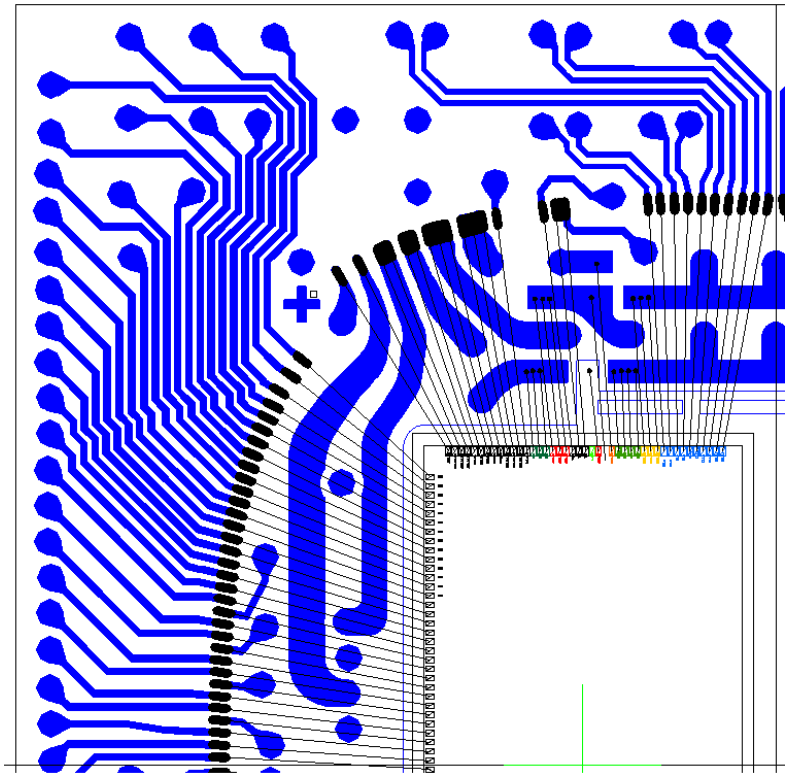
BGA package for the 128-channel assembly

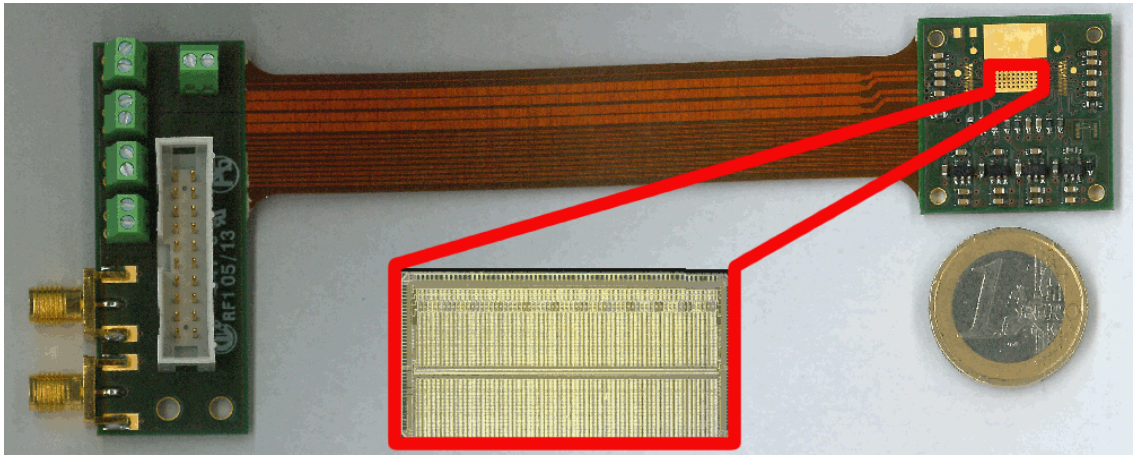
View of the BGA ballout (17x17x1.70 mm 4 Layers PBGA 400) for the 128-channel assembly (left) and corner detail of the package substrate (right):





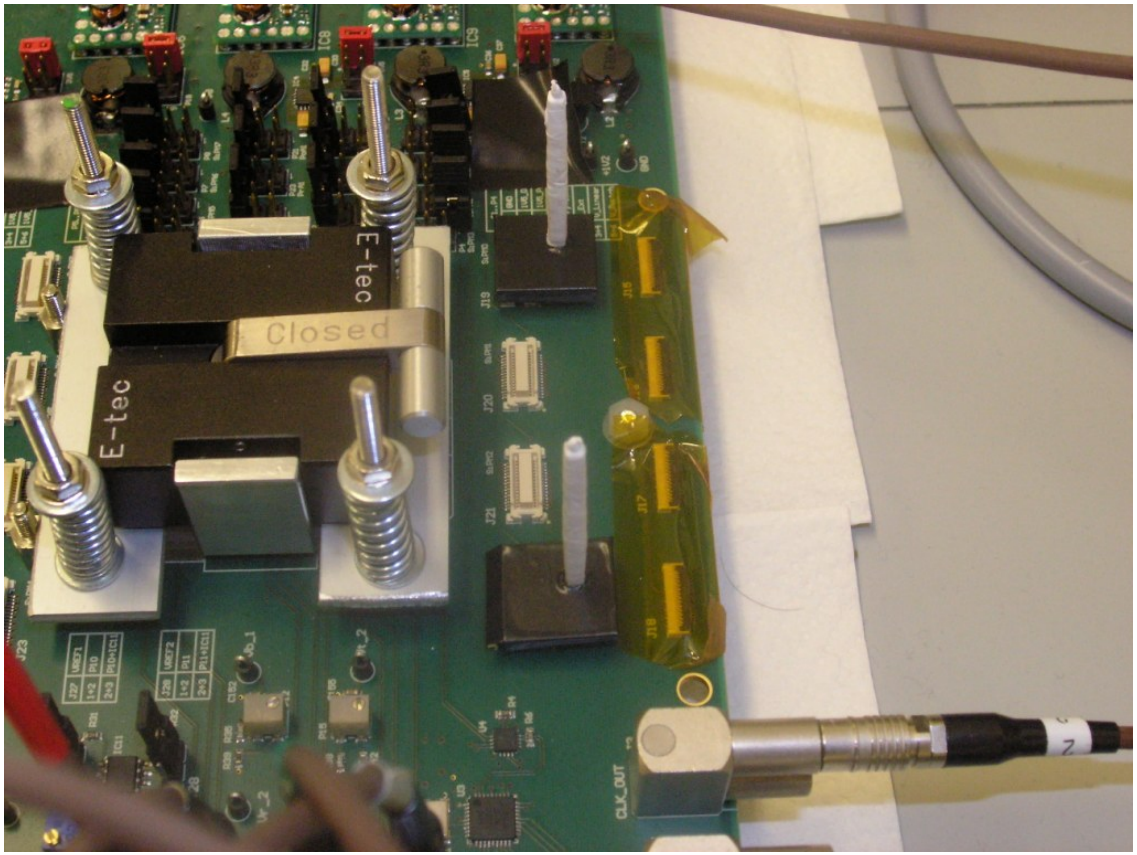
Outline

Active Test setups



- **INFN Torino (IT)**: running since CW7
  - bare 64-channel die bonded to the test-board (3 TB assembled so far)
  - suitable for electrical characterization
  - SPTR tests with MPPCs and laser will be enabled

Active Test setups



- **LIP Lisboa PT)**: running since CW7
  - packaged (BGA) 128-channel SiP (1 TB assembled w/ socket, 1 TB tbd w/ BGA soldered directly)
  - suitable for electrical characterization and tests with crystals
  - socket-based TB used for production qualification

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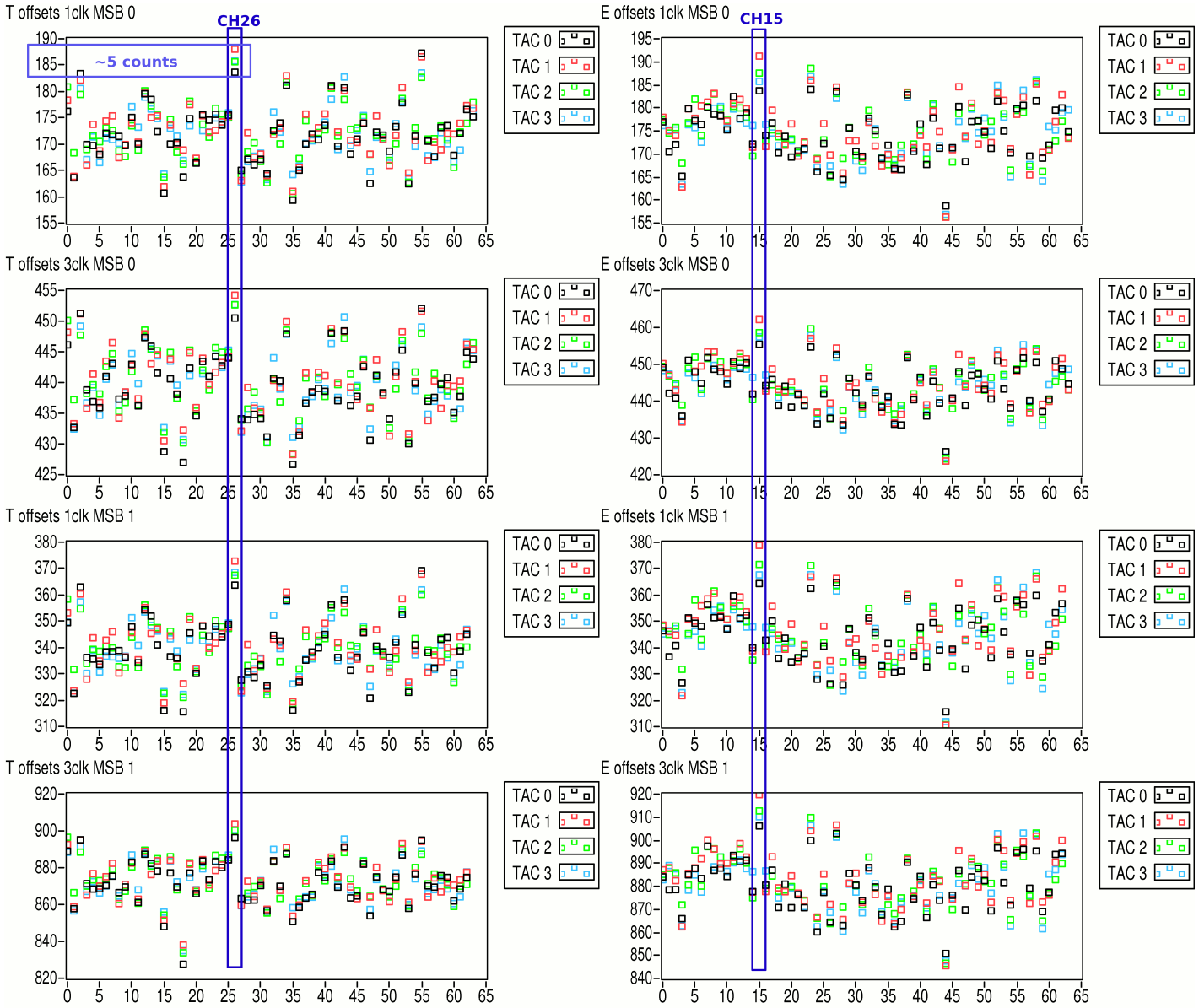
Helpful hints

- Both testbenches are based on a Xilinx ML605 DKIT
- Two data output modes are available: Compact (slot of 5 bytes) and Full (2 slots)
- Full event data mode is used so far, raw data: no arithmetic or gray-to-binary conversion
- Raw data format:
  - **TAC ID** (2-bit, id of TDC buffer used for TAC)
  - **Channel ID** (6-bit)
  - **Tcoarse** (10-bit, coarse time measure of low-Vth rising edge)
  - **Ecoarse** (10-bit, coarse time measure of high-Vth falling edge)
  - **SoC** (10-bit, coarse counter value on (both) TDC fine time operation: start-of-conversion)
  - **Teoc** (10-bit, coarse counter value on T TDC fine time operation: end-of-conversion)
  - **Eeoc** (10-bit, coarse counter value on E TDC fine time operation: end-of-conversion)

TDC calibration for 50 and ps time binnings



Calibration of the TDCs - analysis of results

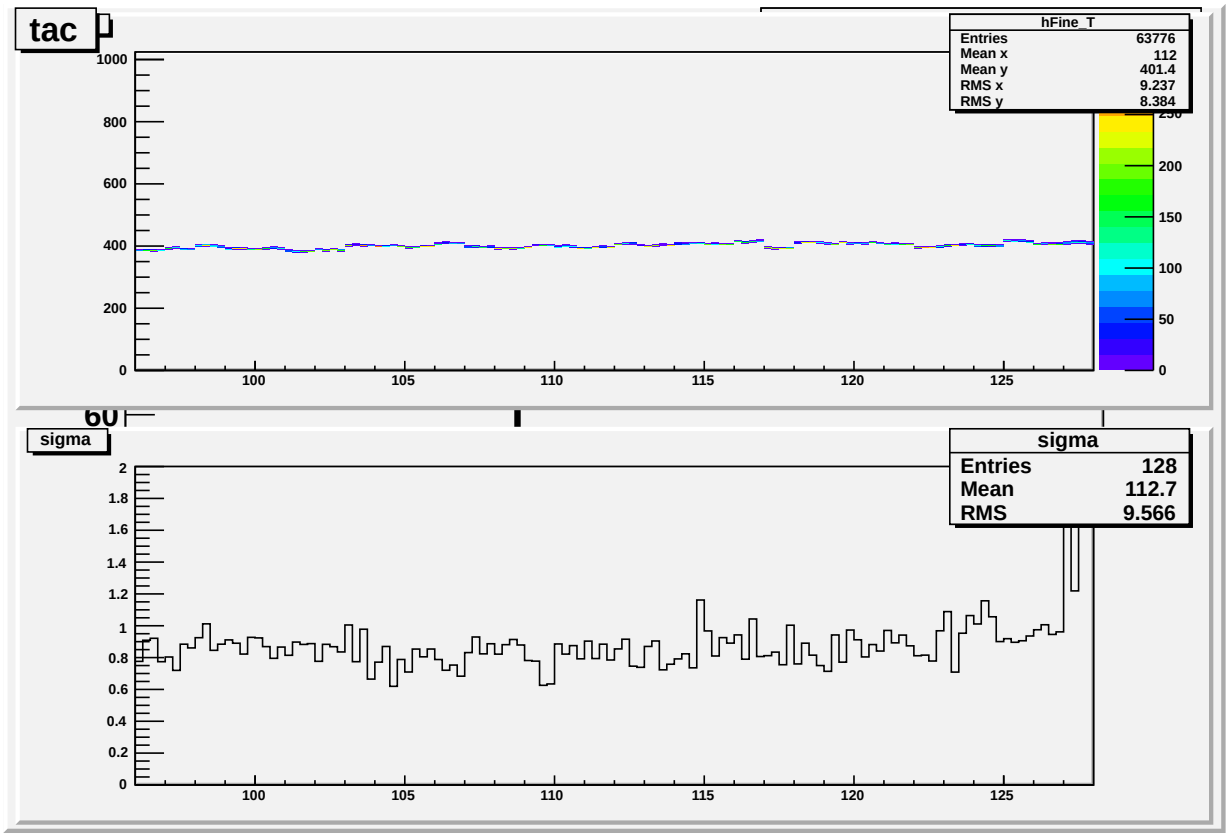
- Mean values of 46 and 24 ps time binnings
- Dispersion of 25 ps binning mode (@160 MHz) seems ok!
- Slope curves (EoC vs. ibias, not plotted) show that calibration dynamic range (fine tunning of the binning) is sufficient
- p-t-p dispersion if TAC_id is not used to reconstruction is up to 5 CLK: need to consider TAC_id
- Strategy:
  - calibrate TDC binning anyway (may be enough for some applications)
  - build offline 256-entry (ch_id, tac_id) look-up table to achieve less than 0.4LSB sigma quantization error

Evaluation of channel resolution

- External test pulse generated by FPGA; allows control of phase and position in frame.
- Pulse generated on clock generated by FPGA PLL has too much jitter
- Clean clock from Si5326 fed back to FPGA and used to generate test pulse
- 32 channels tested: 16 without SiPM, 16 with SiPM
- Test performed both on 128-channel SiP setup and 64-channel bare die
- SiPM capacitance (HV biased) does not impact channel time resolution

Evaluation of channel resolution II

- Low Vth_T (baseline not calibrated, around 1 p.e), High Vth_e
- Equivalent result for internal calib pulse and external pulse (injected with a CR soldered to a DESY mezzanine) - Qin approx 100 pC
- Channel time resolution for calibration pulse below 1 LSB sigma



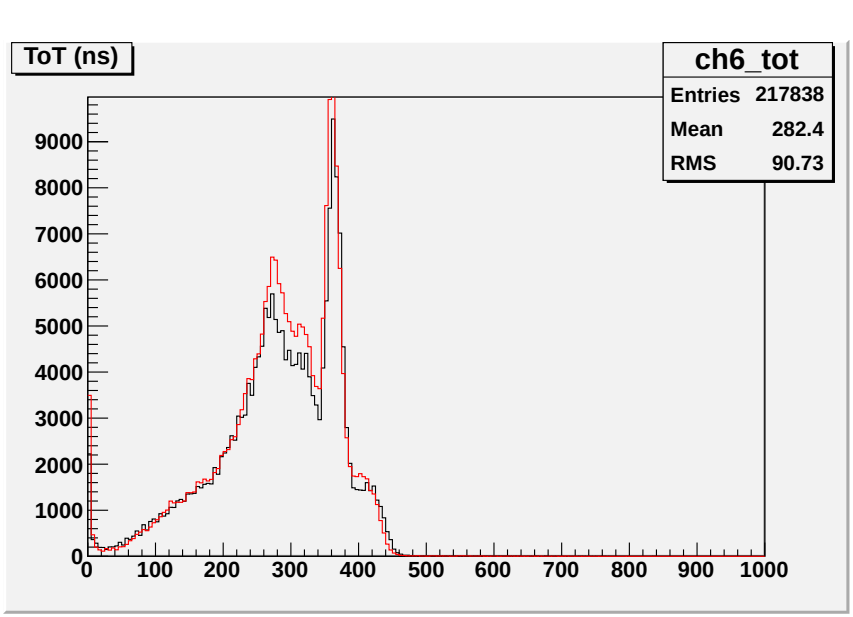
Test setup for coincidence time measurement

- 2x S11828-3344M (4x4 array of 3x3 mm^2 pixels, 50x50 um cells)
- All 32 SiPM pixels are biased.
- Both SiPM arrays are connected to the same ASIC (mechanical constraints)
- 2x LYSO:Ce crystals (2x2x30 mm^3, 4 faces polished)
- ^{22}Na 100 uCi point source

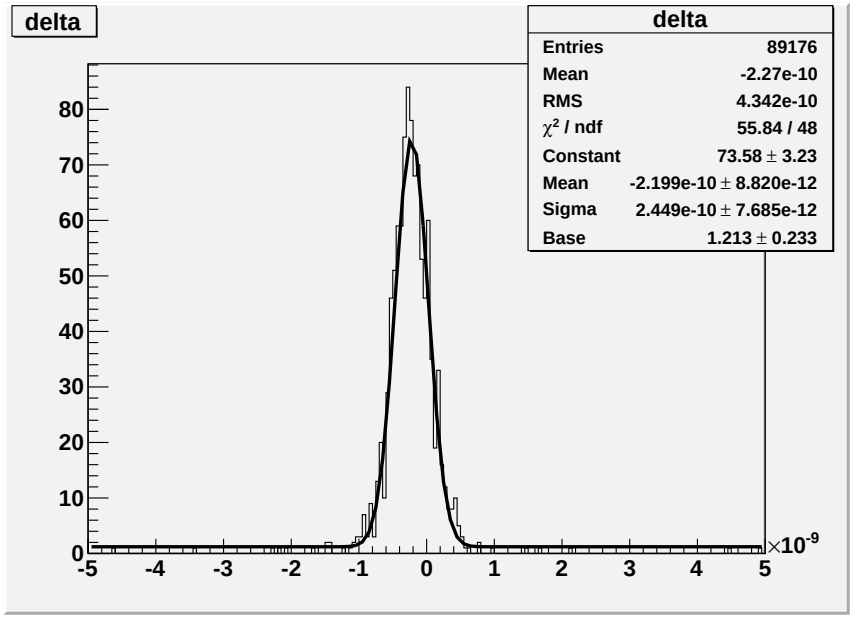
Data acquisition

- Data is taken with the ^{22}Na point source and counter value (tCoarse, tFine, eCoarse, eFine) are recorded for all events
- Using the calibration data, events are processed into an absolute T and ToT value
- ToT value for the 2 channels of interest are plotted
- SiPM bias and vth_T are adjusted to keep the ToT photopeak more or less in the same place for both channels
- From the 2 channels of interest, events from the photopeak are selected and for any pairings, coincidence time difference is plotted into histogram.
- Histogram is fitted to a "gaussian + baseline" function. Baseline accounts for random coincidences.

Sigma of the Day



(a) ToT (ns) (w/o correction)



(b) Coincidence Time (s)

Outline

Summary and Outlook

- Low power (8.7 mW p/channel), low noise readout IC for SiPMs
- 64-channel ASIC tape-out July 2012, internal CERN Engineering Run
- 112 chips p/ wafer, 4 wafers ready
- Compact 17x17 mm 128-channel BGA package
- Characterization started February 2013, test benches at TagusLIP (Lisbon, PT) and INFN (Turin, IT)
- First coincidence measurements with crystals and MPPCs (CW 13,14) show very encouraging preliminary results
- 4x4 crystal matrices (pitch 3.1 mm) compatible with monolithic MPPC arrived from CERN - CW 17

Thank you!

References

[Stevens89] Andrew E. Stevens, Richard P. Van Berg, Jan Van Der Spiegel and Hugh H. Williams
A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors
IEEE JSSC vol 24, no 6, 1989

[Rivetti09] A. Rivetti et al.
Experimental Results from a Pixel Front-End for the NA62 Experiment with on Pixel Constant Fraction Discriminator and 100 ps Time to Digital Converter
NSS MIC Conf. Records 2009

backup slides

Reconstruction of absolute timing

- Time reconstruction of 4 CLK cycles
- Agilent pulse generator triggered by external TP - 25 ps step
- Pulse fed to TDC - Async test-mode: both trigger on rising edge of TP

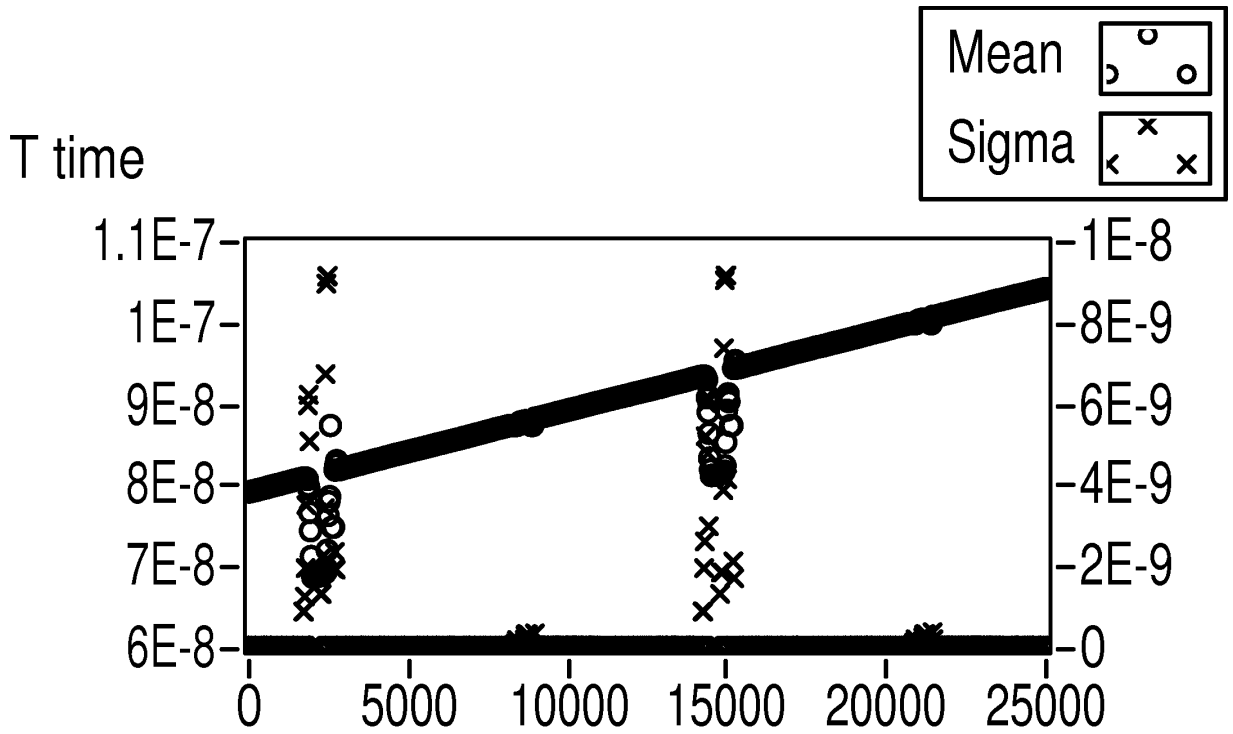


Figure: Y: reconstructed time (s) average (left) and sigma (right), X: phase of the test pulse to clk'event (ps)

Clock transition artifact I

- 400 ps window with no/few events selected
- intrinsic prohibited $t_{su} + t_h$ of flip-flops

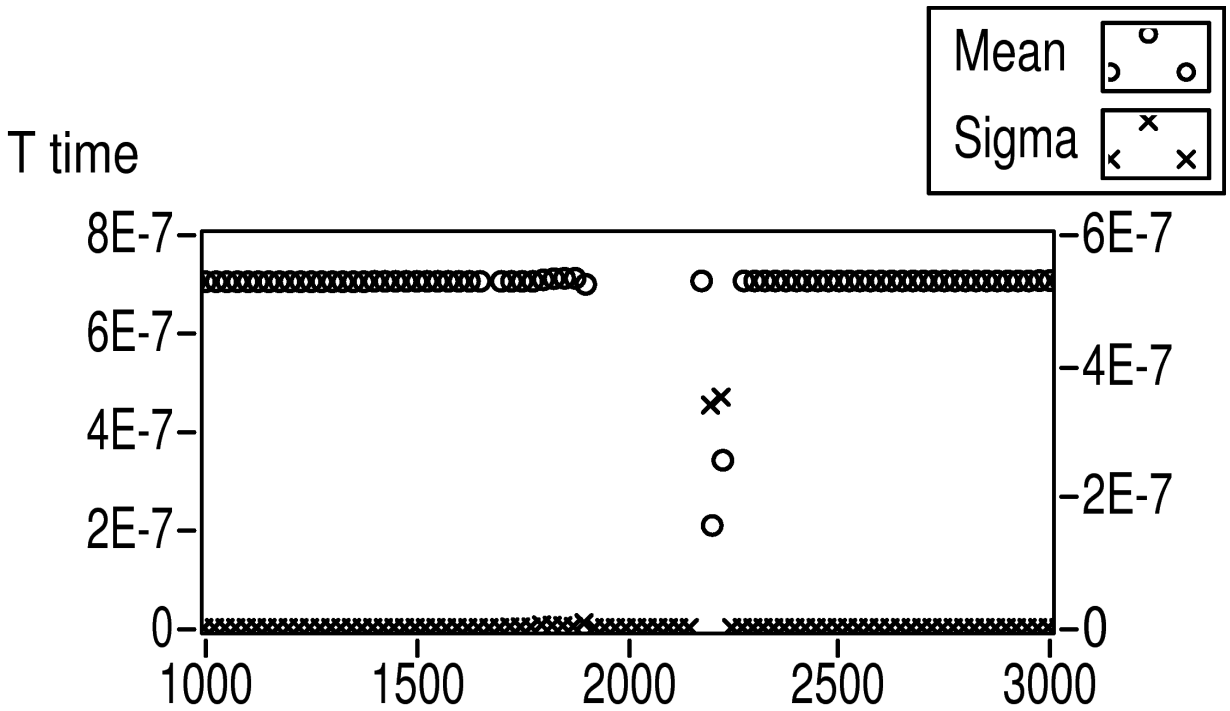


Figure: Y: reconstructed time (s) average (left) and sigma (right), X: TP phase (ps)

Time pick-off method

- **Sampling Techniques**
  - Potentially best time and energy resolution
  - Complex circuitry for such high dynamic range (100 fC - 300 pC)
- **Threshold Techniques**
  - **Constant fraction**
    - Reduces time-walk, potential better time resolution
    - Difficult to implement if signal shape is unknown
    - Difficult to implement for high dynamic ranges
  - **Single threshold**
    - Easiest circuit topology
    - No hit rejection
    - Excessive jitter for ToT measure?
  - **Multiple threshold**
    - Easy circuit topology
    - Low-threshold for good timing
    - High-threshold for dark count rejection and ToT measurement
    - Energy measurement can be used for time-walk correction
    - Low jitter requires very fast and low-noise front-end

Time-to-digital Conversion

Simpler approach: count the cycles of a reference clock of the measurement interval. Need more accuracy? Increase clock frequency. Reasonable? :

- power budget..
- feasibility. Maximum frequency around 5GHz for deep sub-micron CMOS (max 200ps accuracy).

- **Digital-based TDCs**
  The clock is asynchronously subdivided (reference clock interpolation). Multiple phases of CLK are obtained with a chain of delay elements (susceptible to PVT variations) or a DLL.
- **Analogue-based TDCs**
  An analogue integrator perfoms time-to-voltage conversion, which can be then digitized by an ADC. The minimum resolving time Δ_t is dependent on the maximum time to be measured (**DR**) and the number of bits (**N**) of the ADC. $DR = 2^N \cdot \Delta_t$

↪ Analogue interpolation seems to be more suitable for low power, compared to the more power-hungry DLL-based TDCs.

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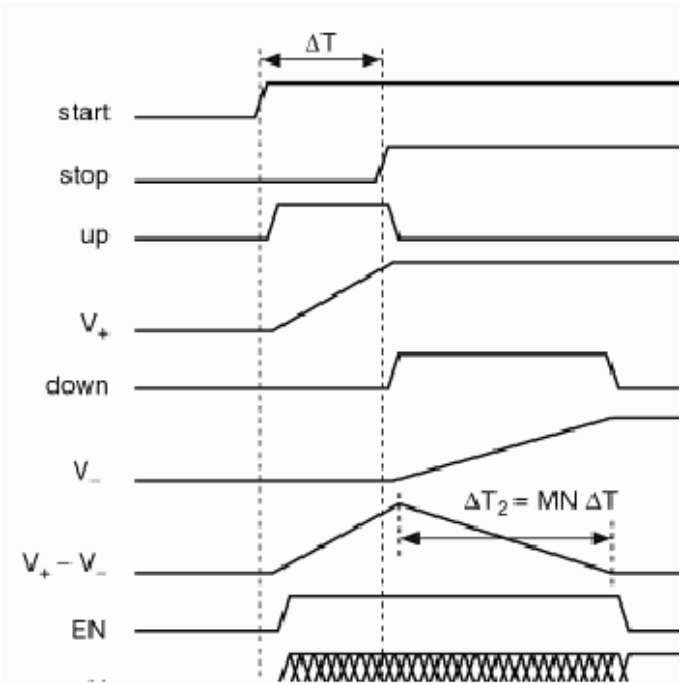
Analogue-based TDC

For short measurement intervals, the analogue integrator can be devised with a current source charging a capacitor during the measurement interval (extensive calibration is needed, non-linearity due to finite Z_{out} of the current source, ..)
Possible way out? A dual-slope analog-to-time interpolation:



from: Stephan Henzler "Time-to-Digital Converters"
Springer series in advanced microelectronics , 2010

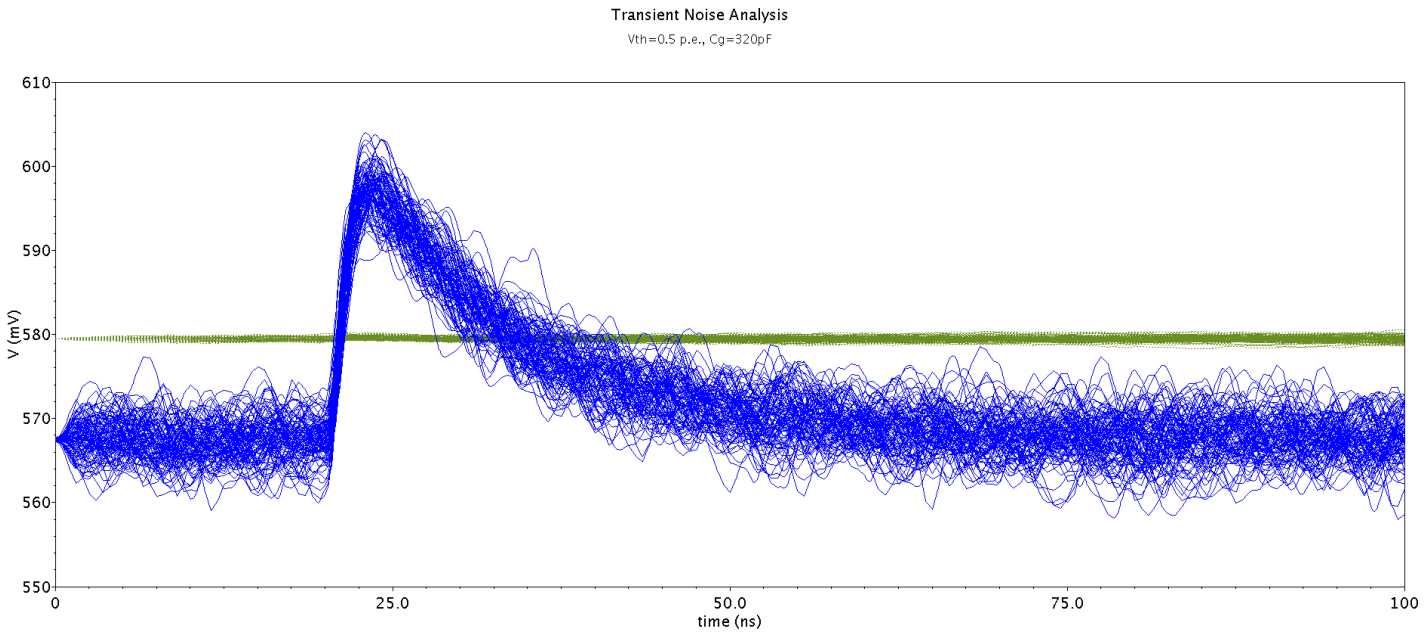
- A ramp is charged by an integration constant τ_k, and discharged with τ_k/n
- DR is multiplied by $n+1$: "time amplification"
- Hence, time resolution can be enhanced just by increasing n
- Digitally-assisted analogue blocks to finely calibrate the time binning

Other features of the TOFPET ASIC:

- Data transmission w/ TX training or CLK_out;
- Synchronous/Async. test for the TDC - internal (GCTRL) or external test pulse;
- Monitoring of front-end discriminator output: time, energy, before/after delay line (jitter assessment);
- Usable for p-type or n-type (hole, electron collection) devices;
- Usable with higher light yield crystals (trimmable coarse gain);
- Zin trimming for line impedance adjustment (independent of SiPM DC bias thanks to closed-loop input stage);
- Channel masking for noisy channels;
- Dark-count rate (DCR) and DC+event overlapping measurements;
- Safe-mode power-on

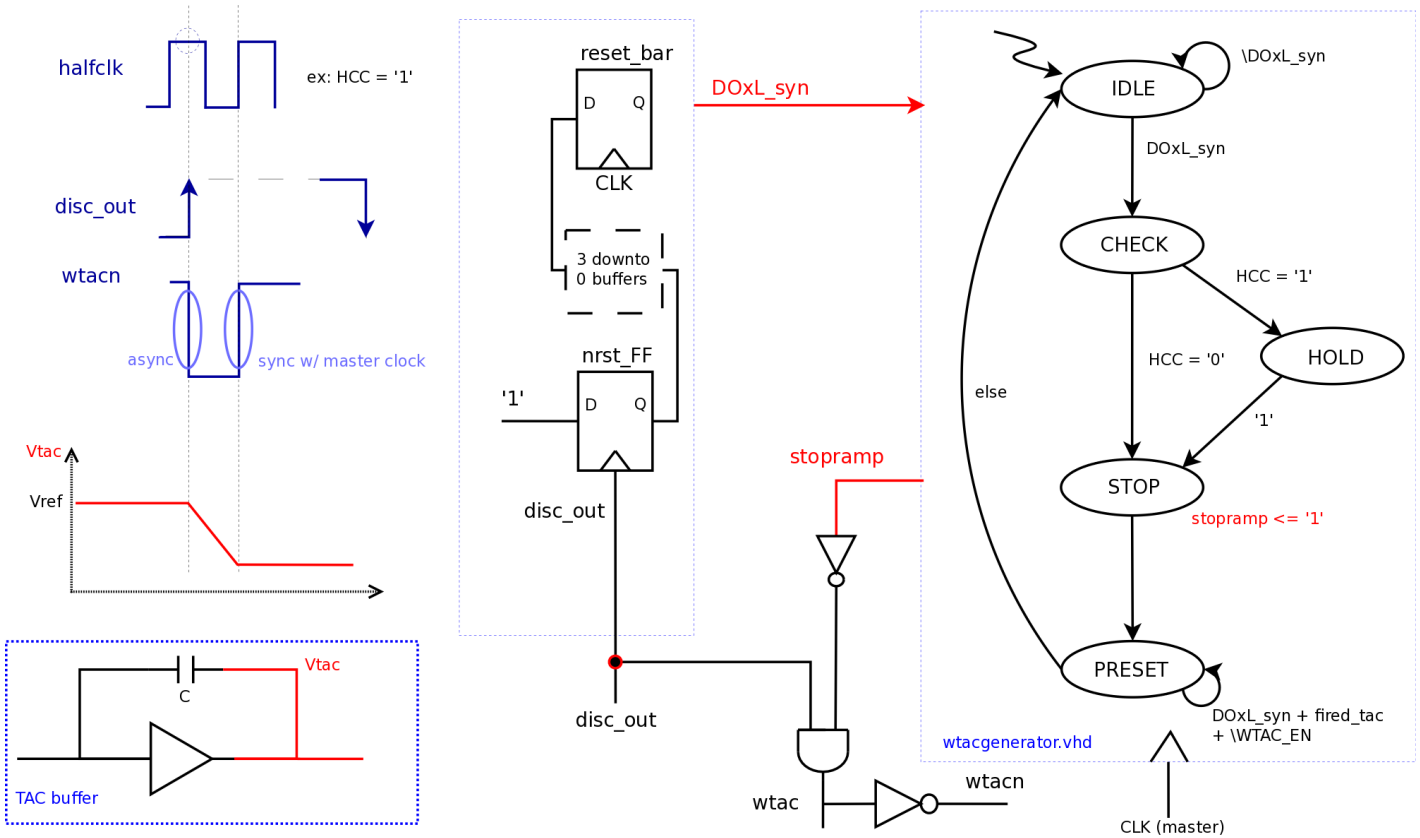
Front-end: single photon count

- Zin trimming for line impedance and BW adjustment is independent of SiPM DC bias thanks to closed-loop input stage
- FE contribution to total jitter is less than 25 ps FWHM
- Trigger level can be set down to 0.5 p.e. with SNR above 23 dB (C_g = 320pF - 9mm^2 MPPC)



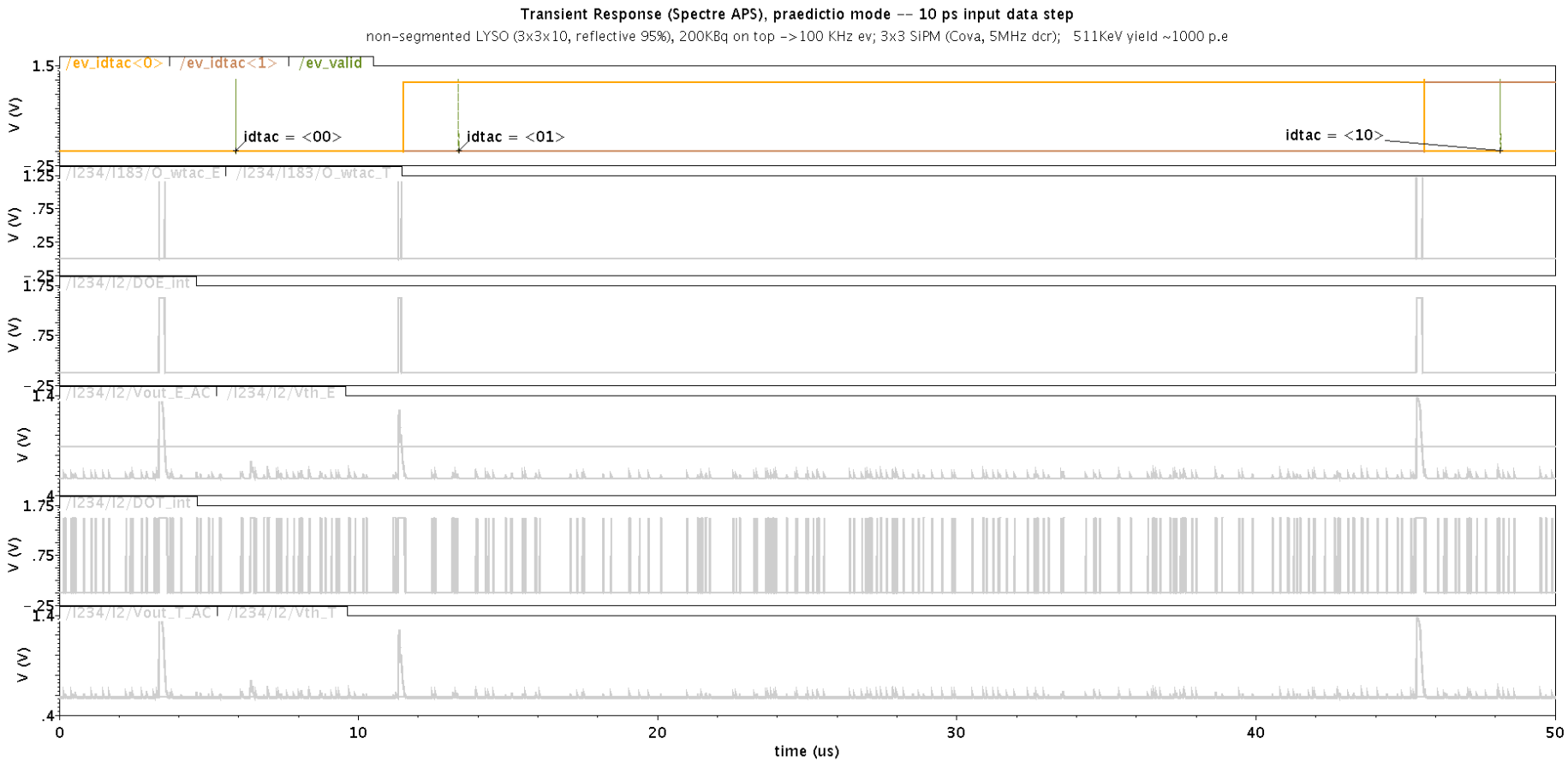
TDC - Time Interpolator

- Phase between trigger and clock edge saved as charge and converted to time domain with a Wilkinson ADC. [Stevens89, Rivetti09]
- 128x time multiplication yields a 50 ps time bin @160 MHz



Geant generated SiPM+LYSO data - TAC ID

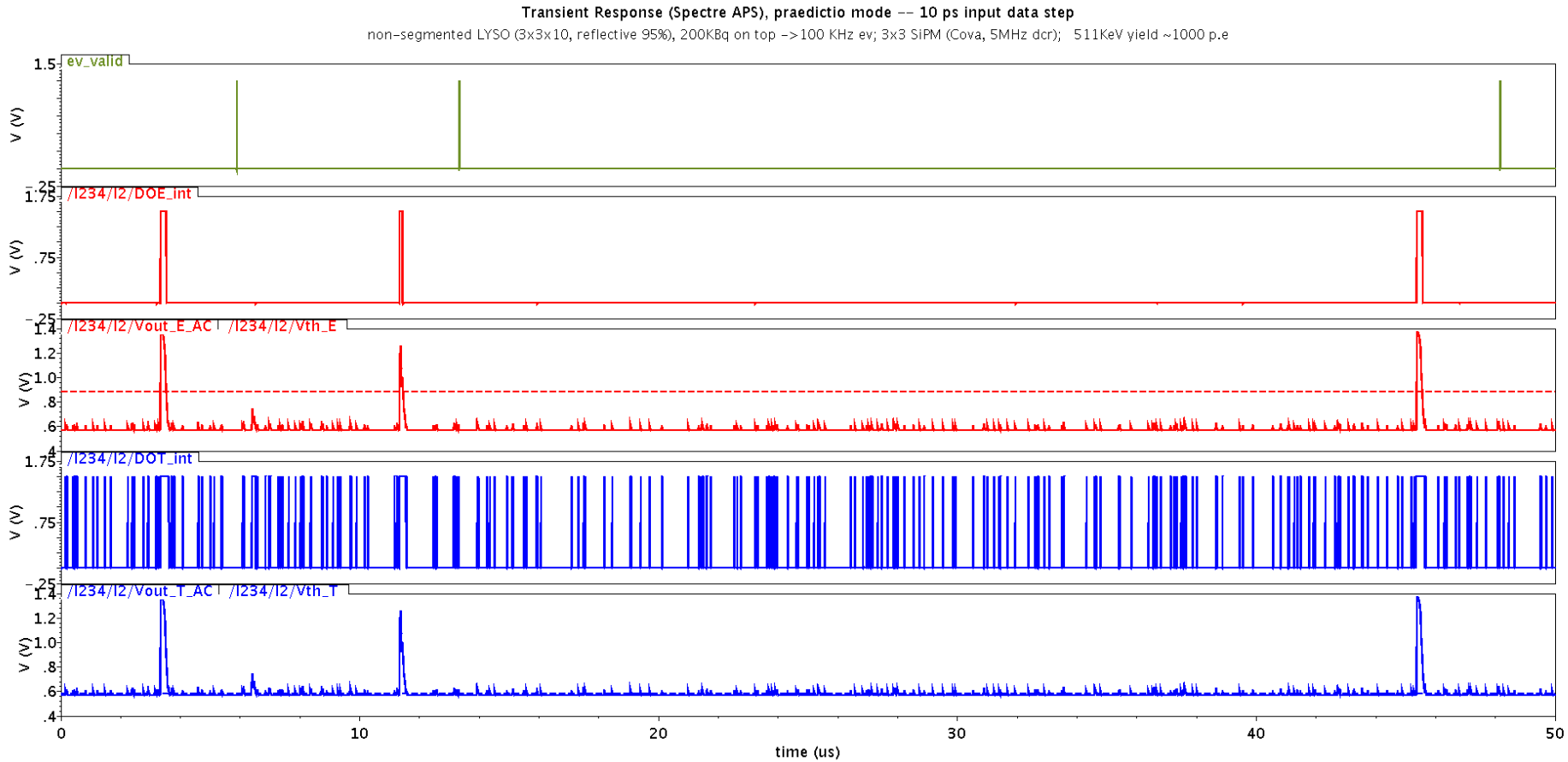
Detail of the channel data register output: id of the TAC written



A low event rate may probably motivate the use of dynamic refresh to the TAC nodes due to the leakage current.

Geant generated SiPM+LYSO data

Simulation of the whole channel (TDC CTRL simulated at transistor level); input is a test vector with data generated from GAMOS/c++ routines [1].



[1] acknowledgment to F. Pennazio, INFN Torino

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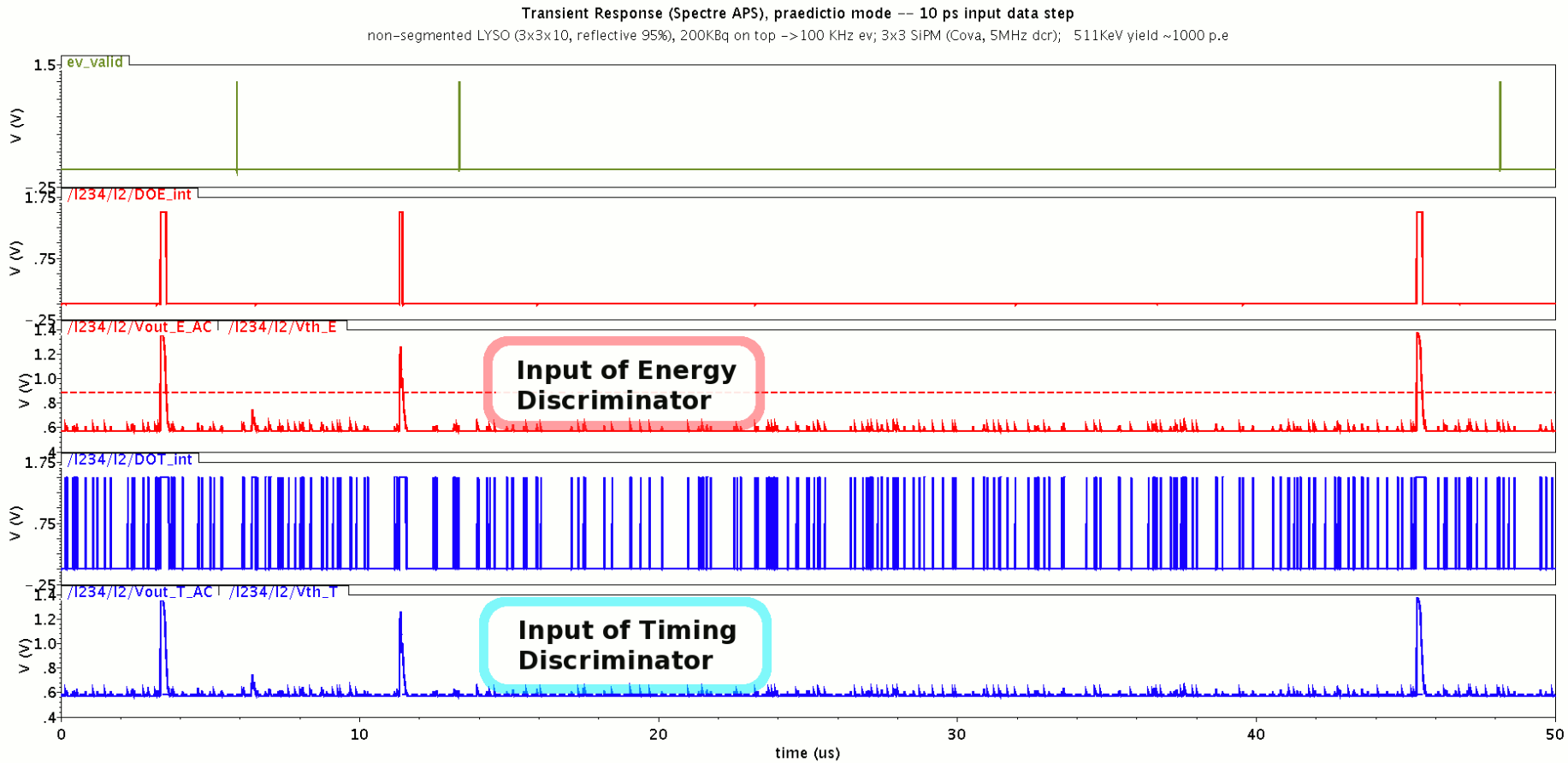

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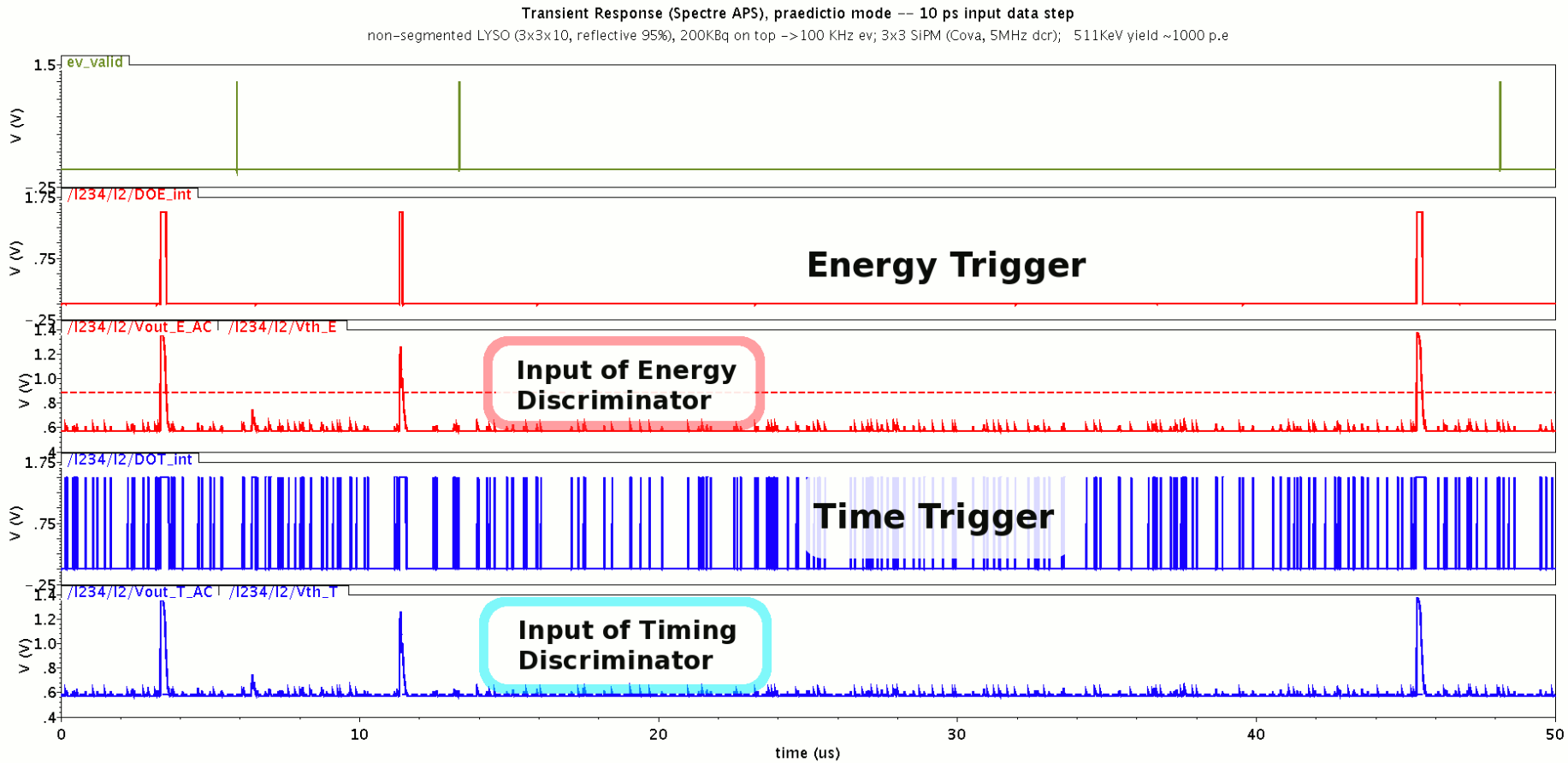

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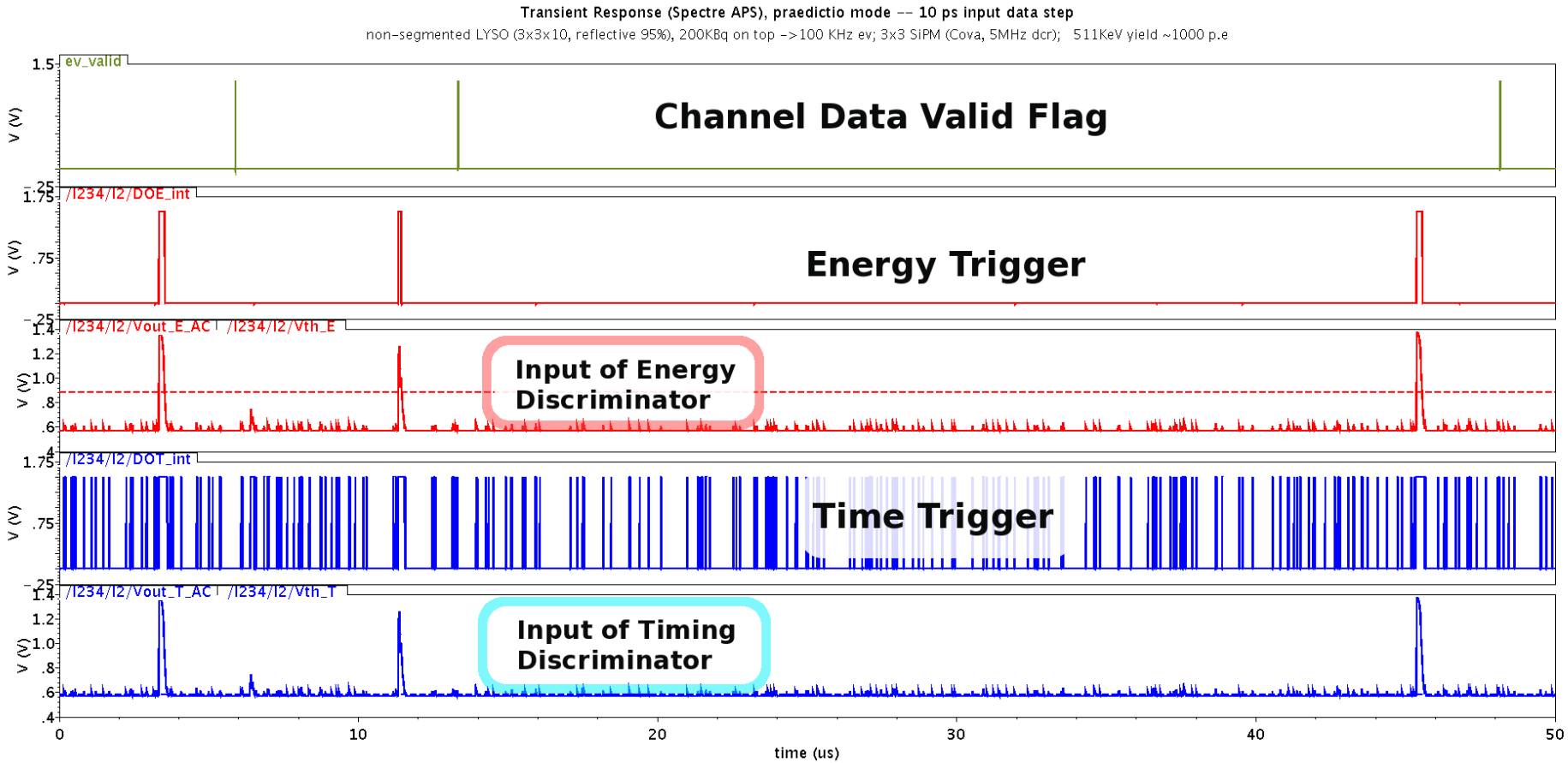

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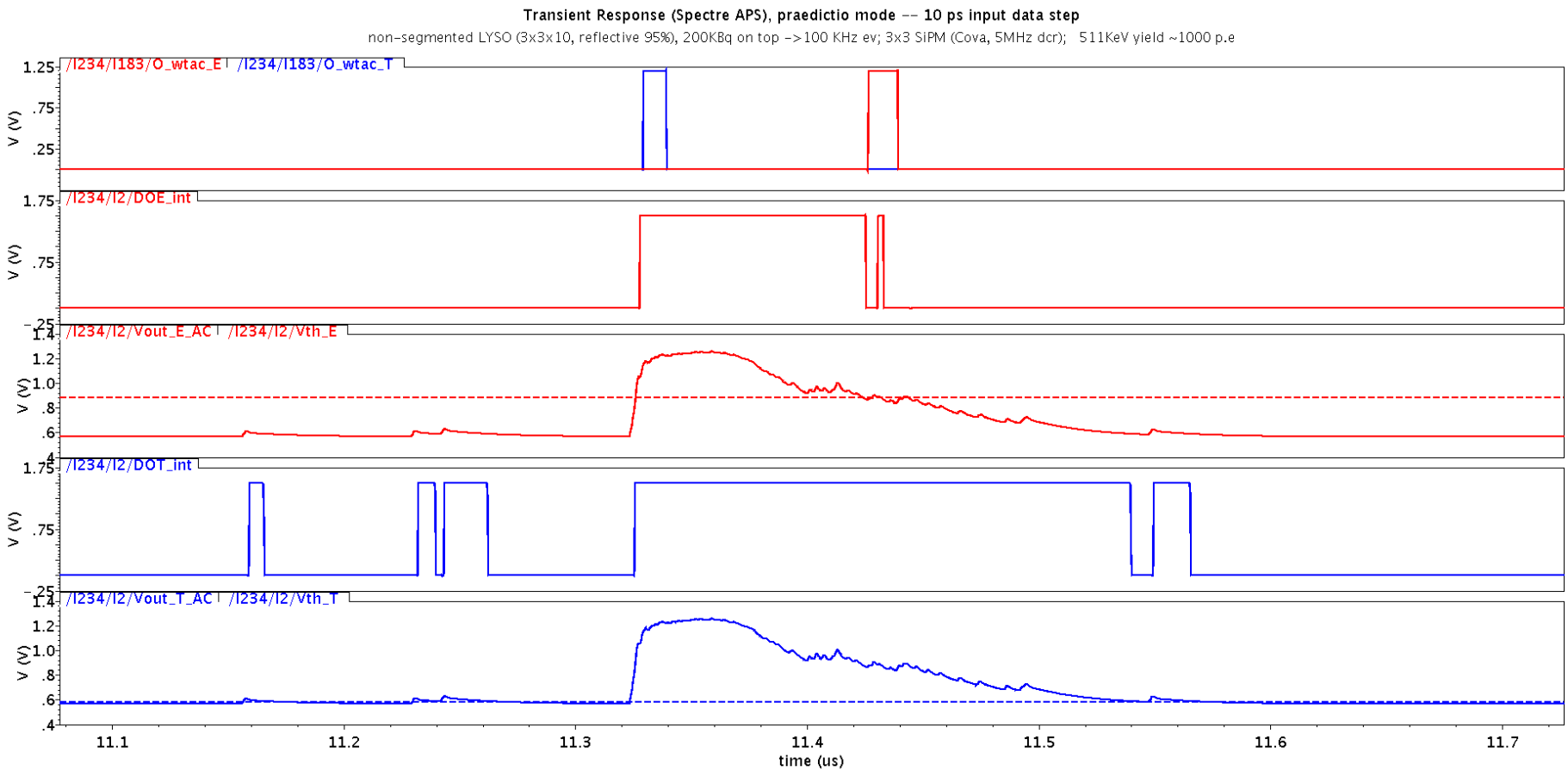
SiPM+LYSO data - detail of event (*praedictio* mode)

Time and Energy thresholds of 0.5 and 7.0 photoelectrons.



Note 1: wtac_T is a write operation after a time trigger - dark pulses masked.
Note 2: Re-trigger of DOE_int due to scintillation statistics and/or spurious pulses is manageable (Vout_E_AC is unfiltered)

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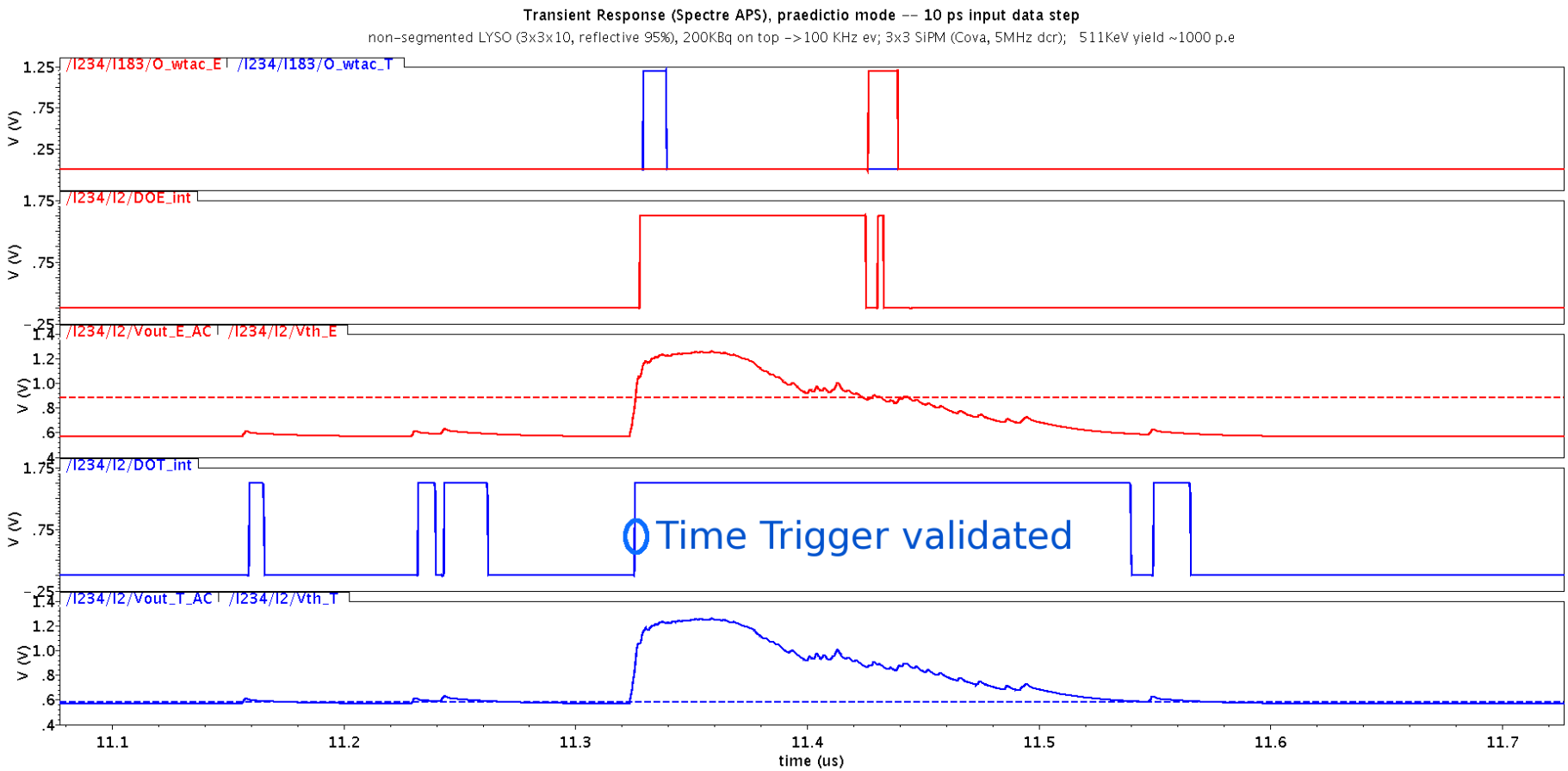

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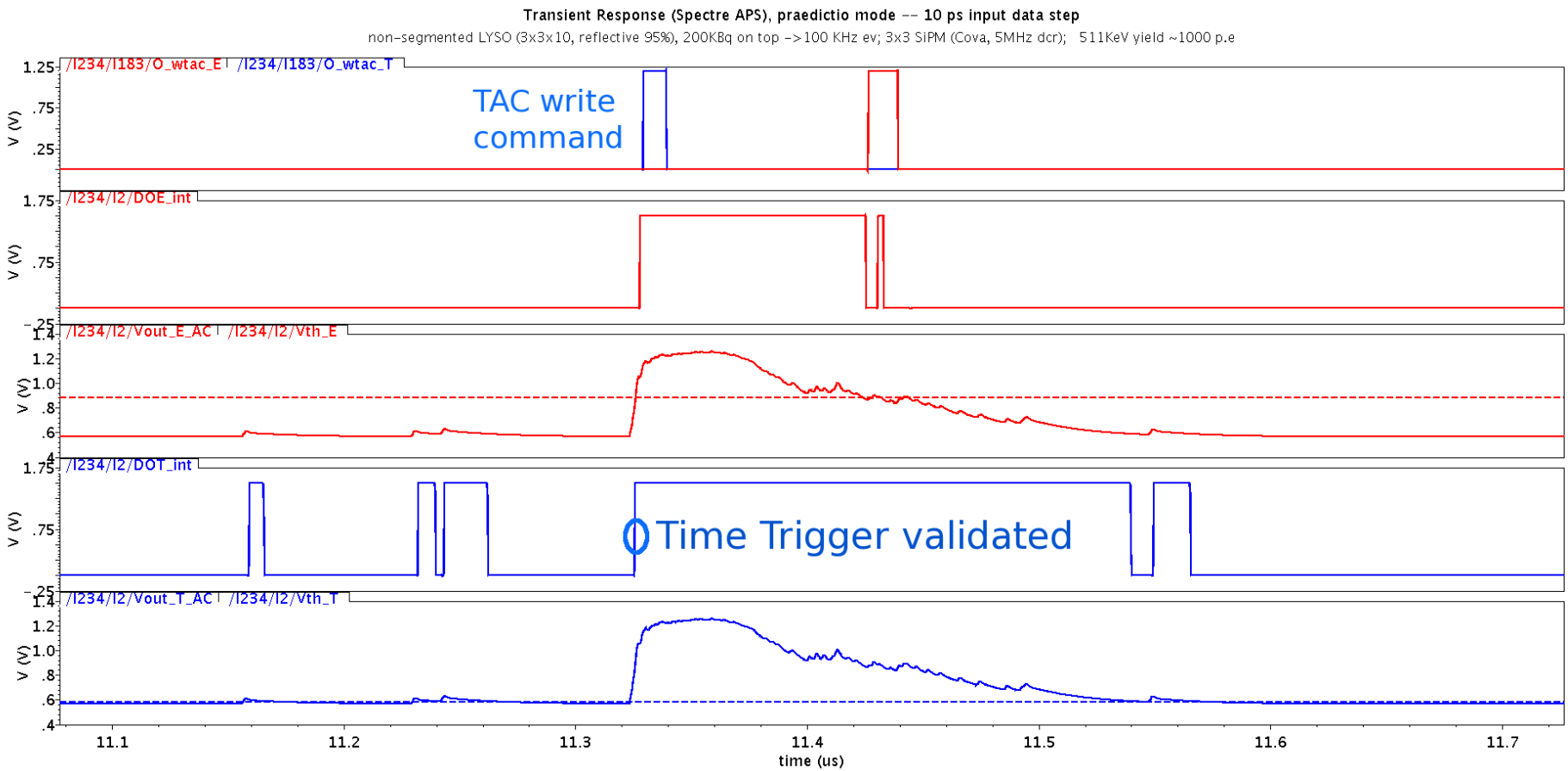

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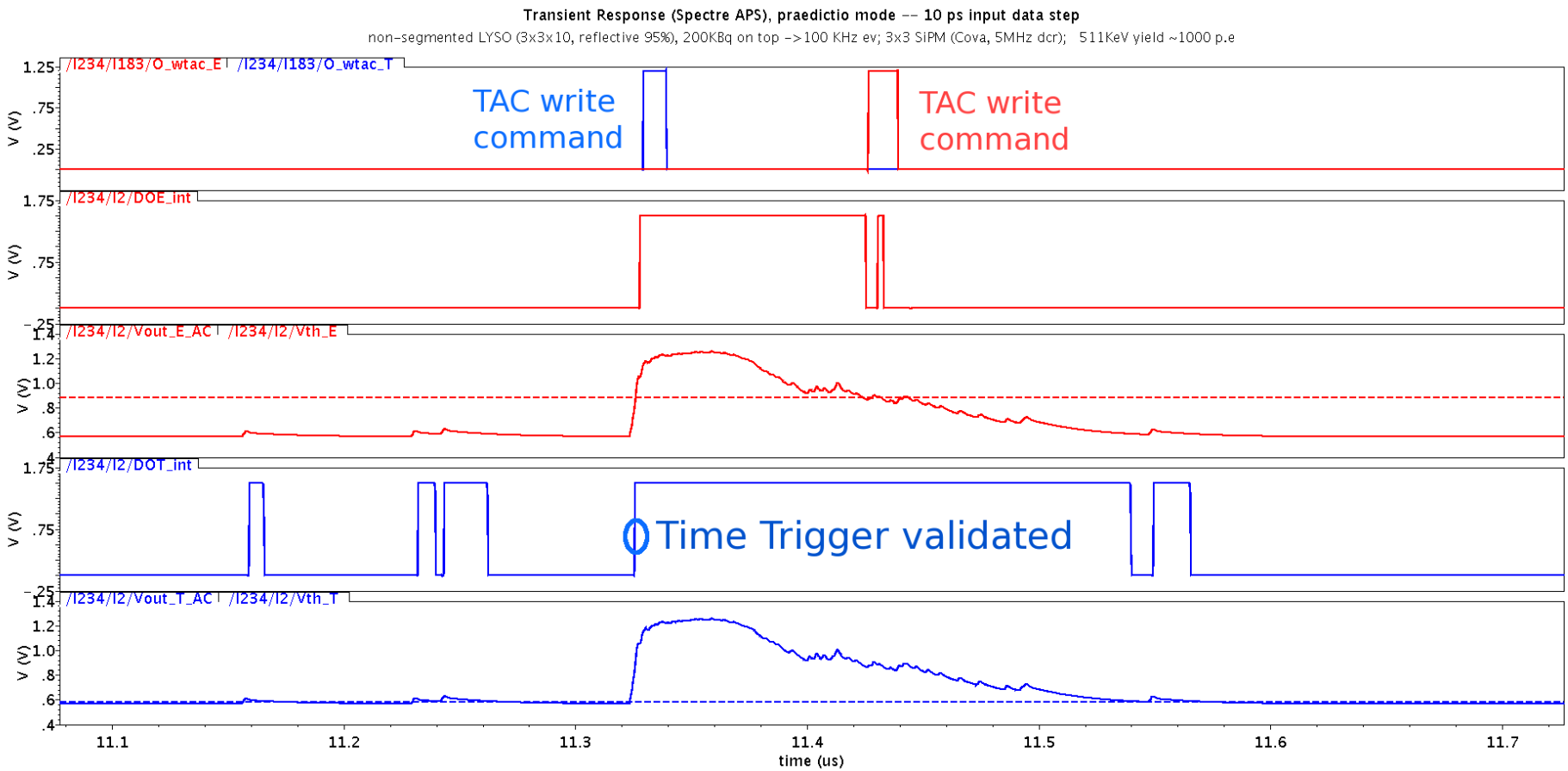

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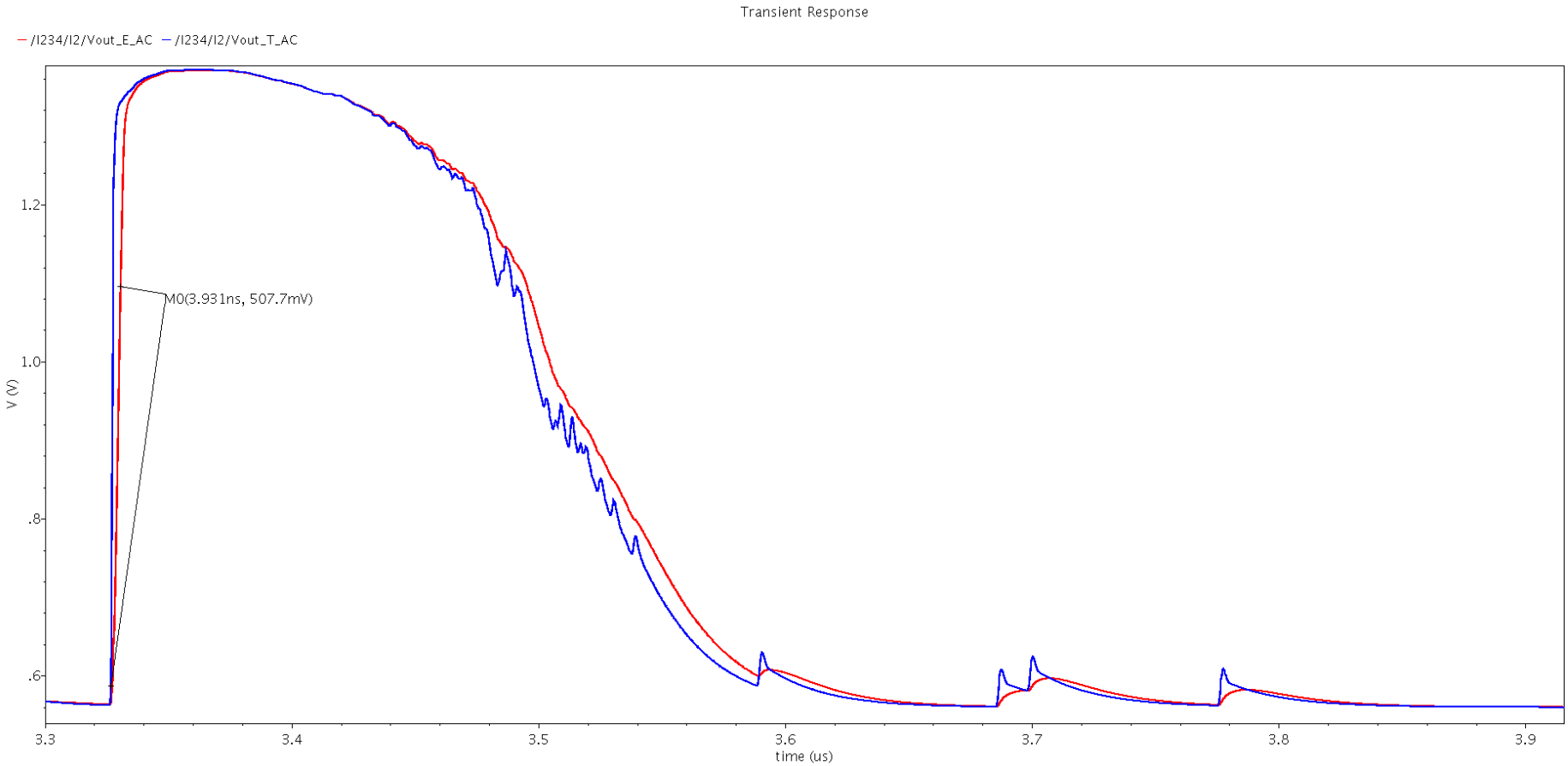
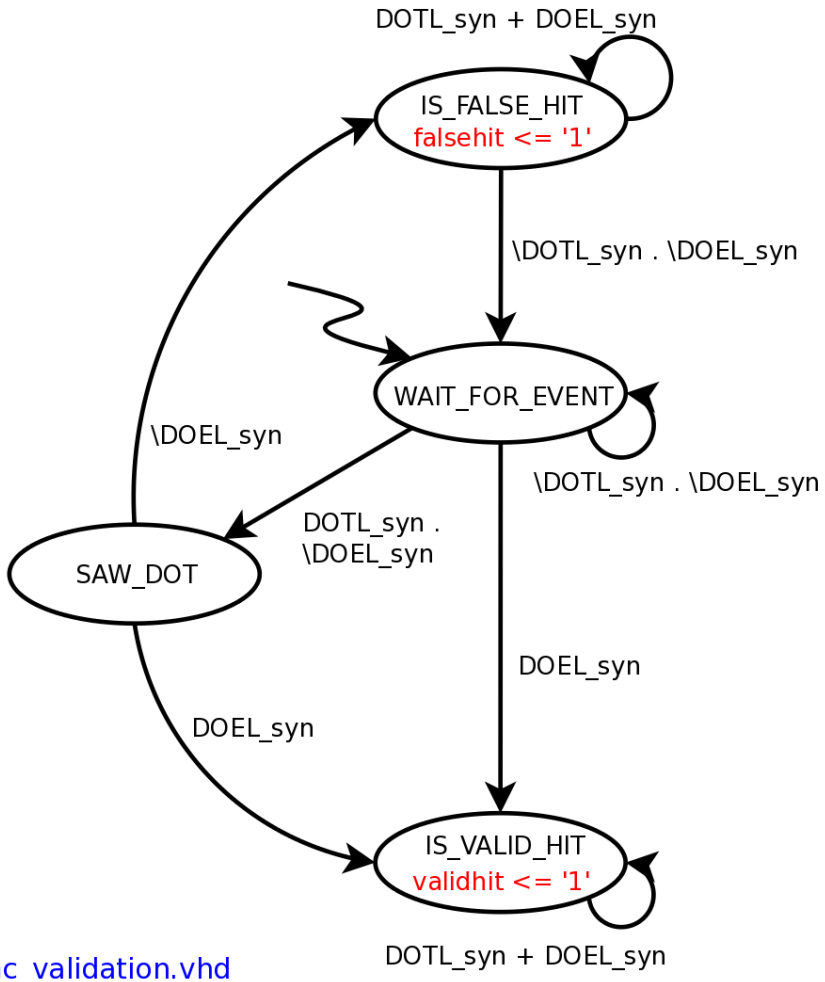
SiPM+LYSO data - detail of event (shaped pulse)

The energy discriminator input Vout_E_AC can be shaped to avoid re-triggering or to guarantee ToT monotonicity:



Since the shaping is applied as RC filtering, the rise time is degraded - the delay of the DOT signal has probably to be widened: likely to increase jitter

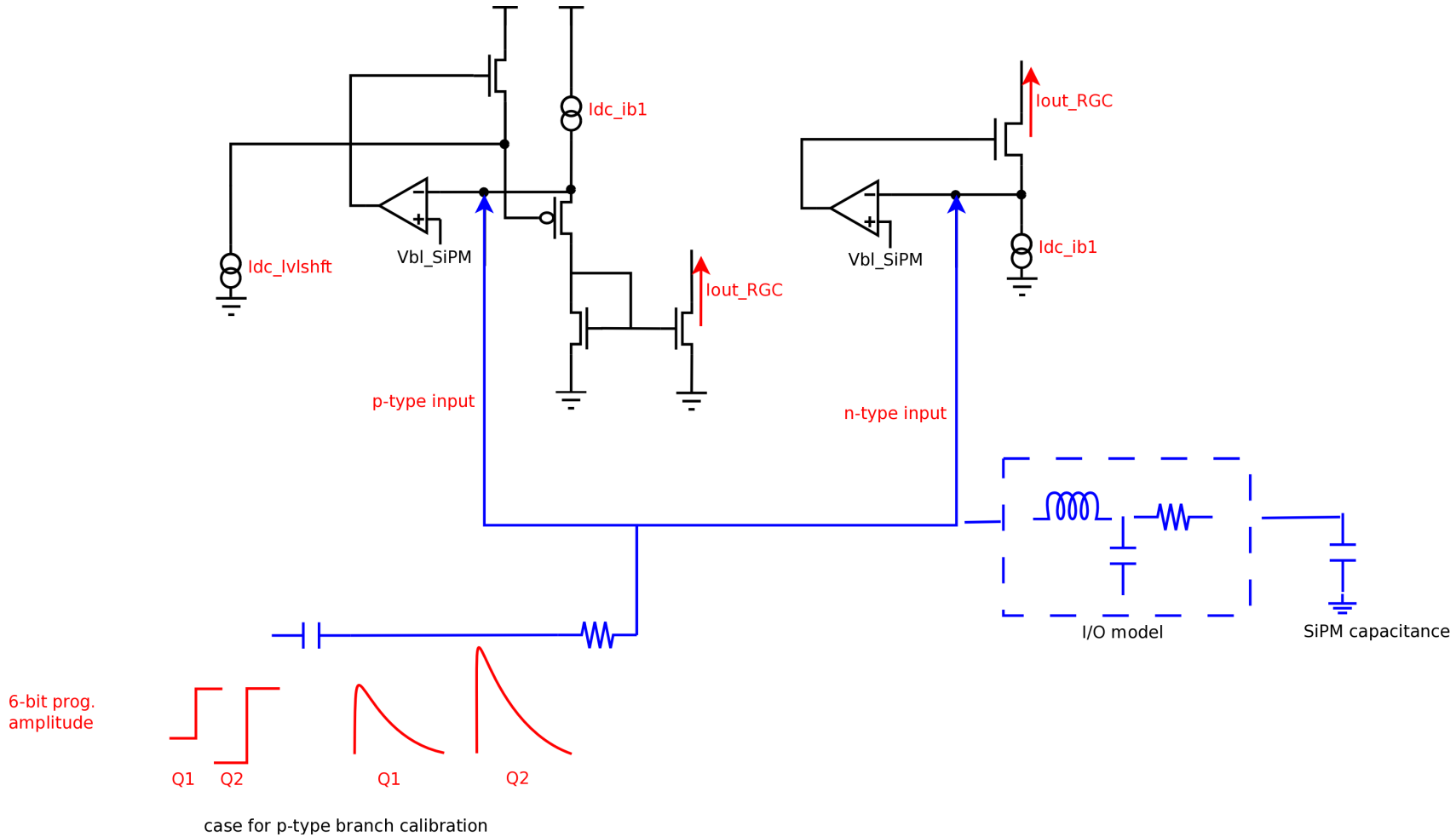
Rejection of dark pulses



sync_validation.vhd

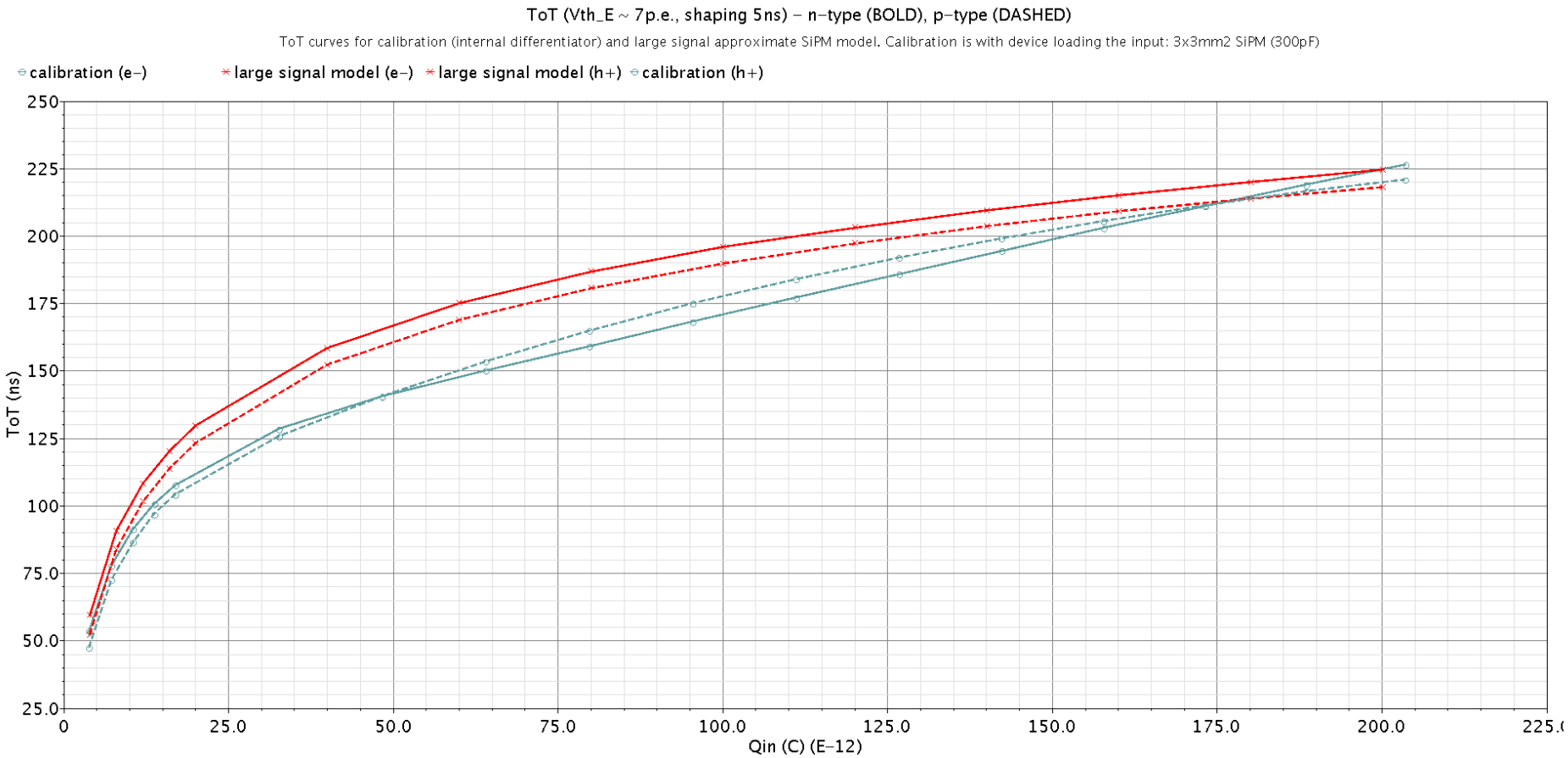
- **SYNC**: The latched and synchronous versions of time (DOTL) and energy (DOEL) triggers are polled every clock (acceptance gate up to 1 clk)
- **ASYNC**: a configurable gate (DOE-DOT) generated by analogue circuitry issues external falsehit and validhit flags - spotting of dc+event overlap
- **PRAEDICTIO**: a delayed version of the DOT is masked unless there is an energy trigger

Calibration mechanism

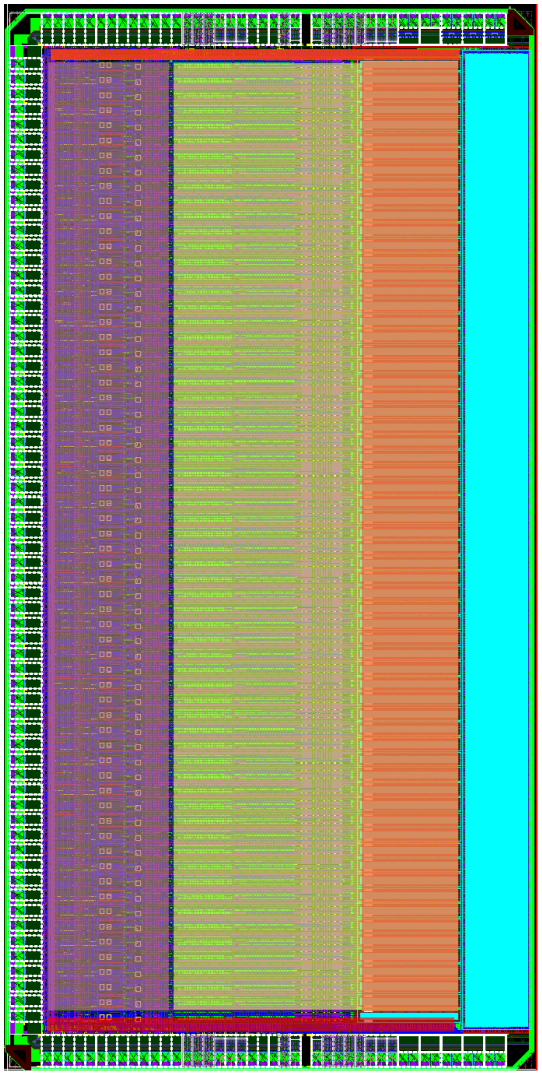


A 6-bit global DAC (current-mode, 20mA conso.) generates a variable amplitude (positive, negative) test pulse, from which an exponential decay is obtained with an RC differentiator.

Time-over-Threshold: internal calibration generator vs. spectre ideal current source



Top floorplan



Front-end

TDC analogue

TDC digital

GCTRL

BIAS cells, golden refs, calibration

- Pre-amplifier, post-amplifier, input Vbl DAC (digital-to-analogue converter), power planes are driven in/out off the chip by dedicated IOs.
- Use of triple-well on sensitive/noisy circuits; Digital block (TDC_CTRL + GCTRL) laid in an island isolated by a 20 μm BFMOAT ring (undoped, highly resistive substrate)
- Two regional pad-rings with independent bias and ESD circuitry.

Bias Reference generators, Safe-mode power-on

Internal biasing is configurable by SPI.

- External bias: VREF for TDC, 2 golden reference voltages for internal current/voltage bias generators;
- Each Bias cell is configurable with a 6-bit DAC;
- GCTRL imposes a default configuration vector (tackles SPI problems, noisy power-on, ...) for a testable chip:
  - SiPM Vbl = 650mV
  - Vth_T = 4 p.e.
  - Vth_E = 7 p.e.
  - n-type input
  - nominal 5k TIA gain
  - 'praedictio' mode active
  - TDC - 1 buffer for synchronization (metastability)
  - 5ns shaping of Vout_E
  - ...