PANDA FEE-DAQ Workshop

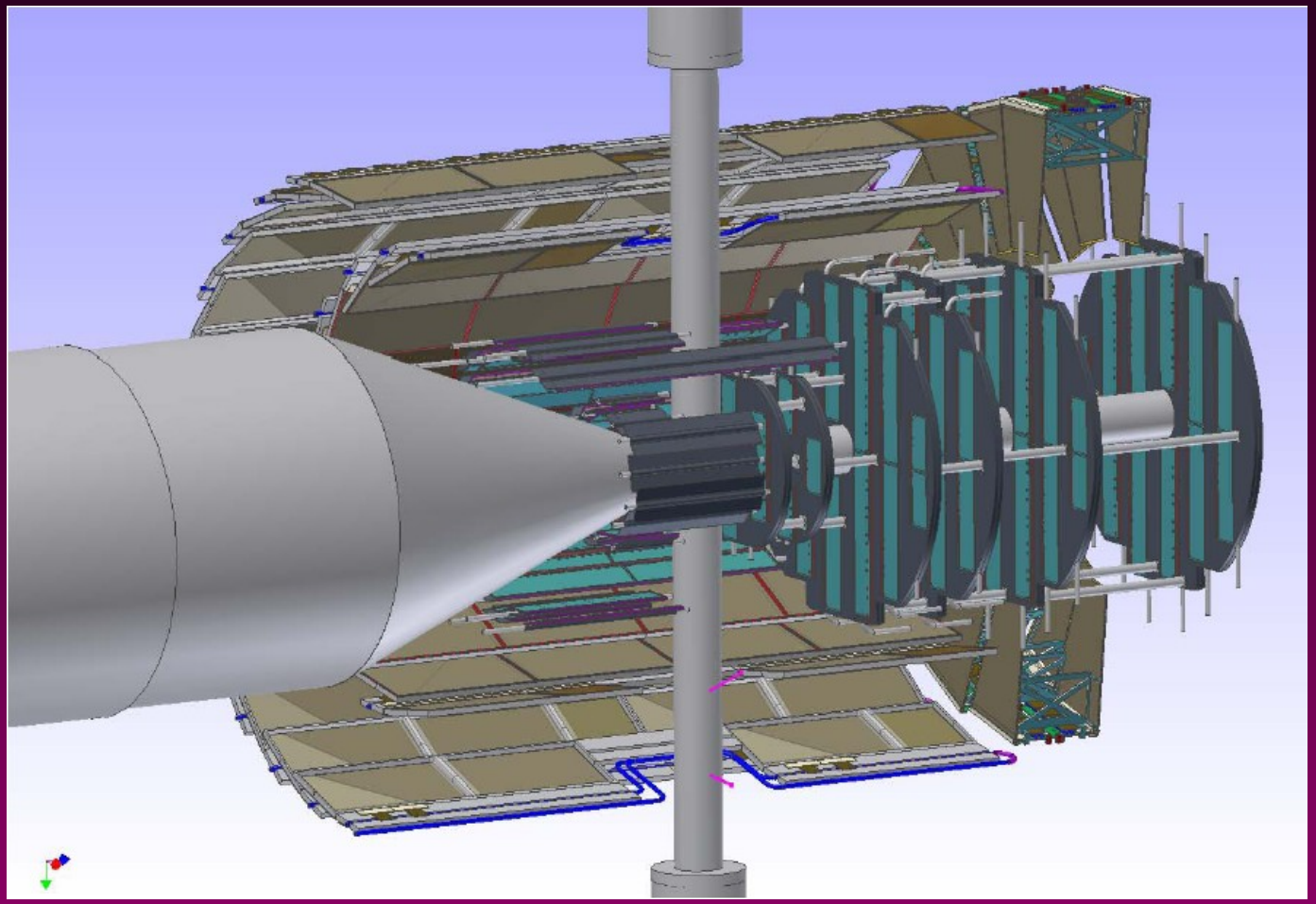
Sezione di Torino

Status report
of the
Silicon Pixel Detector Readout Electronics

G. Mazza
on behalf of the Torino MVD pixel group

PANDA MVD

Sezione di Torino



- Barrel :

  Layer 1 : radius 28 mm, SPDs

  Layer 2 : radius 53 mm, SPDs

  Layer 3 : radius 92 mm, SSDs

  Layer 4 : radius 120 mm, SSDs

- Forward :

  Disks 1-2 : radius 37.5 mm, SPDs

  Disks 3-4 : radius 75 mm, SPDs

  Disks 5-6 : radius 130 mm, SPDs + SSDs

Pixel Detector

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Pixel size	*100 × 100 μm²*
Chip active area	*11.4 × 11.6 mm²* *(116 rows, 110 columns)*
dE/dx measurement	*ToT, 12 bits dynamic range*
Max input charge	*50 fC*
Noise floor	*<32 aC (200 e⁻)*
Input clock frequency	*155.52 MHz*
Time resolution	*6.43 ns (1.86 ns r.m.s.)* *12.86 ns (3.71 ns r.m.s.)*
Power consumption	*< 800 mW/cm²*
Max event rate	*6.1 · 10⁶*
Total ionizing dose	*< 100 kGy*

Module readout

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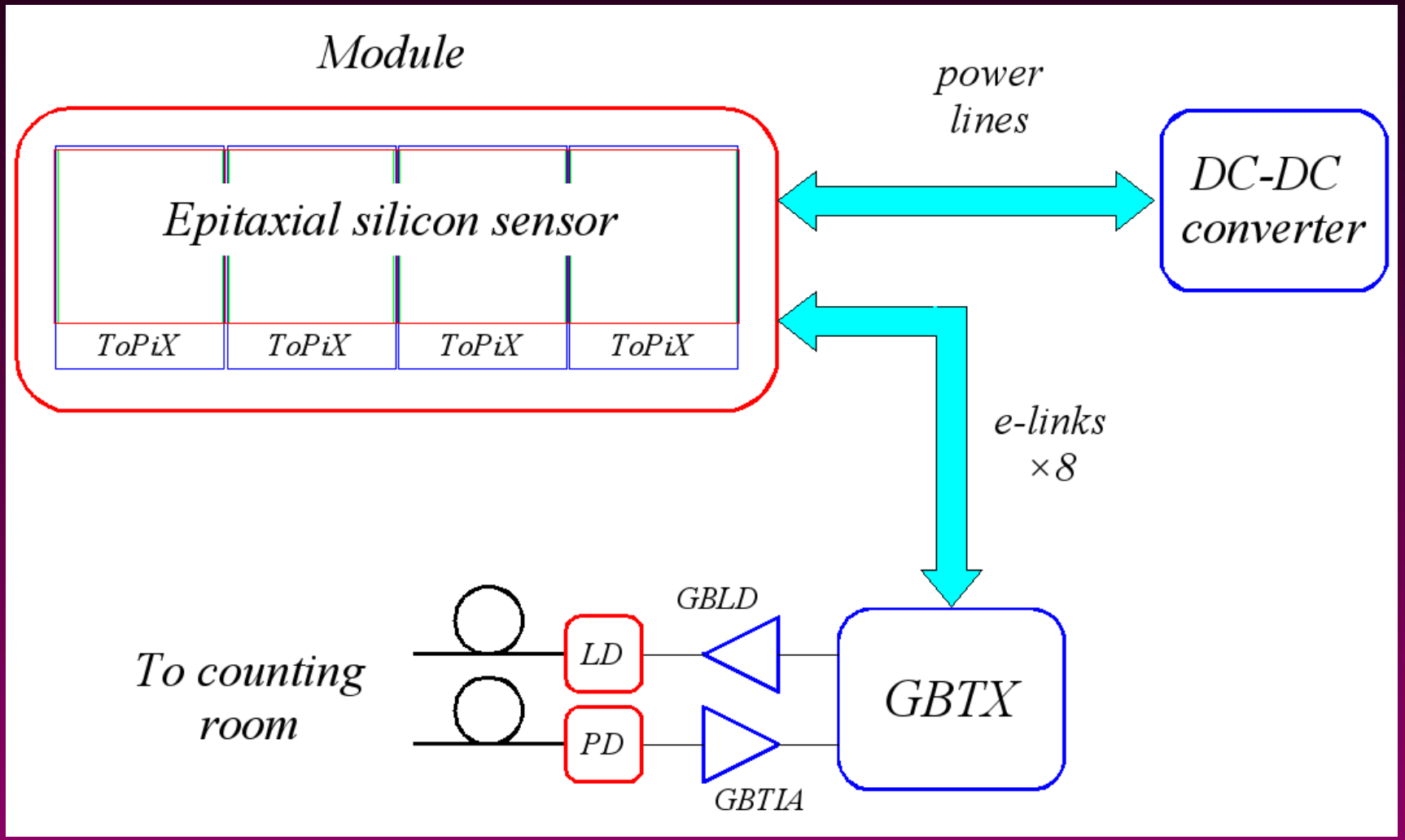

ToPiX v3

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- Layout submitted on February 7th – received May 16th 2011
- 4.5x4 mm^2 die area
- CMOS 0.13 µm DM technology
- Triple redundancy-based SEU protection
- End of column logic
- 160 Mb/s SLVS serial output
- Pads for bump bonding

ToPiX v3 layout

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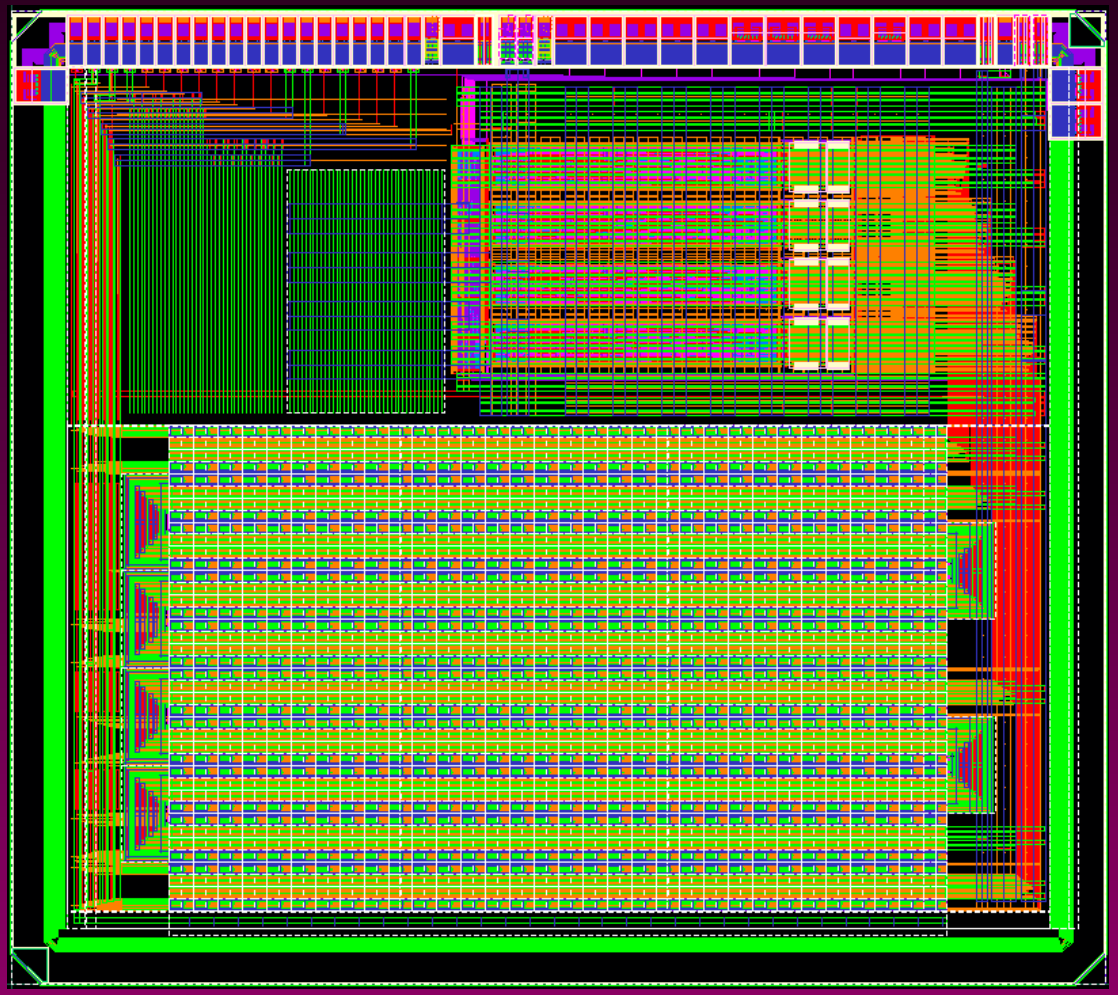

- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

ToPiX test results

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- At 160MHz can only read and program first ~32 pixels of each column
- At 50MHz (with pre-emphasis disabled) full operation
- S-curve working well (programmable internal test pulse)
- Baseline measurements ok
- On-pixel DACs characterised and correction applied
- Transfer function measurements in good agreement with simulations
- Acquisition system is working (4 boards)
- Tested in beam tests at CERN SPS and Julich COSY facilities
- TID (@X ray-CERN) and SEU (@SIRAD-LNL) tests done

Open issues

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- Clock frequency
- Power consumption
- Radiation tolerance
  - TID effects
  - SEU effects

Clock frequency problem

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- At 160 MHz only the columns with 32 double cells work correctly
- Response improves when the frequency is decreased
- Improvements :
  - *Prototype full column has 30% longer bus and 10% more cells than the final chip*
  - *Triple redundancy latches have been connected without buffers*
    - ➔ *but buffers take power !!!*
  - *Change in the leading edge readout timing*
- Bus estimated capacitance : 60.71 fF/dcell (v3), 49.91 fF/dcell (v4 sim. w/o buffers), 26.12 fF/dcell (v4 sim. with buffers)
- Total bus capacitance per line : 8.30 pF (v3), 6.92 pF (v4 sim. w/o buffers), 3.88 pF (v4 sim. with buffers) – *for 128 cells and folded layout*

Timing issue

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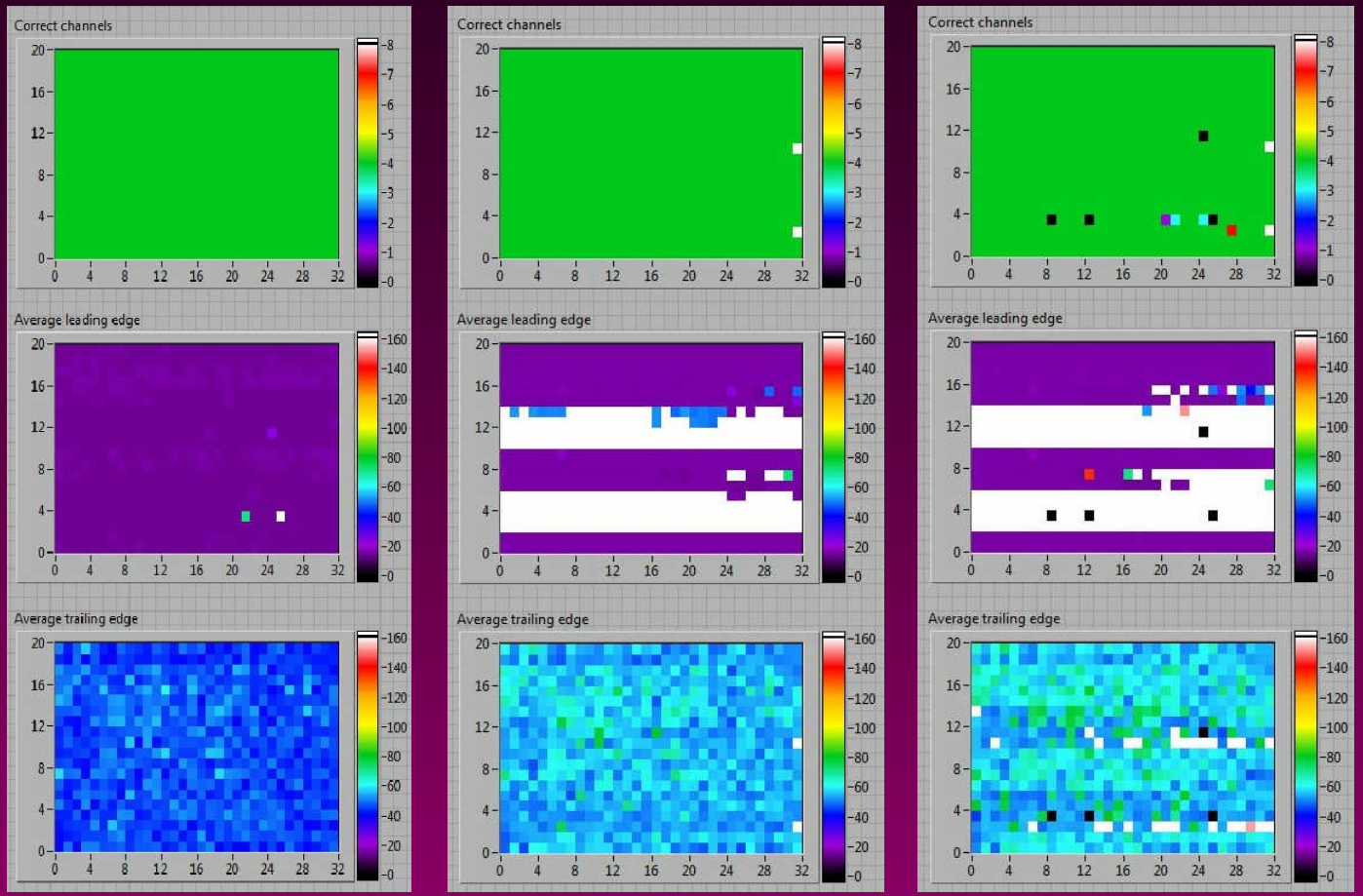
50 MHz *65 MHz* *70 MHz*



- Trailing edge still good @ 65 MHz
- Read leading edge cmd asserted at the same time as read cmd.
- Read trailing edge cmd asserted when read cmd is already high
- *Clock cycle to be inserted between read cmd and read leading edge cmd.*

New line driver

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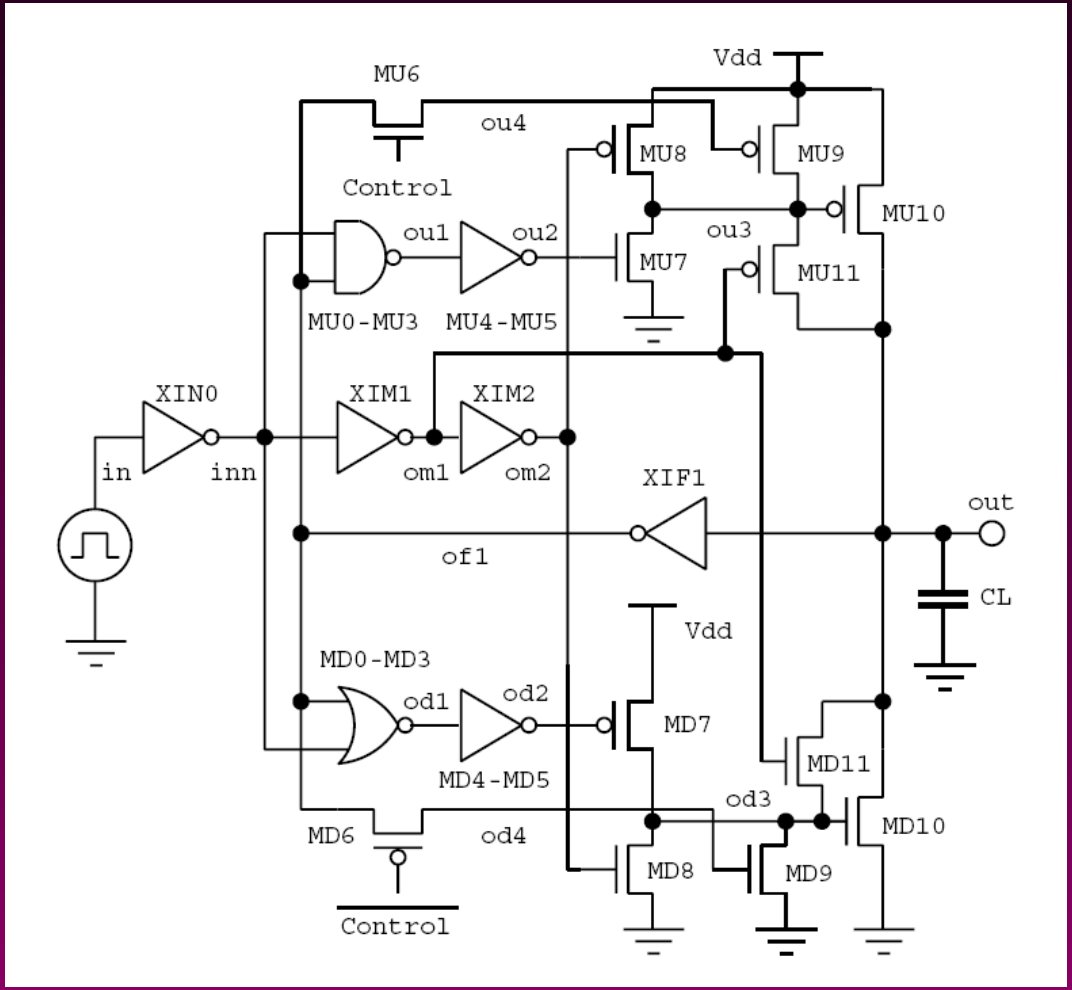

Provides both reduced voltage swing and pre-emphasis or full voltage swing

J.C.Garcia, J.A.Montiel, S.Nooshabadi
Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects
ISCAS 2007

v4 Tx-Rx simulations

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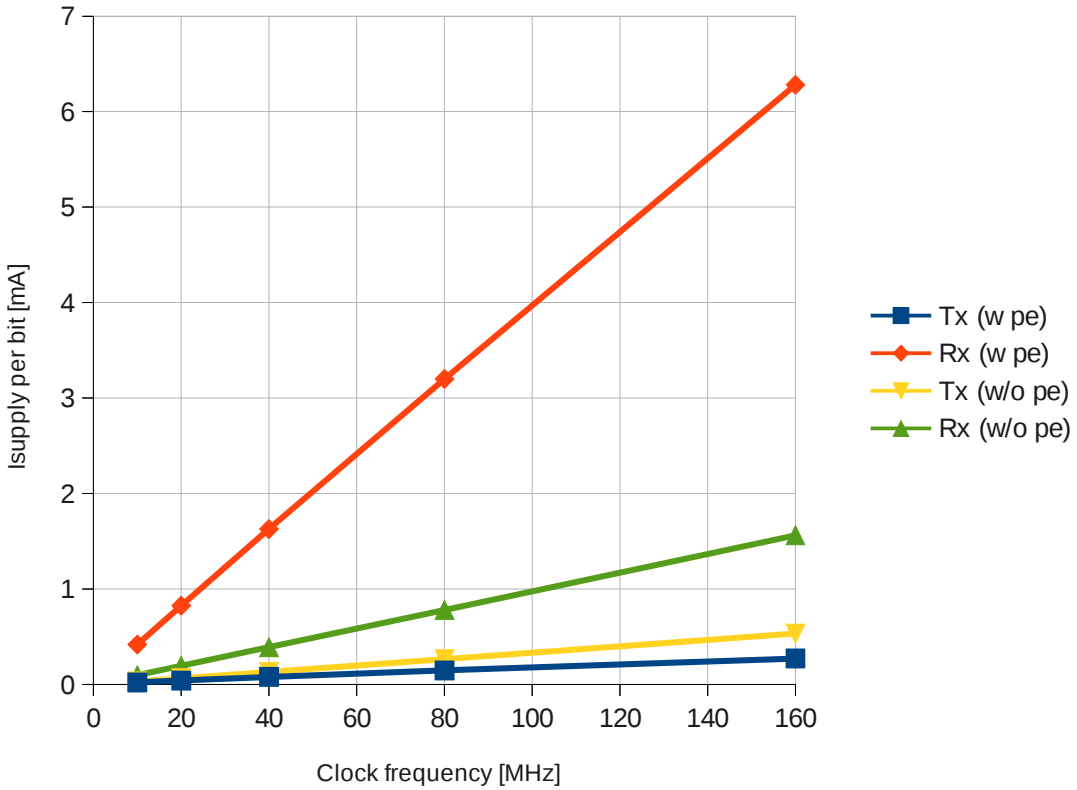

Simulations of the new driver and 128 receivers for different frequencies assuming Gray encoding.

- w pe : with reduced voltage swing and pre-emphasis
- w/o pe : with full voltage swing and without pre-emphasis

On pixel buffers takes the lion's share of the power consumption of the time stamp driver

ToPiX v3 supply

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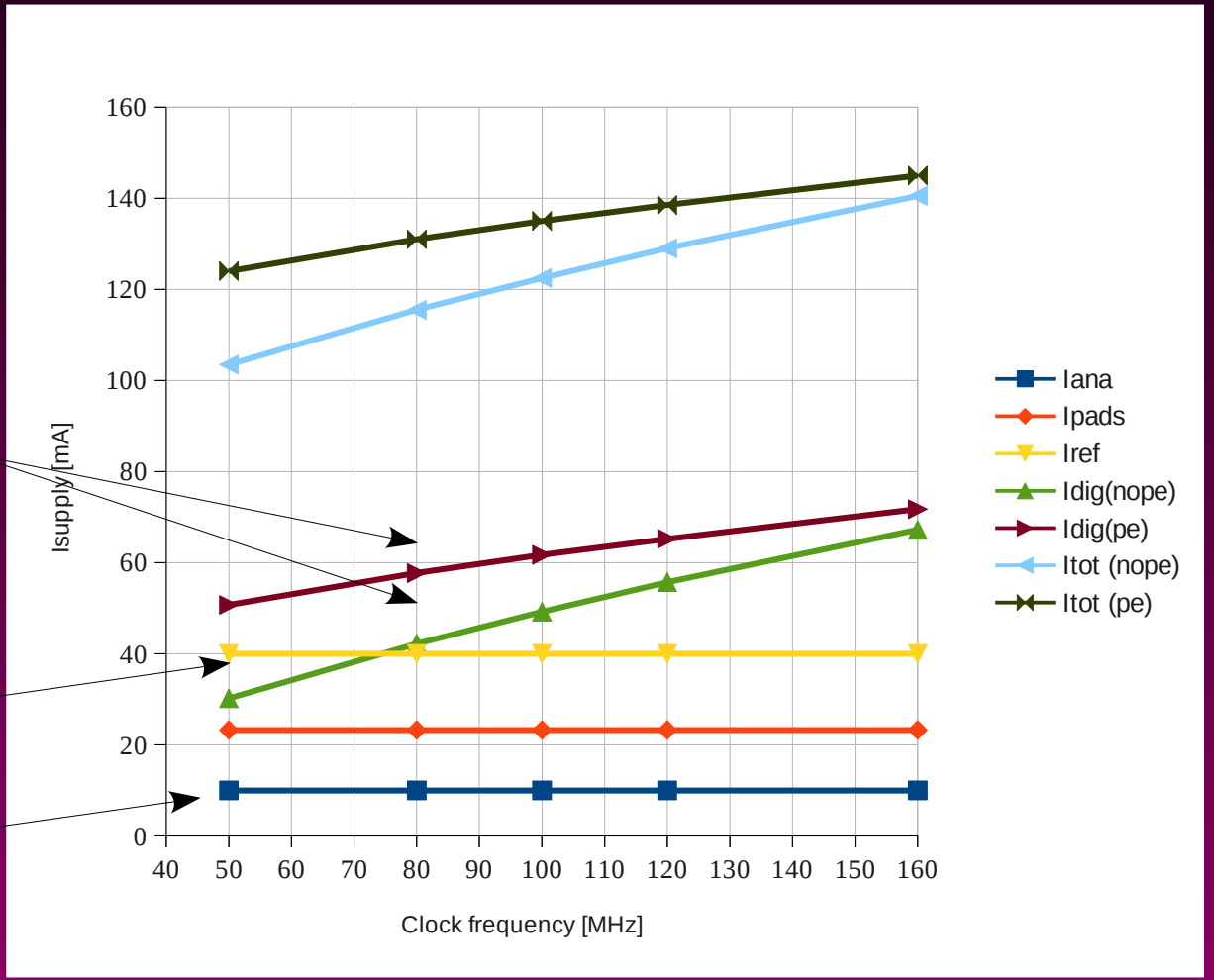
55% from the time stamp counter

Can be made almost negligible (zero in theory)

15 µA/pixel



Pixel cell

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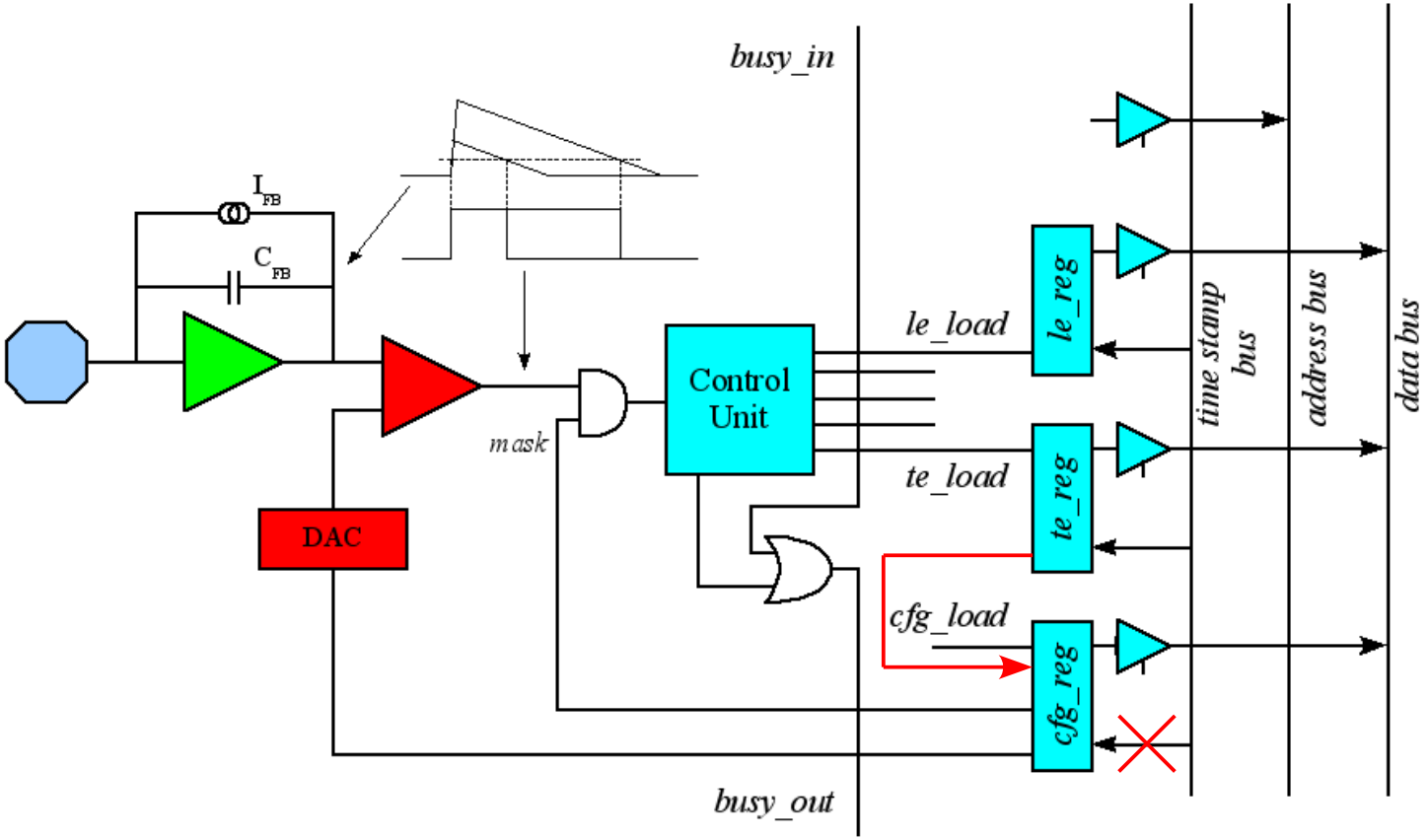

le_reg and te_reg are implemented via DICE-protected latches

cfg_reg is implemented with TMR/Hamming correctted DFF

Time stamp bus is NOT buffered at the pixel level

Time stamp transmission - no pe

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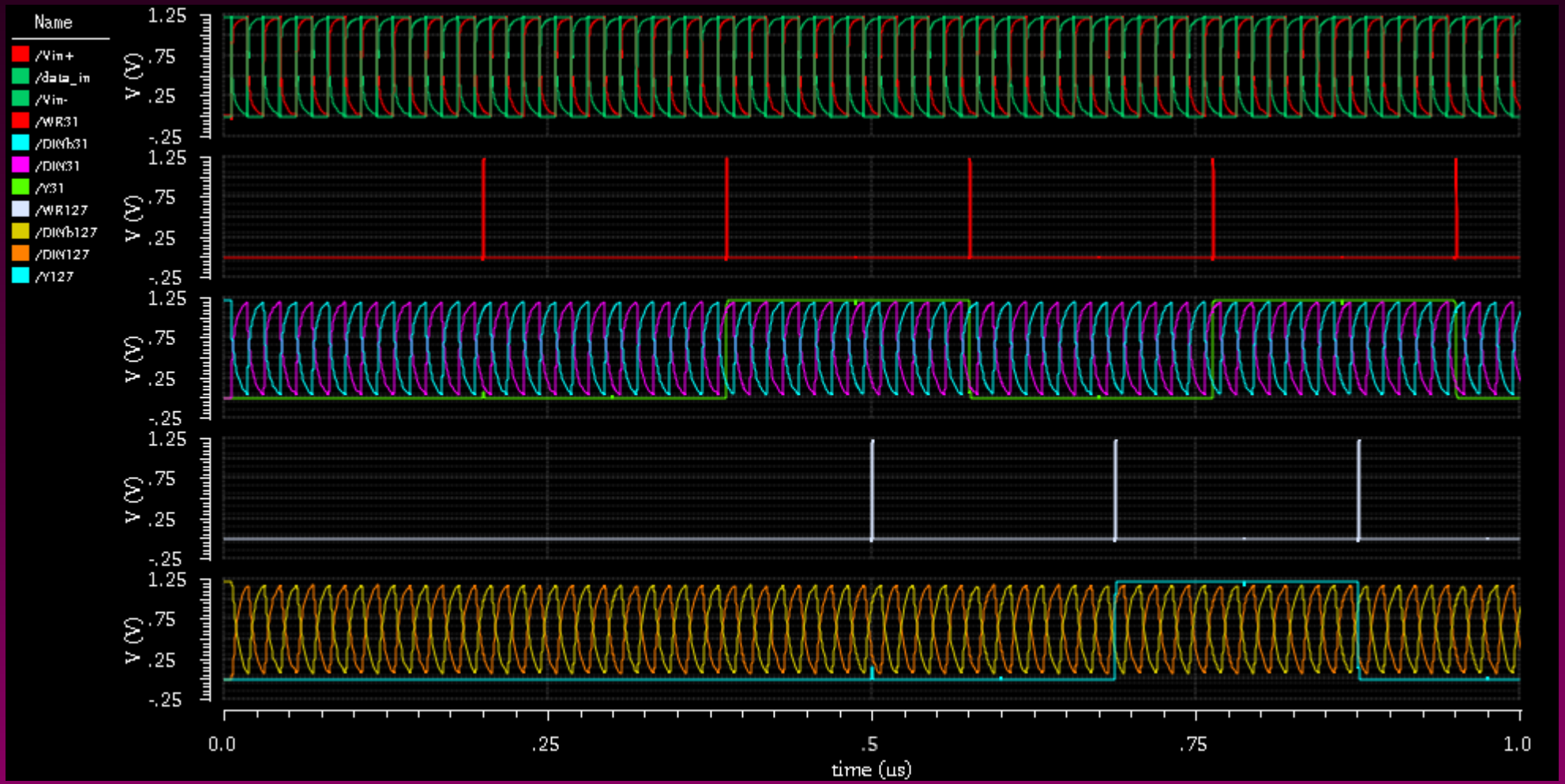
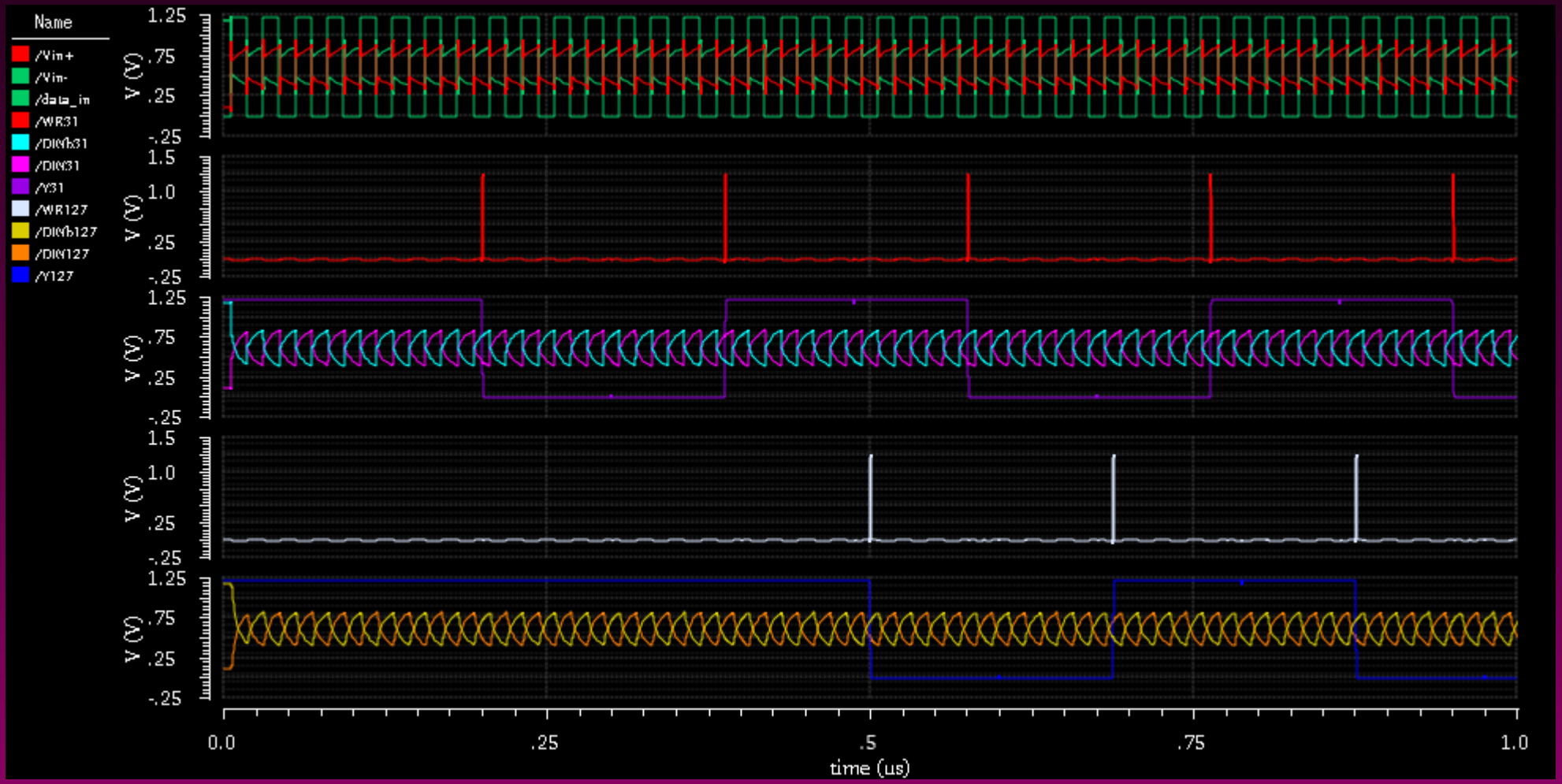


Time stamp transmission - pe

Sezione di Torino



Bus readout

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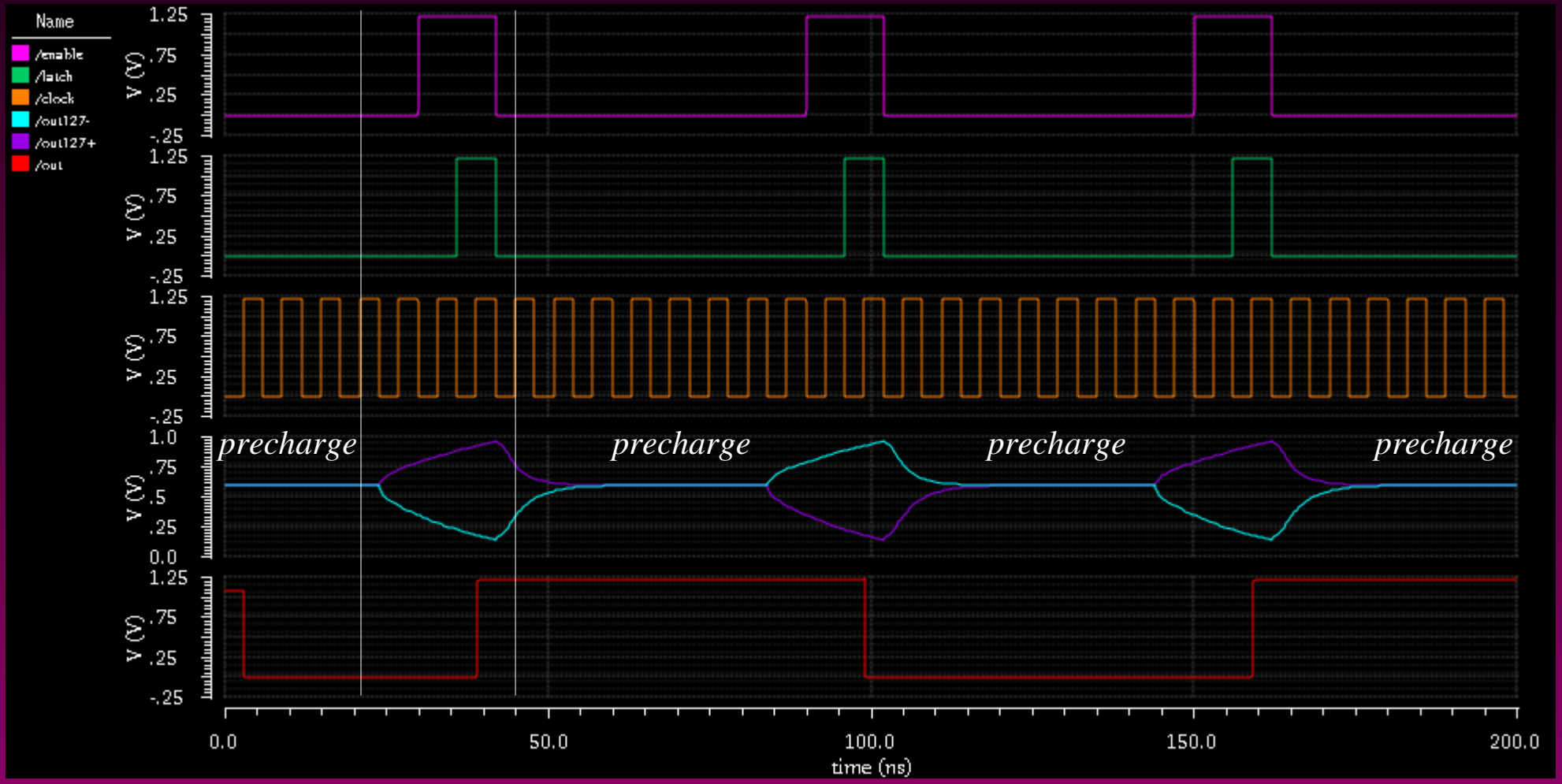

Pixel cell SEU protection

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- Leading edge and trailing edge registers will use latches with DICE scheme
  - 12 bits register size : 4.8 µm × 98.4 µm
- Configuration register will use DFF. Two possible protection schemes :
  - ✔ Hamming encoding with self correction
  - ✔ Triple redundancy
- Automatic P&R for control logic and configuration register over an area of 39.2 µm × 98.0 µm. Occupancy is 82% for Hamming encoding and 90% for TMR.
- Total on-pixel digital area : 50 µm × 100.0 µm (as in ToPiX v3)

TID tests - ToT

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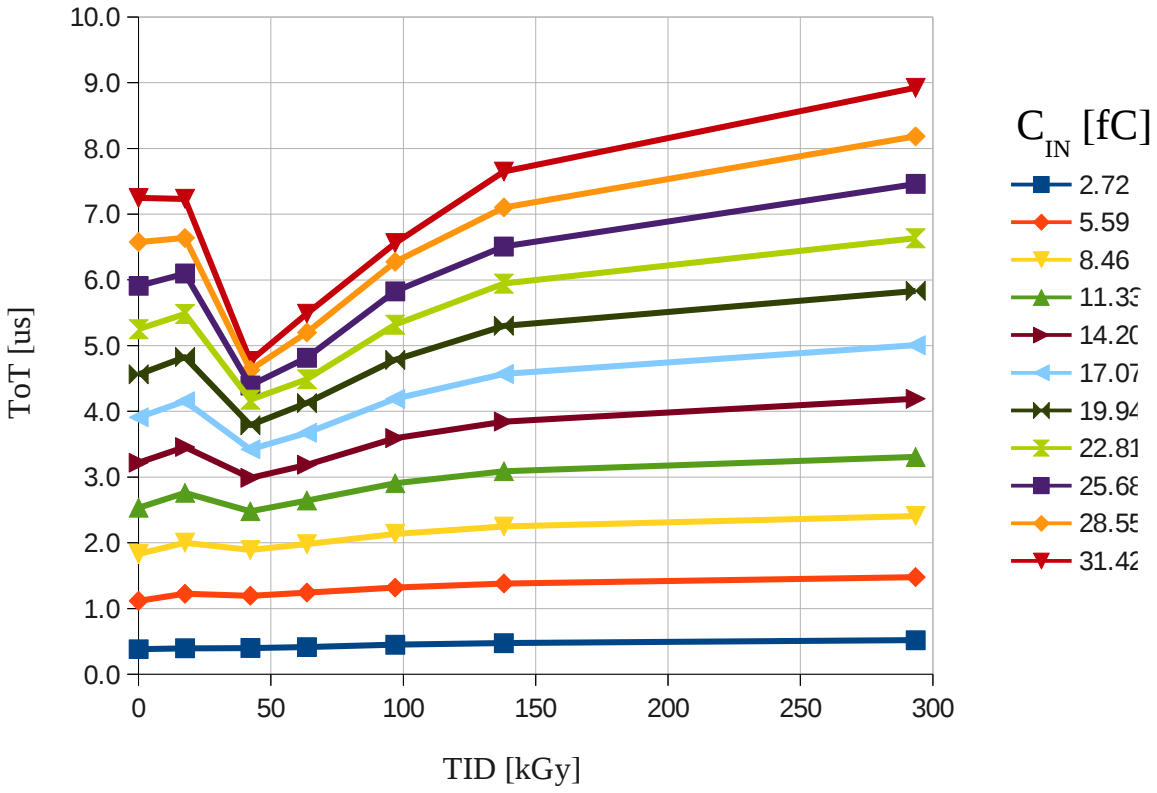
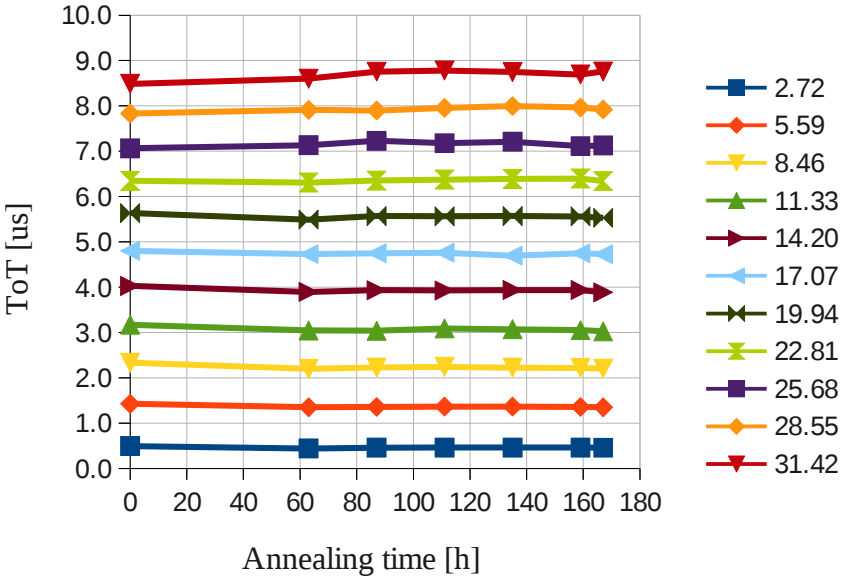
During irradiation



Annealing @ 80 °C



Probably due to effects in the clipping circuit – enclosed layout required ?

ToPiX v4

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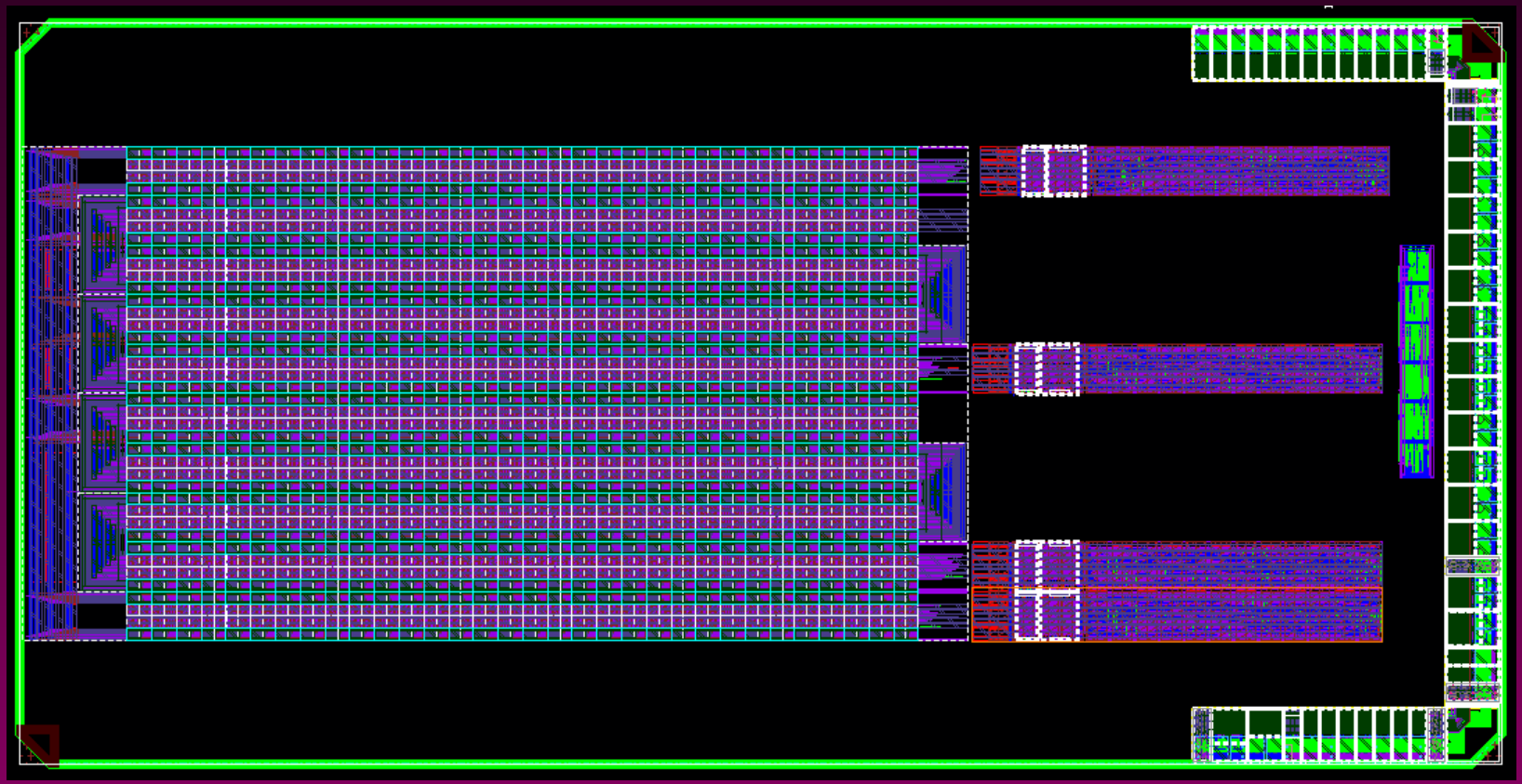

- Size : 6 mm × 3 mm
- Compatible with v3 sensors
- CMOS 130 nm
- New pixel SEU protection scheme
- New column bus Tx and Rx
- Timing optimization and bug fixing
- GBT e-link interface

GBT

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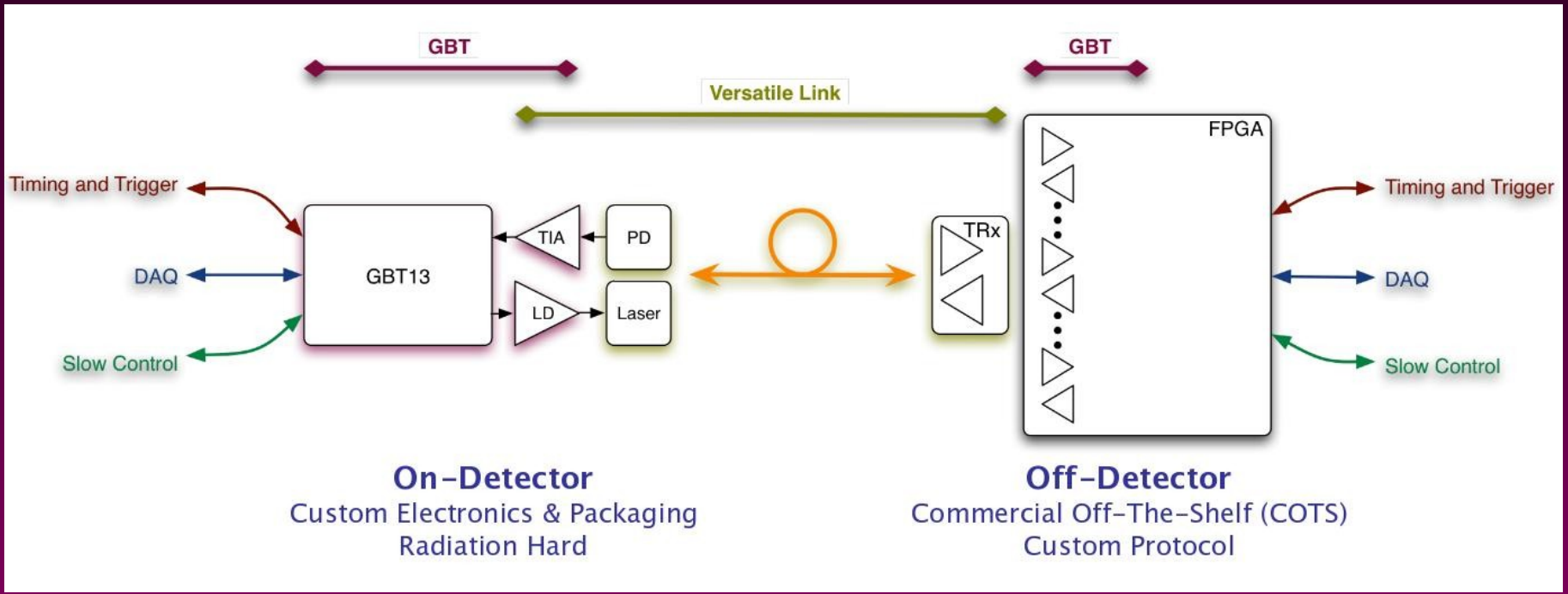
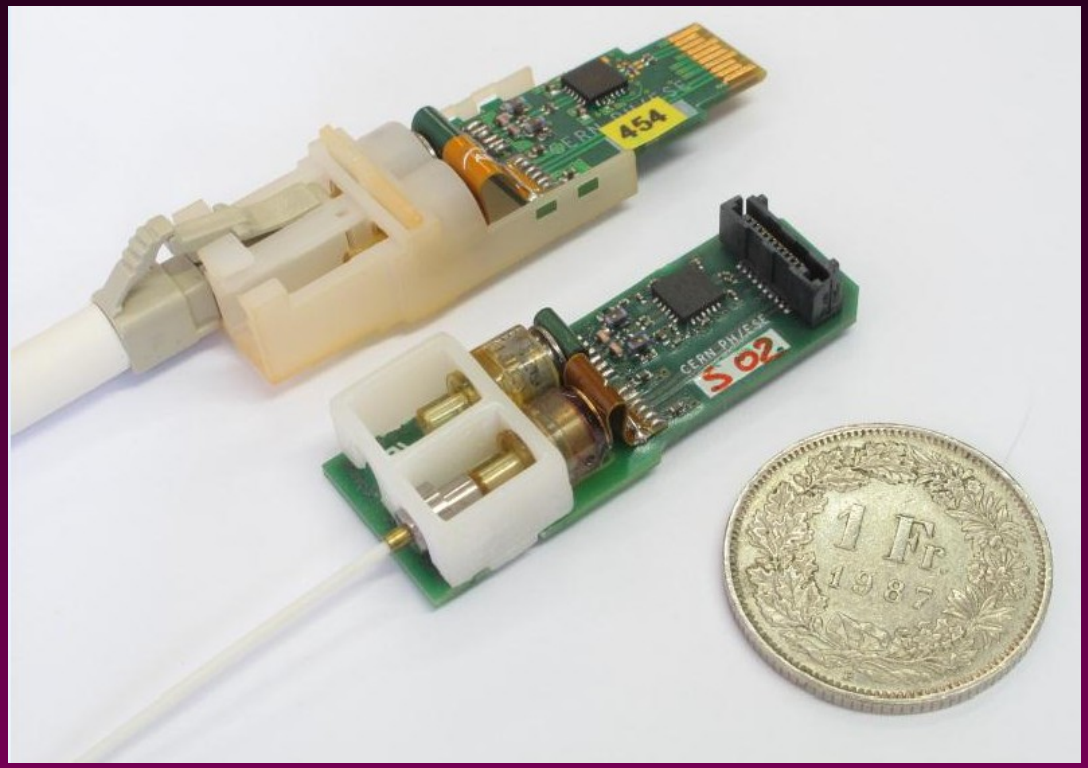


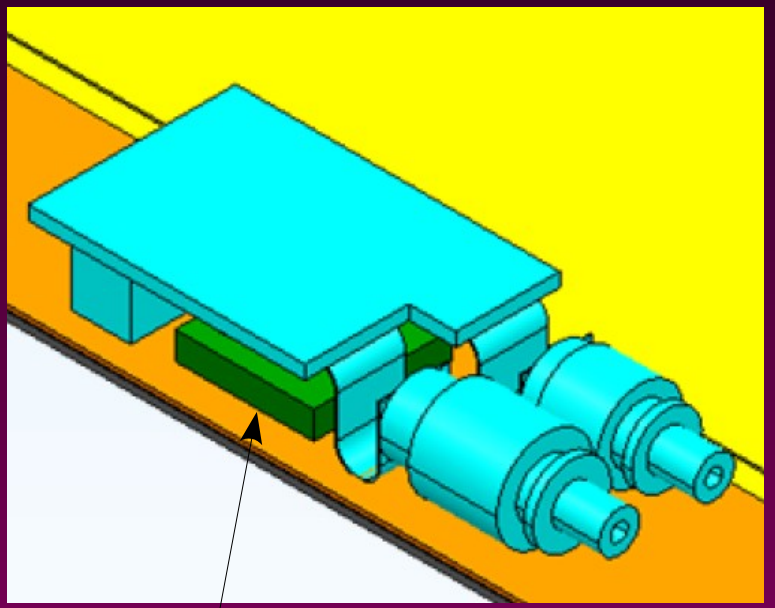
GBT components

Sezione di Torino



Versatile Transceiver
$50\times14\times10$ mm^3
$45\times15\times8$ mm^3
(F.Vasey, J.Troska, C.Soos)

Proposed arrangement for CMS tracker (C.Soos)



GBTx 10×10 mm^2
(P.Moreira et al.)

GBT status

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- GBTX :
  - Final chip received, tests will start in May 2013 *(export license problems have delayed the packaging...)*
  - Max power consumption 2.2 W (with all functionality on)
- GBTIA :
  - Version 2.0 ready for production – performances slightly worse than v1.0
  - Version 2.1 (bug fixing) currently under test
- GBLD :
  - Current version (GBLD v4) can work up to 7.5 Gb/s with a power consumption of ~300 mW (with VCSELs)
  - A low power version (GBLD v5) targeted at VCSELs has been submitted and is expected to return from foundry in June. Expected power saving 40% (up to 65% if double power supply is available)

GBT plans

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- GBT chipset production foreseen in Q2 2014
- To be installed by LHC experiments during LS2 (2018)
- LpGBT : low power GBT
  - Target power consumption : 500 mW *(75% reduction !)*
  - Technology : CMOS 65 nm (apart from GBLD)
  - 2 GBTX versions (LpGBT with SerDes only and full GBTX)
  - High bandwidth (4.8 Gb/s downlink, 4.8/9.6 Gb/s uplink)
  - Development will start in 2014
  - *Not yet an approved project...*

Power regulator

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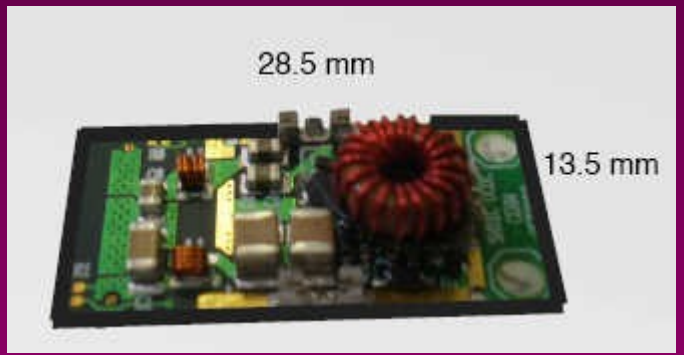
- ToPiX power supply 1.2 V – I_{DC} ~ 1 A (estimated)

  → *voltage drop on cables is not negligible*

- A DC-DC converter solution compatible with the radiation levels and the magnetic field of a silicon tracker is under development @ CERN for sLHC
- Current CERN version : V_{IN} 10÷12 V, V_{OUT}=1.2÷3.3 V, I_{OUT} < 3 A
- V_{OUT}= 1.5 V, I_{OUT} < 3-4 A now avail.
- Tests with ToPiX v3 ongoing



Conclusions

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- Development of the ToPiX v4 has been delayed by concerns regarding radiation tolerance.
- Pixel cell registers, bus drivers and precharge logic have been completely redesigned in order to increase speed while reducing power. Design is well advanced.
- To be done :
  - Radiation tolerance improvement of the analog part
  - Chip control unit with GBTX interface
- GBT project toward mass prodution in 1.5 years
- Tests on voltage regulators and low mass cables ongoing

PANDA FEE-DAQ Workshop

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Backup slides

Full chip estimate

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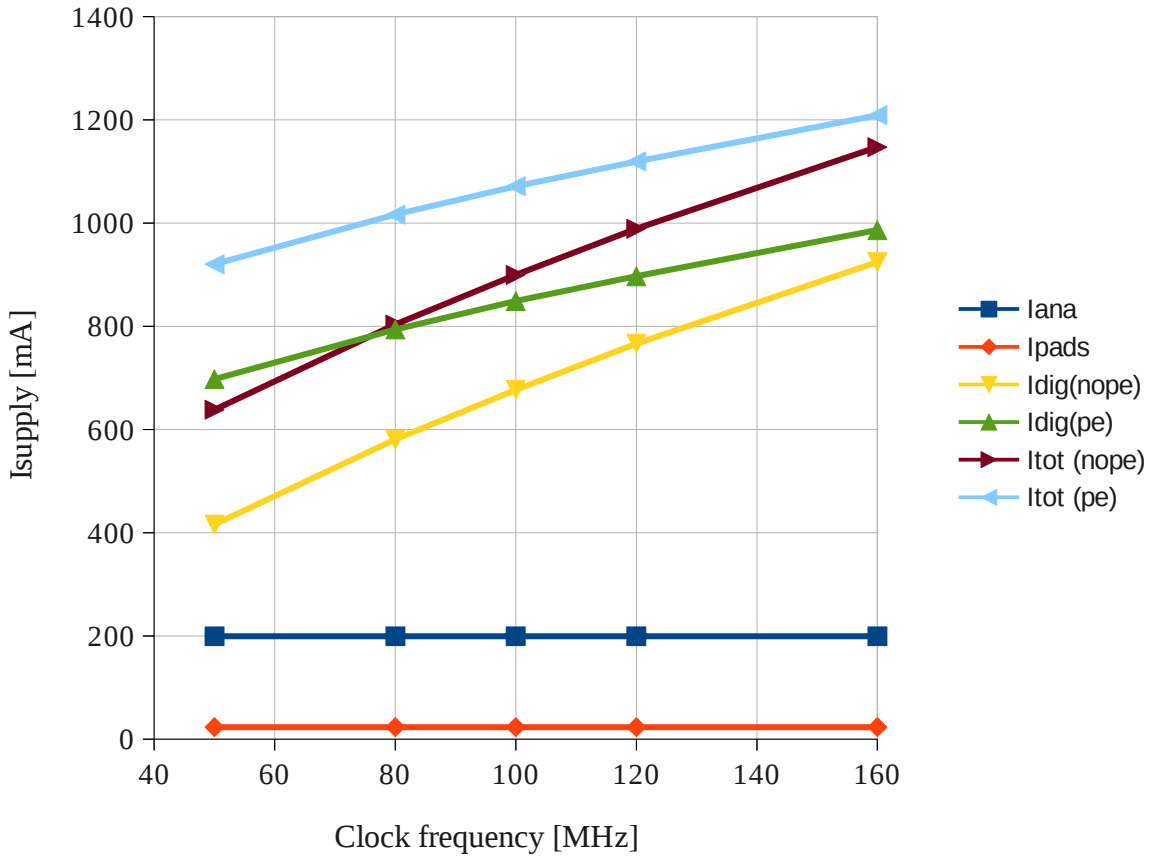

- Very rough estimate
- Still room for improvements (ToPiX v3 not really designed having low power in mind...)
- Time stamp column drivers taken from NA62 GtkTo → room for improvement
- *However, power is dominated by digital logic, therefore it is* $\propto$ *fclock*

GBLD I2C SEU results

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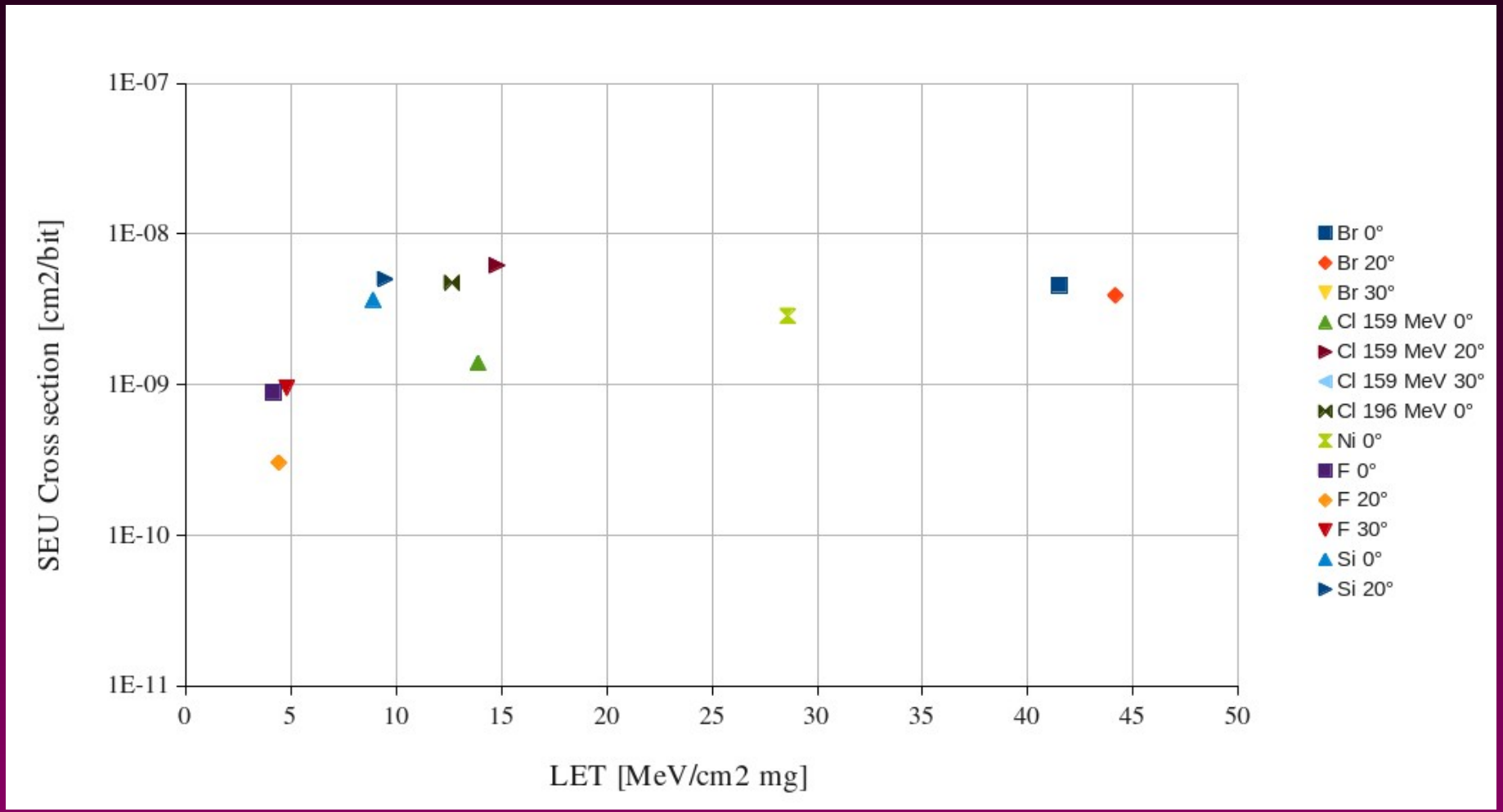

ToPiX + sensor

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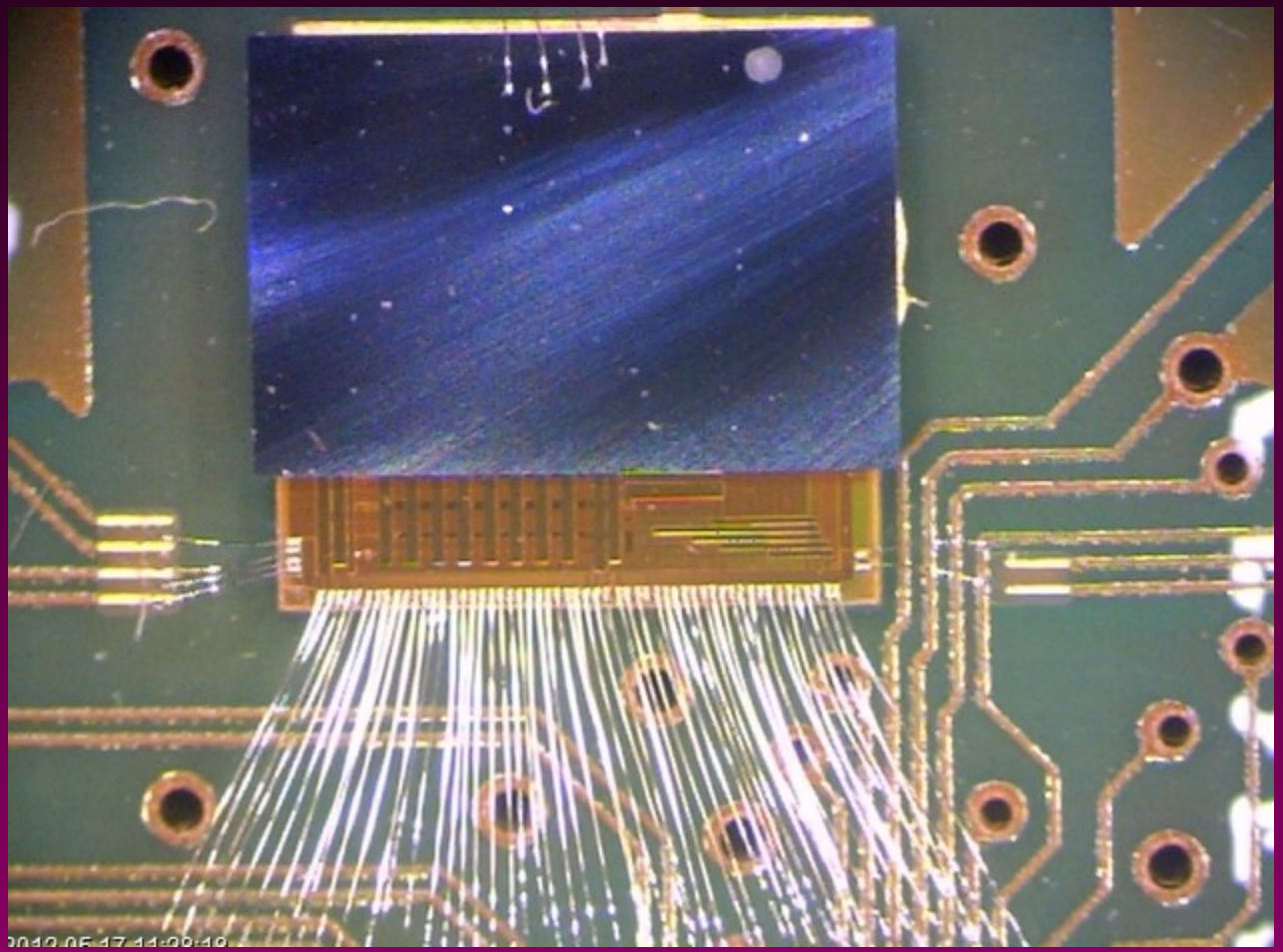

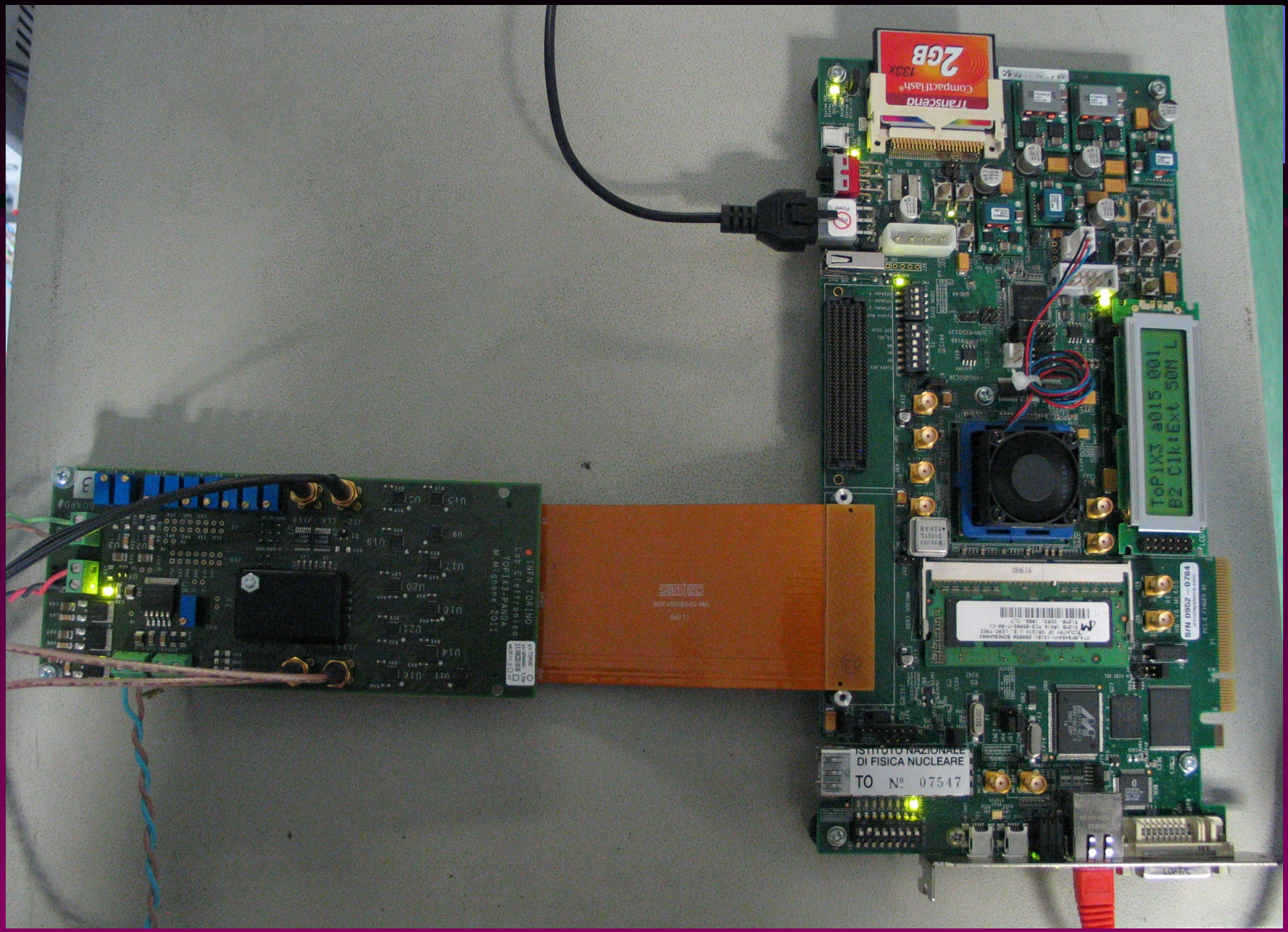
Transcend
CompactFlash
2GB
133x
INFN TORINO
Lab. Elettronica
TOF1X3-PANDA
M.Mignone 2013
ISTITUTO NAZIONALE
DI FISICA NUCLEARE
TO Nº 07547

Baseline correction

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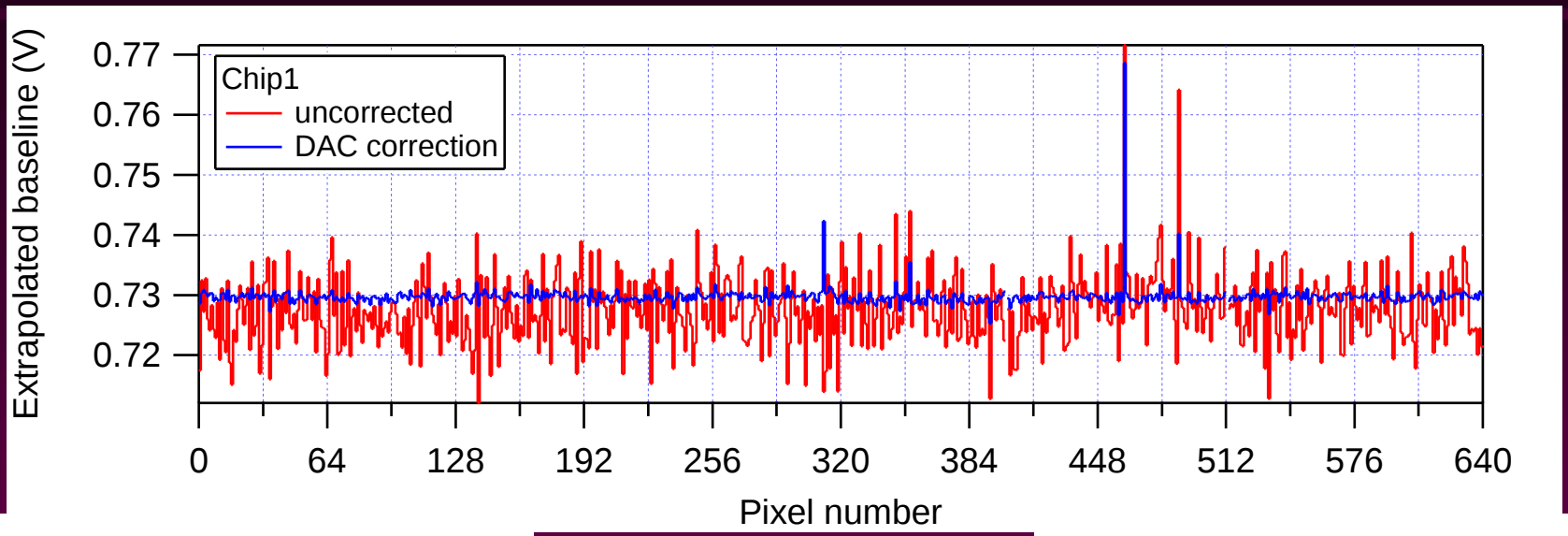
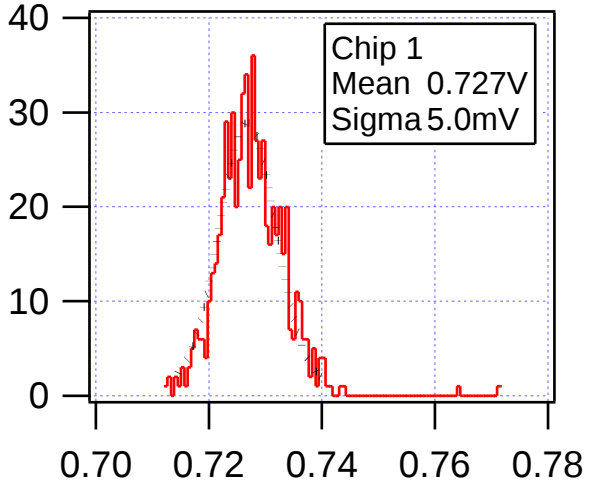
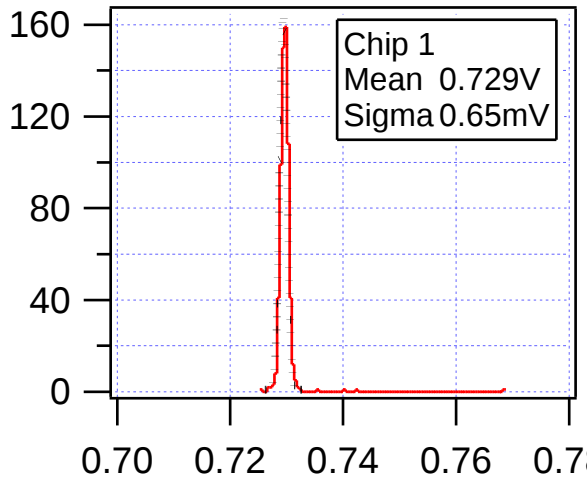
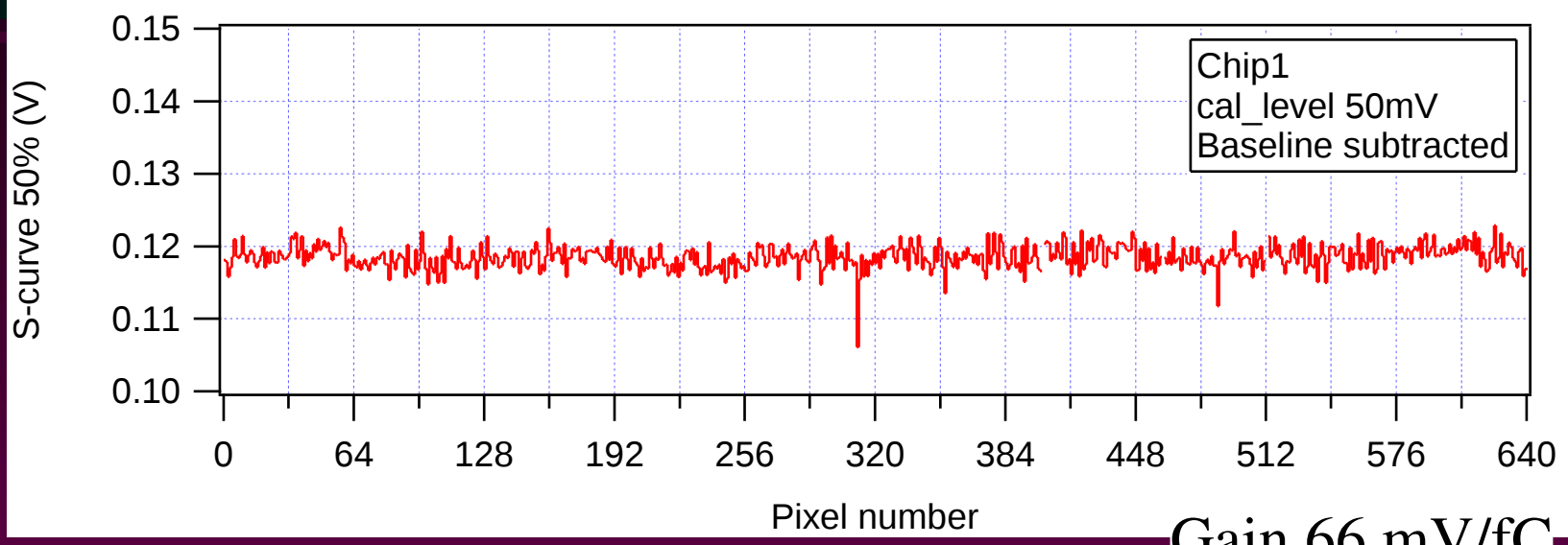




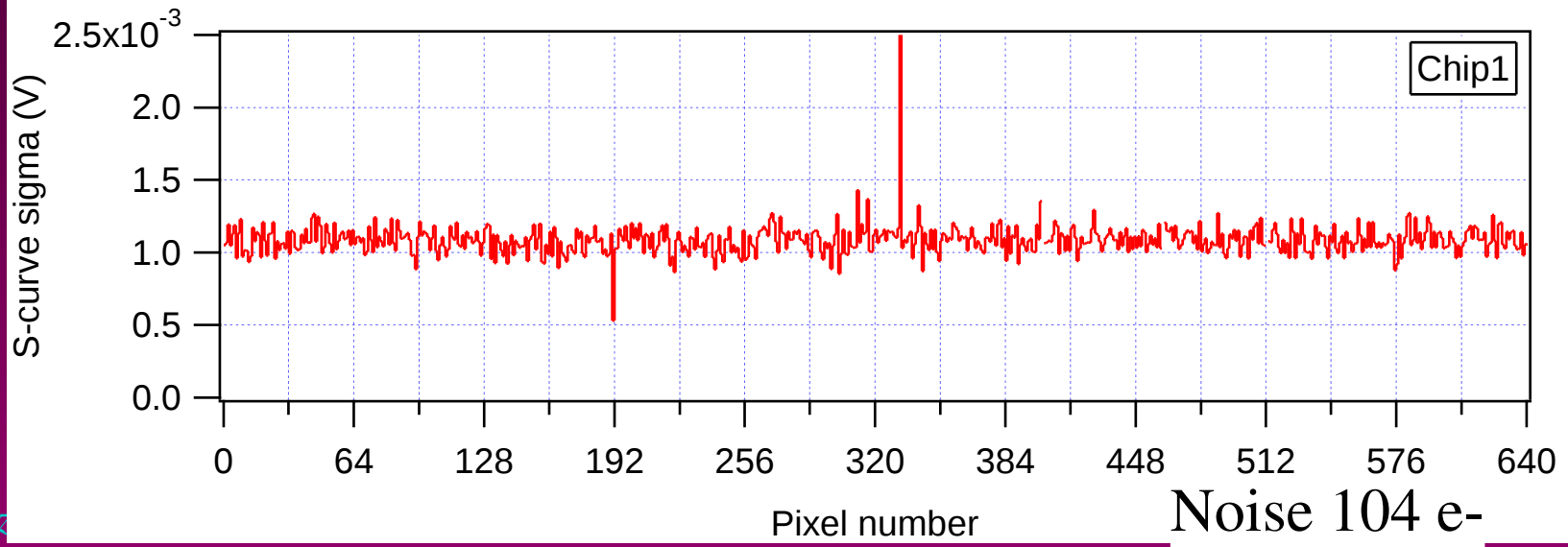
DAC correction



Gain & Noise



Gain 66 mV/fC



Noise 104 e-

ToT @ 5 nA

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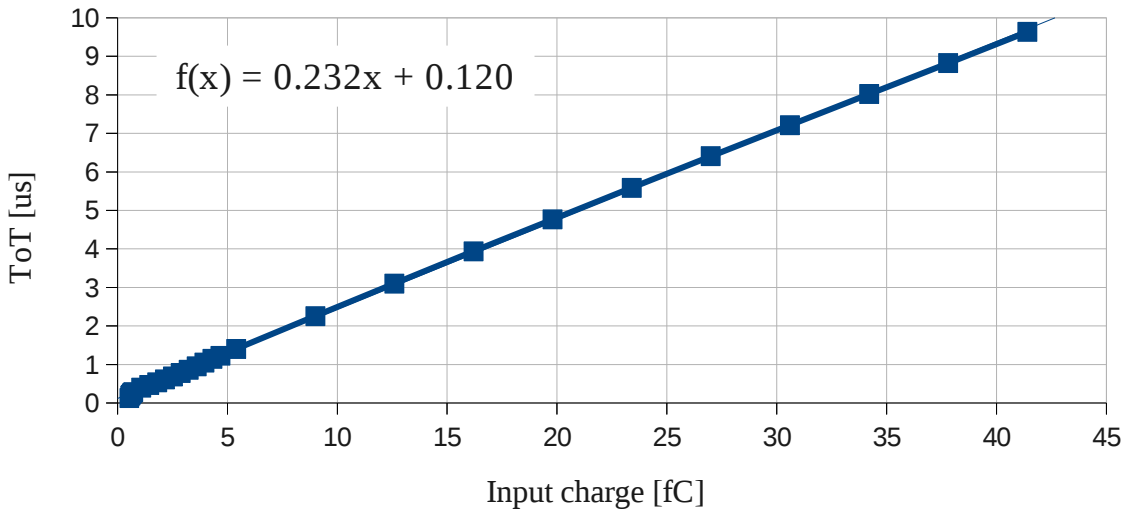
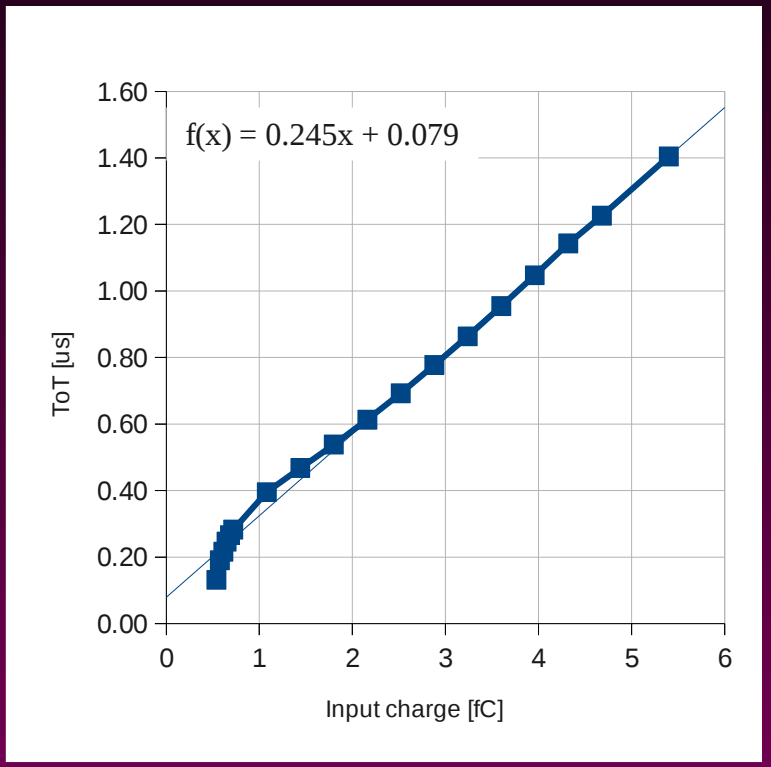
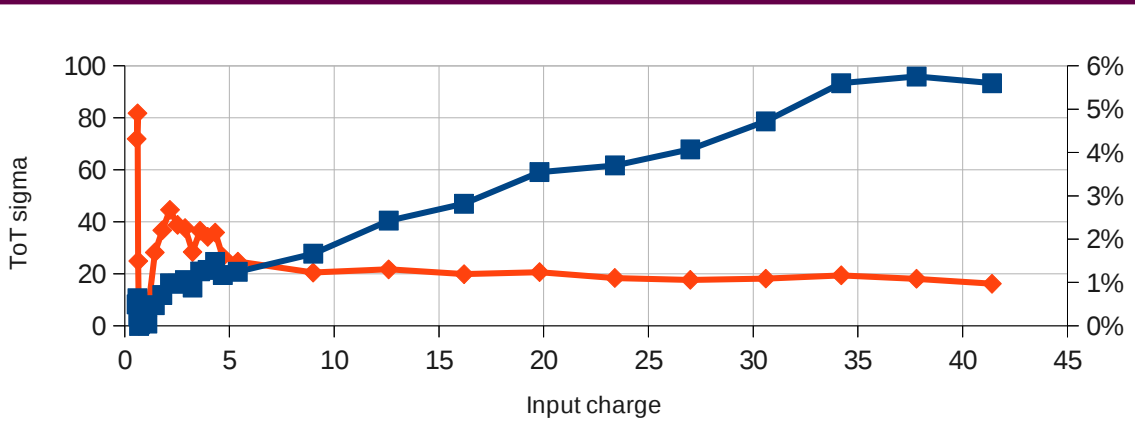
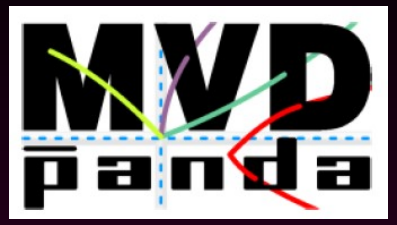






$I_{FB} = 5\ nA$

Simulated gain : 202 ns/fC



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