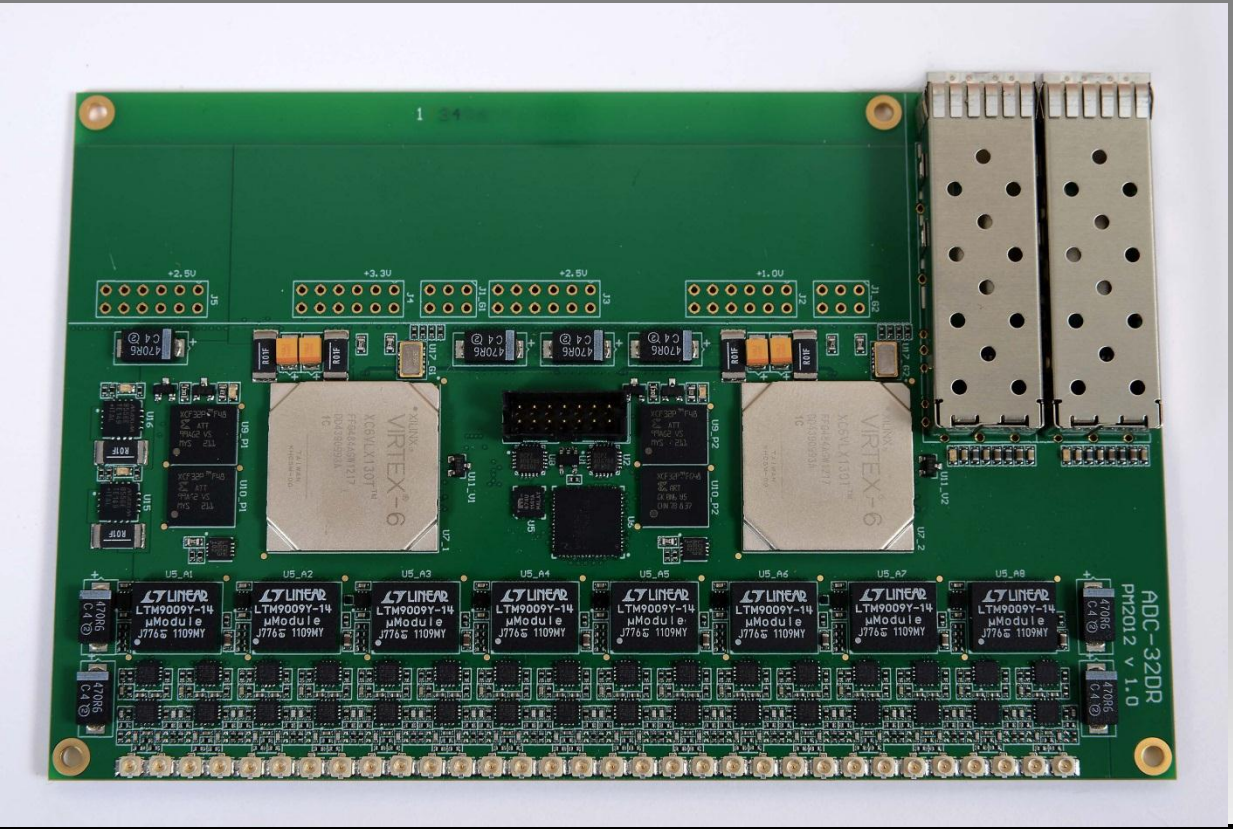
A 32-channel, 14-bit, dual range, 80-125 MSPS ADC for the EMC-Endcap



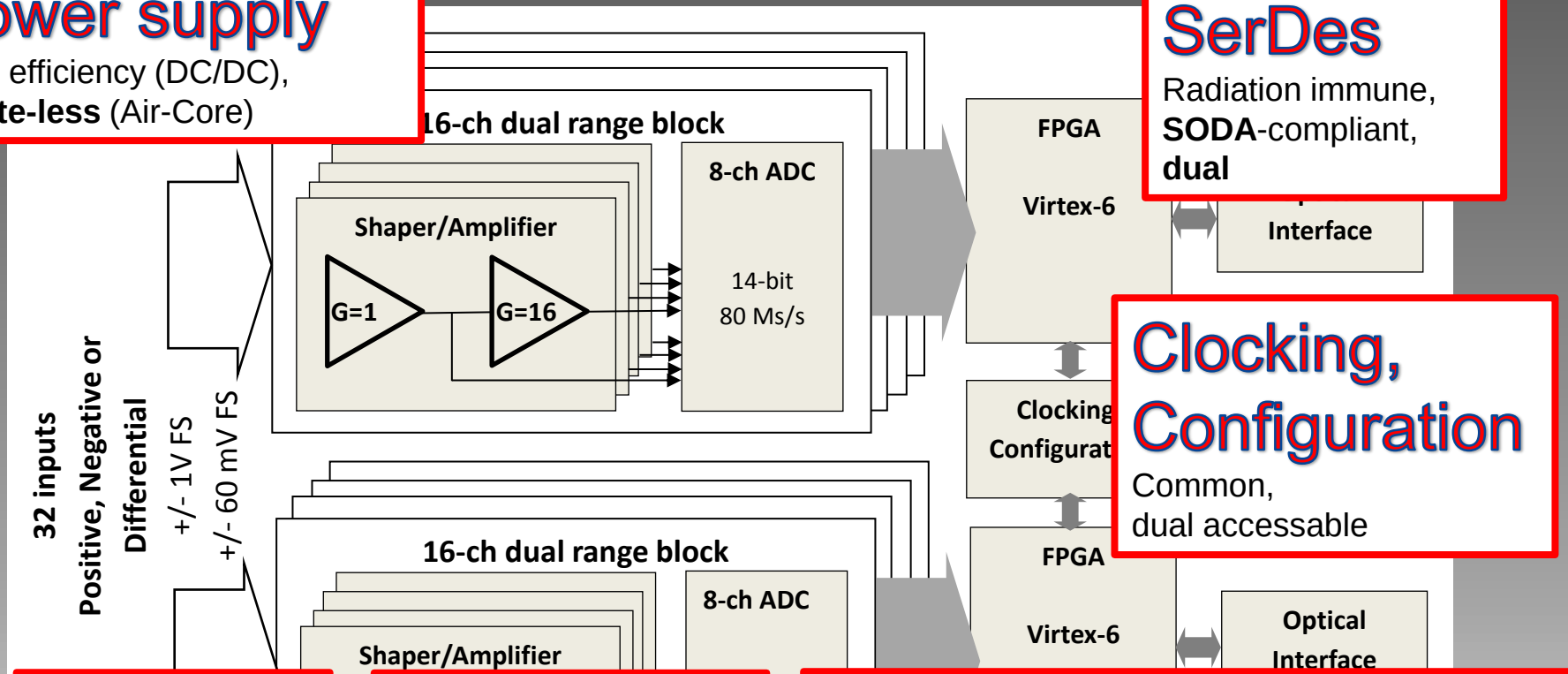
Design Idea

Power supply

High efficiency (DC/DC),
ferrite-less (Air-Core)

SerDes

Radiation immune,
SODA-compliant,
dual



Clocking, Configuration

Common,
dual accessable

Amplifier

Fully differential,
BW > 100 MHz,
SR > 100 V/us,
Pd < 50 mW/ch,
Active filter

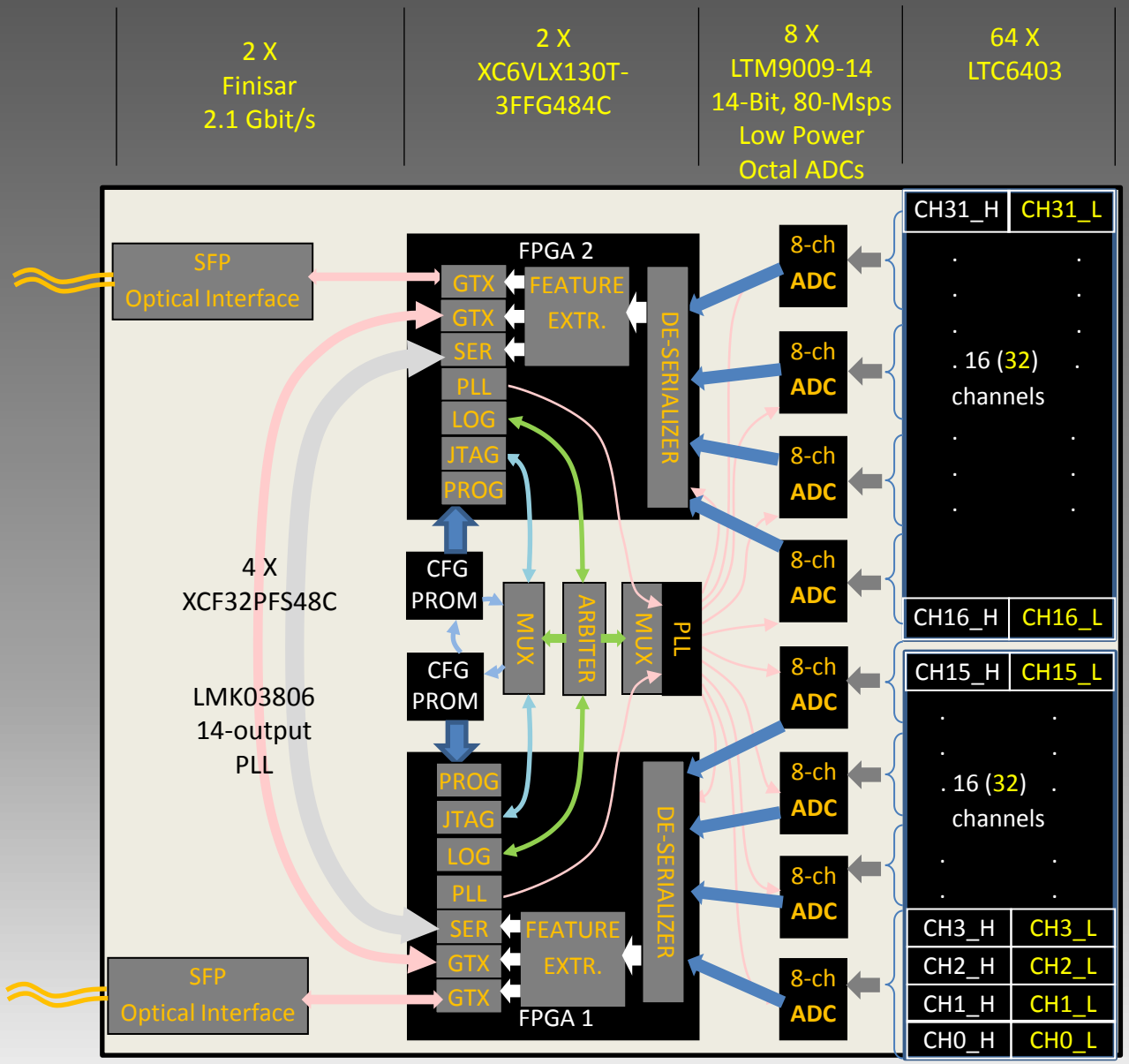
ADC

EOB > **14–bit**,
Sampling rate ~**80Ms/s**,
Pd < 100 mW/ch,
32 (64) ch. per board

FPGA

Radiation immune
(RT-Flash or Tripple Modular Redundancy)
or partially reconfigurable with watchdog,
32/64 channels per board

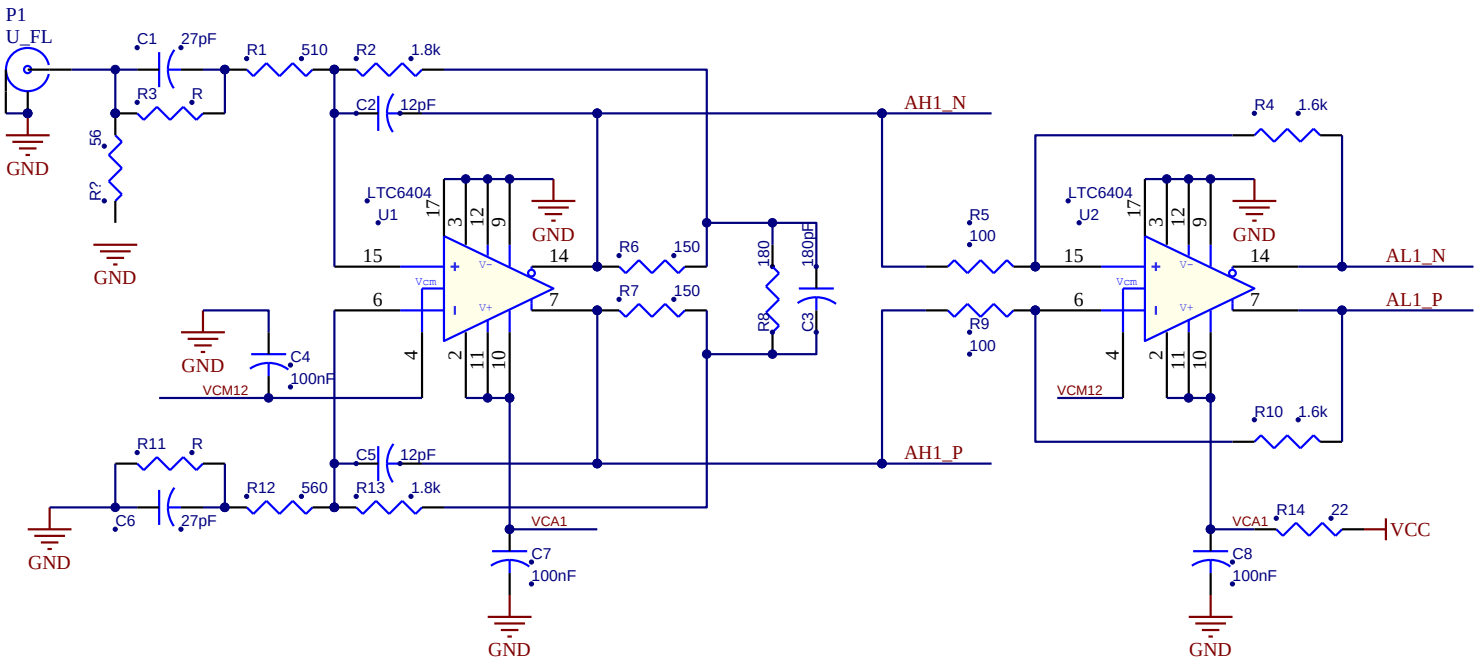
ADC for EMC-Endcap – Design idea



ADC for EMC-Endcap

– identyfying componenets

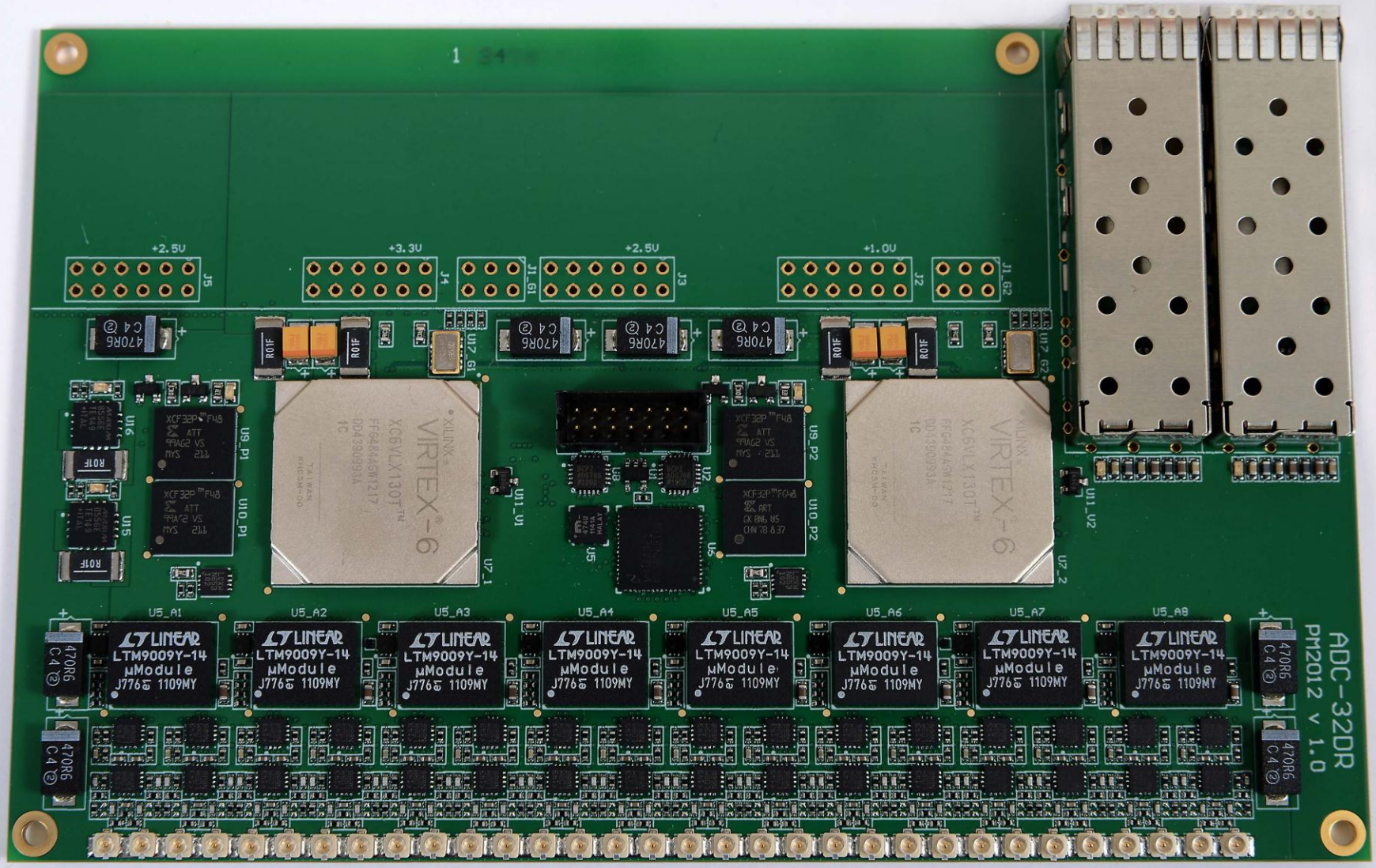
KVI – shaper / active filter



(by Franz Schreuder)

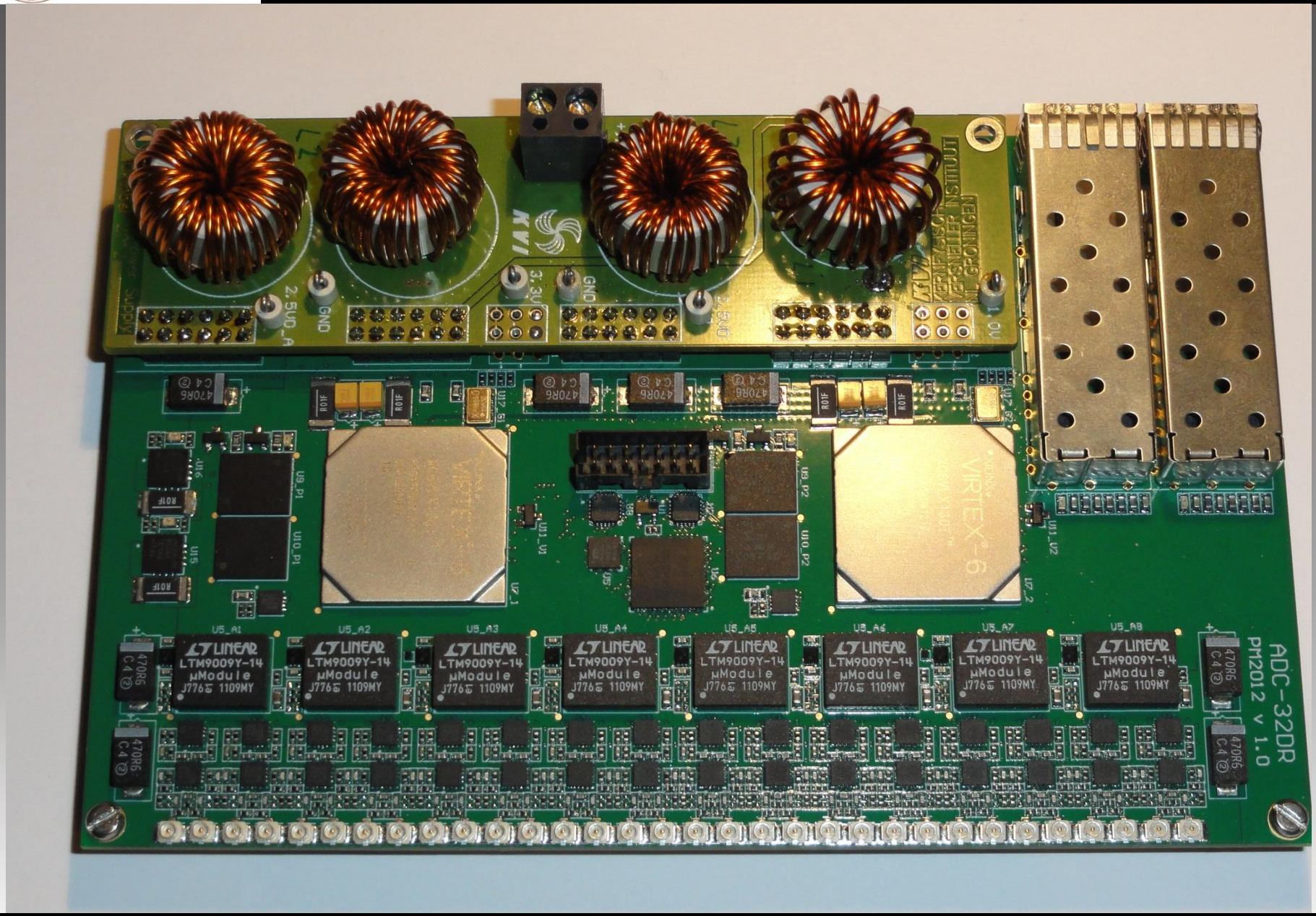
ADC for EMC-Endcap

- Ready prototype



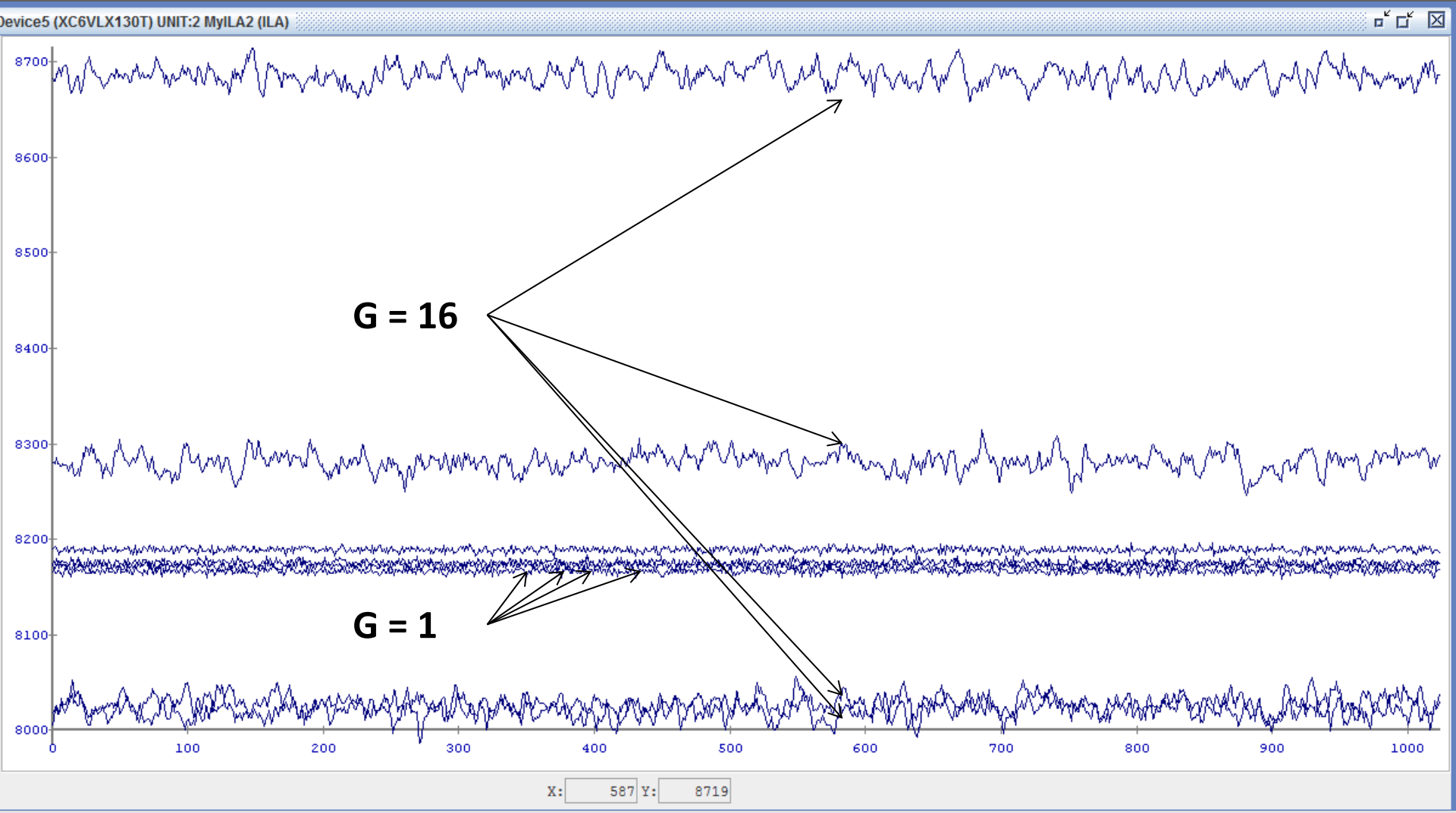
ADC for EMC-Endcap

- Ready prototype



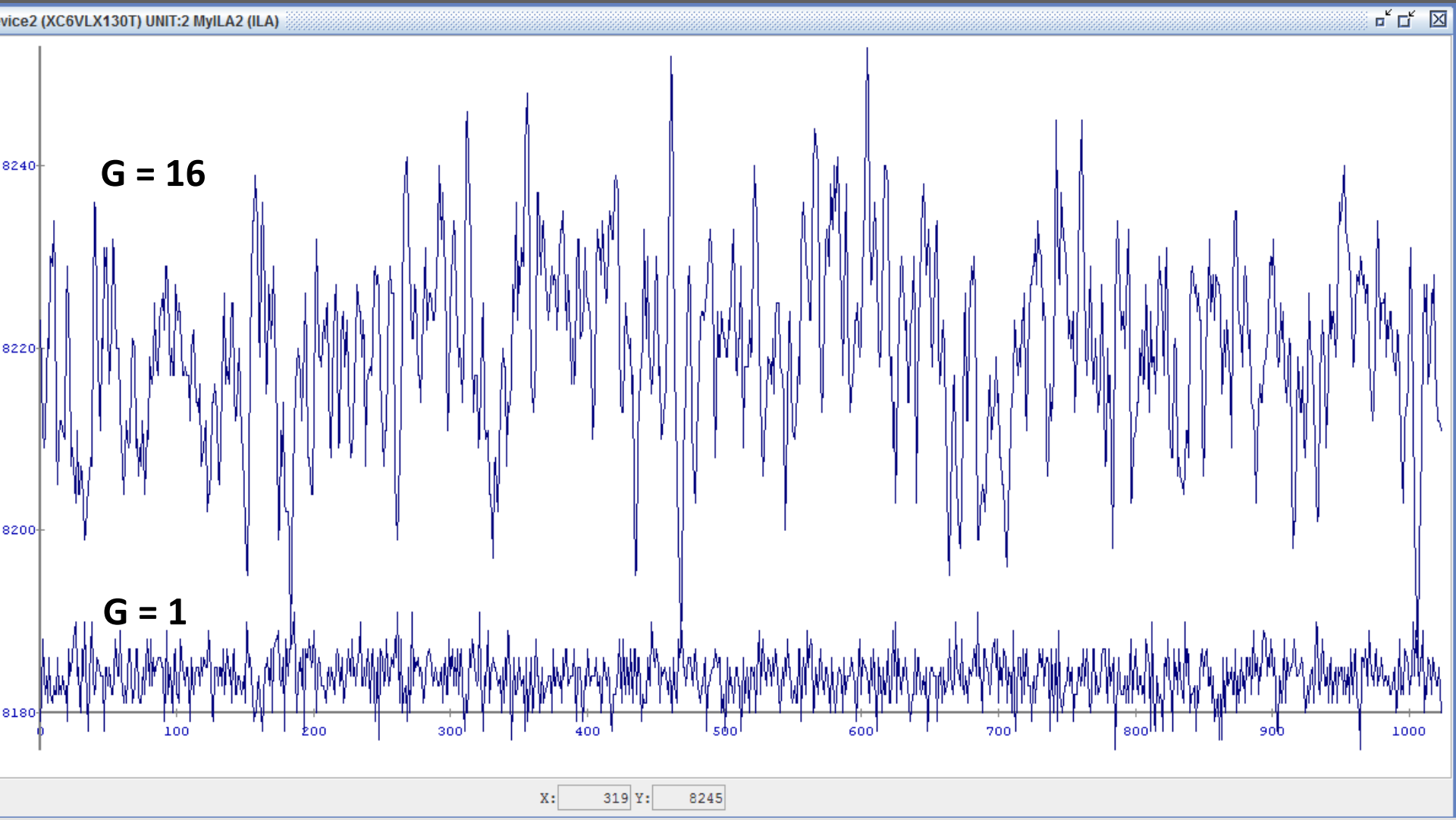
ADC for EMC-Endcap

- Noise tracks



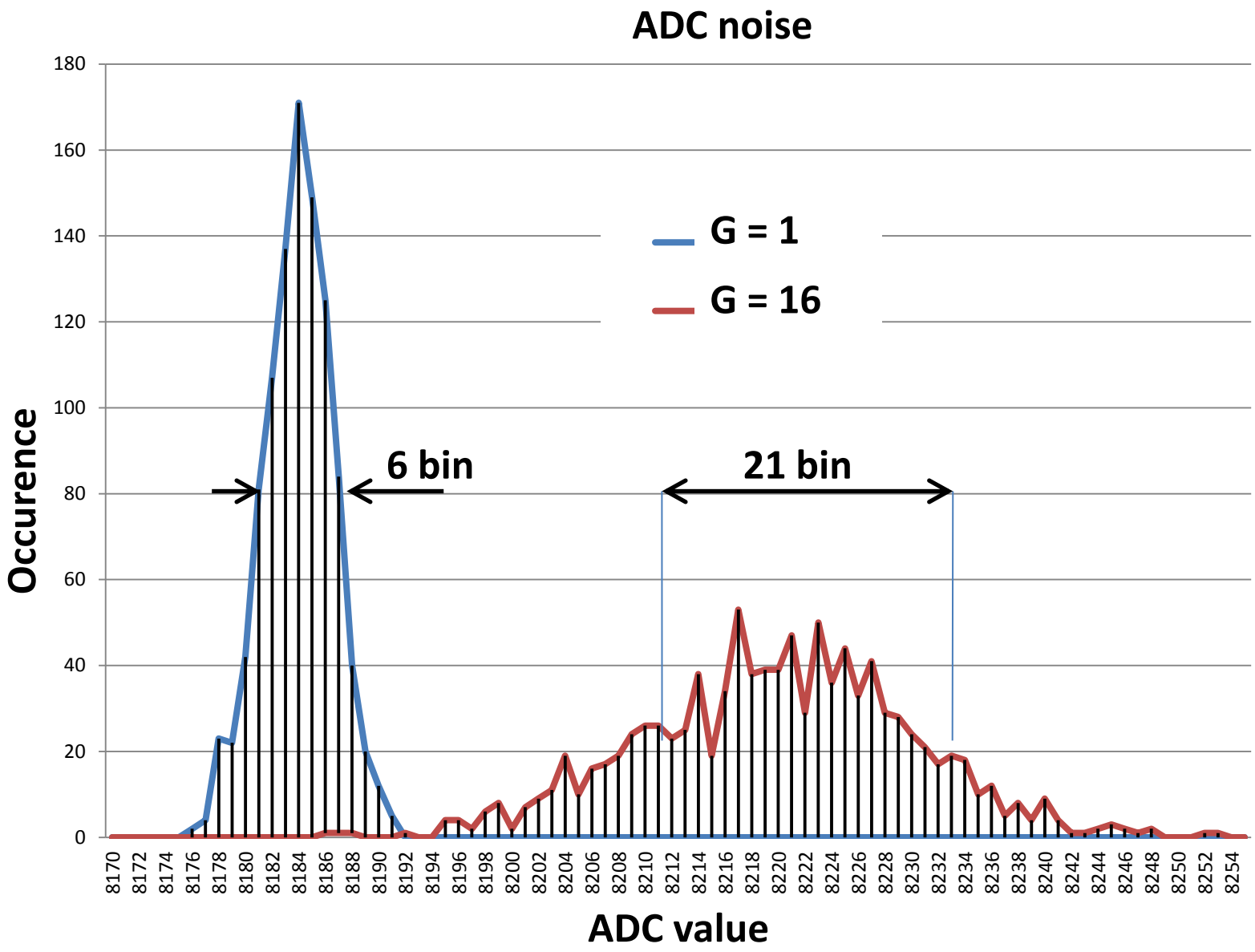
ADC for EMC-Endcap

- Noise track



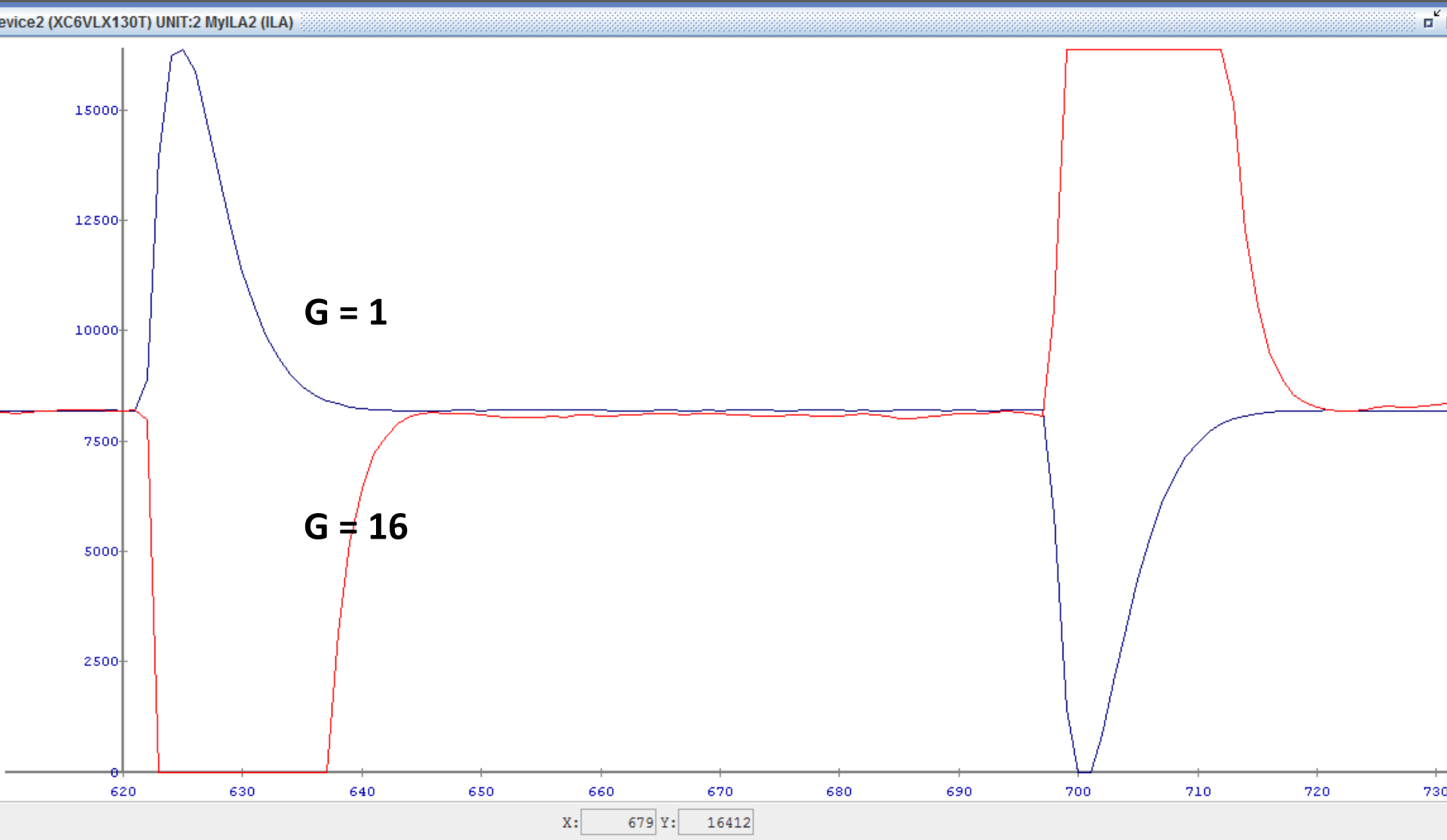
ADC for EMC-Endcap

Noise – amplitude spectrum



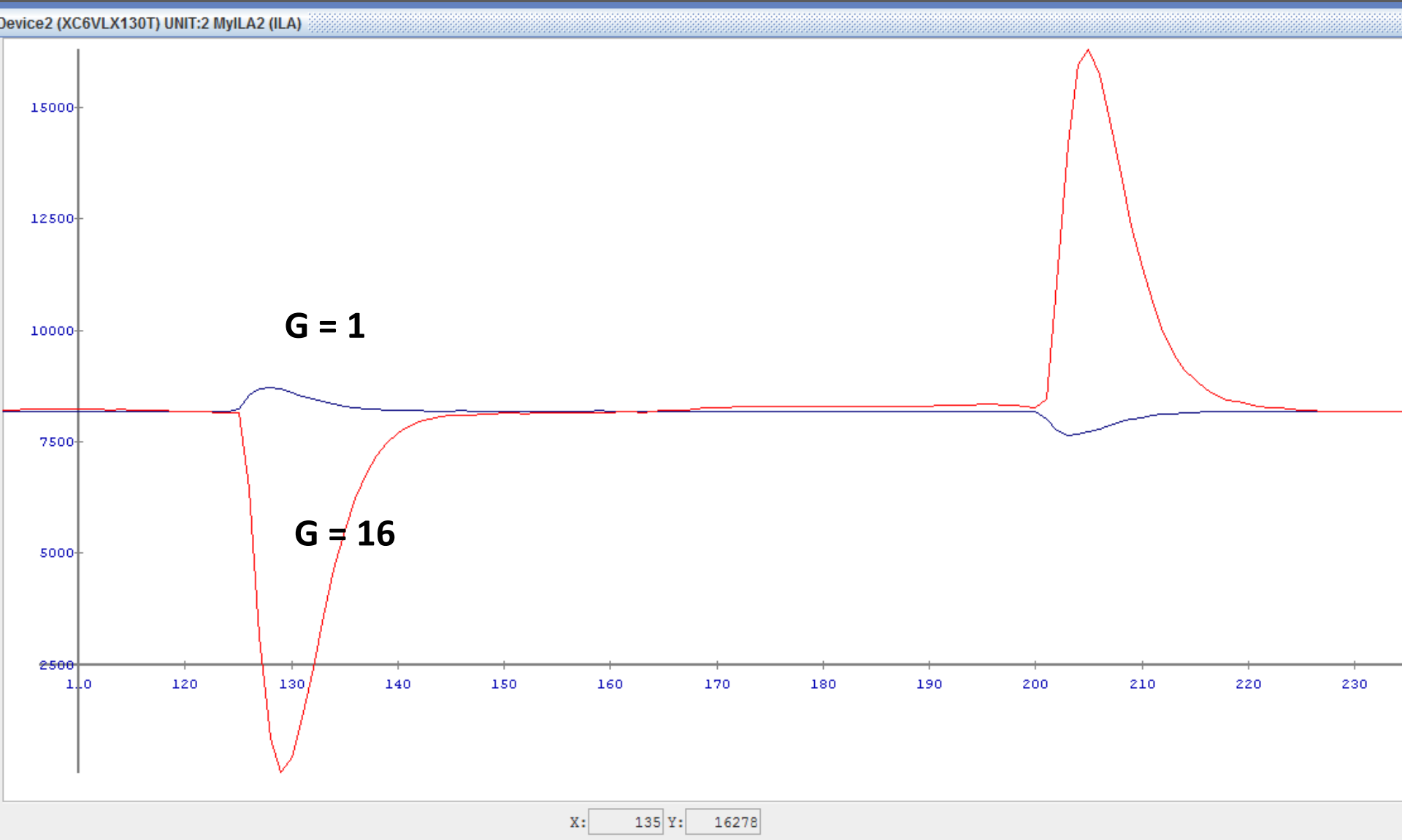
ADC for EMC-Endcap

- 1V pulse - bipolar



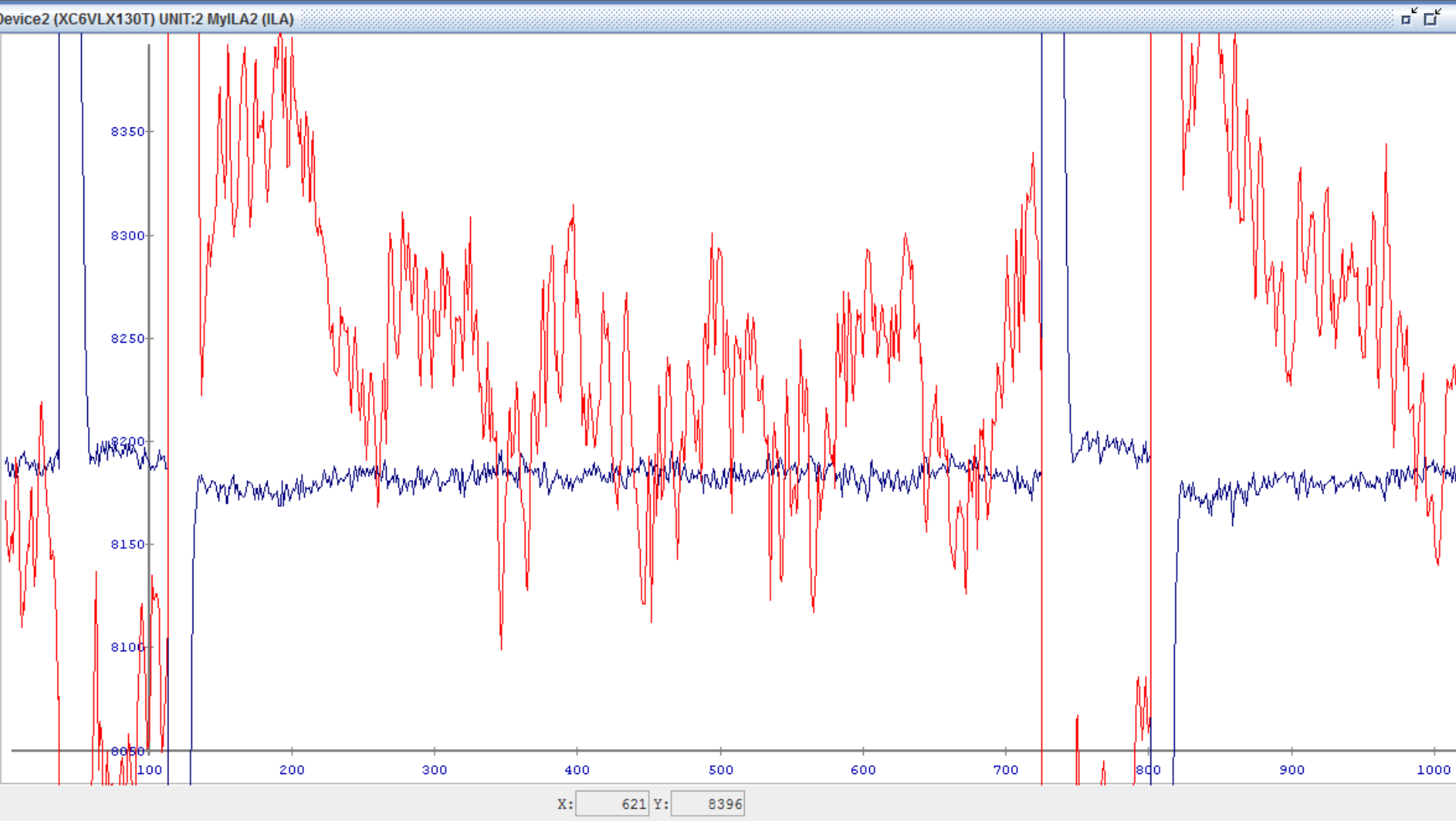
ADC for EMC-Endcap

- 60 mV pulse - bipolar



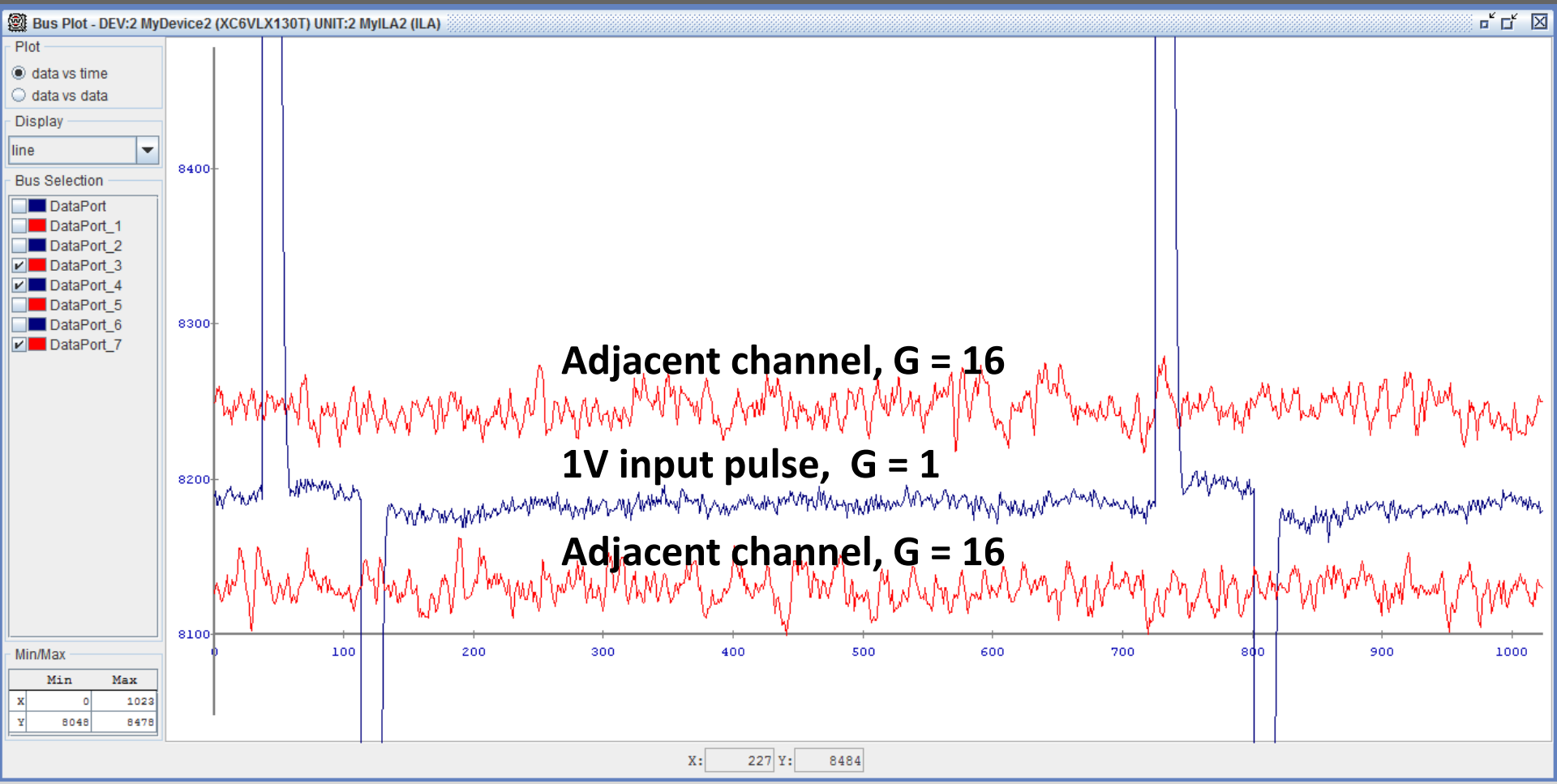
ADC for EMC-Endcap

- Noise track



ADC for EMC-Endcap

- Cross-talk



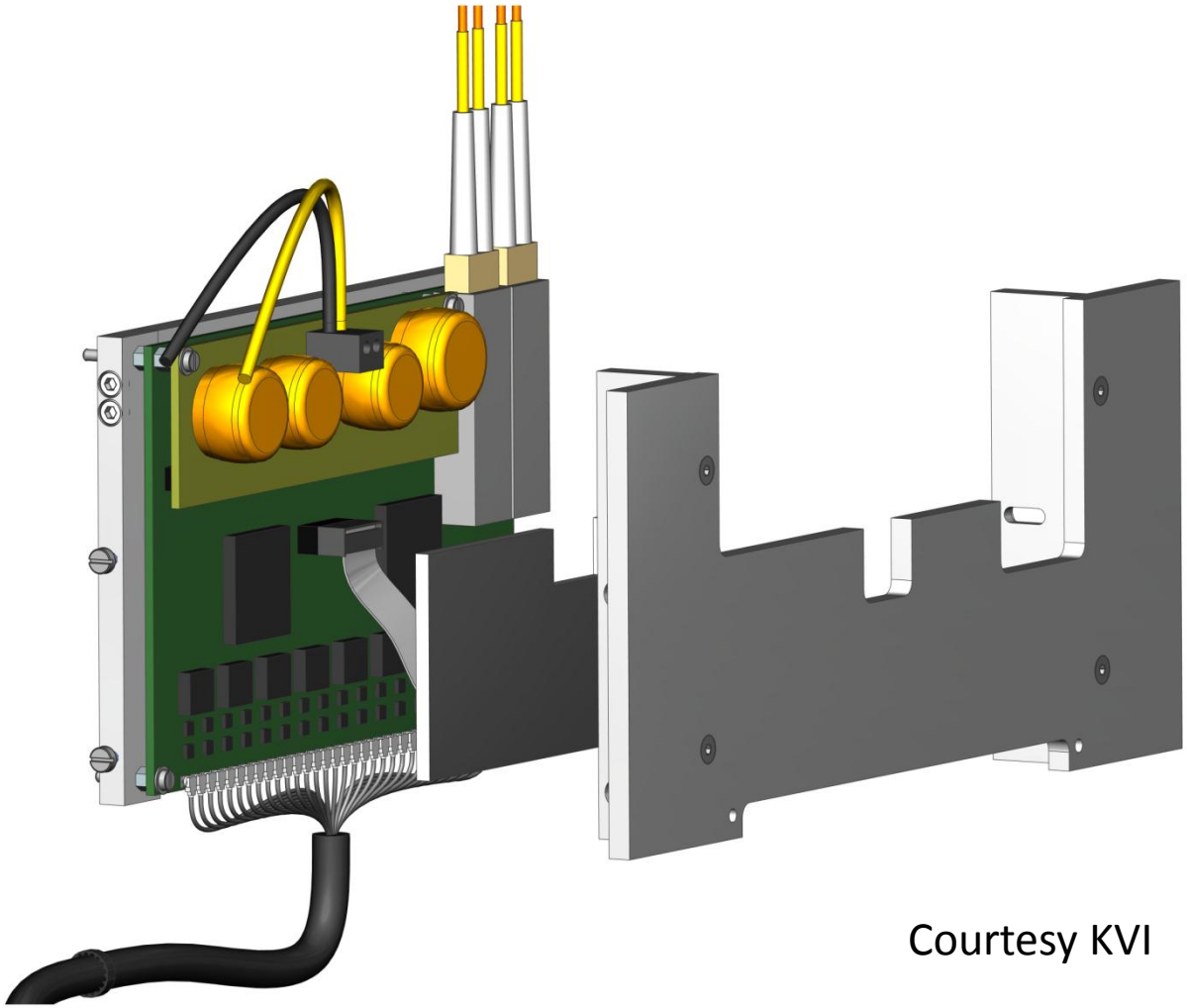
ADC for EMC-Endcap

- Power requirements

Analog (LDO filtered)	
+2.2V (1.8V) – 3.2A (ADC)	7.0 W
+2.9V (2.5V) – 1A (AMP)	2.9 W
Digital	
+1.0V – 6A (FPGA)	6.0W
+1.2V – 1.2A (FPGA)	1.5W
+1.8V - 0.8A (ADC)	1.5W
+2.5V – 3.0A (FPGA)	7.5W
+3.3V – 0.4A (PLL), 0.5A(SFP)	1.3W
TOTAL NETTO POWER	28 W

ADC for EMC-Endcap

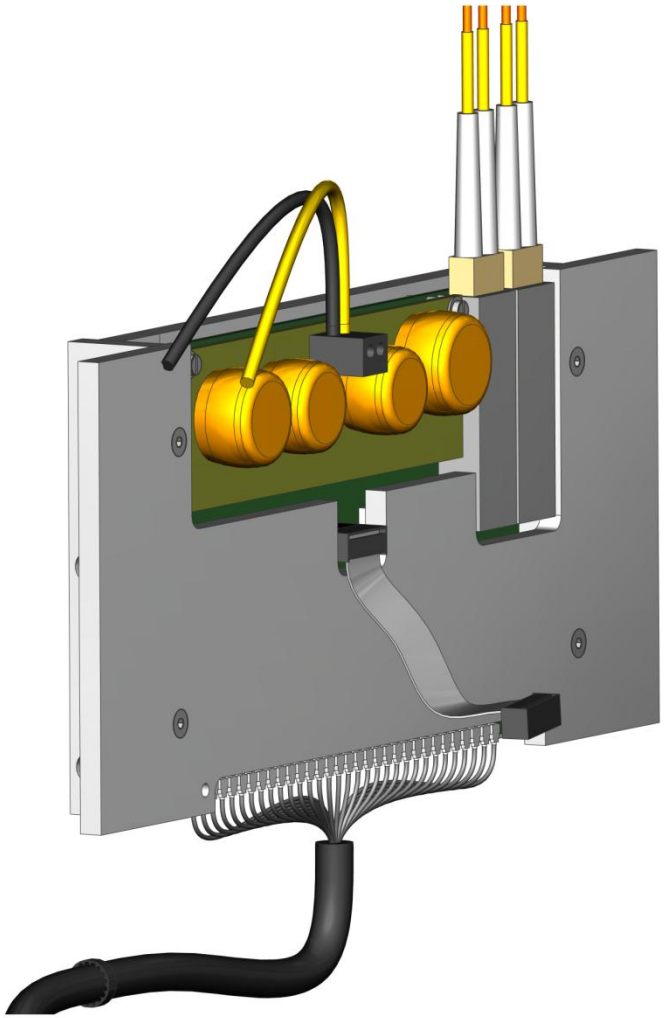
- Encapsulation and Cooling



Courtesy KVI

ADC for EMC-Endcap

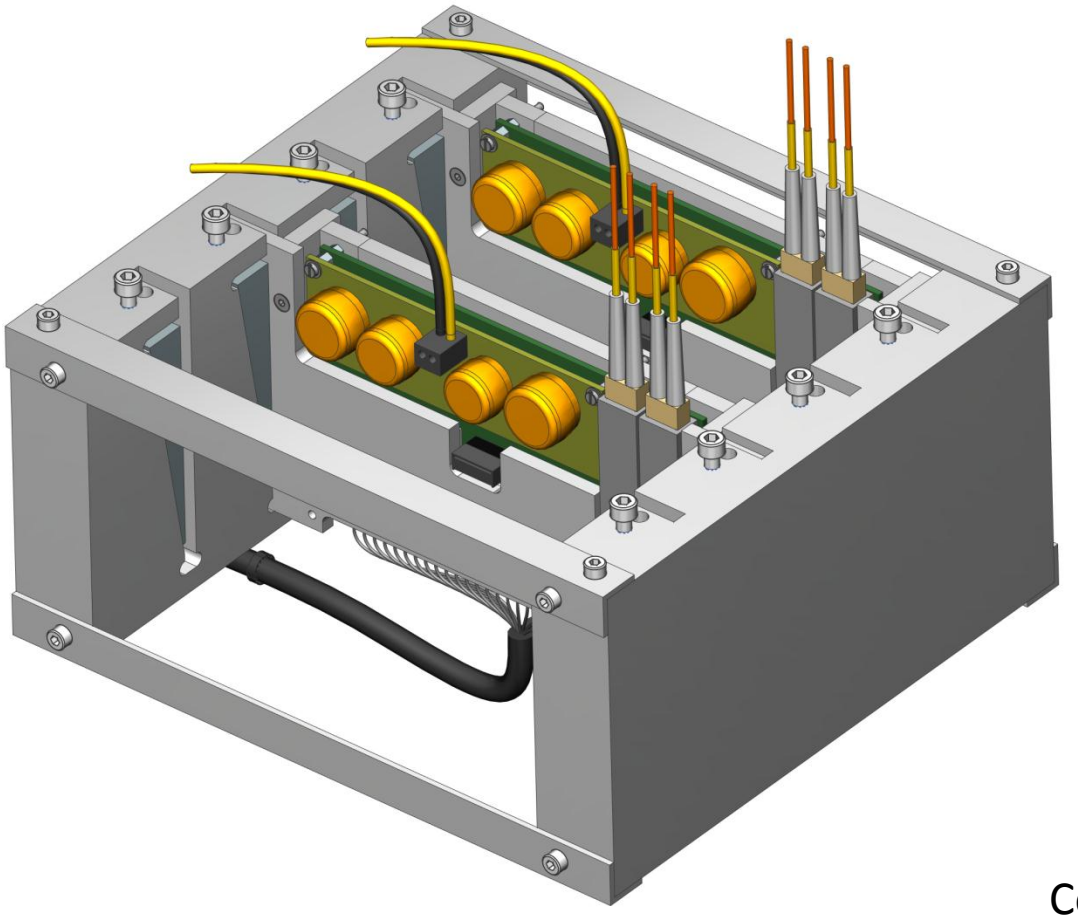
- Encapsulation and Cooling



Courtesy KVI

ADC for EMC-Endcap

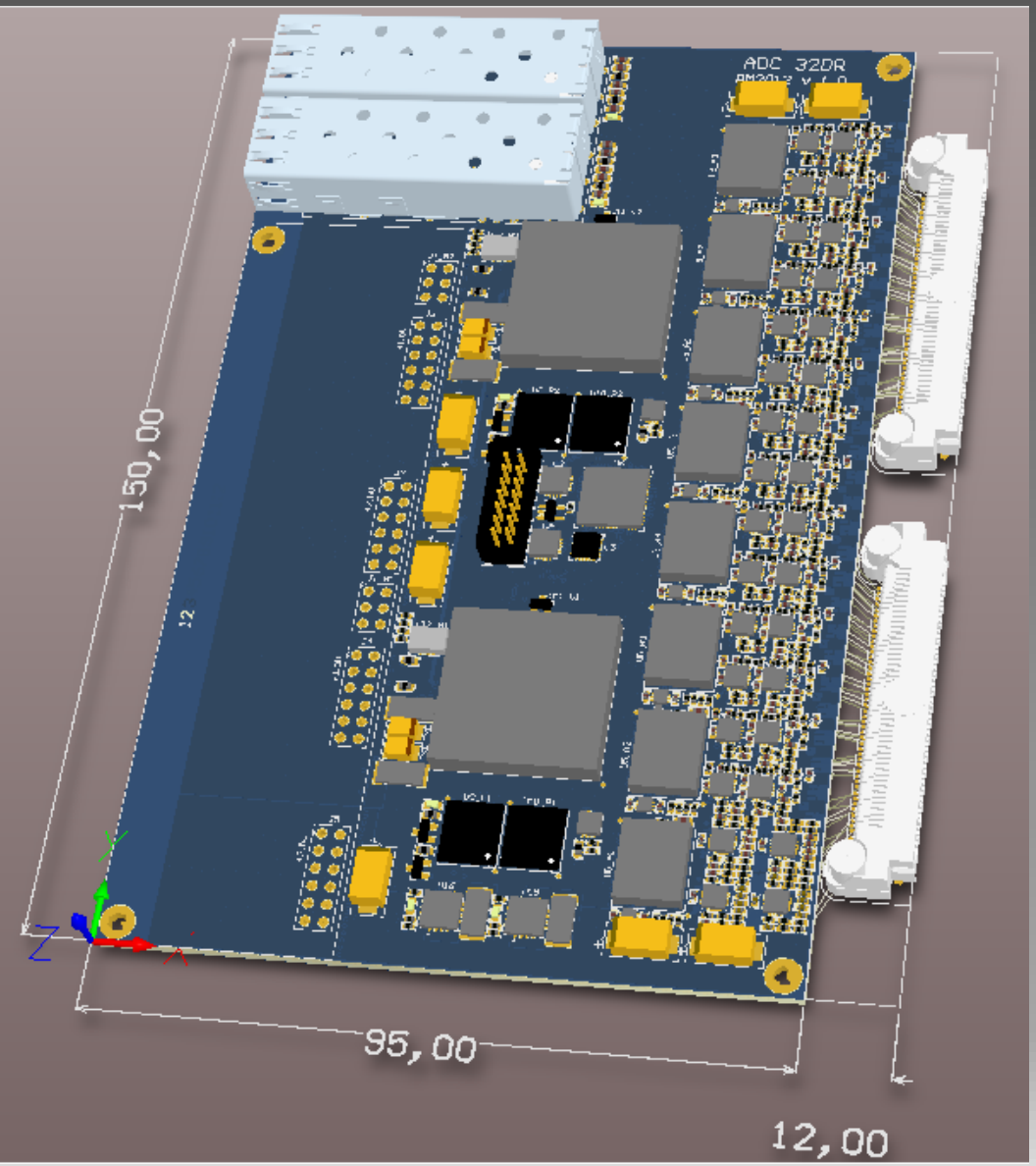
- Encapsulation and Cooling



Courtesy KVI

ADC for EMC-Endcap

- Development - Time plan



V1.1 – June 2013

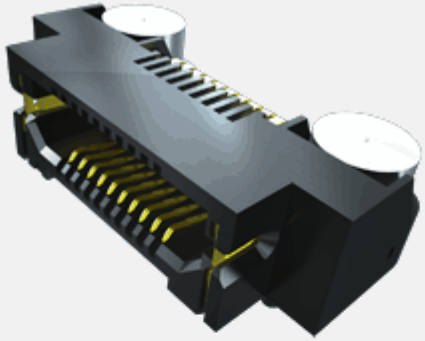
* Design clean-up
* 64 – channels with individual gain and filter settings.
  ”Basel” preamp configuration –
  32-ch. with gain G = 0.2
  (currently G = 1)
  32-ch. with gain G = 2
  (currently G = 16)
* Block connectors –
  Samtec ERF8-049-XX-X-D-RA
  (currently uFL)

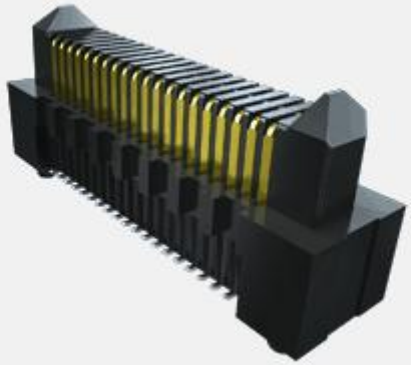
V2.0 – December 2013

* Low-power symmetrizng op-amps
  ADA4940-2
  (currently LTC6403)
* Kintex-7
  (currently Virtex-6)

- Connections

Backplane solution



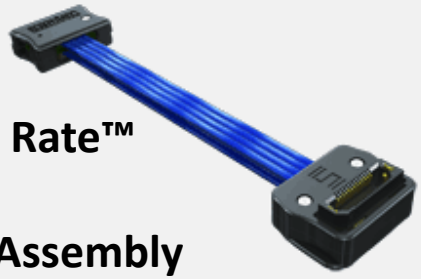


ERM8

Direct cable connection solution

ERDP

0,80 mm Edge Rate™
High Speed
Twinax Cable Assembly



ERCD

0,80 mm Edge Rate™
High Speed
Coax Cable Assembly

Thank You !

Special thanks to Frans Schreuder, Peter Schakel