The **G**SI **E**vent Driven **T**DC **GET4**

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GSI - EE - ASIC-Design

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Outline

Motivation

There are FPGA-TDCs with very high resolution. Why designing a TDC-ASIC?

- FPGA-Designer claim faster and more easy designs but efforts in manpower and expertise have to be studied in detail
- Very small devices fit close to the detector
- Reduction of costs
  - Cheaper devices
  - Lower requirements on PCB layout, 4 layers are fine
  - Less needed infrastructure: Number of power domains etc...
  - Digitising close to the detector typically reduces number of needed connectors
- Radiation hardness
- Power consumption
- Integration of analogue front end possible

Requirements

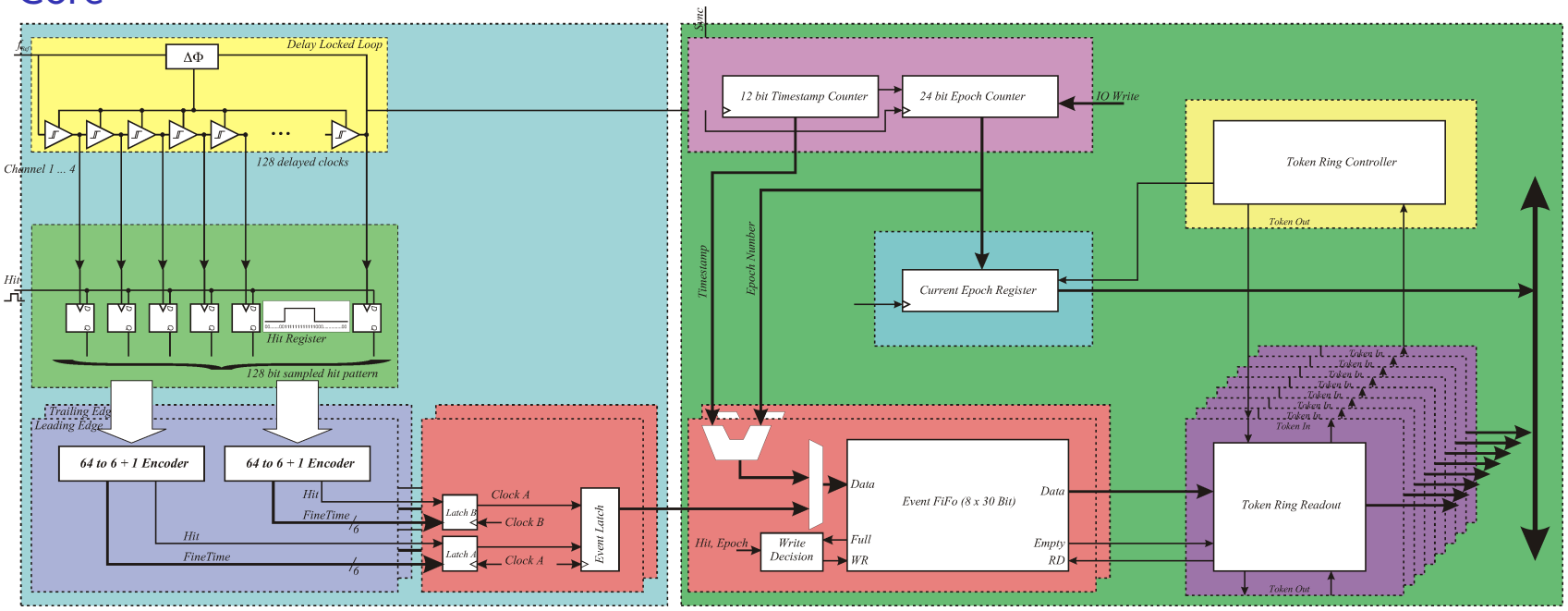
Development is driven by CBM time of flight detector

Parameter		
time resolution	≤ 25	ps
double hit resolution	≤ 5	ns
channel event rate	100	kHz
time over threshold measurement	≤ 1	ns
power consumption	≤ 30	mW/Ch
number of channels	65000	

- Trigger-less / Event driven read out!

The GET4 ASIC

TDC Core



- 128 phase shifted clock signals by a delay locked loop $\Rightarrow$ 50 ps binning
- 128 bit hit register encoded by 2 64 bit encoder $\Rightarrow$ 1 event / 3.2 ns
- Separate encoders for leading and trailing edge
- Synchronised time stamp and epoch counter
- Derandomisation FIFO with 8 words depth

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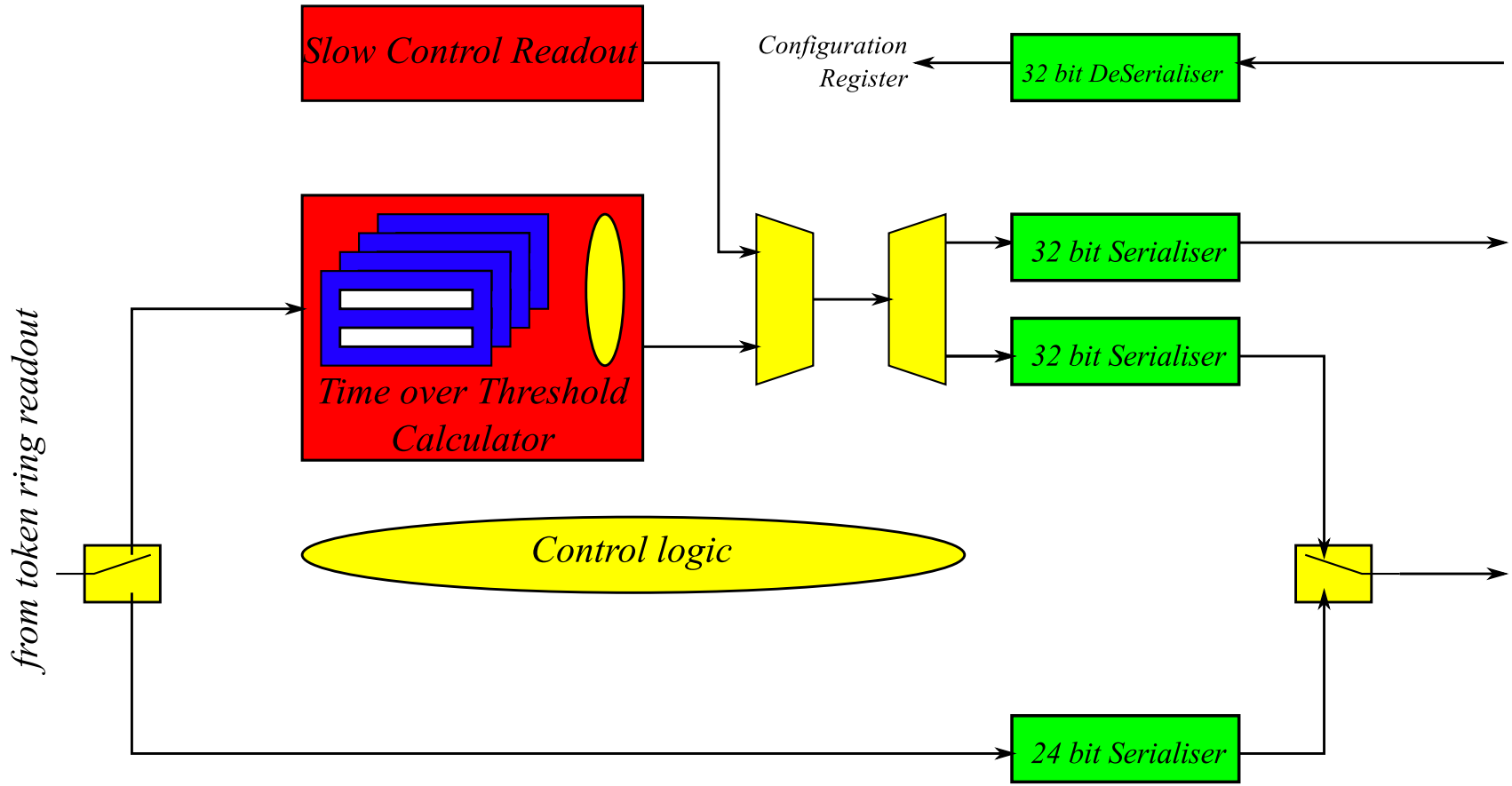
TDC Readout



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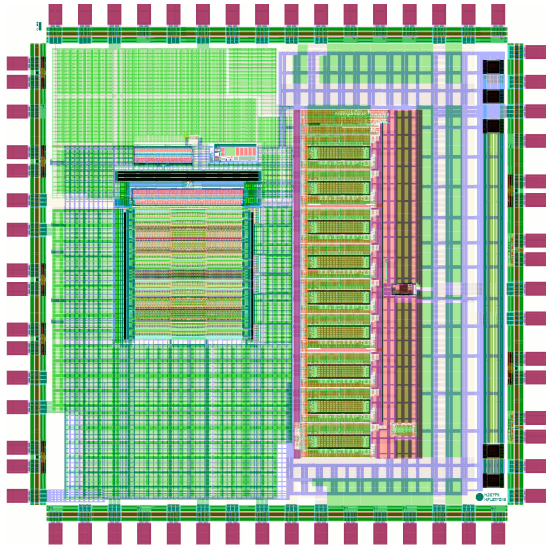
Additional Features

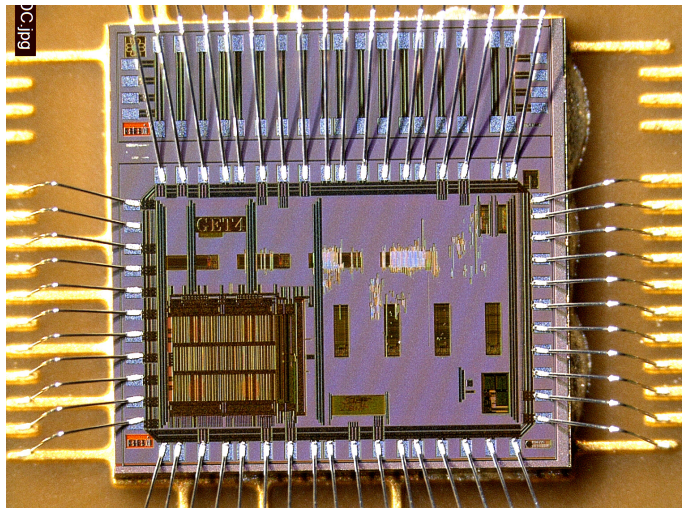
- SPI Master interface
  - Programming of threshold DAC in front end
- Test pattern generator
  - Asynchronous test patterns by free running ring oscillator
  - Independent test pattern for each channel
  - Test pattern length: 24 samples
- Pulse counter and dead time counter
- SEU counter (detected errors in hamming protected registers)
- On Chip diagnostics
  - Configurable test outputs for many internal signals (For lab-tests during development)
  - Error messages for various error states
  - Bit error rate test on downstream link

The GET4 ASIC

Prototypes

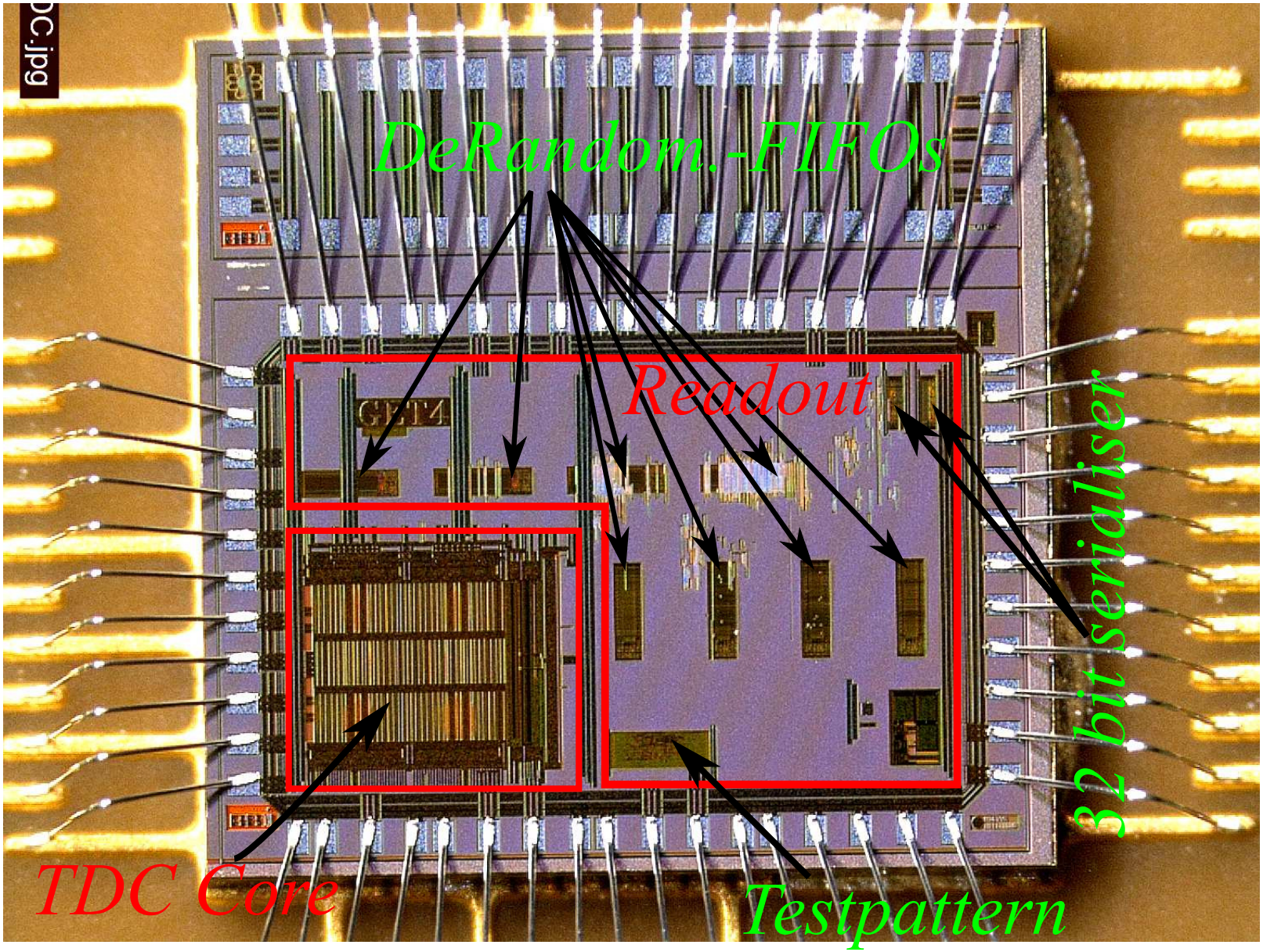
- 2008:
  First Prototype
- 2012:
  First fully equipped prototype
  GET4 V1.00 (subm.: V1.11)
  - UMC 180 nm 1P6M CMOS technology
  - $3240 \times 2260\ \mu\mathrm{m}^2$
  - Power supply: 1.8V core, 3.3V IO
- 2013:
  Bug-fixed version GET4 V1.20





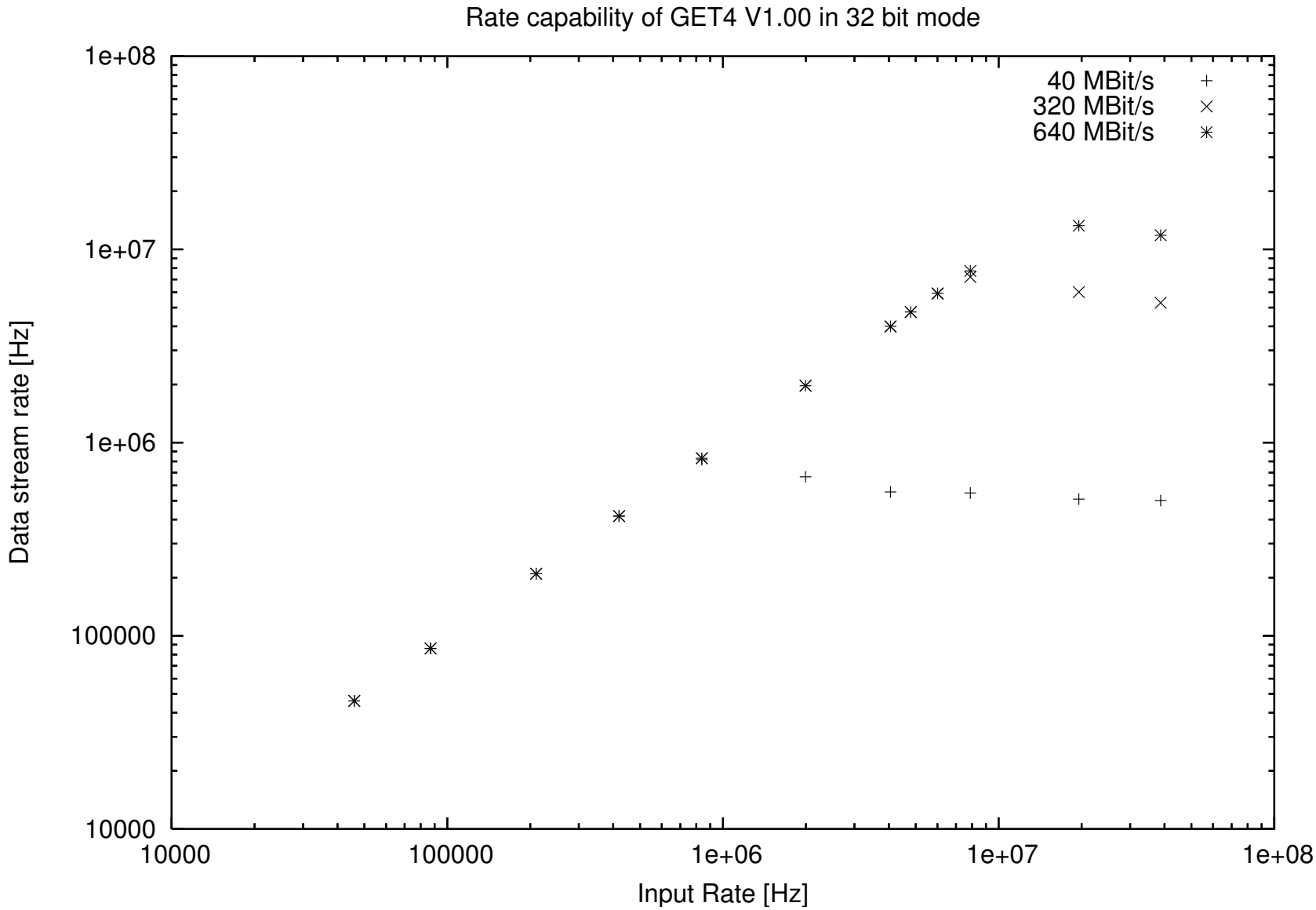
The GET4 ASIC

Prototypes



Performance

Rate capability 32 bit read out mode



Simulation with Poisson distributed stimulus.

Performance

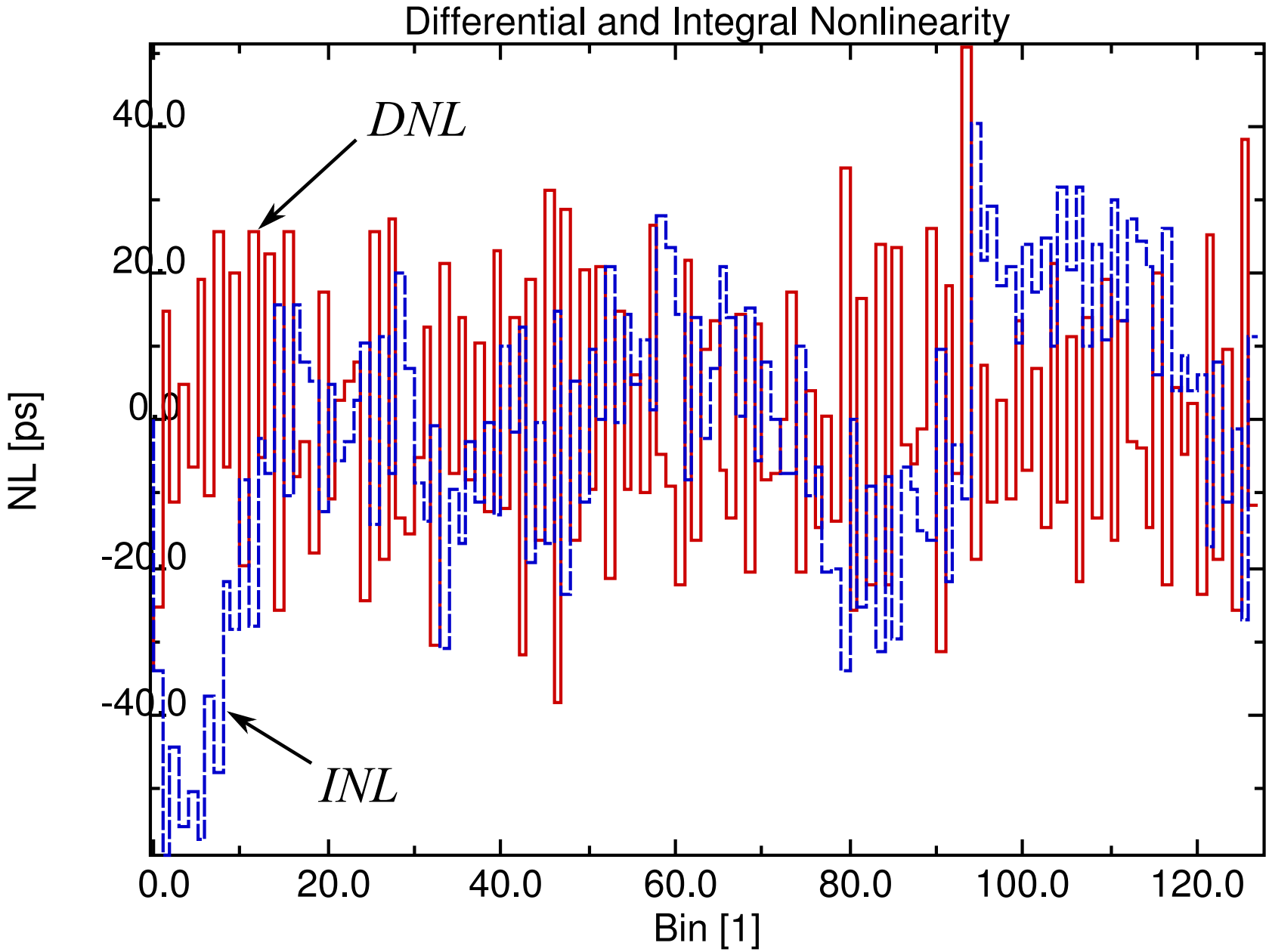
Rate capability: Comparison

data rate	max. event rate			
	24 bit mode		32 bit mode	
MBit/s	MHz/chip	MHz/ch	MHz/chip	MHz/ch
40	0.661	0.165	0.815	0.204
160	2.774	0.694		
320			7.194	1.799
640			13.284	3.321

Enhancement by 32 bit mode: $\approx 30\%$

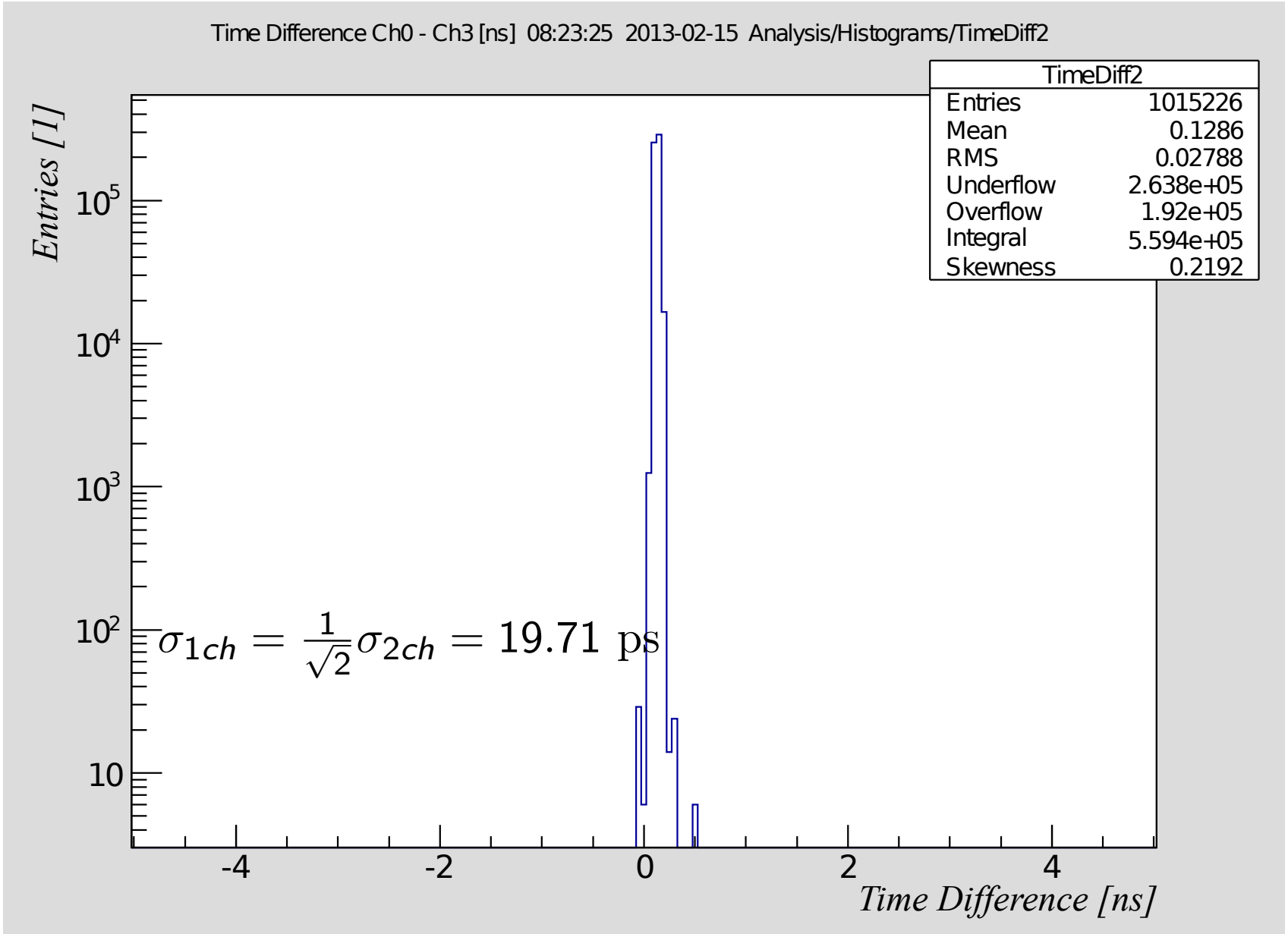
Performance

Linearity



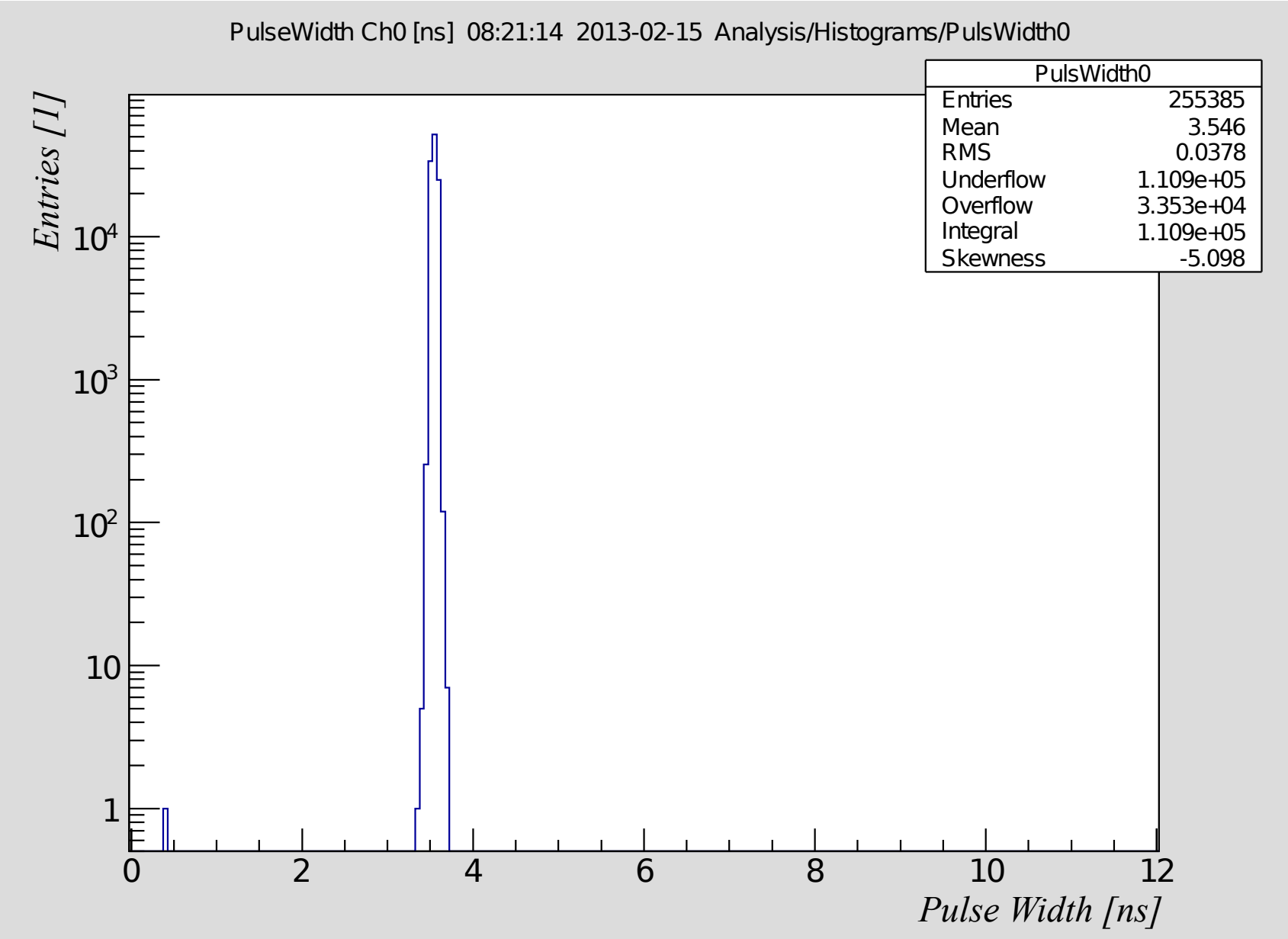
Performance

Times Resolution



Performance

Pulse Width Measurement

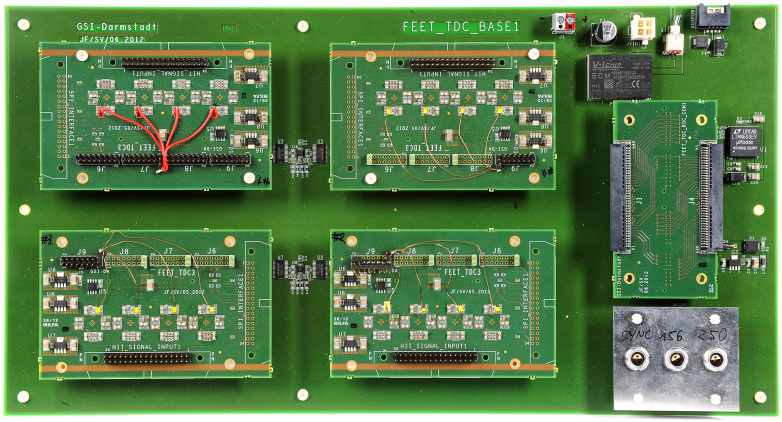


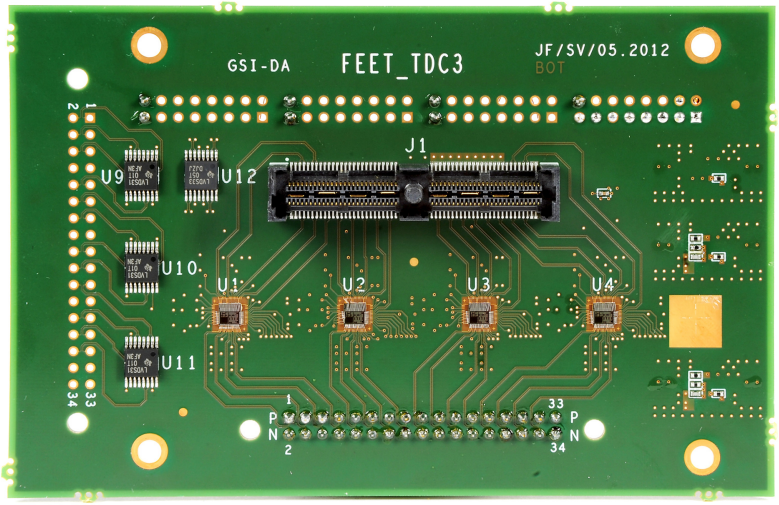
Performance

Summary

- Rate capability: 3.3 MHz / channel or 13.3 MHz / chip
- Burst rate: 320 MHz / channel
- Time resolution: $\leq$ 20 ps
- Double hit resolution: $\leq$ 3.2 ns
- Pulse width measurement: Pulses $\leq$ 1 ns have been seen!
- Power consumption: $\approx$ 27 mW/ch

Setup for Evaluation and Test





- For detector tests a TDC front end board was developed
  - Main board for four piggy boards
  - Each piggy board carries four GET4 TDC ASICs
  - $\Rightarrow$ 16 channels / Piggy board, 64 channels / main board
  - Successfully used in beam time with RPC detectors in Oct/2012

  Readout with SYSCORE V2 board developed at Heidelberg
  - Limited availability
  - Very CBM specific back end (CBMnet)
- $\Rightarrow$ Current discussion: Using TRB3 for readout

Outlook

- A set of minor bugs was found in GET4 V1.11
  $\Rightarrow$ Bug-fixed version V1.20 submitted in Feb. 2013
- SEU-test with protons is planned for June at COSY
- Next beam tests with detector:
  - End of 2013 at COSY
  - Early 2014 at GSI
- Future plans
  - Read out controller ASIC for daisy chain read out of many GET4 ASICs
    $\Rightarrow$ Reducing number of needed connections
  - Integration of PADI- preamplifier and discriminator and GET4 on same Chip