# Status of the HitDetection ASIC

Holger Flemming,Sven Löchner, Peter Wieczorek, Harald Deppe
GSI - EE - ASIC-Design

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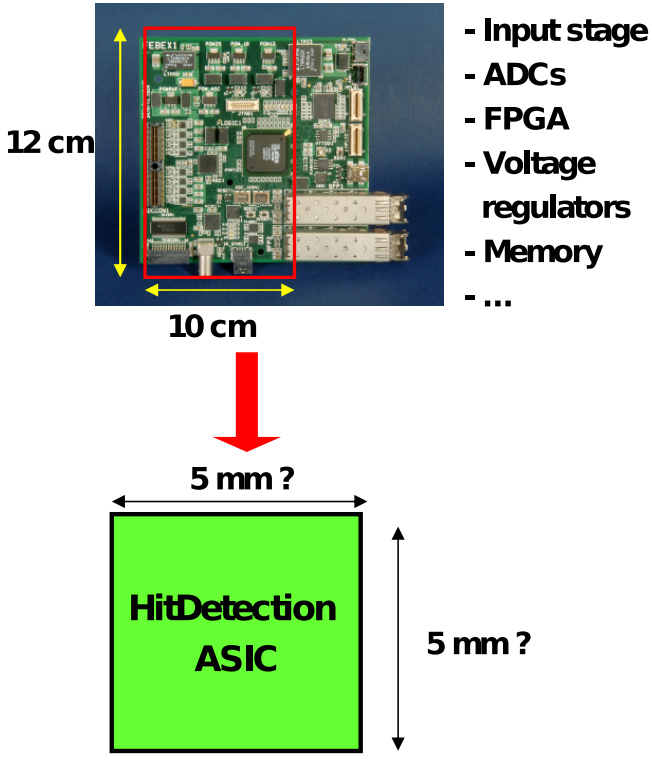
# Outline

# Motivation

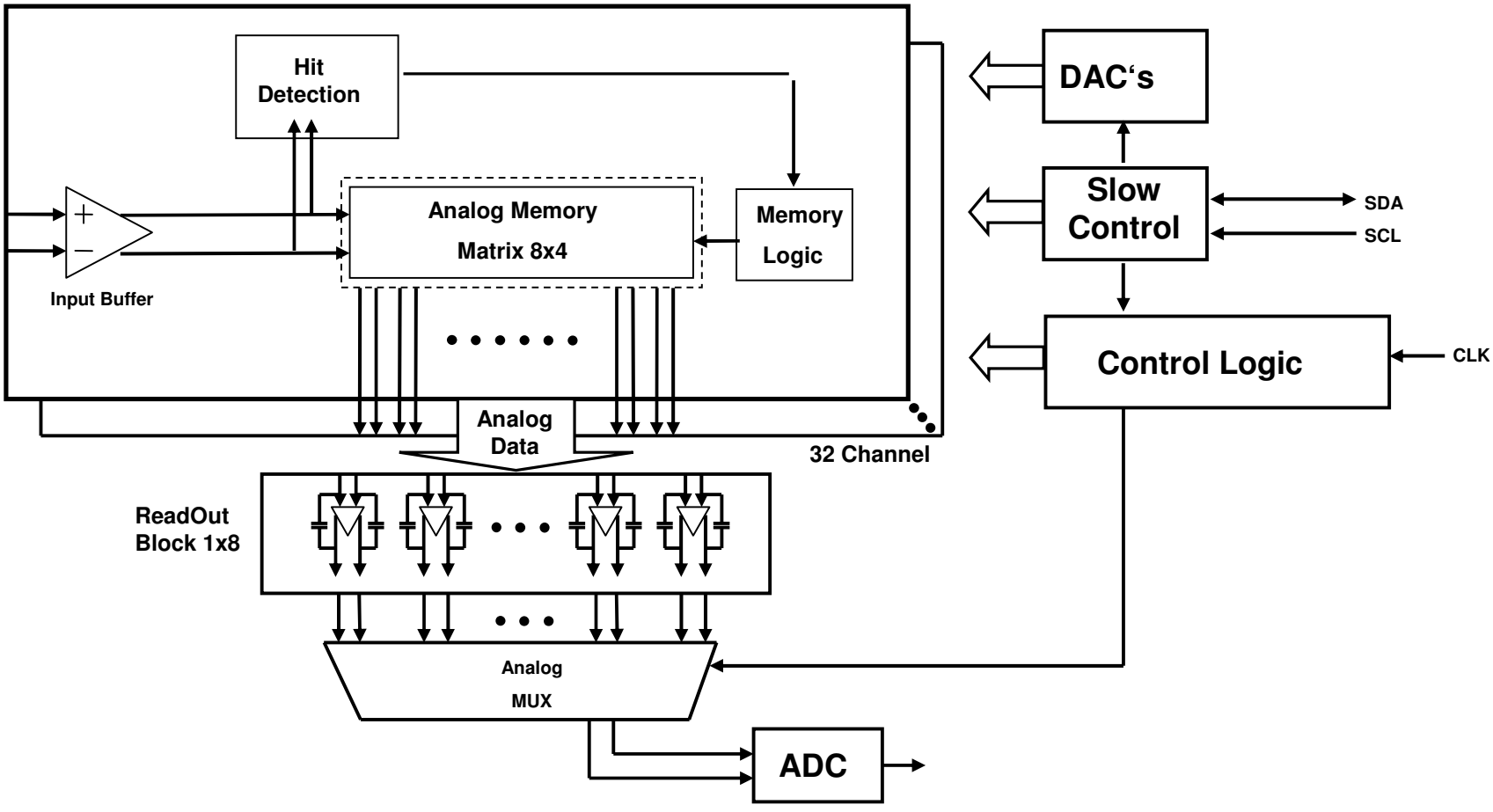
- Concept of HitDetection ASIC by Igor Konorov
- Multi purpose transient recorder ASIC
- Less external components
  - Higher reliability
  - Lower power consumption
  - Lower number of supply voltages
  - Cost reduction
- Radiation tolerance



# Requirements

- Sampling rate configurable up to 100 MS/s
- Dynamic range $\leq 1000$
- Differential inputs
  - Input range: $\pm 1$ V
  - Good common mode reduction over large range
- Event rate $> 100$ kHz/ch
- Configurable number of samples / hit
- Self triggered operation

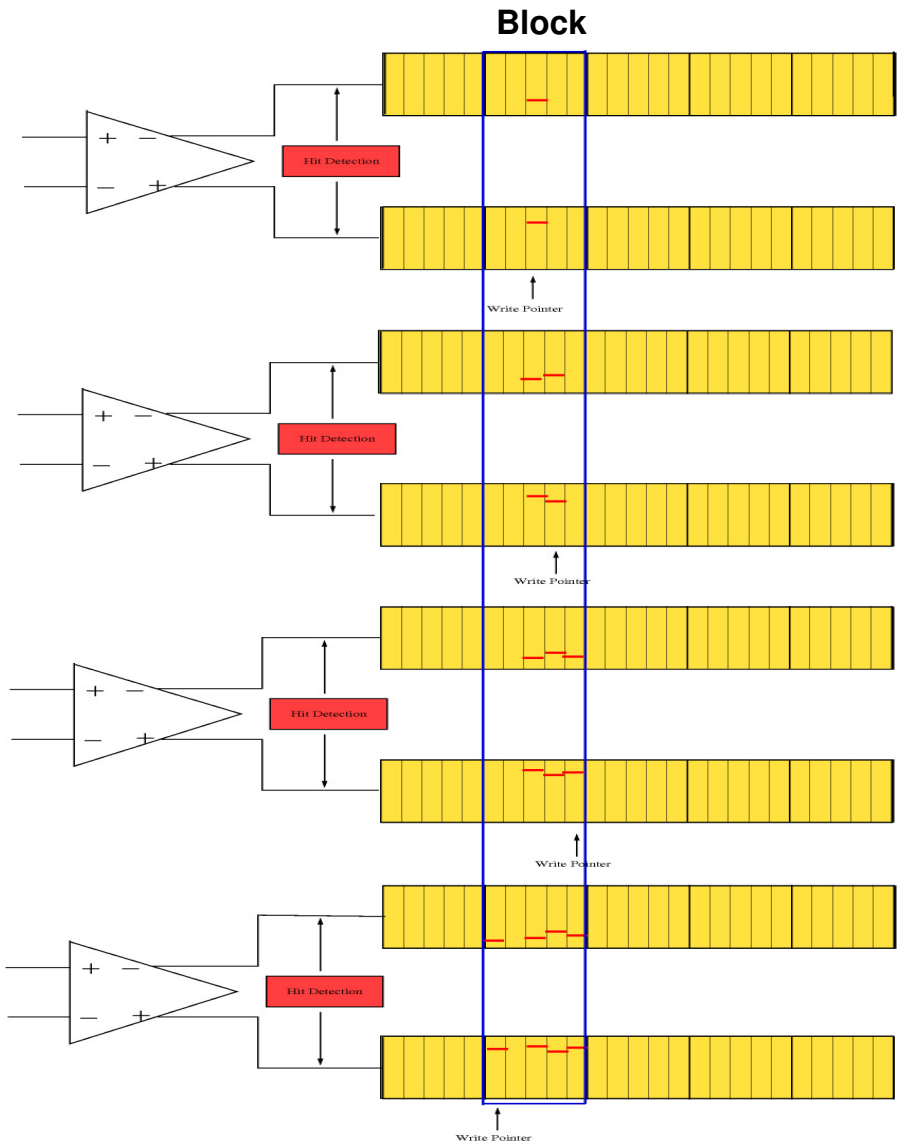
# Concept


Hit
Detection
Analog Memory
Matrix 8x4
Memory
Logic
Input Buffer
Analog
Data
32 Channel
ReadOut
Block 1x8
Analog
MUX
ADC
DAC‘s
Slow
Control
SDA
SCL
Control Logic
CLK

# Concept

## Analogue Signal Storage and Derandomisation

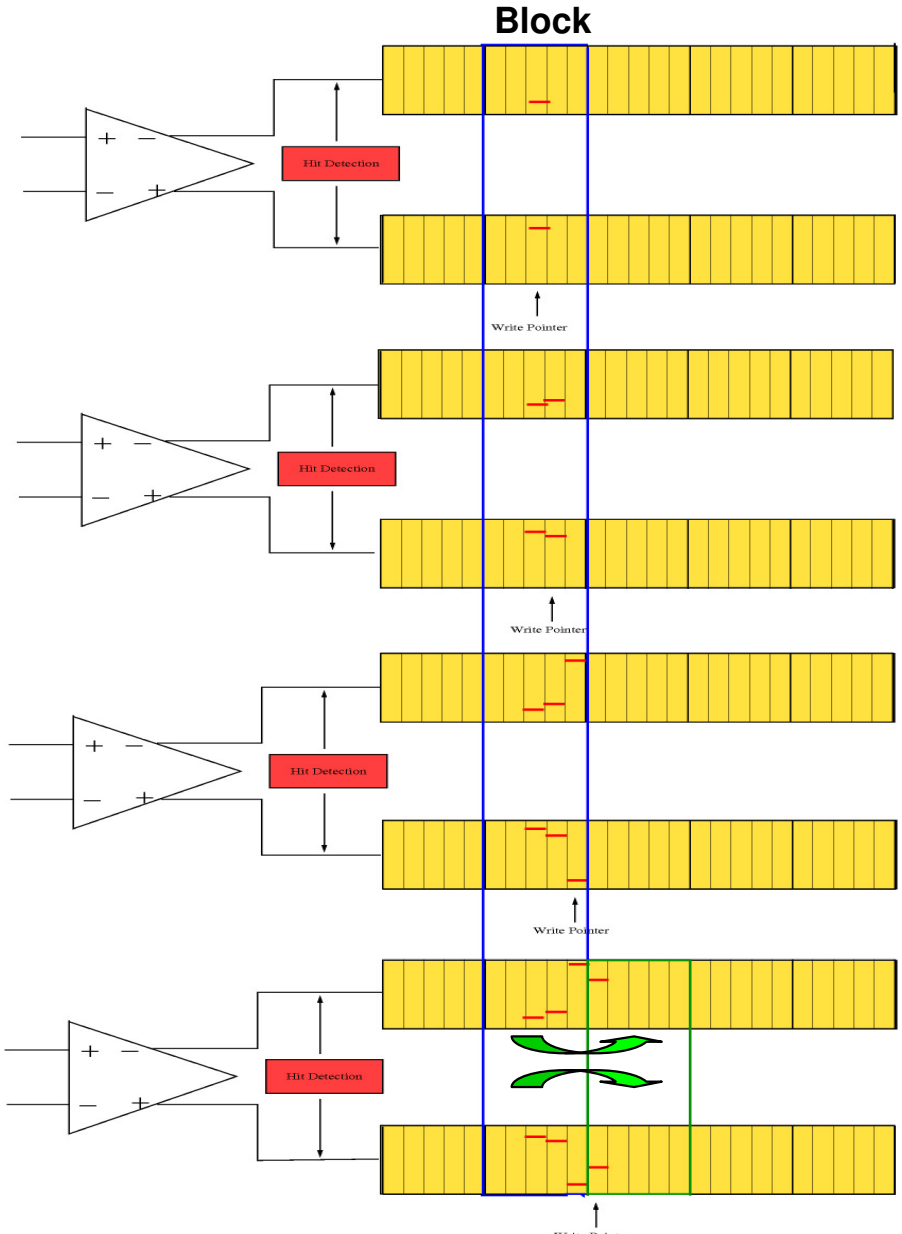
- Capacitor array used as analogue memeory
- Analogue memory is divided into blocks with configurable size
- Signals from input receiver are sampled and stored at position of write pointer
- Write pointer circles inside of one block



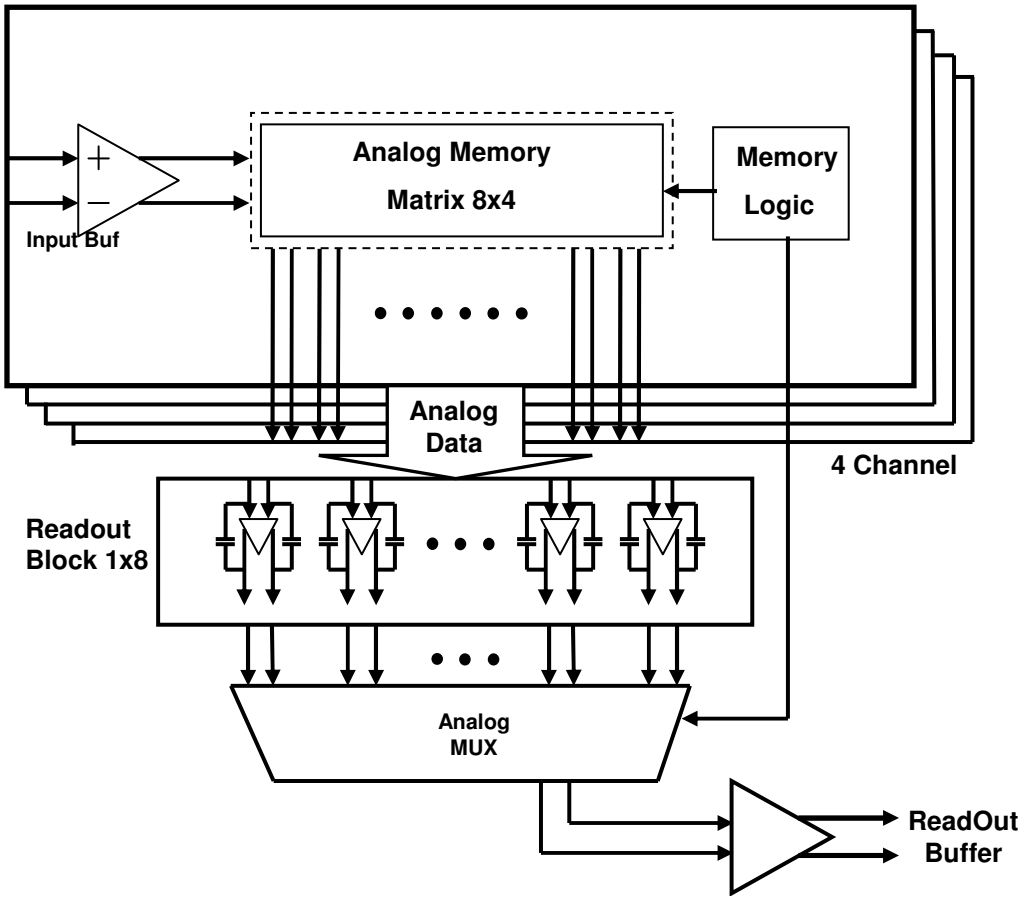
# Concept

## Analogue Signal Storage and Derandomisation

- Signals from particle energy deposits are detected by the hit detection unit
- Write pointer switches to the next memory block
- Signal transient is stored in previous block
- Analogue readout when shared ADC is available
- Block is avialbale again for signal storage



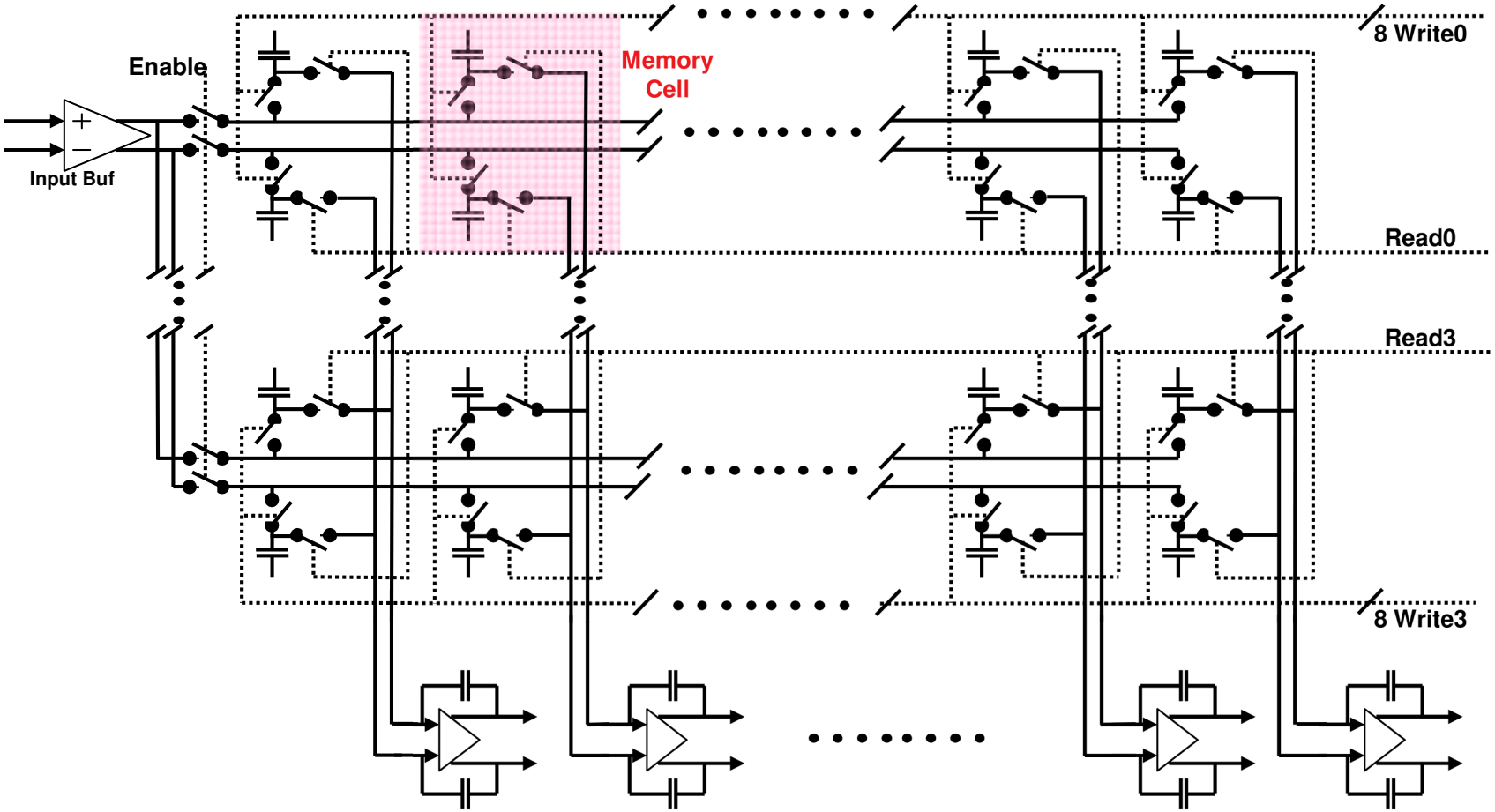
# First Testchip: HitDetMEM1.0




- HitDetMEM 1.0 includes:
  - Differential input buffers
  - External trigger
  - Analogue memory
  - Differential integrator
  - Analogue output multiplexer
- UMC 180 nm CMOS
- Chip size: $3240 \times 1525\ \mu\mathrm{m}^2$

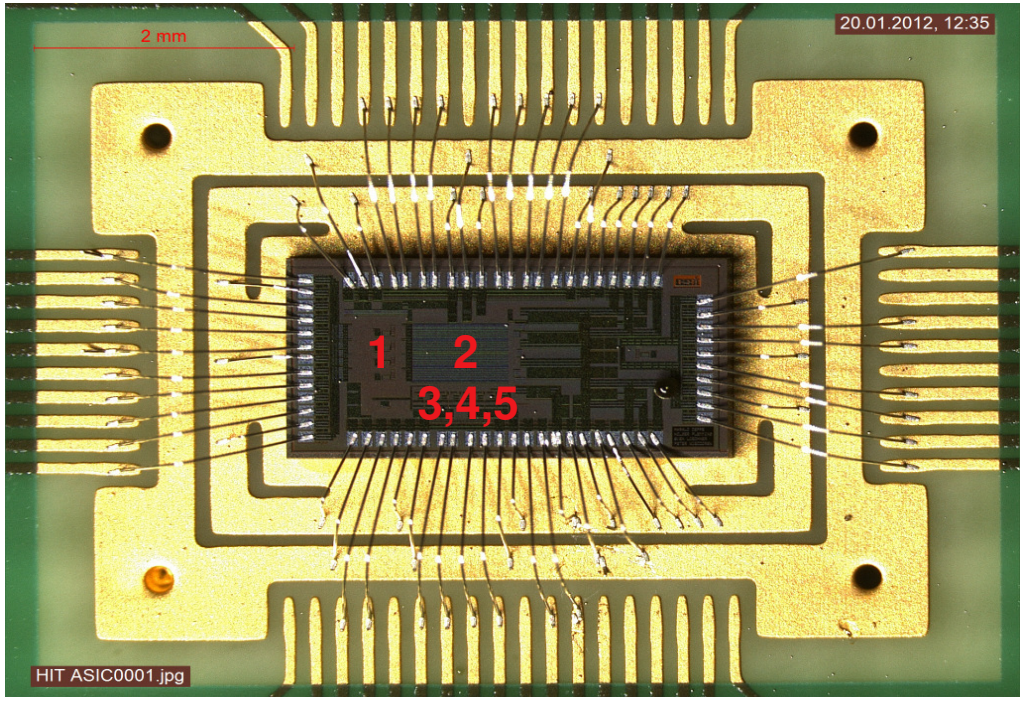
# First Testchip: HitDetMEM1.0

## Channel Memory Matrix



# First Testchip: HitDetMEM1.0

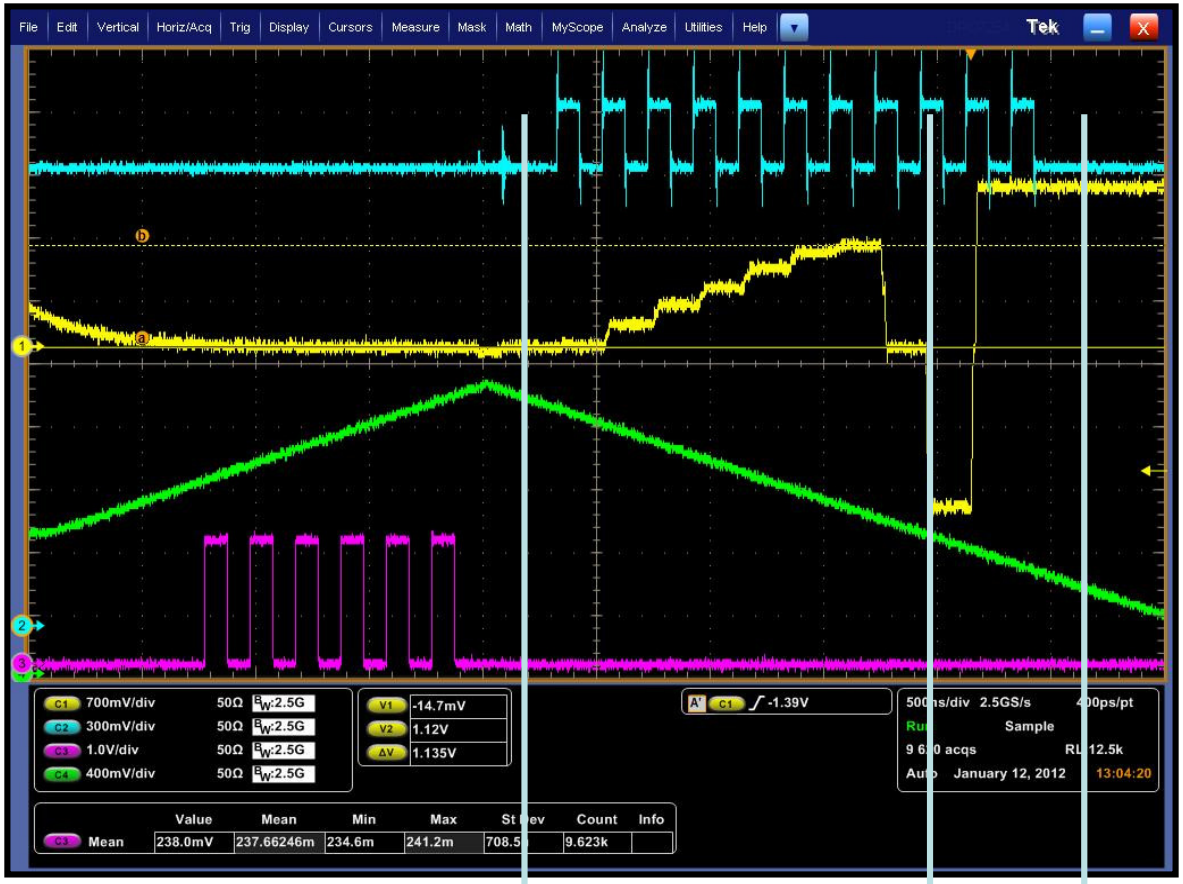
## Functional Tests




1. Differential input buffer ⇒ works
2. Analogue memory ⇒ works
3. Differential integrator ⇒ works
4. Analogue multiplexer ⇒ works with limitations
5. Output buffer ⇒ works

# First Testchip: HitDetMEM1.0

## Functional Tests




**MuxClk (blue)**

**Analog out (yellow)**

**Input (+) ramp (green)**

**S – Clk (violet)**

**Analog data** **Digital**

# First Testchip: HitDetMEM1.0

## Summary of Test Results

- Input stage needs improvement in speed
- Sampling rate of 100 MS/s is obtained
- Quantitative measurements of noise not possible due to improper power connection of analogue multiplexer

$\Rightarrow$ Second test chip HitDetMEM2.0

- Four different improved input stages
- Power connection of analogue multiplexer

# Outlook

- HitDetMem2.0 was submitted Oct 2012 and is currently under test
- Very critical part: Hit detection unit
  - Should be able to detect hits in pile-up-situation
  - $\Rightarrow$ needs a differentiating characteristics
- 12 bit pipeline ADC under development
- First full HitDetection ASIC prototype planned for end of 2013 / early 2014