PANDA MDC Review Meeting
11/12/2024 *GSI*

Review of MDC - ASIC

Michele Caselle, Francesca Lenta, Gianni Mazza, Giulio Dellacasa and Olena Manzhura

on behalf of PANDA-MVD Collaboration

JINST Paper accepted

Authors: M. Caselle, O. Manzhura, D. Calvo, G. Dellacasa, S. Chilingaryan, F. Cossio, A. Kopmann, F. Lenta, G. Mazza, M. Peter, V. Sidorenko, T. Stockmanns, N. Tröll, K. L. Unger, H.-G. Zaunick and J. Becker and K.-T. Brinkmann

Title: Performance of the DAQ system of the PANDA Micro-Vertex Detector

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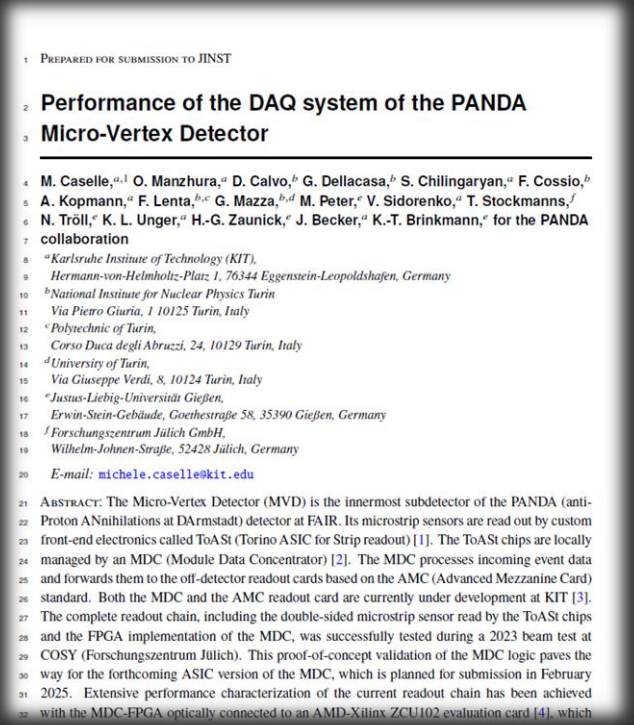

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Performance of the DAQ system of the PANDA Micro-Vertex Detector

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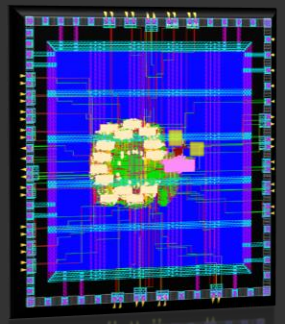
Abstract: The Micro-Vertex Detector (MVD) is the innermost subdetector of the PANDA (anti-Proton ANnihilations at DArmstadt) detector at FAIR. Its microstrip sensors are read out by custom front-end electronics called ToASt (Torino ASIC for Strip readout) [1]. The ToASt chips are locally managed by an MDC (Module Data Concentrator) [2]. The MDC processes incoming event data and forwards them to the off-detector readout cards based on the AMC (Advanced Mezzanine Card) standard. Both the MDC and the AMC readout card are currently under development at KIT [3]. The complete readout chain, including the double-sided microstrip sensor read by the ToASt chips and the FPGA implementation of the MDC, was successfully tested during a 2023 beam test at COSY (Forschungszentrum Jülich). This proof-of-concept validation of the MDC logic paves the way for the forthcoming ASIC version of the MDC, which is planned for submission in February 2025. Extensive performance characterization of the current readout chain has been achieved with the MDC-FPGA optically connected to an AMD-Xilinx ZCU102 evaluation card [4], which

Preamble, funding strategy, planning

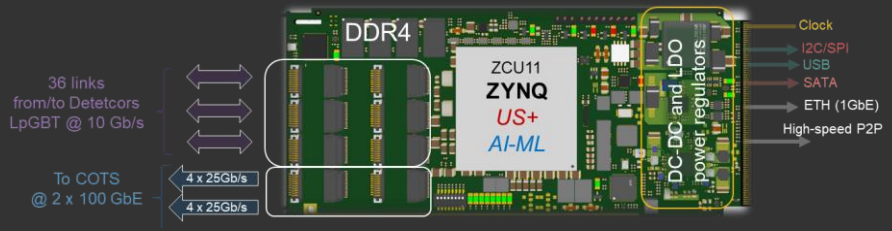
Strategic Vision and Funding Scheme: “GSI-KIT Collaboration"

- The MVD, which will be placed in the innermost detector layer, will provide high resolution tracking for primary interactions and secondary vertices of short-lived particles and delayed decays. To complete the DAQ system of MVD two devices have been developing

- Module Data Concentrator (ASIC)
  - Financed by ***BMBF*** (05P21VKFP1)
  - KIT granted the neutral extension up to Sep. 2025



AMC Data Concentrator Board



- Development of a “common DAQ infrastructure” for current and future GSI experiments
  - Financed by ***GSI*** (80%) and ***KIT*** (20%)

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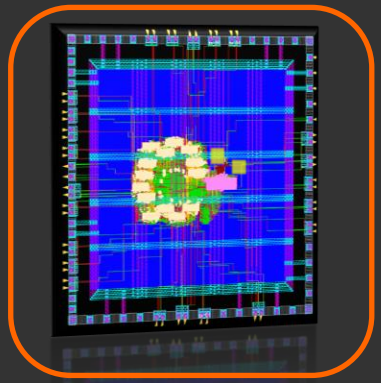
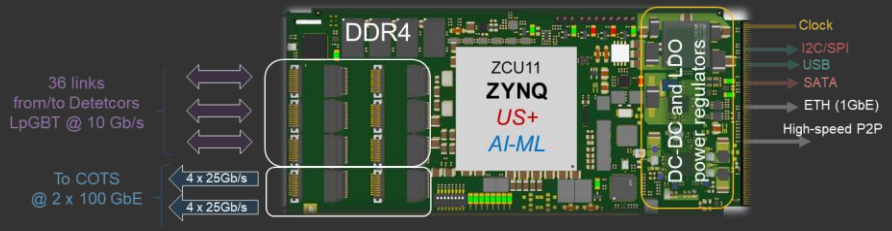


Review

AMC Data Concentrator Board



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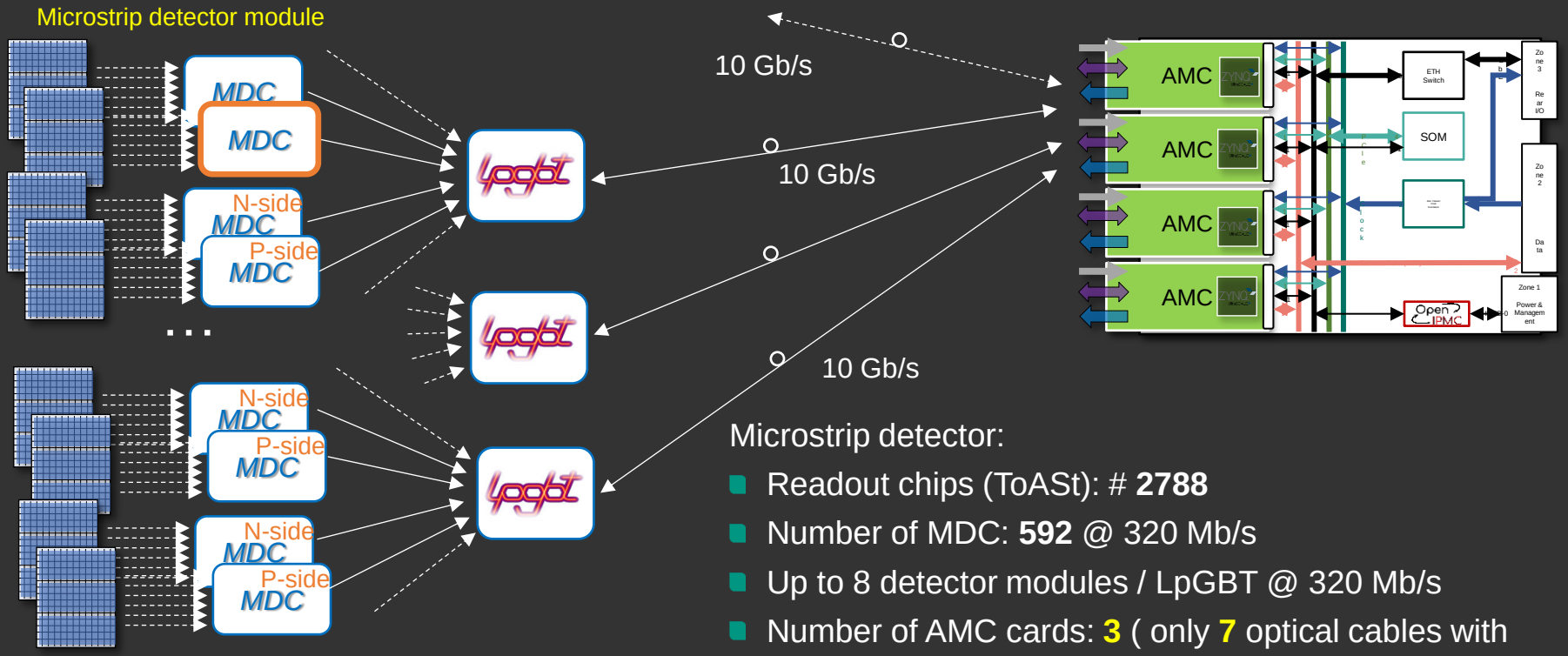
Towards to detector layout simplification

Reduce the number of optical links from/to off-line electronics

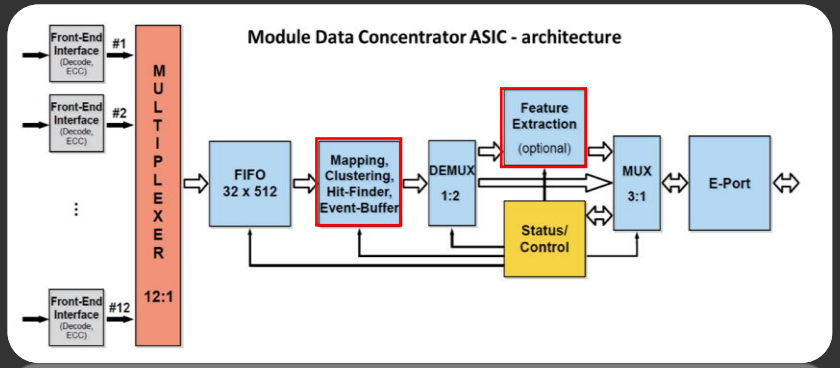


Microstrip detector:

- Readout chips (ToASt): # **2788**
- Number of MDC: **592** @ 320 Mb/s
- Up to 8 detector modules / LpGBT @ 320 Mb/s
- Number of AMC cards: **3** (only **7** optical cables with 12 full-duplex fibers each)
- Number of ATCA carried card: **1**

From TDR to real ASIC

Preliminary work before the ASIC development

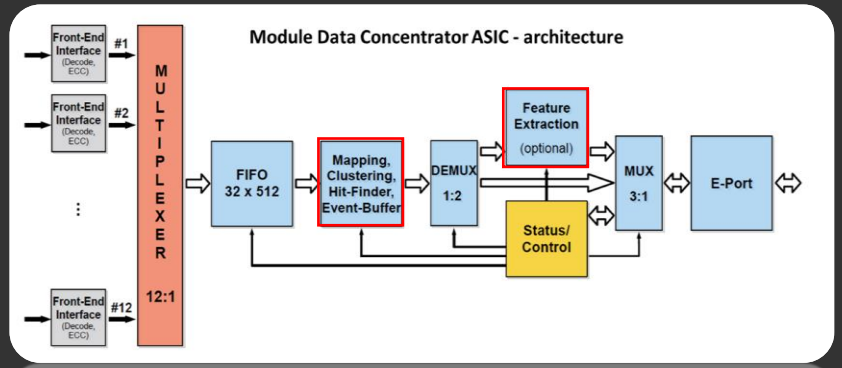


Module Data Concentrator (TDR)

- Up to # 12 channel links from front-end interfaces
- Several data processing had been considered:
  - Mapping cluster, Hit Finder, Feature Extraction
- Large FIFO 32x512
- e-port based on GBTX, one link for data @ 160 Mbps

From TDR to real ASIC

Preliminary work before the ASIC development



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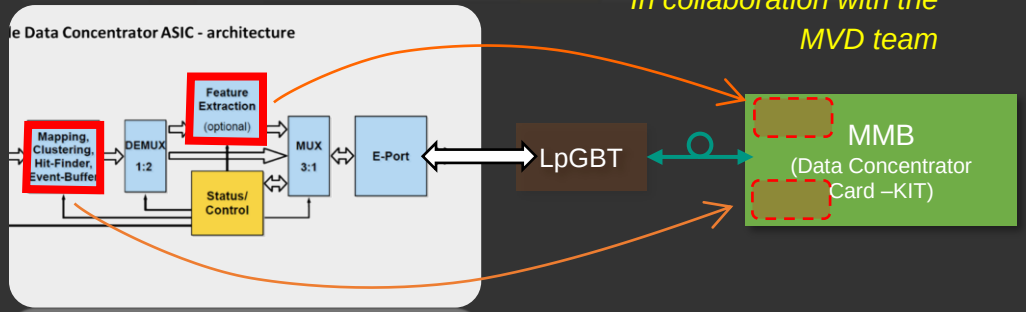


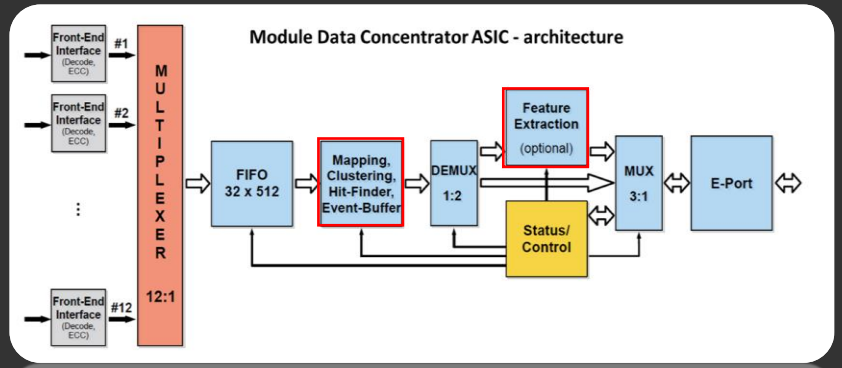
In collaboration with the MVD team

Module Data Concentrator (Current design)

- Moving the data processing to more flexible programmable logic (off-detector), more flexibility and intelligent (ML) data processing on ZYNQ US+
- Reduce the complexity of MDC

From TDR to real ASIC

Preliminary work before the ASIC development



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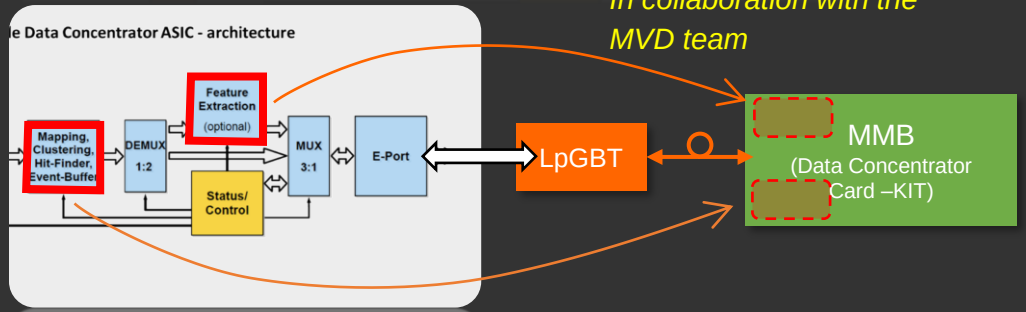


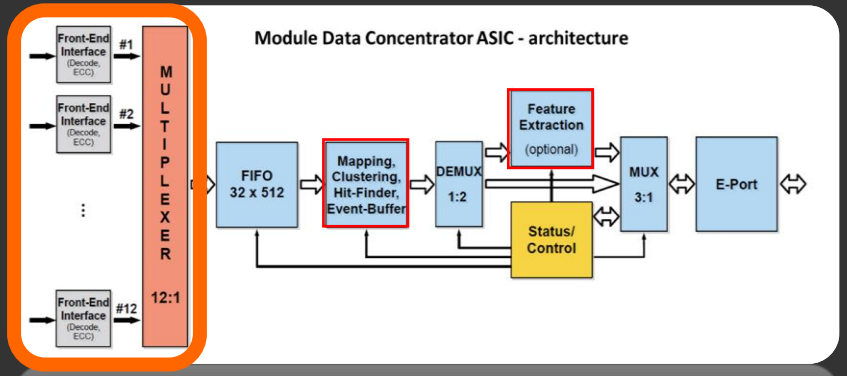
In collaboration with the MVD team

Module Data Concentrator (Current design)

- E-port based on LpGBT, two links operating @ 320 Mbps (total data throughput up to 640 Mbps)
- Reduce main FIFO 32x256 (less logic / area / power)

From TDR to real ASIC

Preliminary work before the ASIC development



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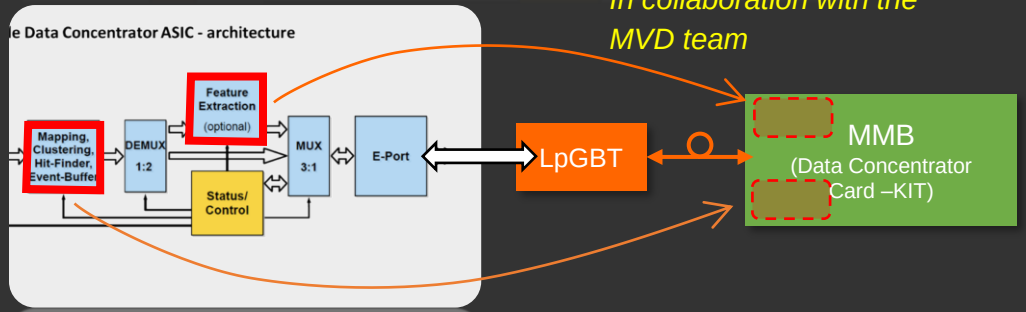


In collaboration with the MVD team

Module Data Concentrator (Current design)

- Increasing the number of input channels up to 16 links. Technically driven and highly advantageous, as it broadens the potential applications of the PANDA microstrip detector across various experiments

Data Concentrator - Requirements

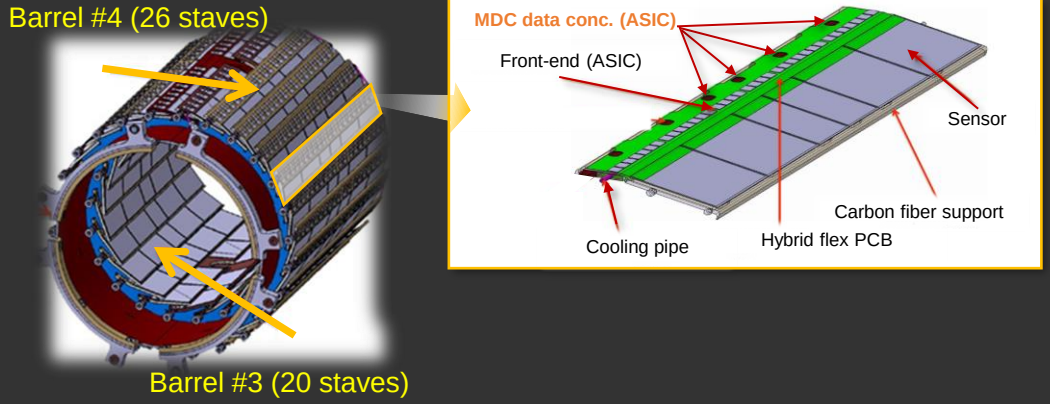
Low-power, small-area, rad-tolerant CMOS ASIC

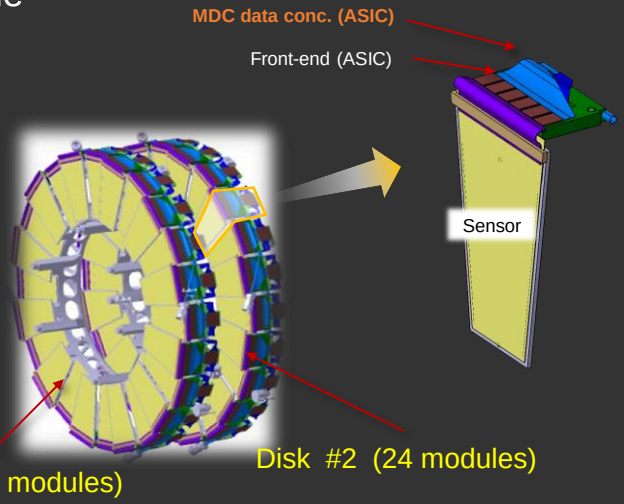
- **High-Speed front-end interface:**
  - Supports auto-detection and data link negotiation
- **Clock and Interface:**
  - Master clock operation at 80/160/320 MHz via LpGBT and e-link-based interface (LpGBT compliant) for seamless integration
- **Robust Design Features:**
  - Triple Modular Redundancy (TMR) logic for enhanced fault tolerance, built-in data consistency checks and command / configuration protection logic for reliable operation
- **Optimized for On-Detector Module:**
  - Designed as a low-power device to accommodate limited cooling resources, and fully integrated solution tailored for on-detector environments.
- **Technology and Production:**
  - Developed in the same CMOS technology as ToASt (UMC 110 nm), fabricated within the same engineering

Silicon Strip Detector

Complex detector modules for both barrel and disk

- **Barrel**
  - # 64 square sensors: 512 x 512 channel
  - # 184 rectangular sensors: 512 x 895 channels
- **Disk**
  - # 48 trapezoidal sensors: 768 channels per side





- ***Strategy***: one MDC version for all detector modules shapes with intelligent power management of no-active link and spares links

MDC vs detector module shapes

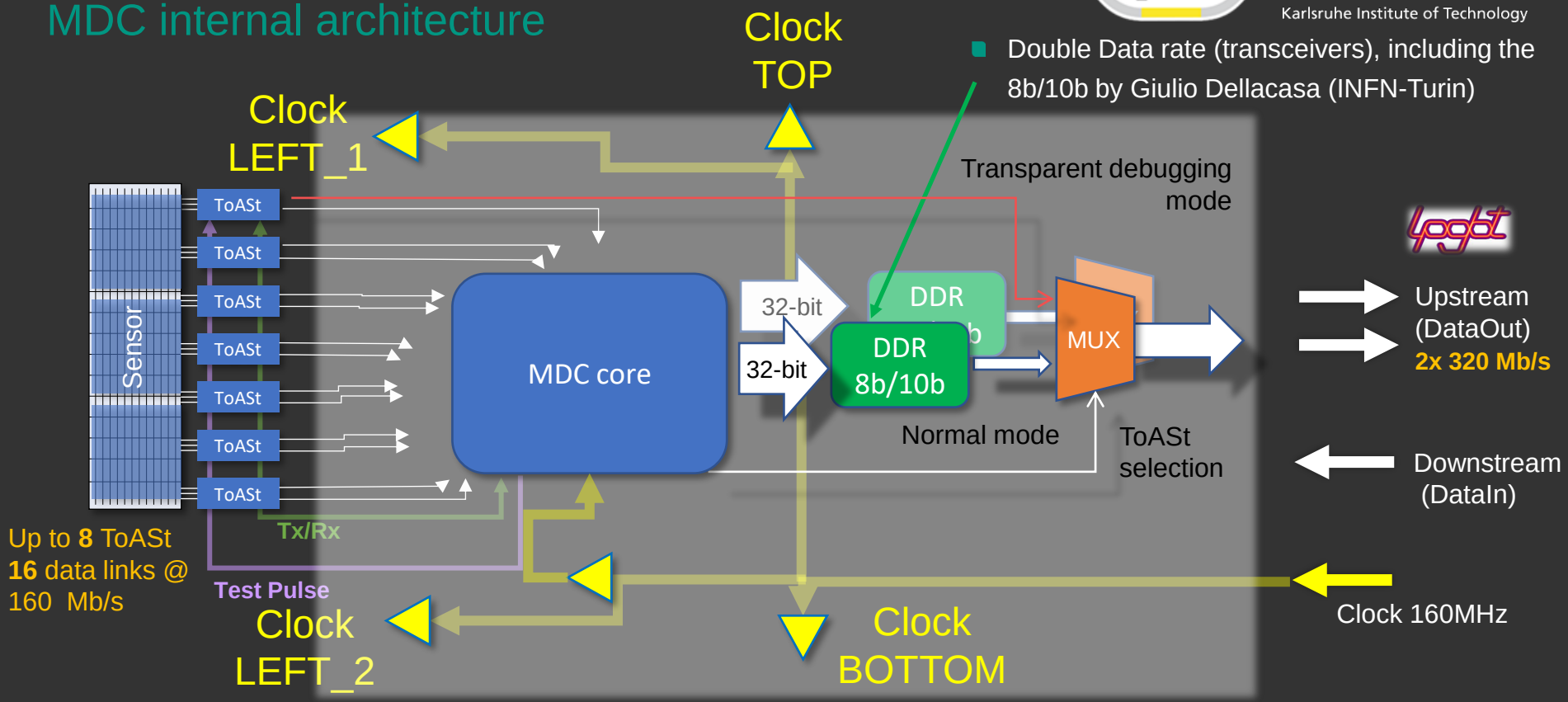
One MDC version for all detector modules shapes

- The strategy is to keep the inactive readout channels as spare links. These can be used in case of physical damage or if additional data throughput is needed due to an increase in local data events.
- The employment of two MDC controllers (one per side) per each detector module

Module Shape	Position	Number of ToASt	#Channels	Occupancy	Additional links
Rectangular	Barrel	7 (p side) + 7 (n-side)	512 x 895	low or moderate	Spares links available (also for high occupancy scenario)
Square	Barrel	4 (p side) + 4 (n-side)	512 x 512	Very high	Several spares' links (per side)
Trapezoidal	Disk	6 (p side) + 6 (n-side)	768 x 768	Very high or moderate	Up to 4 spares links (per side)

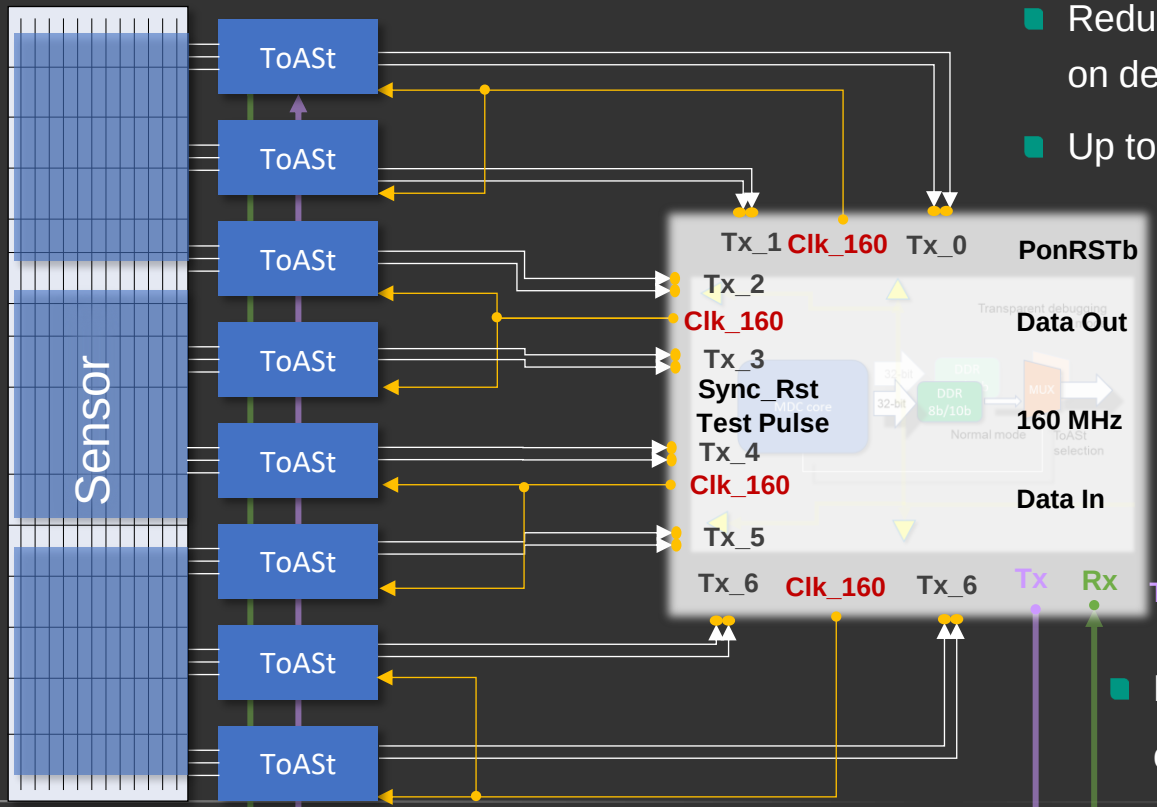
MDC TOP module

MDC internal architecture



MDC (Module data Concentrator)

Floorplan ASIC and connections



- Reduced number of passive components on detector module
- Up to # 4 clock lines for clock distribution

2 x 320 Mb/s
Upstream (DataOut)

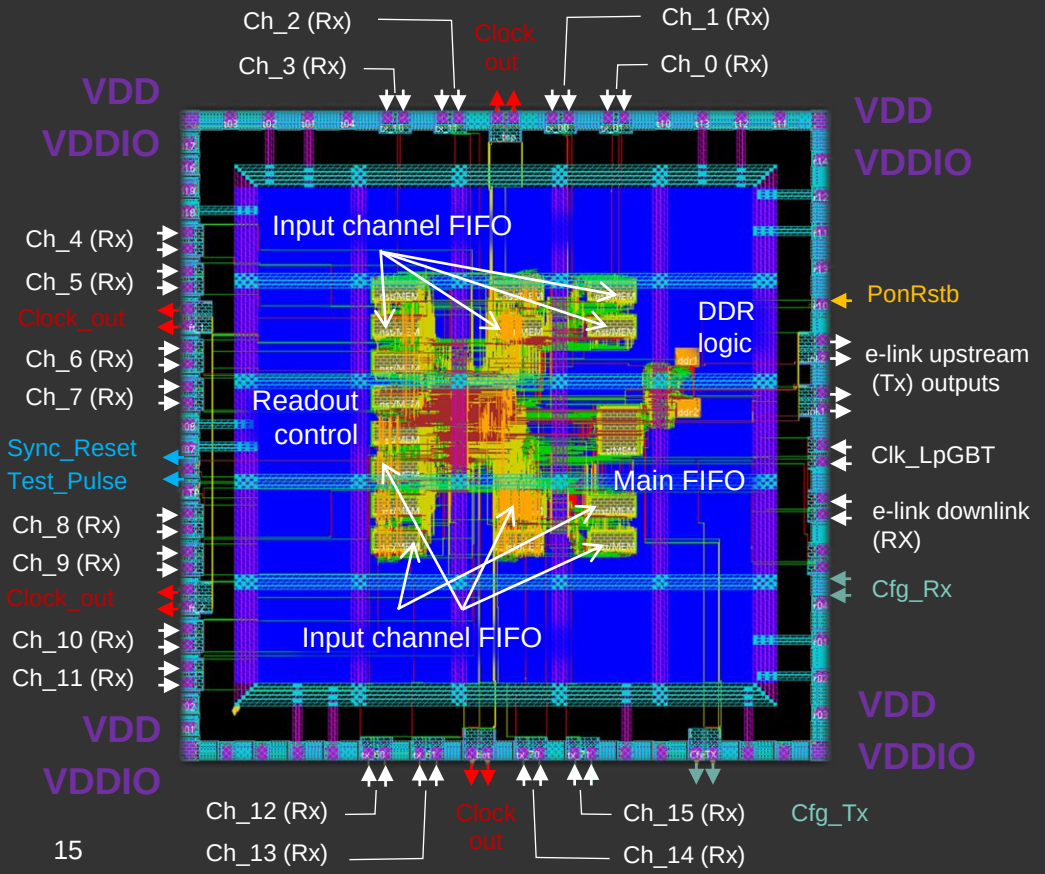
Clock LpGBT

Downstream (DataIn)

- Programmable polarity of differential clock and input pin (P/N) connections

MDC current version

Floorplan ASIC and connections



- Die size of 3.38 x 3.38 mm^2
- Low-power CMOS technology
- Double Data rate (block), including the 8b/10b conversion and fast serializer, capable to operate up to 800 Mb/s
- Estimated power (*preliminary*) of 66 mW at a 333 MHz clock toggle rate @ 1.2V
- Area occupancy < 10 % for the logic

The submission of the ASIC is booked for March (2025) in 110 nm CMOS

Expected occupancy

Detector occupancy on hot region of PANDA / Bandwidth

MVD internal note: https://panda-wiki.gsi.de/pub/Mvd/MvdPublic/PandaMVDnote-004.pdf

Mcps → million counts per second	Barrel part	Forward part	Sensor level	Front-end level	Readout channel
Pixel part					
Digitised hits N_{dig} / [10^6]	$6.7 \mapsto 4.2$ ($1.5 \mapsto 15$) GeV/c	$16.6 \mapsto 32.2$ ($1.5 \mapsto 15$) GeV/c	$\lesssim 0.89$ $\langle \lesssim 0.21 \rangle$	$\lesssim 0.29$ $\langle \lesssim 0.04 \rangle$	$2 \cdot 10^{-4}$ $\langle 3.5 \cdot 10^{-6} \rangle$
Average count rate $\langle \dot{N}_{\mathrm{dig}} \rangle$ / [Mcps]	$233 \mapsto 364$ ($1.5 \mapsto 15$) GeV/c		$\lesssim 8.9$ $\langle \lesssim 2.1 \rangle$	$\lesssim 2.9$ $\langle 0.4 \rangle$	$\lesssim 0.002$
Expected data rate $\langle \dot{N}_{\mathrm{dig}} \rangle \cdot f_{\mathrm{DAQ}}$ / [MB/s]	$\lesssim 2200$		45 $\langle 12 \rangle$	17 $\langle 2 \rangle$	–
Estimated peak rate $\langle \dot{N}_{\mathrm{dig}} \rangle \cdot f_{\mathrm{peak}}$ / [Mcps]	–		–	> 4.0 < 14.5	$\lesssim 0.01$
Strip part					
Digitised hits N_{dig} / [10^6]	$21.1 \mapsto 17.6$ ($1.5 \mapsto 15$) GeV/c	$5.0 \mapsto 8.4$ ($1.5 \mapsto 15$) GeV/c	0.30 $\langle 0.10 \rangle$	0.09 $\langle 0.02 \rangle$	$8 \cdot 10^{-4}$ $\langle 1.5 \cdot 10^{-4} \rangle$
Average count rate $\langle \dot{N}_{\mathrm{dig}} \rangle \cdot f_{\mathrm{r/o}}$ / [Mcps]	$418 \mapsto 416$ ($1.5 \mapsto 15$) GeV/c		4.8 $\langle \lesssim 1.6 \rangle$	1.5 $\langle \lesssim 0.3 \rangle$	$\lesssim 0.013$
Expected data rate $\langle \dot{N}_{\mathrm{dig}} \rangle \cdot f_{\mathrm{r/o}} \cdot f_{\mathrm{DAQ}}$ / [MB/s]	$\lesssim 2500$		29 $\langle 10 \rangle$	9 $\langle 2 \rangle$	–
Estimated peak rate $\langle \dot{N}_{\mathrm{dig}} \rangle \cdot f_{\mathrm{r/o}} \cdot f_{\mathrm{peak}}$ / [Mcps]	–		–	> 2.0 < 5.5	> 0.02 < 0.07

Table 6.3: Main results of the count rate study performed with 2 million DPM events. Average count rates are obtained with the nominal interaction rate of $2 \cdot 10^7$ s^{-1}, i.e. $\langle \dot{N}_{\mathrm{dig}} \rangle = 10 \cdot N_{\mathrm{dig}} \cdot$ s^{-1}. Given numbers at sensor, frontend and channel level represent the maximum values obtained for a single element. Mean values of all elements in the corresponding setup are indicated with $\langle ... \rangle$.

Source TDR

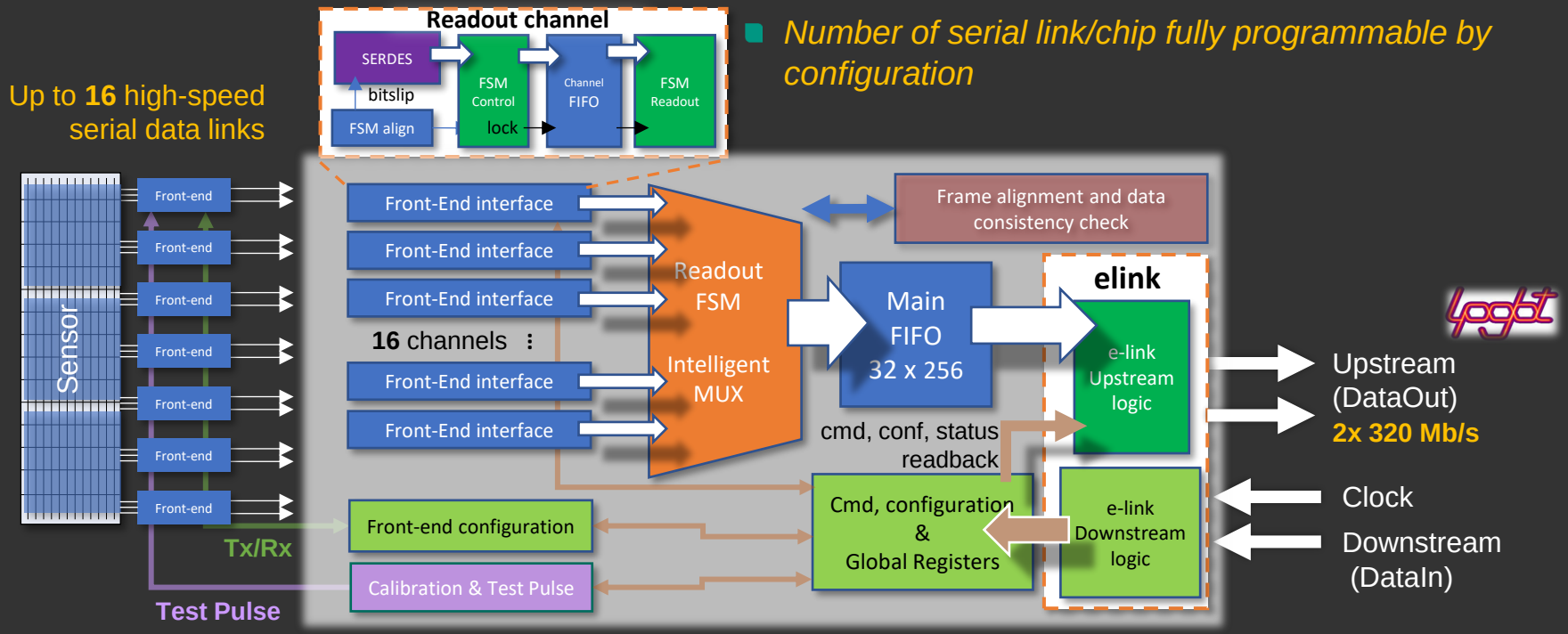
- High luminosity scenario: 2 10^7 interaction/s is expected the maximum count rate sensor (module) 4.8 Mcps in the hot region, factor of 1.6 cnt/hit, which considers an induced charge sharing between neighbouring channels (from TDR)
- Occupancy count rate (worse case for forward module) Mhit/s / f_{DAQ} = 4.8 Mcps / 39 kf/s = < 124 cnt/frame
- Equivalent to a data rate of < **155 Mb/s**
- The MDC has been designed to support a maximum data rate of = 640 Mb/s * 8/10 (encoding) = **512 Mb/s** (two outputs), or 320 Mb/s * 8/10 = **256 Mb/s** (one output)

- It enhances flexibility in designing future detector modules, enabling operation under high-occupancy conditions. This capability is particularly beneficial for large-area hadron-beam therapy and for deploying microstrip detectors in AMBER experiments at CERN's SPS facility.

MDC Core logic

MDC Core logic

ASIC architecture



Sensor and front-end

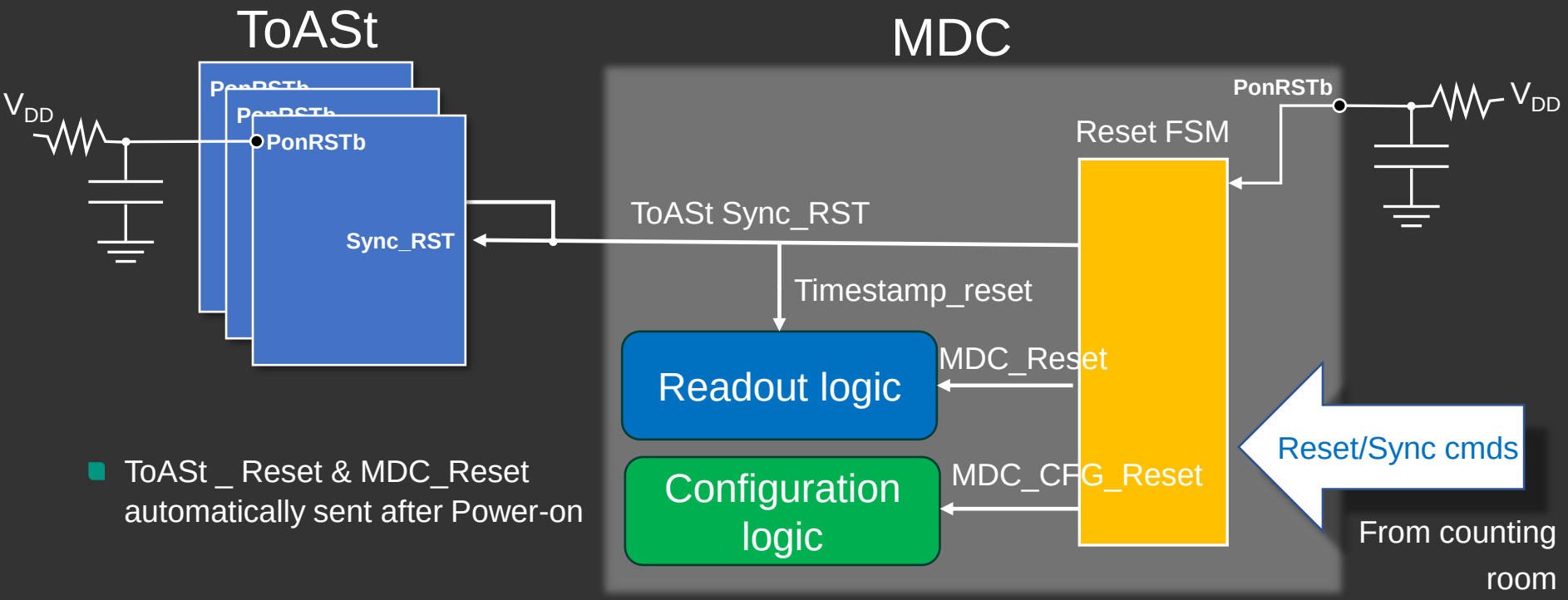
DC ASIC architecture

E/O link interface

MDC/ToASt reset and initialization

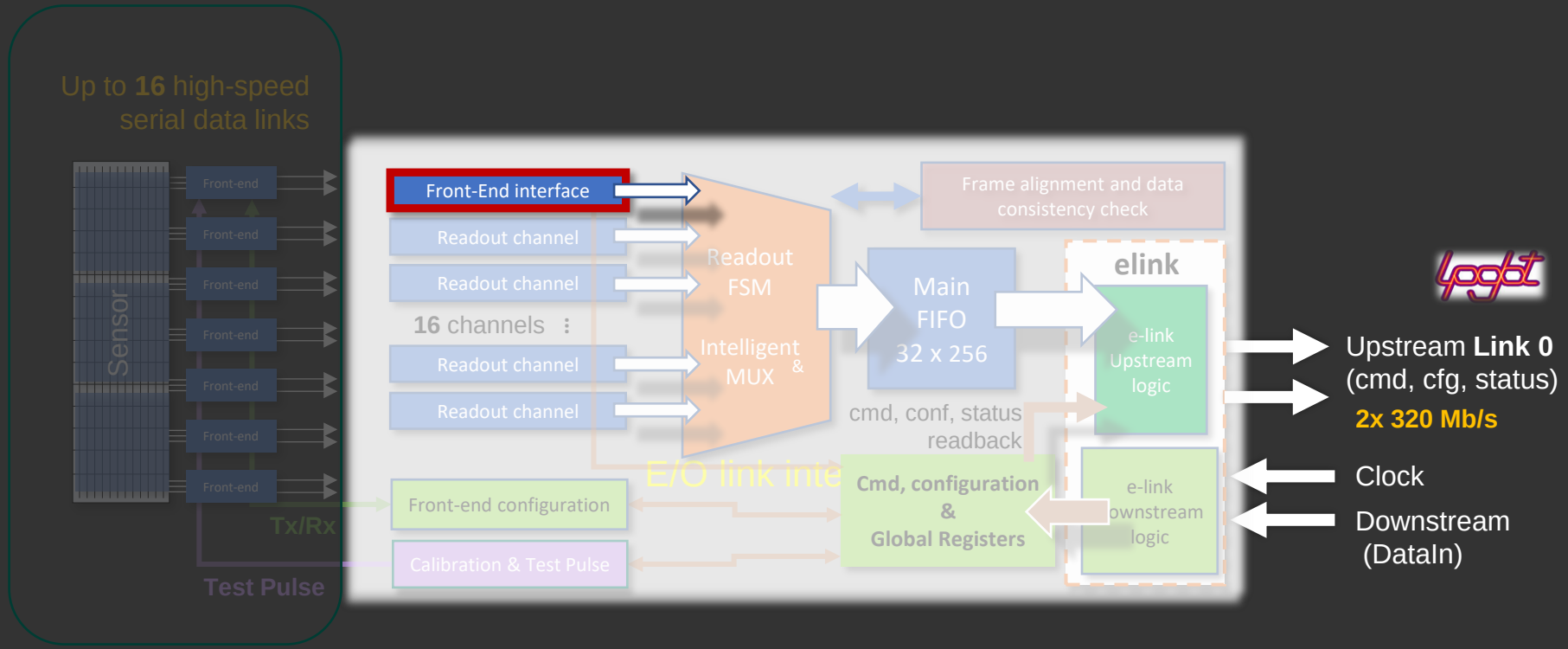
Reset signals, reset tree, initialization and default configuration

- PonRST: only to reset and initialize the reset logic



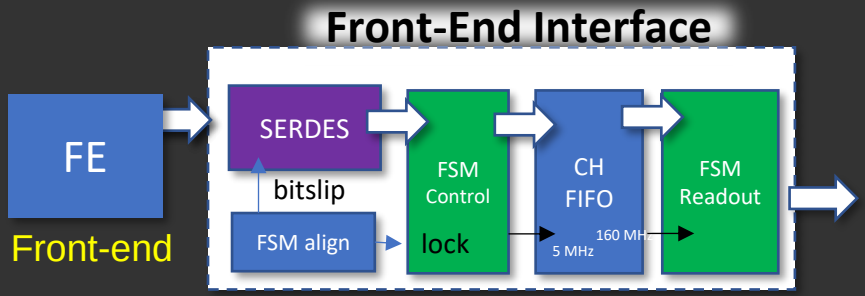
- ToASt _ Reset & MDC_Reset automatically sent after Power-on

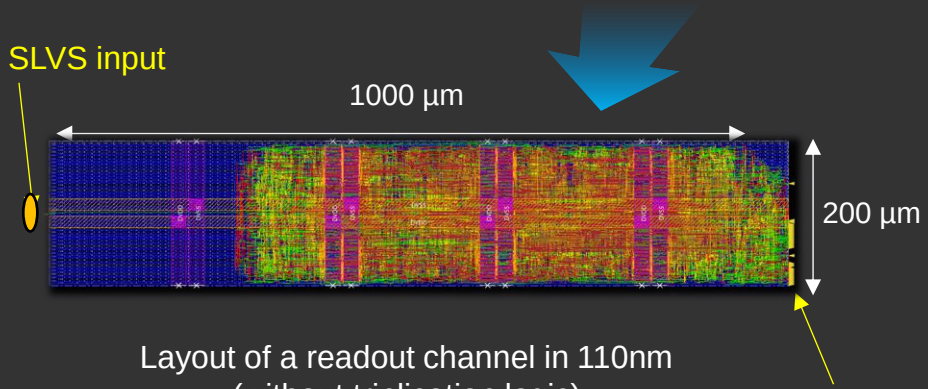
MDC – Front-End Interface



Readout channel

High efficiency, low-power, small-area logic





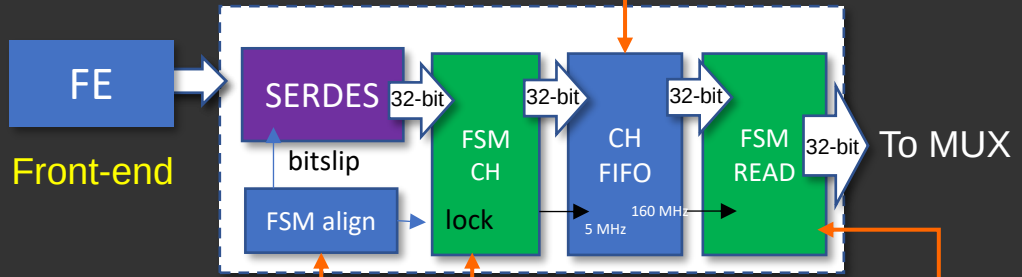
Layout of a readout channel in 110nm
(without triplication logic)

Features:

- Auto-detection/negotiation of active data links, training patter fully programmable
- No-active links are kept in low-power mode
- Density < 50 %
- FIFO by low-leakage transistor, Faraday memory generator
- Estimated power of 0.8 mW @ 1.2V

Readout channel

High efficiency, low-power, small-area logic



FIFO channel:

- Width: 32-bit, Depth: 64
- "Almost Full" threshold set at 56 entries
- "Full" threshold set at 60 entries
- Capacity: Sized at twice the capacity of the ToASt event FIFO

- **FSM_READ**:
- Transfer the event temporarily stored in the channel FIFO to the MUX logic

Channel negotiation and lock logic

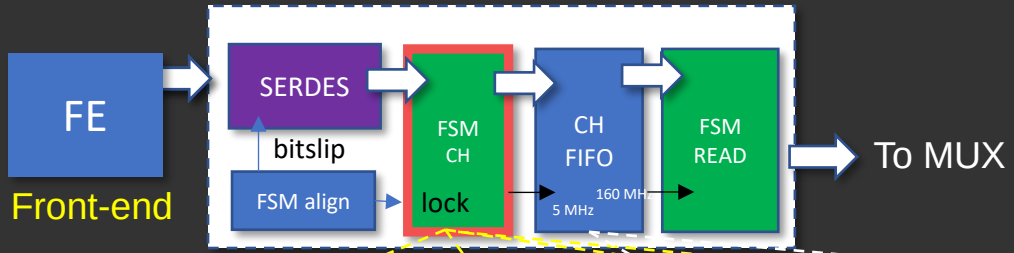
- Training patter (configurable by register)
- Channel LOCK

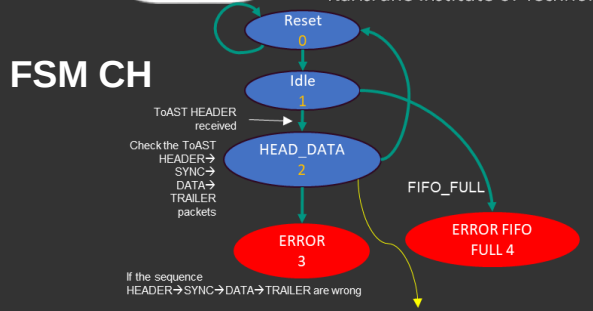
FSM_CH:

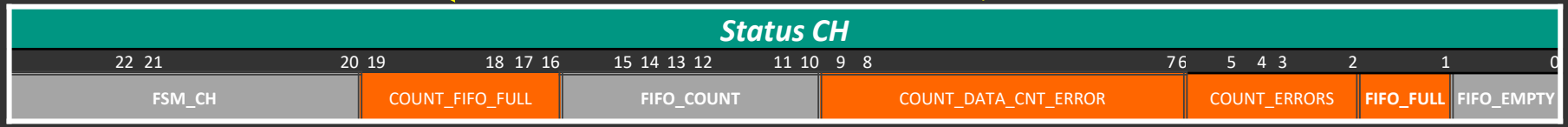
- Checks the incoming ToASt packets (HEADER->SYNC->DATA->TRAILER)
- Save the data in the channel FIFO
- Provides the number of data words present (frame)

Readout channel – FSM-channel

High efficiency, low-power, small-area logic







- **COUNT_FIFO_FULL**: Tracks the number of occurrences where the FIFO reaches a FULL state
- **COUNT_DATA_CNT_ERROR**: Records the instances where the number of data words differs from the count specified in the ToASt trailer field
- **COUNT_ERRORS**: Counts the occurrences where HEADER->SYNC->DATA_TRAILER packets are not correctly formatted or processed

Logic tested during beam tests

Readout channel – FSM-channel

Post-layout simulation

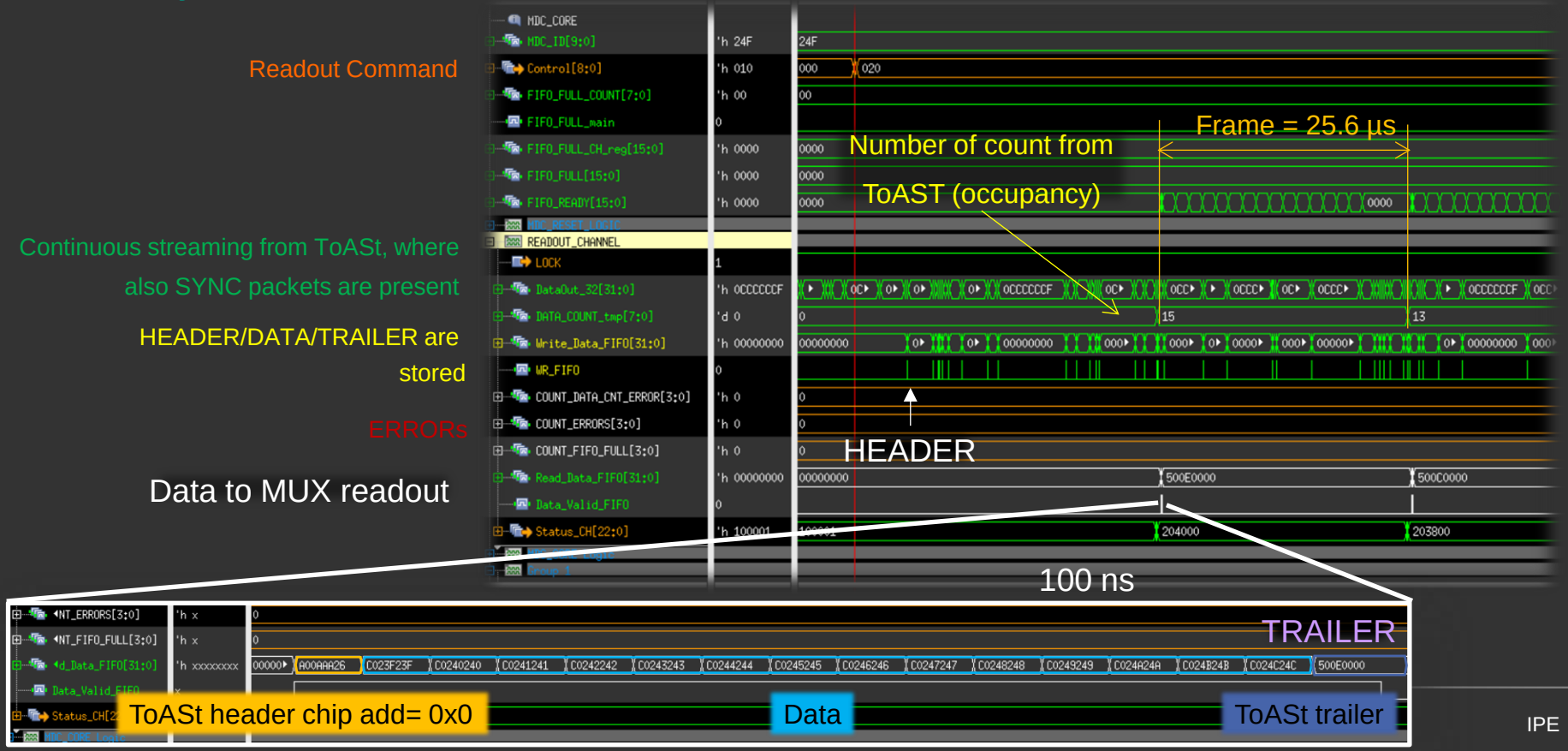
Readout Command

Continuous streaming from ToASt, where also SYNC packets are present

HEADER/DATA/TRAILER are stored

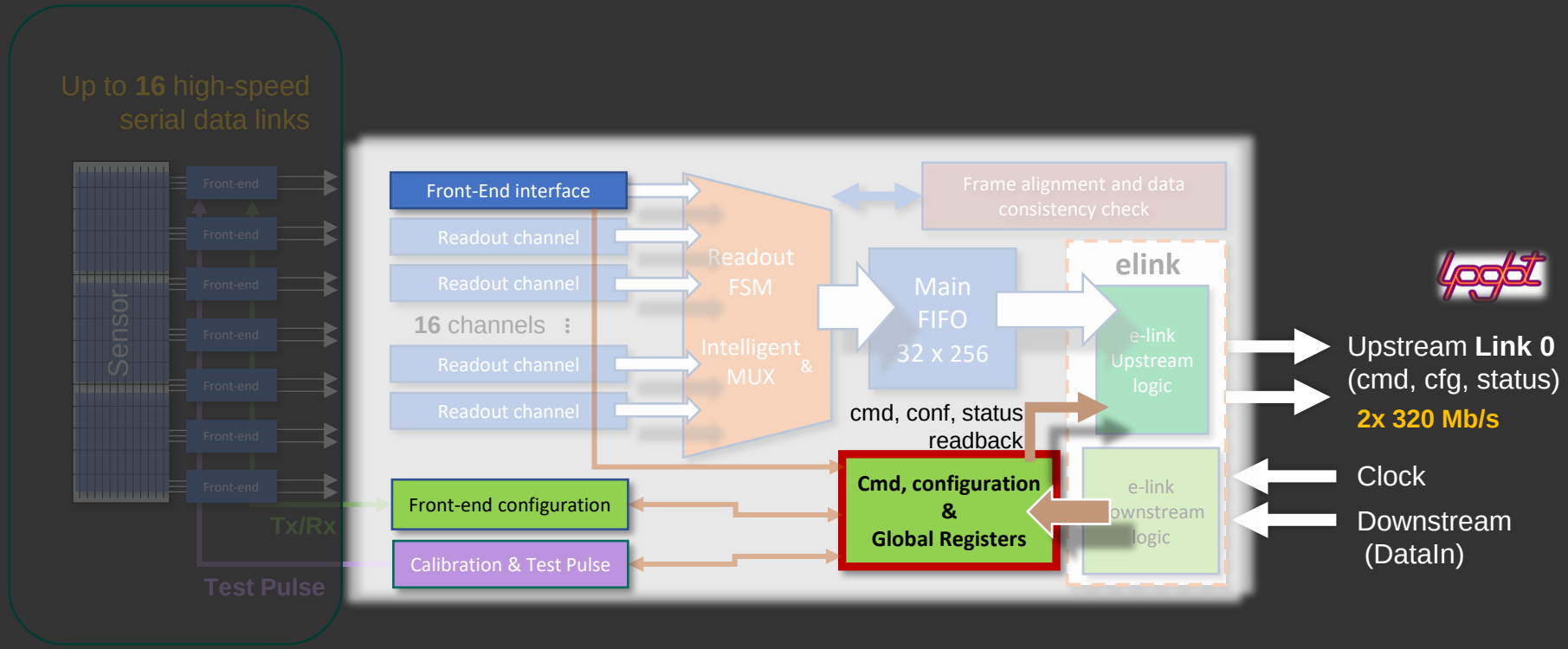
ERRORs

Data to MUX readout



MDC - Configuration Registers

User configuration space (commands / configurations / status)



Sensor and front-end

DC ASIC architecture

E/O link interface

MDC - Configuration Registers

User configuration space (commands / configurations / status)

Karlsruhe Institute of Technology

Register	Read/Write access	Register global address	Description
MDC_ID	R/W	0x00	**Detector module address (ID)**
MDC Command	R/W	0x01	Commands from off-detectors (see next slides)
FIFO_FULL_COUNTS	R	0x02	Number of times that the Main fifo is fully (automatically sent to off-det.)
MDC Status 1	R	0x03	Status 1 (see next slides)
Number of Test Pulse	R/W	0x04	Number of test pulse SET
Test Pulse delay (6.25 ns steps)	R/W	0x05	Delay and polarization Test pulse
Number of Test Pulse acquisition acquired	R	0x06	Number of test pusle acquired
ToASt_Configuration	R/W	0x07	ToASt configuration instruction
ToASt_Configuration_ReadBack	R	0x08	ReadBack the configuration DATA
ToASt_Configuration FSM status	R	0x09	Status 4 (see next slides)
Status channel 0	R	0x0A	Status_CH_0 (see next slides STATUS_CH)
Status channel 1	R	0x0B	(see sheet STATUS_CH)
Status channel 2	R	0x0C	(see sheet STATUS_CH)
Status channel 14	R	0x18	(see sheet STATUS_CH)
…	R	…	..
Status channel 15	R	0x19	(see sheet STATUS_CH)
TX_Out_inv_settings	R/W	0x1A	Data links inversion
CfgRX_TX_settings	R/W	0x1B	Cfg_TX output current control, Cfg_TX inversion and Cfg_RX inversion
GBT_CLK_settings	R/W	0x1C	Upstream LpGBT current control, Upstream GBT inversion, Downlink inversion, clock_out current control and clock_out inversion
SYNC_PATTERN (MSB)	R/W	0x1D	Programmable training pattern
SYNC_PATTERN (LSB)	R/W	0x1E	

See previous slide

MDC – Command/Status Registers

User configuration space (commands)

MDC Command (ADD =x01)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Future cmd (not used)								Start ToASt configuration sequence	Start Test Pulse	Start READOUT	Prepare acquisition	MDC CFG logic RESET	Time stamp ToAST reset (short sync reset)	Global Reset ToAST (long sync reset)	MDC_RESET

- MDC Configuration Register & configuration logic RESET
- Timestamp reset (ToASt and MDC, time event sync)
- ToASt (long reset / full reset)
- MDC, FIFOs, readout FSMs reset (no MDC Configuration Register)

Same definition of beam test system

MDC – Command/Status Registers

User configuration space (commands)

MDC Command (ADD =x01)

15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Future cmd (not used)	Start ToASt configuration sequence	Start Test Pulse	Start READOUT	Prepare acquisition	MDC CFG logic RESET	Time stamp ToAST reset (short sync reset)	Global Reset ToAST (long sync reset)	MDC_RESET

- To check if all FSMs and FIFOs are in ready for acquisition
- Start readout of the ToASt (data move from ToASt -> counting room)
- Start test pulse / calibration sequence (like beam test)
- Upon receiving the ToASt instruction sequences, this command initiates the ToASt configuration process

Same definition of beam test system

MDC – Command/Status Registers

User configuration space (status and errors)

- STATUS_1: 16 bits channel locked (active high)

Status 1 (channels looked)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel 15 locked	Channel 14 locked	Channel 13 locked	Channel 12 locked	Channel 11 locked	Channel 10 locked	Channel 9 locked	Channel 8 locked	Channel 7 locked	Channel 6 locked	Channel 5 locked	Channel 4 locked	Channel 3 locked	Channel 2 locked	Channel 1 locked	Channel 0 locked

- STATUS_CH, 16 status channel registers (one per each channel)

Status CH

22 21	20 19	18 17 16	15 14 13 12	11 10	9 8	7 6	5 4 3	2	1	0
FSM_CH	COUNT_FIFO_FULL		FIFO_COUNT		COUNT_DATA_CNT_ERROR		COUNT_ERRORS	FIFO_FULL	FIFO_EMPTY	

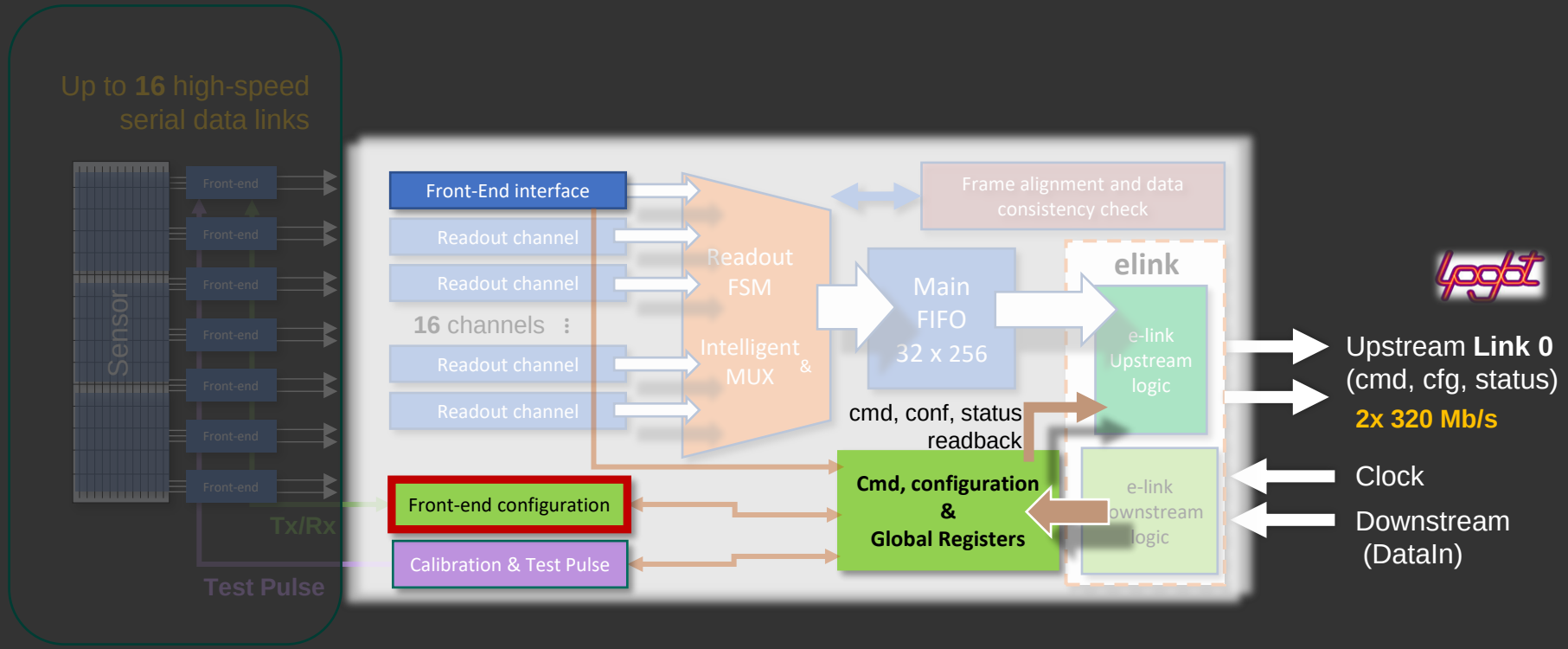
- STATUS_CFG: configuration is pending, tracks the number of errors encountered during the ToASt CFG

Status CFG ToASt Configuration

15 14 13 12	11	10 9 8	7	6	5	4 3 2 1 0
Number of Errors during configuration	ReadBack_FIFO_empty	FSM_RX_CFG	ReadBack_FIFO_full	sync_FIFO_full	sync_FIFO_empty	FSM_SHIFT

MDC - Configuration Registers

User configuration space (commands / configurations / status)



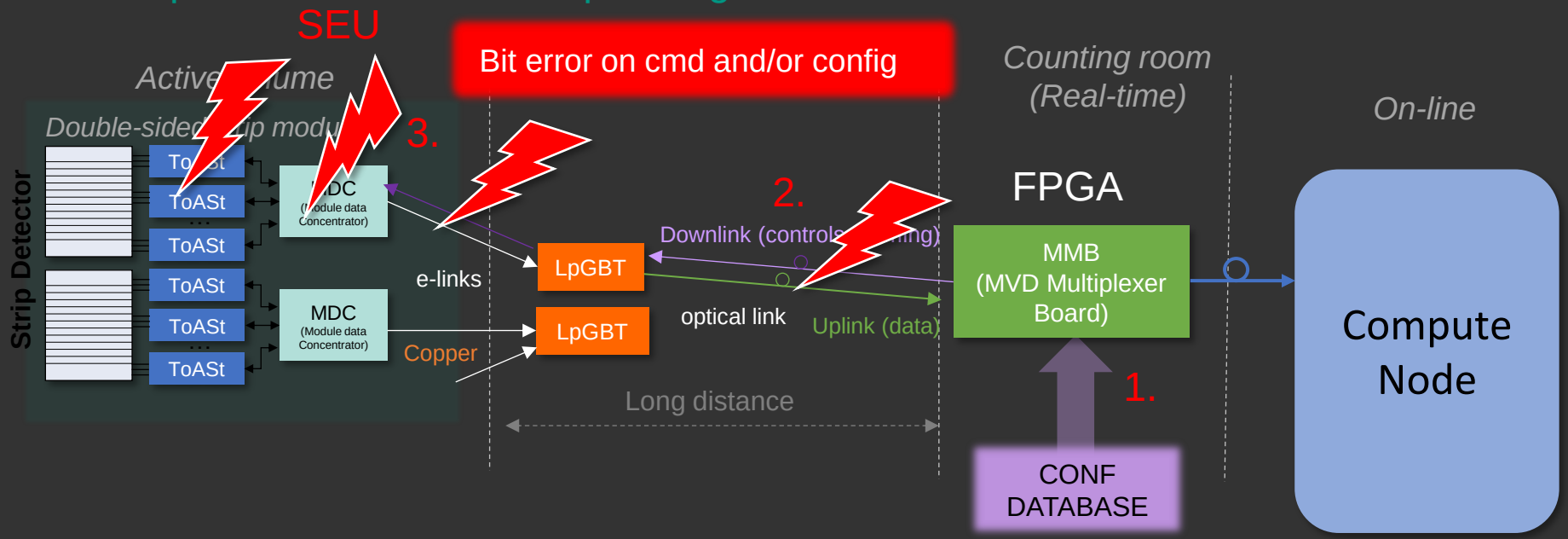
Sensor and front-end

DC ASIC architecture

E/O link interface

Commands & configurations logic

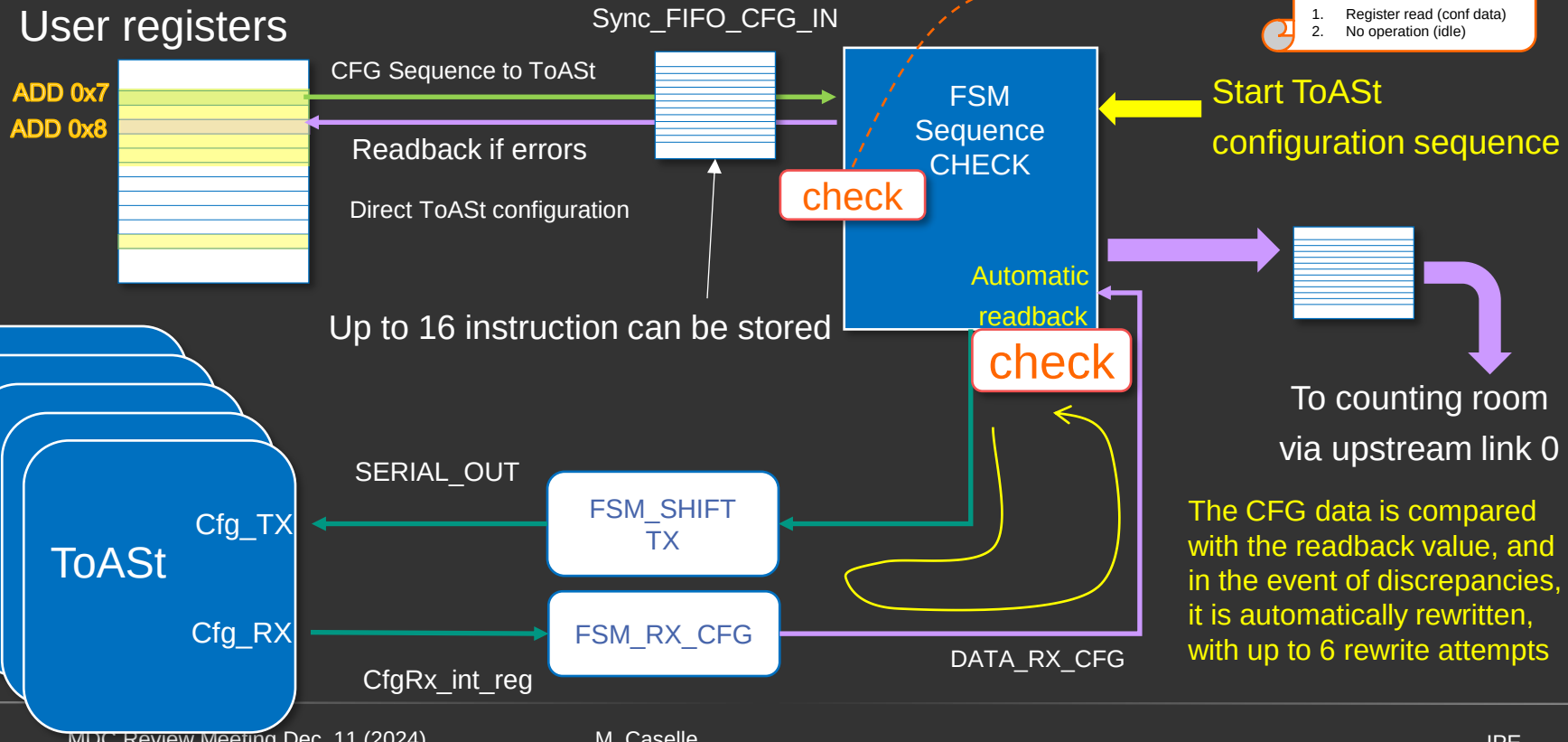
Critical point for all detectors operating in harsh environments



- Without well-designed and robust configuration logic, the detector may produce not consistent data and/or serious consequences in the functionality

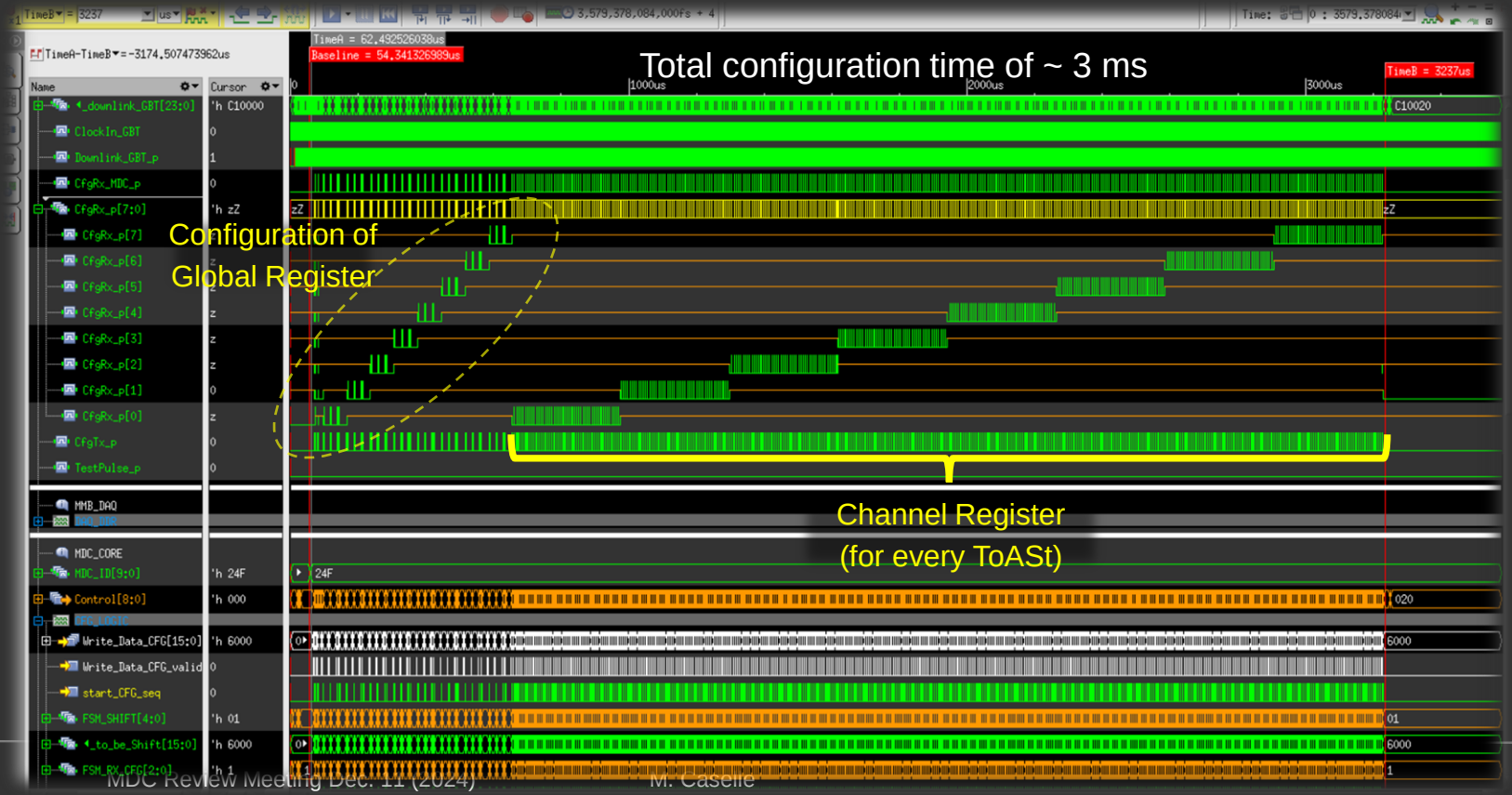
Commands and configuration logic

ToAst configuration and “error protection” architecture



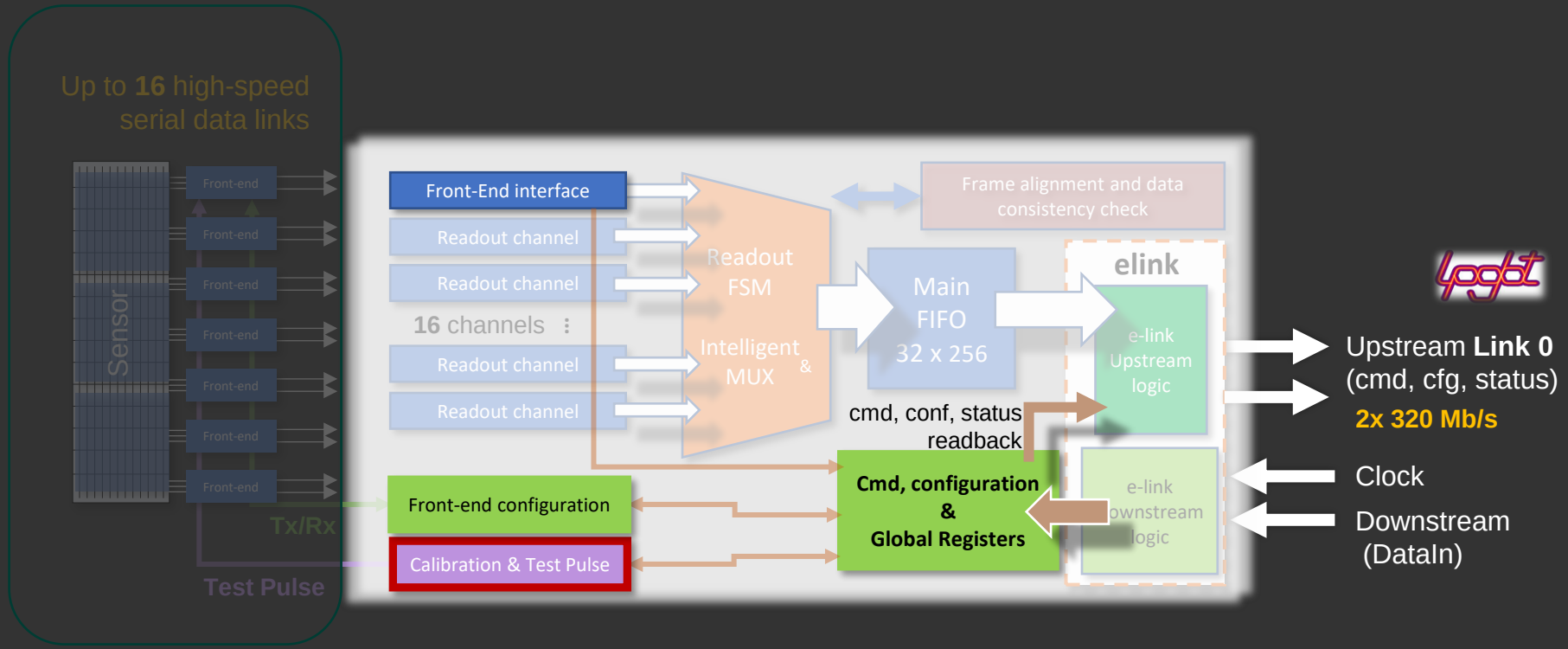
Commands and configuration logic

Simulations



MDC - Configuration Registers

User configuration space (commands / configurations / status)



Sensor and front-end

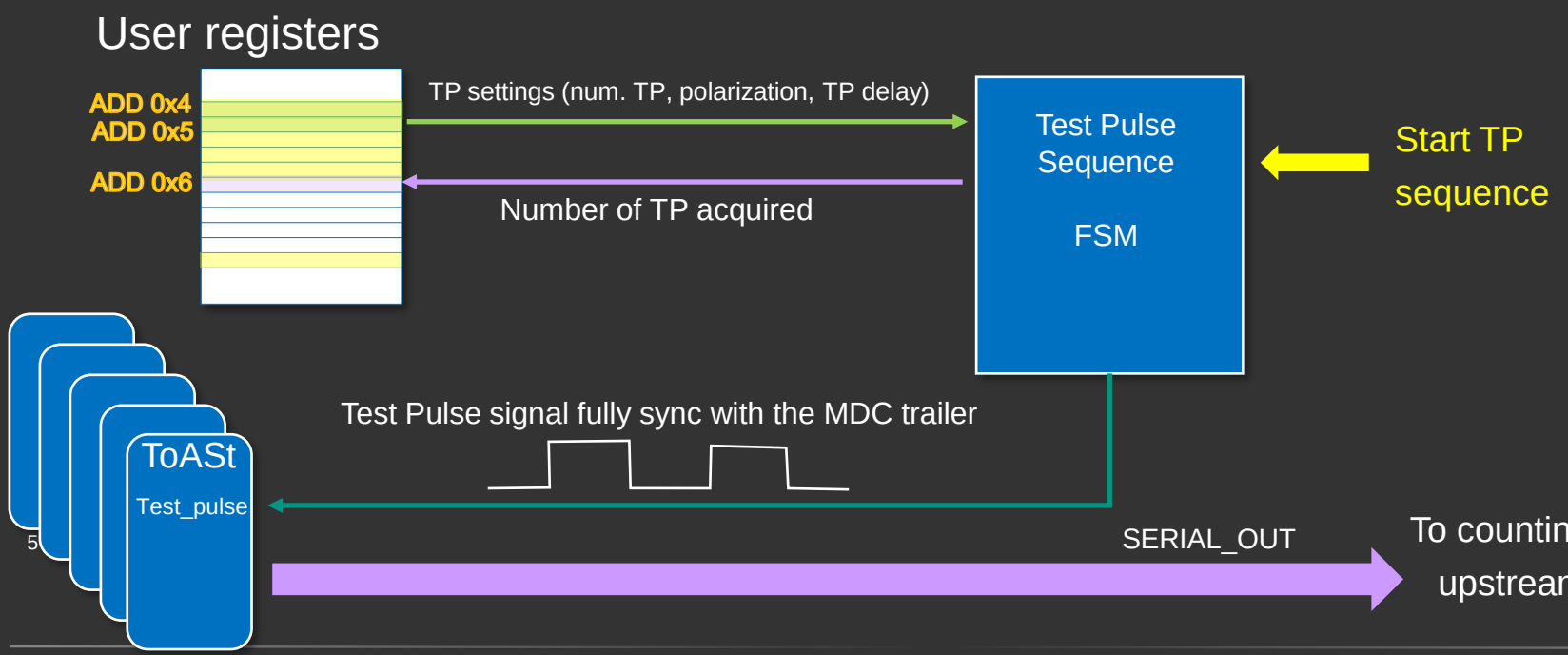
DC ASIC architecture

E/O link interface

On-detector calibration logic

Programmable test pulse sequence

- A fully programmable test pulse sequence to speed up the S-curve characterizations and front-end test



Test Pulse

Post-layout simulation

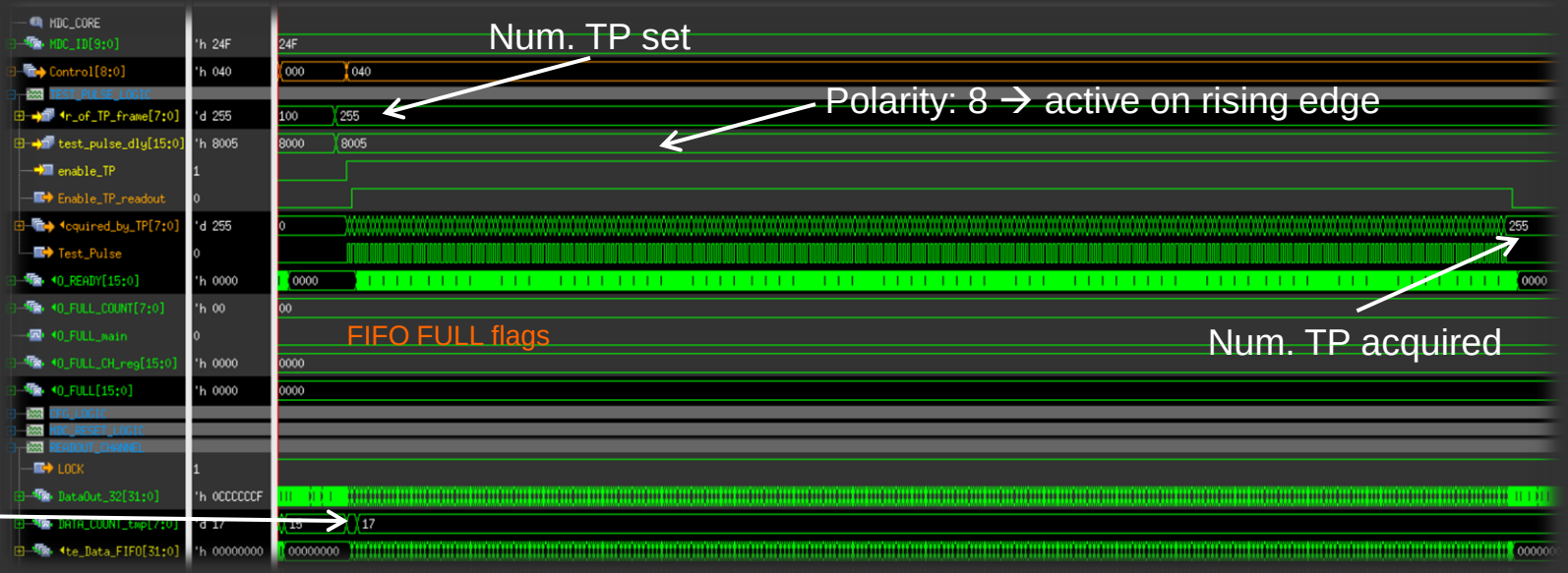
Command

Test Pulse settings

Nun. TP = 255

Active on rising edge

16 channels enable per link, 32 channels enable per ToASt (***50 % occupancy***)



- **Test Conditions**: 8 ToASt chips with 2 data links enabled, MDC configured with 2 data links enabled
- **Results**: The MDC demonstrated the capability to sustain continuous occupancy exceeding 50% per ToASt chip

Test Pulse

Post-layout simulation

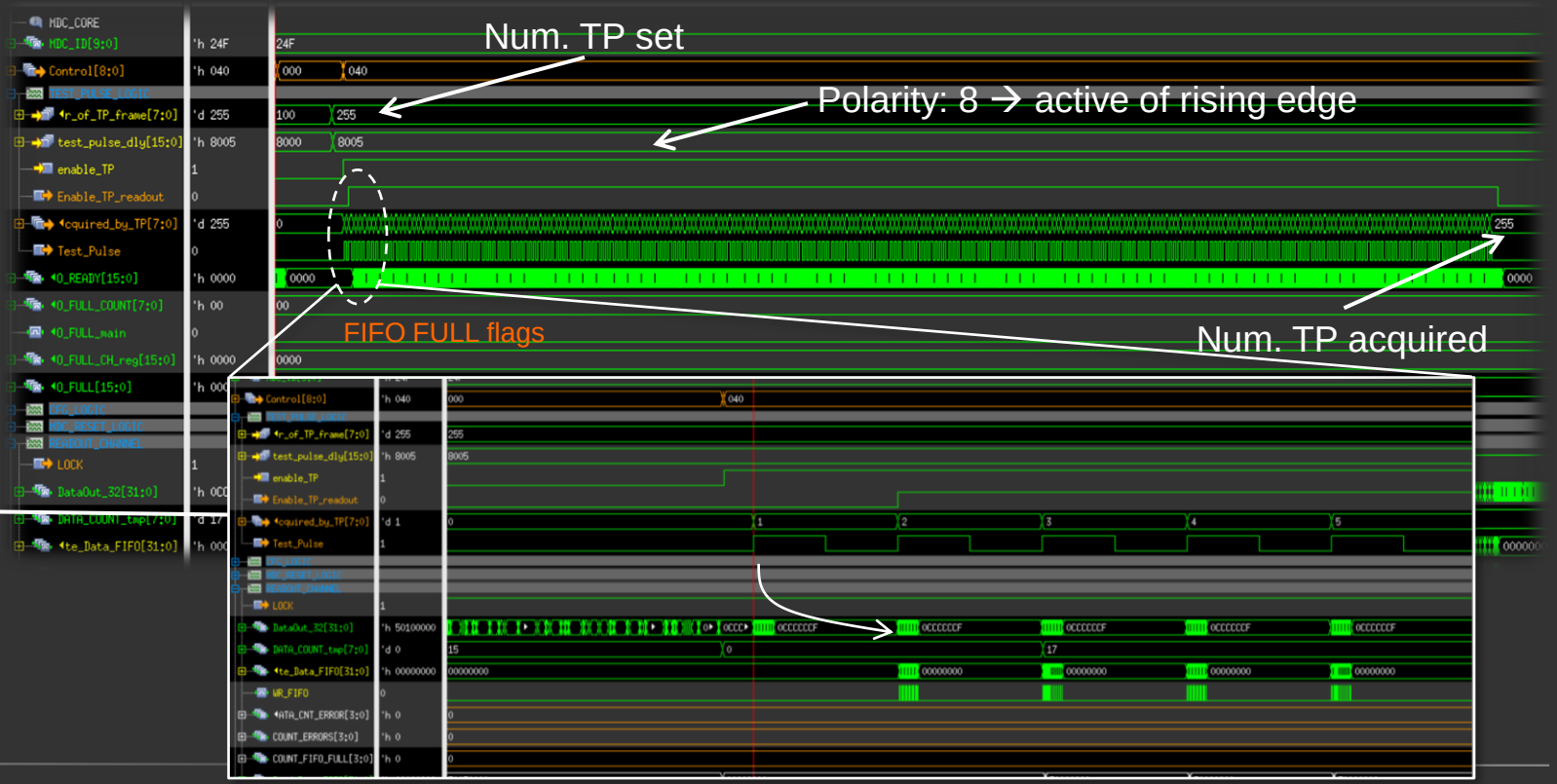
Command

Test Pulse settings

Nun. TP = 255

Active on rising edge

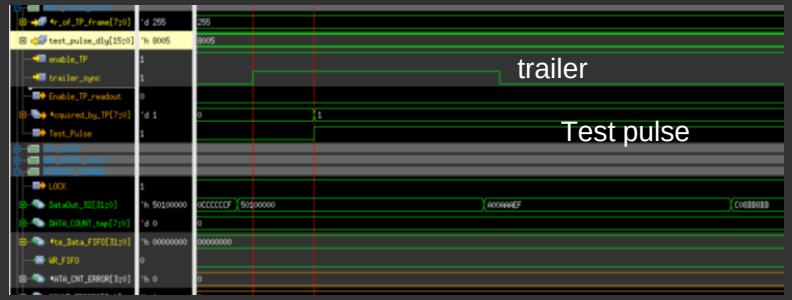
16 channels enable per link, 32 channels enable per ToASt (***50 % occupancy***)



On-detector calibration logic

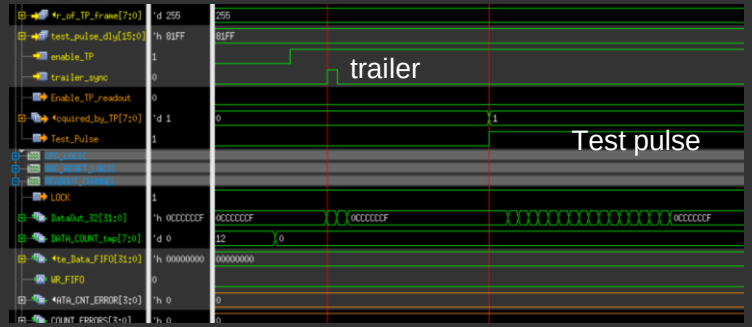
Programmable delay between the trailer and active edge

- Precisely calibrate the Time of Arrival (ToA) for all ToASt chips using a highly accurate reference
- Verify that all ToASt chips are properly synchronized in timing



TP delay set to = 5,

equivalent to TP delay = 0.05 µs



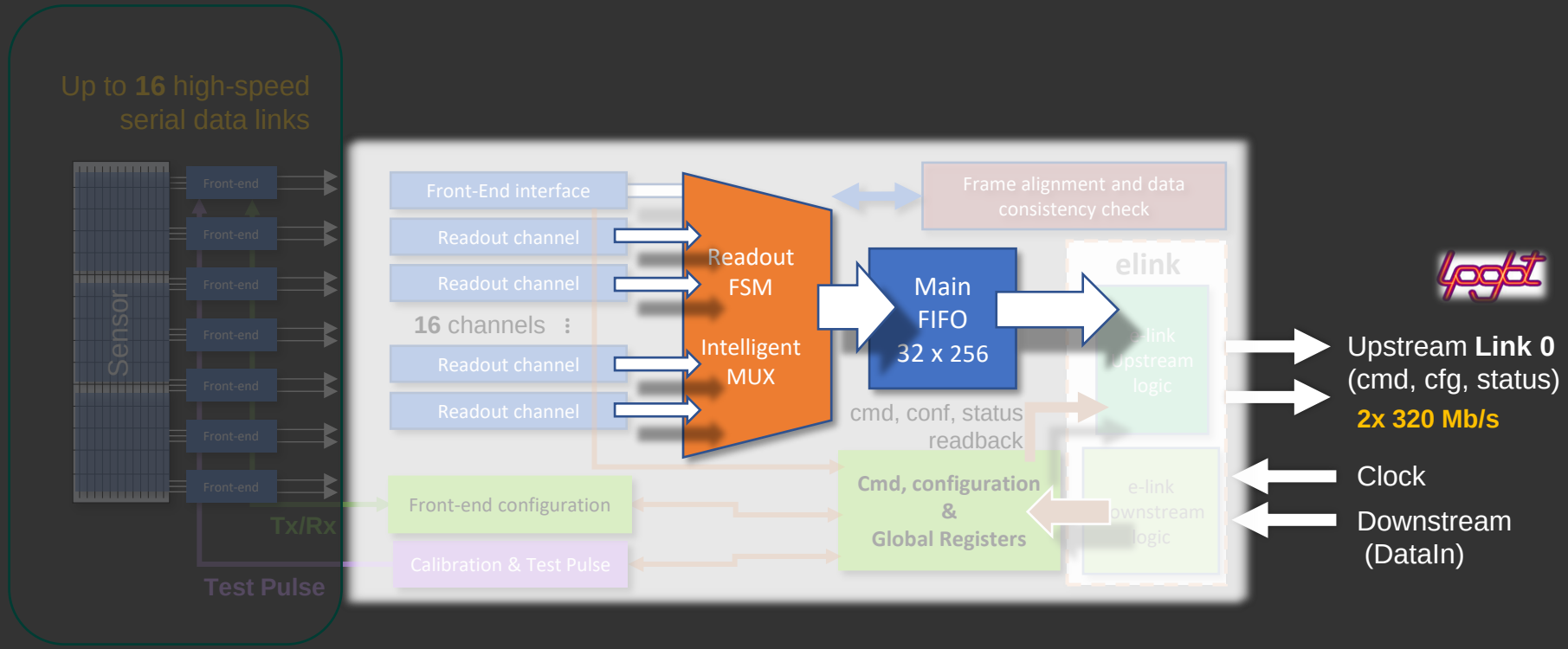
TP delay set to = 511,

equivalent to TP delay = 3.213 µs

- TP delay step of 6.25 ns → see next slides for ToA testing in the continuous integration setup

MDC – Main readout unit

Developed for high-data throughput



Sensor and front-end

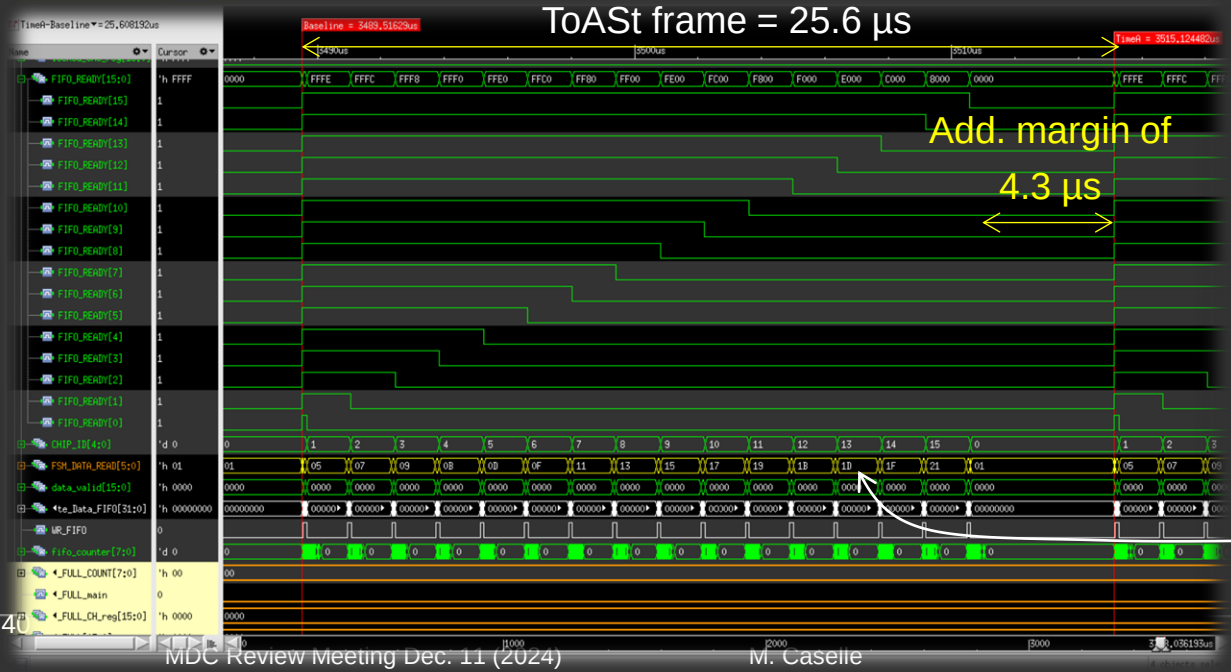
DC ASIC architecture

E/O link interface

MDC – Main readout unit

Developed for high-data throughput

- A READY flag is asserted as soon as data becomes available in the FIFO channel
- Channels are read out sequentially in the order: ch0 → ch1 → ch2 → … → ch15
- Channels that are not locked or not present are automatically skipped



Fixed occupancy: close to 50 % per ToASt, readout of num. 8 ToASts.

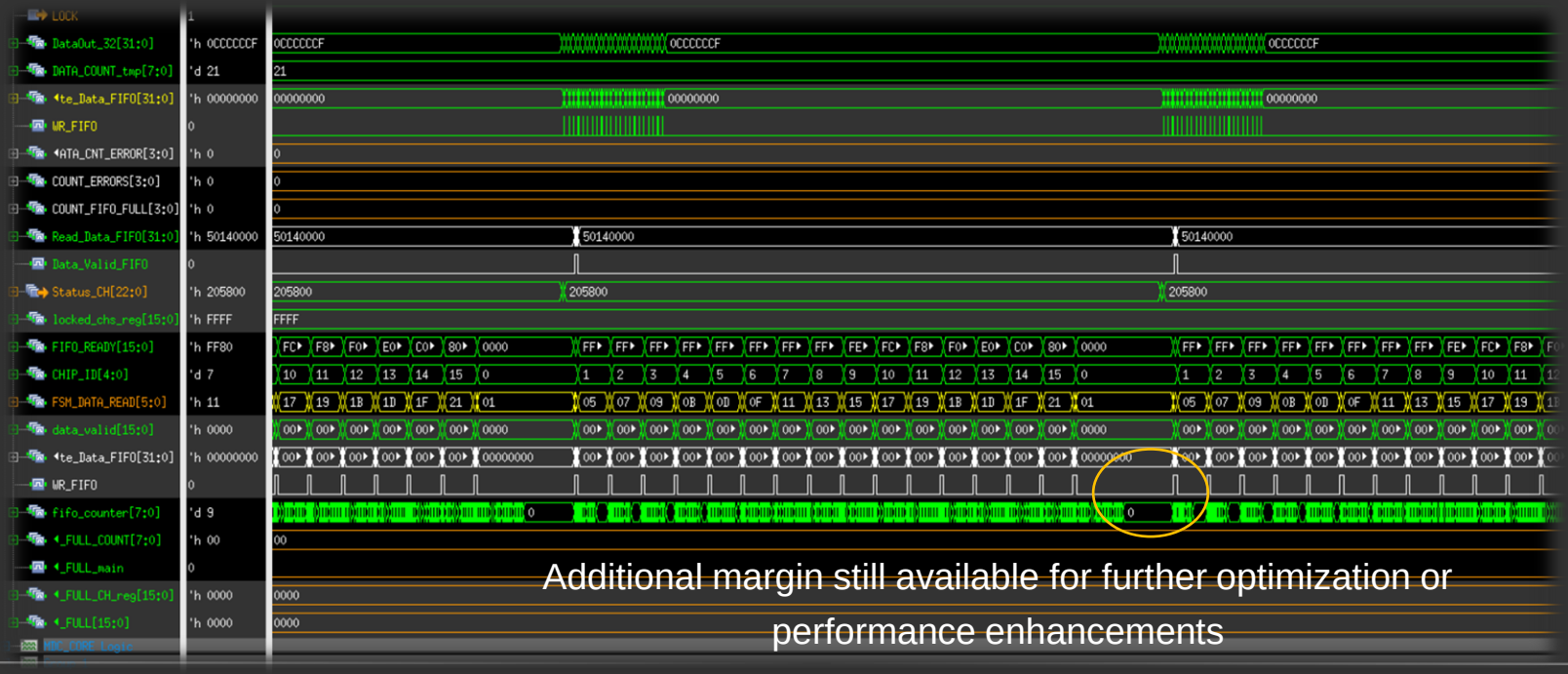
Channel ready for readout

An additional delay is introduced between the readout of two consecutive channels to prevent the FIFO full condition

MDC – Stress testing

Pushing the system to peak performance

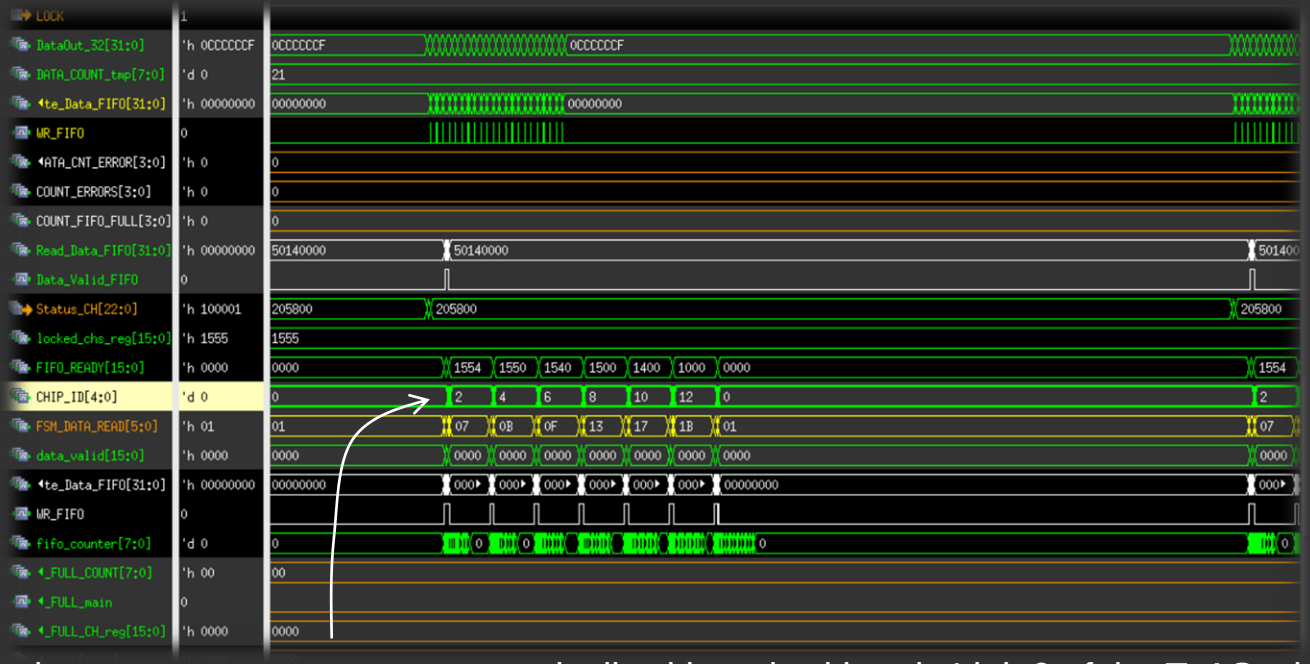
- Number of 20 cnt per link → equivalent to a ToASt occupancy of 62.5%, with 8 ToASt (supermodule)
- data rate of = 40 * 8 * 32 * 39 kpfs = 400 Mb/s



MDC – Main readout unit

MDC configuration of rectangular detector module

- ToASt occupancy of 30%, only 7 ToASt with one link activated

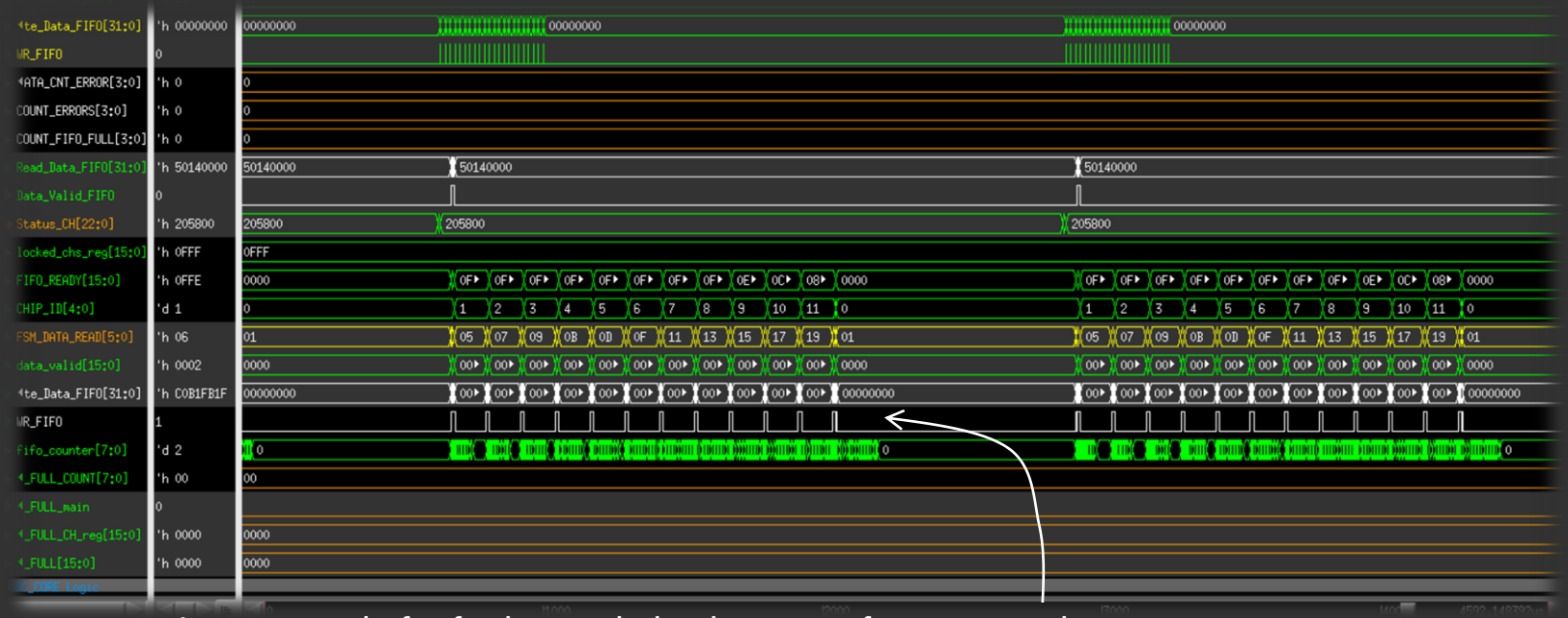


Channels that are not present are automatically skipped, with only Link 0 of the ToASts being read out

MDC – Main readout unit

MDC configuration of trapezoidal detector module

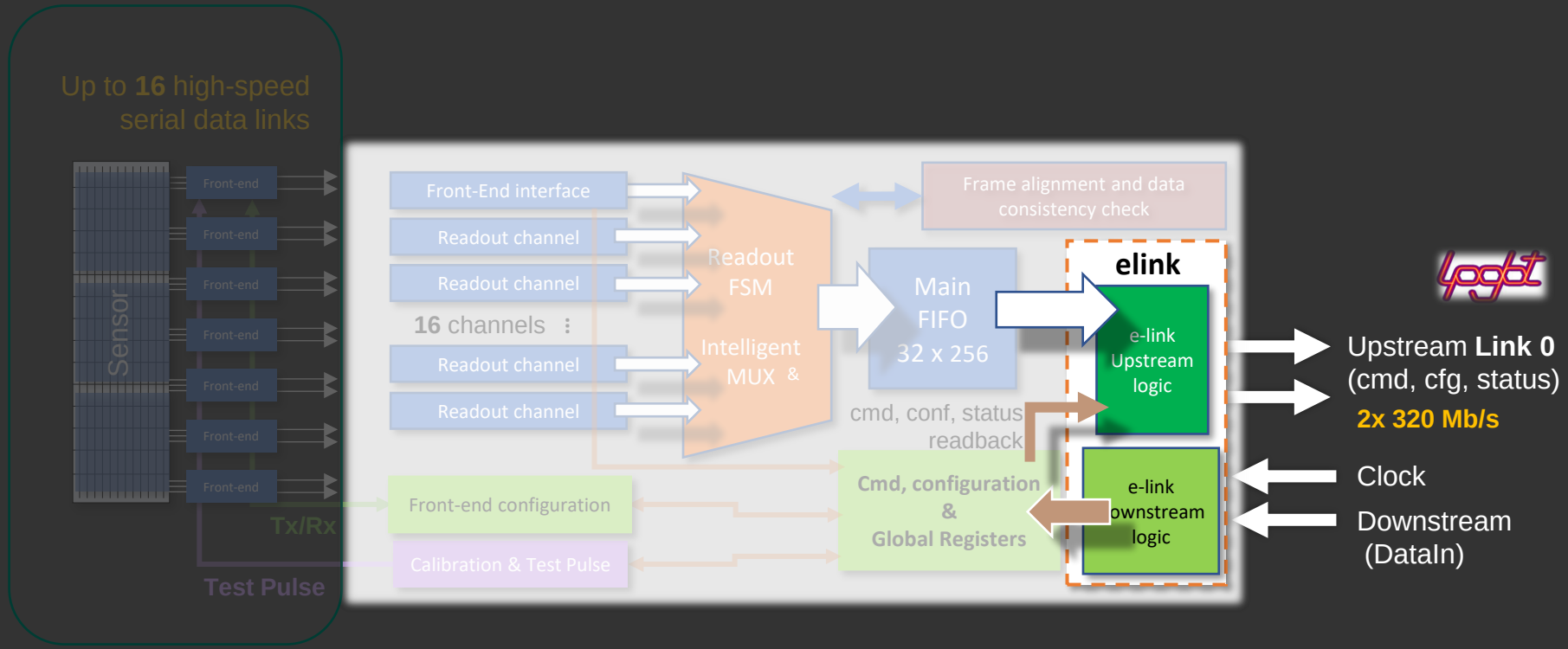
- ToASt occupancy of 60%, 6 ToASt, two links per ToASt activated



Large margin for further optimization or performance enhancements

MDC - Configuration Registers

User configuration space (commands / configurations / status)



Sensor and front-end

DC ASIC architecture

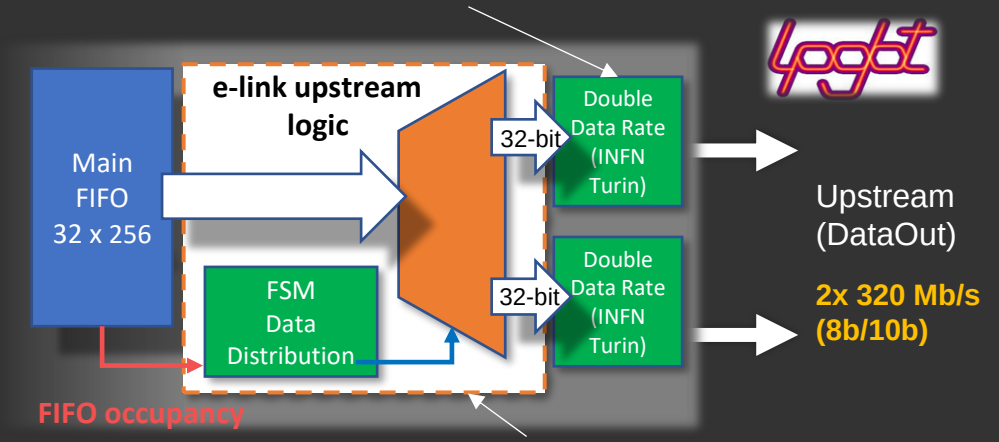
E/O link interface

MDC (Module data Concentrator)

Intelligent Data Distribution System Across Upstream Links

- In case of high data occupancy, data are evenly distributed across both links, as illustrated below
- In case of small amount of data, data are transmitted through link 0, avoiding the need to duplicate header and trailer packets
- Capable of sustaining a very high occupancy rate

Developed by Giulio Dellacasa



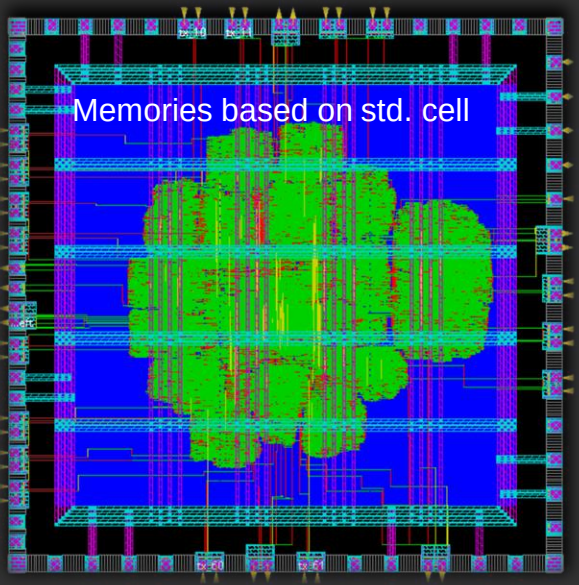
Developed by Francesca & Michele

Optimization

Comparison w/wo faraday memories

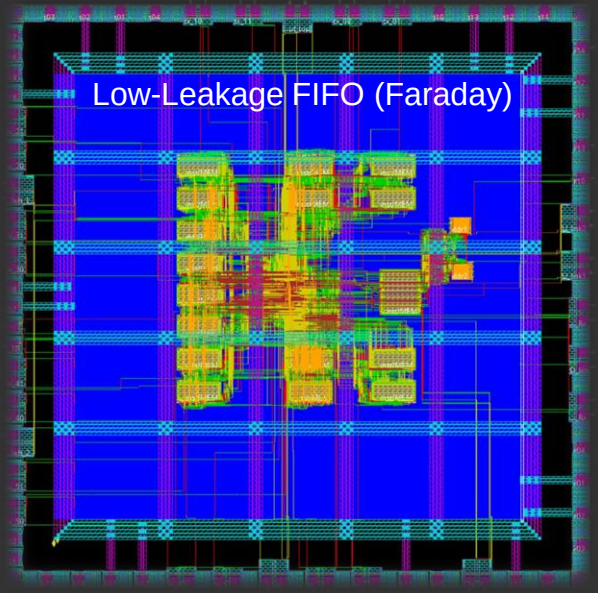
Drastic reduction of power consumption and occupancy

PANDA CM 2024_1



Estimated power consumption: 165 mW @ 1.2V
Density: 40%

Current design



Estimated power (preliminary): 66.64 mW @ 1.2V
Density: < 10 %

X 2.5

Timing verification

Post-layout, final chip

mcaselle@ipeasic1:~/PANDA/innovus/reports/MDC_TOP_DDR/timeDesign

```
#############################################################
#  Generated by:      Cadence Innovus 21.35-s114_1
#  OS:                Linux x86_64(Host ID ipeasic1.ipe.kit.edu)
#  Generated on:      Fri Dec  6 18:18:28 2024
#  Design:            MDC_TOP_DDR
#  Command:           time_design -sign_off -expanded_views -report_prefix 5_ro
 -timing_debug_report -report_only
#############################################################

------------------------------------------------------------------
         time_design Summary
------------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.026  |  0.026  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|         All Paths:|  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
|av_normal_typ       |  2.296  |  2.296  |  0.000  |
|                    |  0.000  |  0.000  |  0.000  |
|                    |    0    |    0    |    0    |
|                    |  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
|av_normal_max       |  0.026  |  0.026  |  0.000  |
|                    |  0.000  |  0.000  |  0.000  |
|                    |    0    |    0    |    0    |
|                    |  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
|av_normal_min       |  3.660  |  3.660  |  0.000  |
|                    |  0.000  |  0.000  |  0.000  |
|                    |    0    |    0    |    0    |
|                    |  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
|av_normal_pwr       |  3.411  |  3.411  |  0.000  |
|                    |  0.000  |  0.000  |  0.000  |
|                    |    0    |    0    |    0    |
|                    |  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
```

Setup

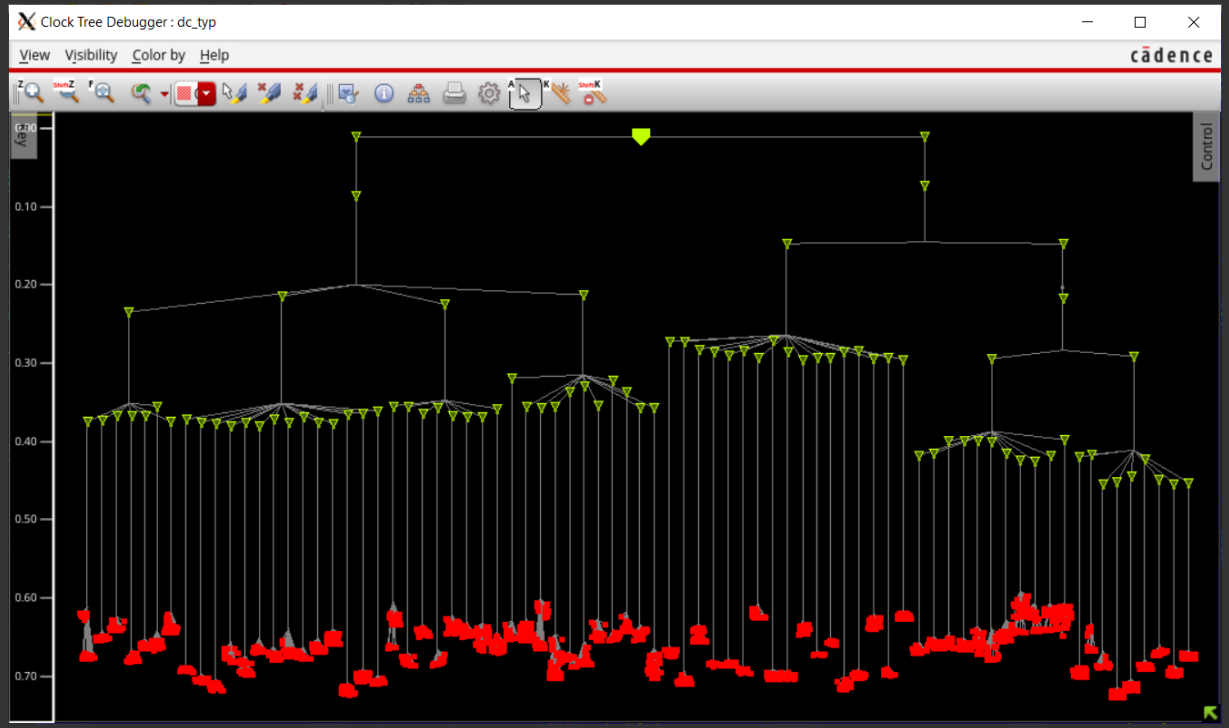
mcaselle@ipeasic1:~/PANDA/innovus/reports/MDC_TOP_DDR/timeDesign

```
#############################################################
#  Generated by:      Cadence Innovus 21.35-s114_1
#  OS:                Linux x86_64(Host ID ipeasic1.ipe.kit.edu)
#  Generated on:      Fri Dec  6 18:18:44 2024
#  Design:            MDC_TOP_DDR
#  Command:           time_design -sign_off -hold -expanded_views -rep
ng_debug_report -report_only
#############################################################

------------------------------------------------------------------
         time_design Summary
------------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.186  |  0.186  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|         All Paths:|  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
|av_normal_typ       |  0.340  |  0.340  |  0.000  |
|                    |  0.000  |  0.000  |  0.000  |
|                    |    0    |    0    |    0    |
|                    |  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
|av_normal_min       |  0.186  |  0.186  |  0.000  |
|                    |  0.000  |  0.000  |  0.000  |
|                    |    0    |    0    |    0    |
|                    |  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
|av_normal_pwr       |  0.252  |  0.252  |  0.000  |
|                    |  0.000  |  0.000  |  0.000  |
|                    |    0    |    0    |    0    |
|                    |  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
|av_normal_max       |  0.582  |  0.582  |  0.000  |
|                    |  0.000  |  0.000  |  0.000  |
|                    |    0    |    0    |    0    |
|                    |  14769  |  14769  |    0    |
+--------------------+---------+---------+---------+
```

Hold

Internal clock tree distribution

Max time skew between logic nodes



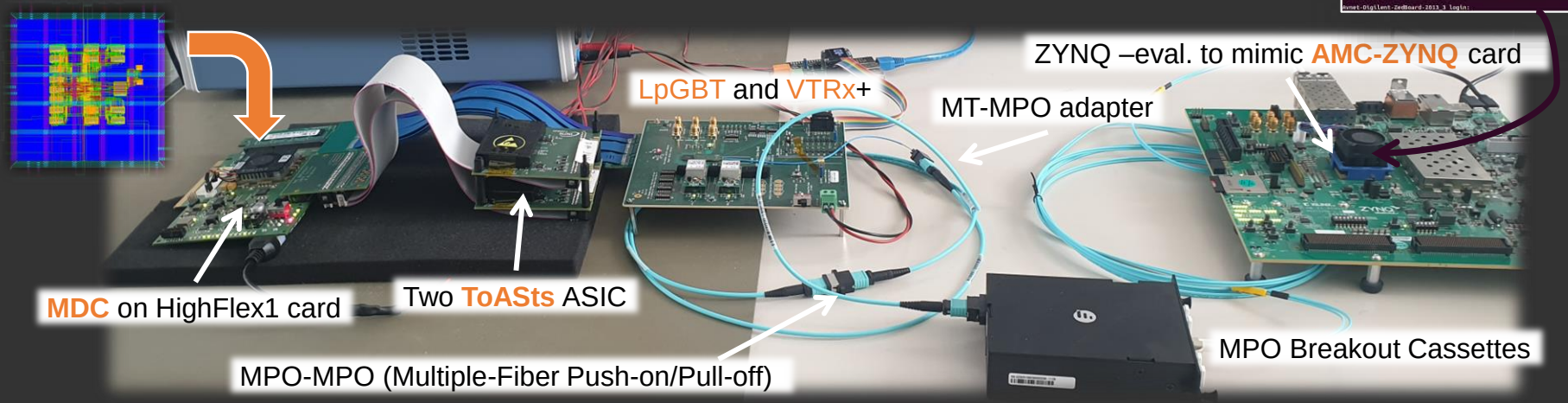
Clock propagated to final logic node “load” with a limited time skew

Integration and test of MDC deployed on FPGA

MDC qualification & test

Assessment of Digital Performance and ToASt System Integration

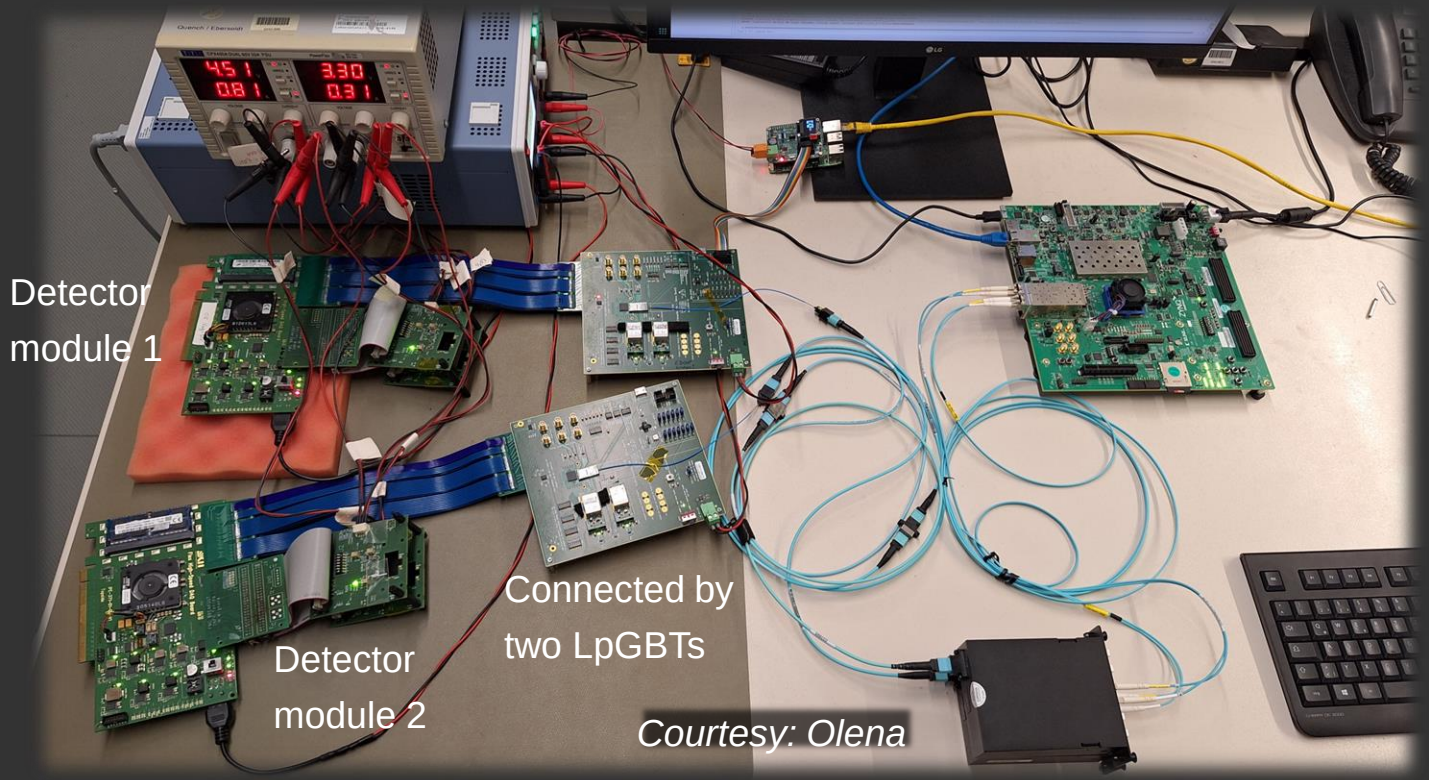
- *Complete Readout Chain*: All main HW components integrated: ToASt chips (w/wo sensors), MDC (FPGA-based), LpGBT and VTRx+ , off-detector card (ZCU102 emulating AMC cards)
- Preliminary FPGA firmware implemented on the off-detector system
- Software & low-level drivers deployed on PetaLinux (FPGA-ZYNQ platform)



PhD of Olena Manzhura

MDC qualification & test

Assessment of Digital Performance and ToASt System Integration



MDC qualification & test

Data throughput test

- *Objective:* Measure the data occupancy that the MDC can handle using real ToASt chips connected to the MDC-FPGA implementation (same Verilog source) and read out via LpGBT.
- *Test Setup:* Two ToASt chips configured in a small-detector module setup, four links operating in parallel.
- *Method:* Inject test pulses across all channels on both ToASt chips at 100% occupancy, each ToASt chip operates with two active links operating at their maximum frame rate of 39.06 kfps

Num. of ToASt Framerate

- Data generated is = 64 x 2 x 32 x 39 kfps ~ 160 Mb/s

Channels/ToASt 32 bit/data

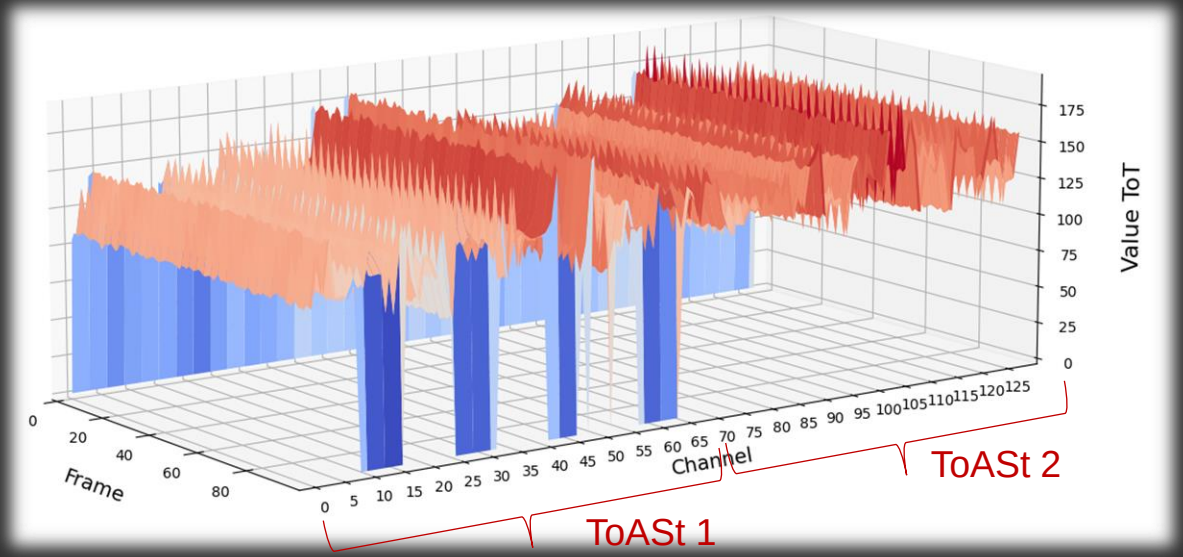
This corresponds to the maximum data rate of ***155 Mb/s*** expected for the hot module in a high-luminosity scenario, handling 2×10^7 events

•The plots are consistent and identical for every sequence.
•Achieved a sustained data rate of approximately 160 Mb/s.

MDC qualification & test

Data throughput test

- Test pulse sequences were repeated several hundred times



- No data loss was detected across all test pulse sequences.
- The plots are consistent and identical for every sequence.
- Achieved a sustained data rate of approximately 160 Mb/s.

Courtesy: Olena

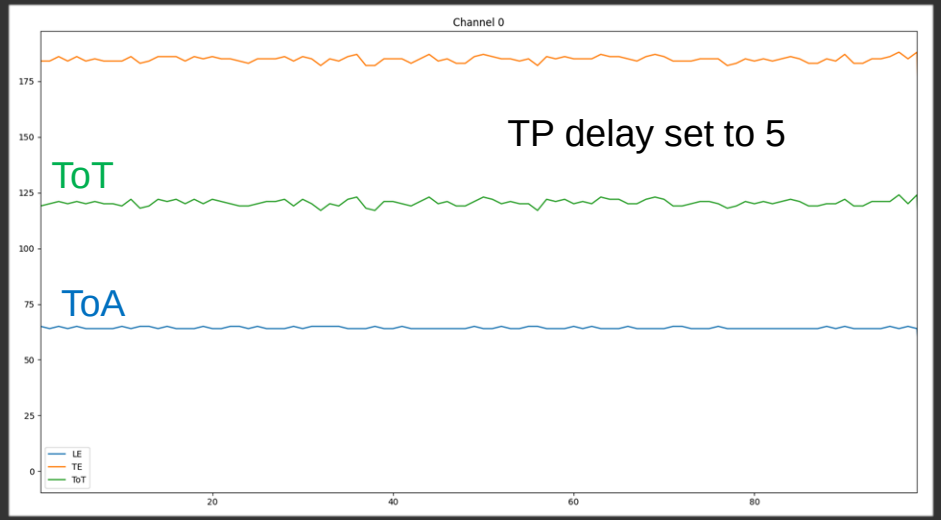
- The MDC architecture, connected to the LpGBT, can sustain a data rate equivalent to that expected from the hot detector module in a high-luminosity scenario

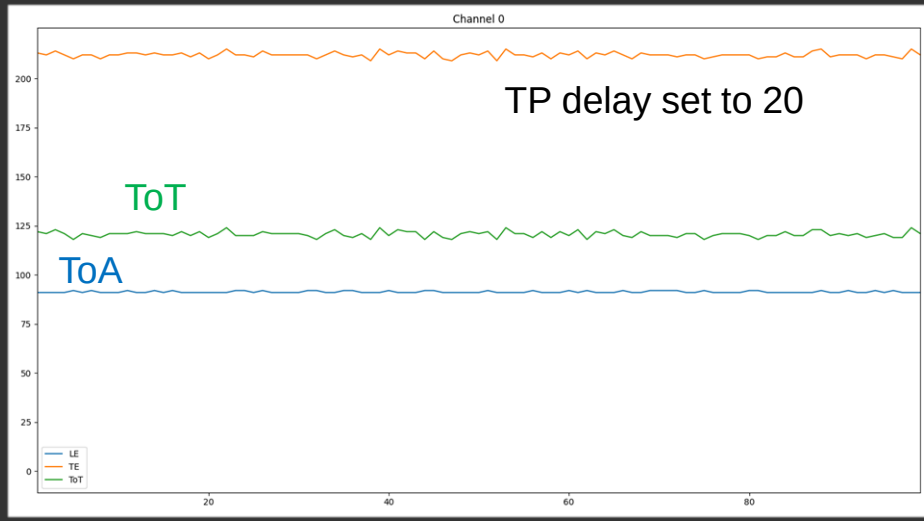
MDC qualification & test

Test Pulse delay test

Courtesy: Olena

- Test pulse sequences were repeated several hundred times





TP delay set to 5 → ToA of ~ **65** cnt

TP delay set to 5 → ToA of ~ **90** cnt

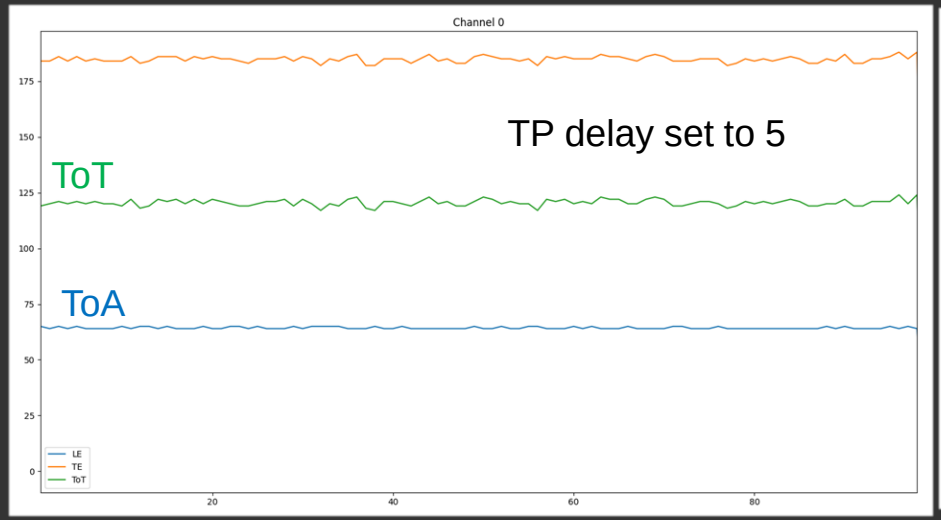
MDC qualification & test

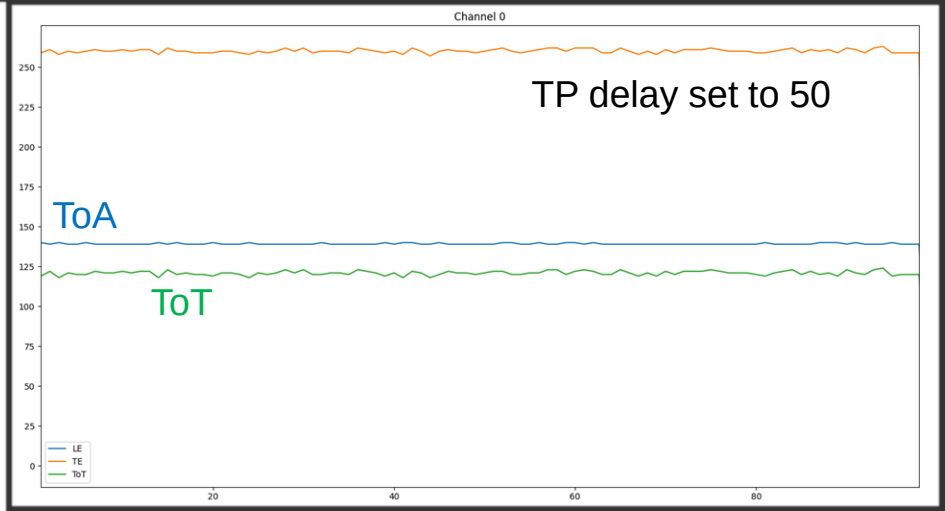
Test Pulse delay test

Karlsruhe Institute of Technology

Courtesy: Olena

- Test pulse sequences were repeated several hundred times





TP delay set to 5 → ToA of ~ **65** cnt

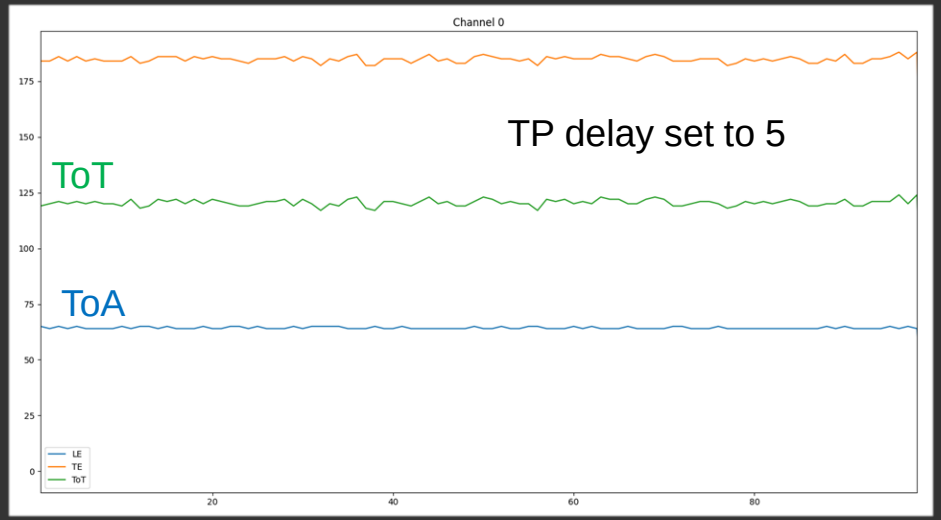
TP delay set to 50 → ToA of ~ **140** cnt

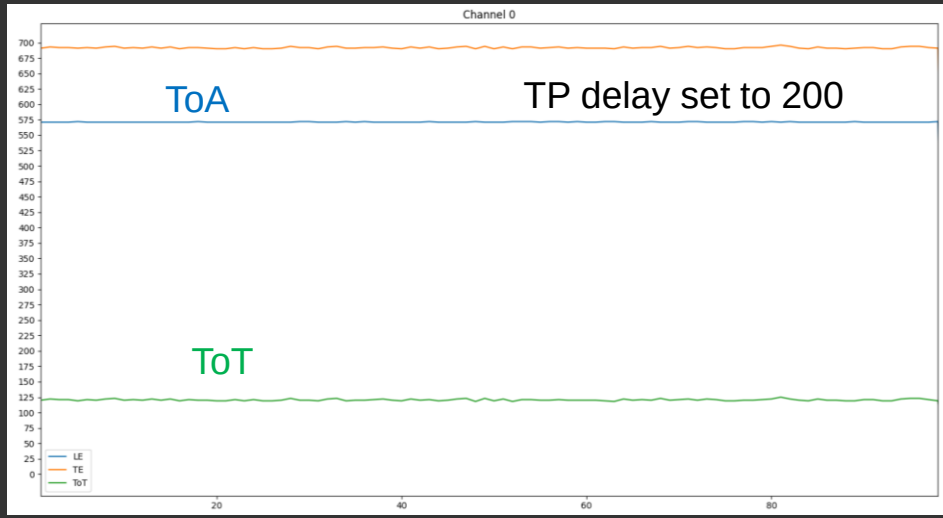
MDC qualification & test

Test Pulse delay test

Courtesy: Olena

- Test pulse sequences were repeated several hundred times





TP delay set to 5 → ToA of ~ **65** cnt

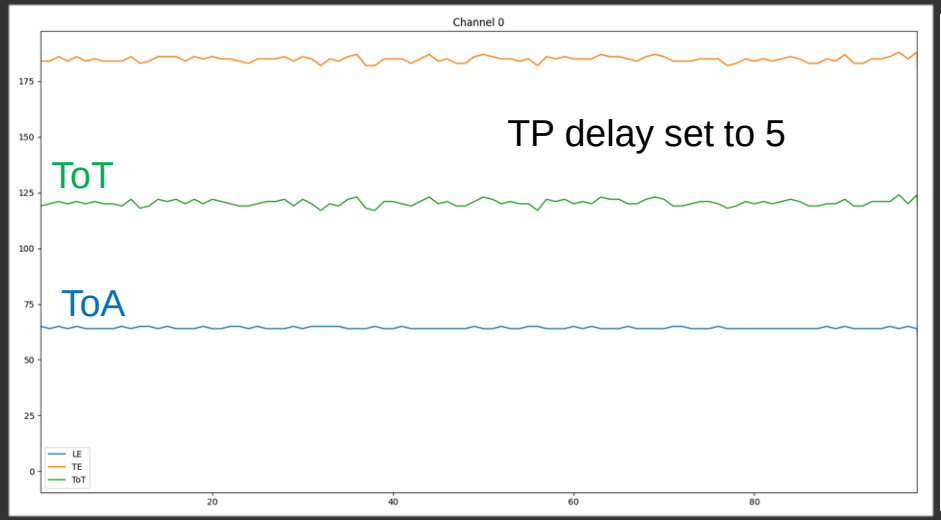
TP delay set to 200 → ToA of ~ **570** cnt

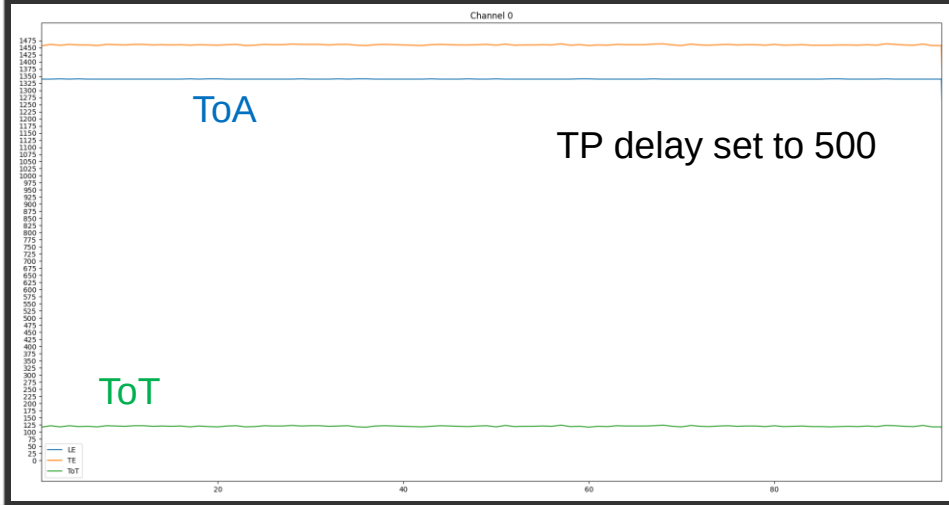
MDC qualification & test

Test Pulse delay test

Courtesy: Olena

- Test pulse sequences were repeated several hundred times





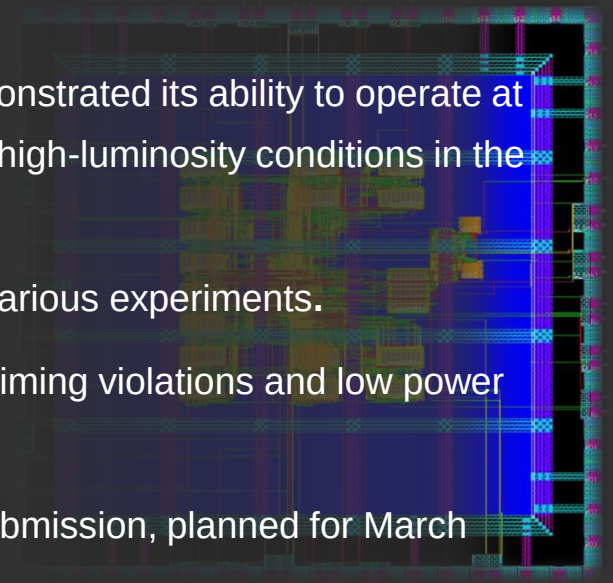
TP delay set to 5 → ToA of ~ **65** cnt

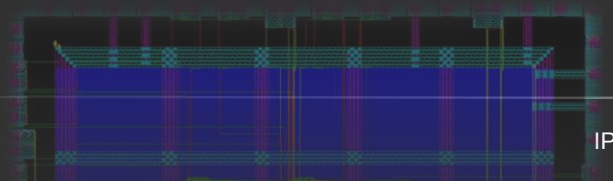
TP delay set to 500 → ToA of ~ **1340** cnt

Conclusions

What's next

- **Simulation:** MDC sustains 62.5% occupancy per ToASt, with 8 activated ToASts and two links each (data rate > 400 Mb/s)
- **Performance:** The MDC-FPGA, integrated with ToASt, has demonstrated its ability to operate at over 160 Mb/s, matching the maximum data rate required under high-luminosity conditions in the hot-detector region at PANDA
- **Versatility:** MDC has applications beyond PANDA, suitable for various experiments**.**
- **ASIC implementation**: The ASIC version is fully routed with no timing violations and low power consumption
- **Next Steps**: A verification with ToASt/Gianni is needed before submission, planned for March 2025





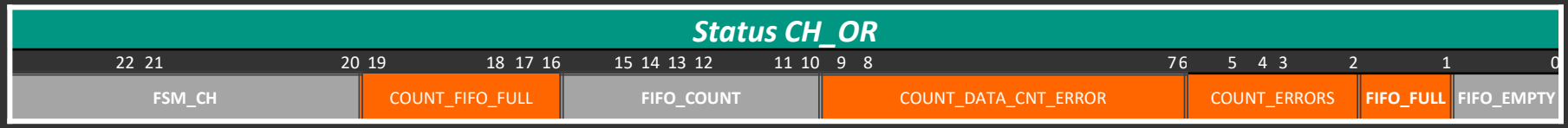

Thank you for your attention

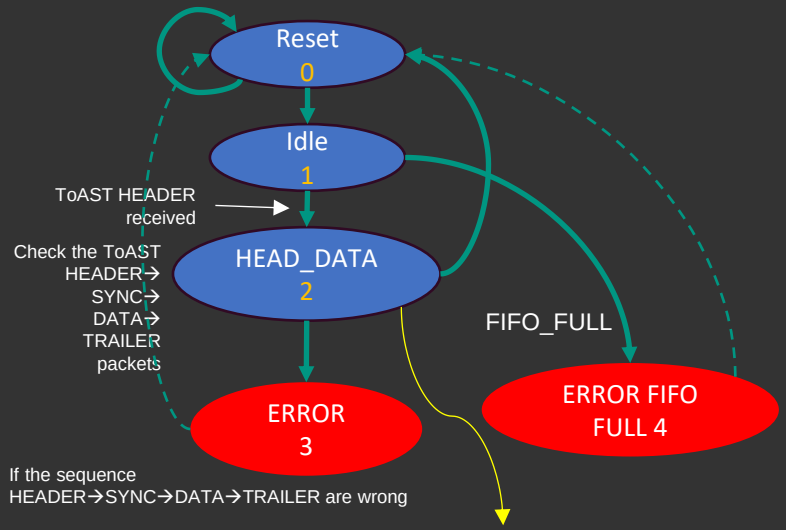
feedback

Open discussion

MDC – Command/Status Registers

User configuration space (status and errors)





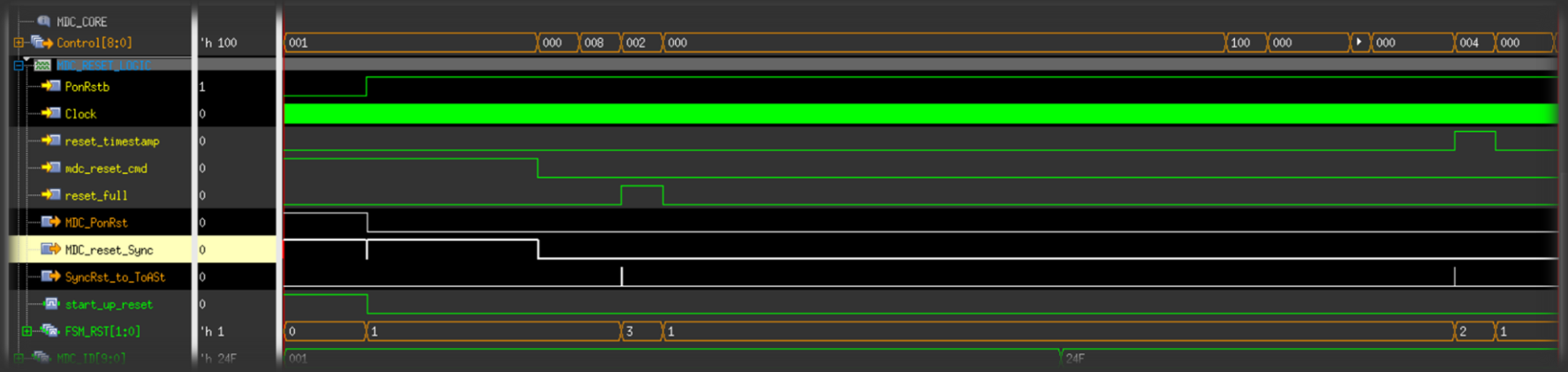
Provides DATA_COUNT_tmp counts the number of data received in one frame (between HEADER and TRAILER)

- **COUNT_FIFO_FULL**: Tracks the number of occurrences where the FIFO reaches a FULL state
- **COUNT_DATA_CNT_ERROR**: Records the instances where the number of data words differs from the count specified in the ToASt trailer field
- **COUNT_ERRORS**: Counts the occurrences where HEADER->SYNC->DATA_TRAILER packets are not correctly formatted or processed
- ➔ copy to MDC trailer, sent together the data

MDC/ToASt reset and initialization

Post-layout simulation

- PonRST: only to reset and initialize the reset logic

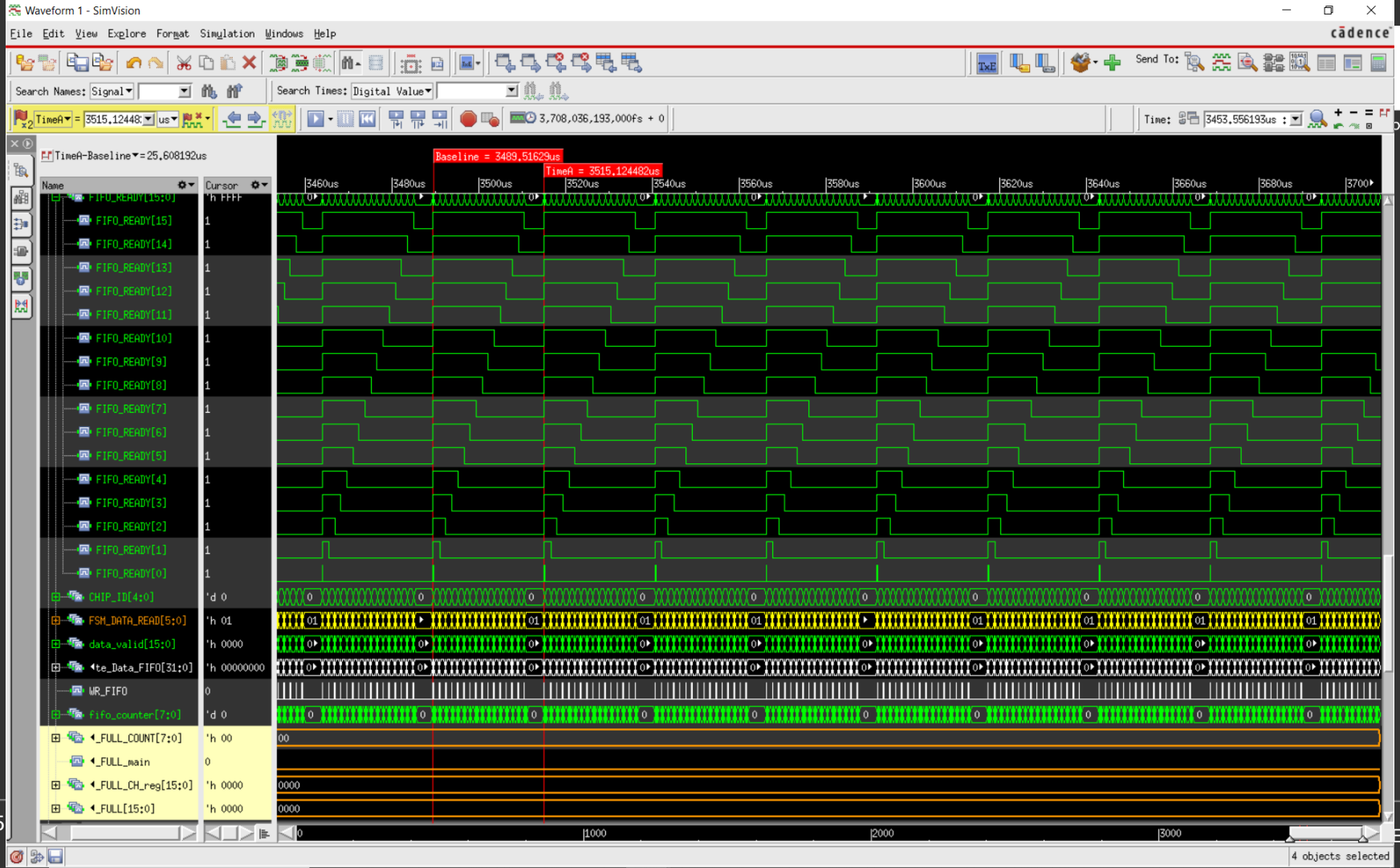


PonRST is low (RC)

Commands and configuration logic

ToAst configuration and “error protection” architecture

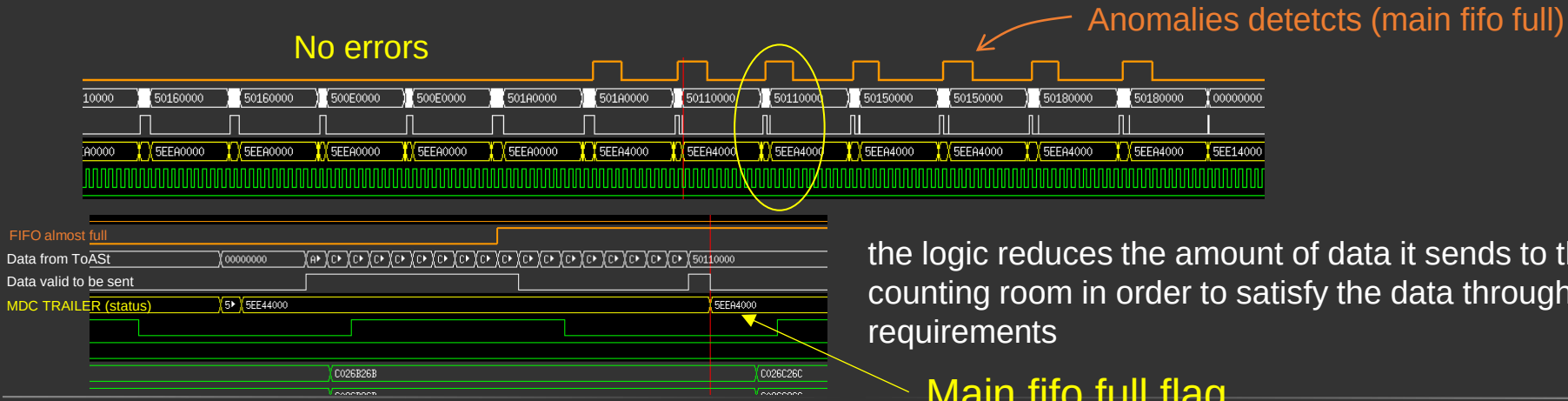
- Procedure like beam test setup
- MDC receive the configuration sequences (readout back on the configuration commands, possible)
- Configuration sequence checked by dedicated logic
- Status_CFG [15:12] counts the number of wrong configuration sequences or commands
- Configuration sequences, saved in FIFO, FIFO depth is . The large FIFO provides the possibility to optimize the configuration of long sequences, multiple ToASt global/local registers in less time.
- For every writing operation on global/local ToASt register, the automatically readback is performed
- In case of errors the information is sent to the counting room
- Broadcast or individual ToASt configuration operation are both implemented (like beam test setup)


Waveform 1 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Search Names: Signal
Search Times: Digital Value
Send To:
TimeA-Baseline=25.608192us
Baseline = 3489.51629us
TimeA = 3515.124482us
Name
Cursor
FIFO_READY[15]
FIFO_READY[14]
FIFO_READY[13]
FIFO_READY[12]
FIFO_READY[11]
FIFO_READY[10]
FIFO_READY[9]
FIFO_READY[8]
FIFO_READY[7]
FIFO_READY[6]
FIFO_READY[5]
FIFO_READY[4]
FIFO_READY[3]
FIFO_READY[2]
FIFO_READY[1]
FIFO_READY[0]
CHIP_ID[4:0]
FSM_DATA_READ[5:0]
data_valid[15:0]
te_Data_FIFO[31:0]
WR_FIFO
fifo_counter[7:0]
FULL_COUNT[7:0]
FULL_main
FULL_CH_reg[15:0]
FULL[15:0]
4 objects selected

Detection of anomalies and errors

Continuous readout operation also in presence of critical conditions

- Several critical errors could compromise the detector readout, for example, SEU (MDC, ToASt), high occupancy due to a significant number of fake or noisy channels, etc.
- The ***goal*** is to develop a continuous readout mechanism capable of sending information of the anomalies and errors to an off-detector location.
- High-granularity detector recovery mechanism at level of off-detector



the logic reduces the amount of data it sends to the counting room in order to satisfy the data throughput requirements

Main fifo full flag