The TRB Readout System

Outline

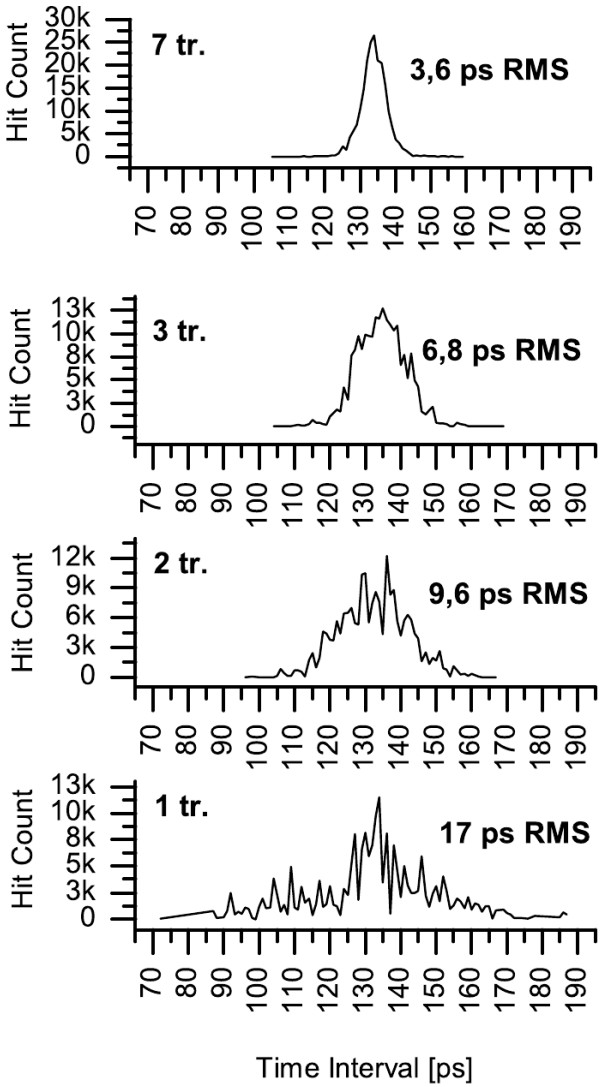
- Motivation
- TRB3 + FEE
  - Two years ago and now
- Applications
- Conclusion

Motivation: Digital Electronics as FEE

- **Use commercial off the shelf FPGAs as FEE**
  - Easily available, industrial quality design, package and documentation
  - Upgrade included (new silicon on the roadmap)
  - Amount of internal resources is very large
  - Vendor independent
- **How to reach that goal?**
  - We “misuse” digital FPGAs in the asynchronous and analogue domain for:
    - Precise Time to Digital Conversion (TDC)
    - Discrimination, ADC, QDC
  - We keep the design small and simple

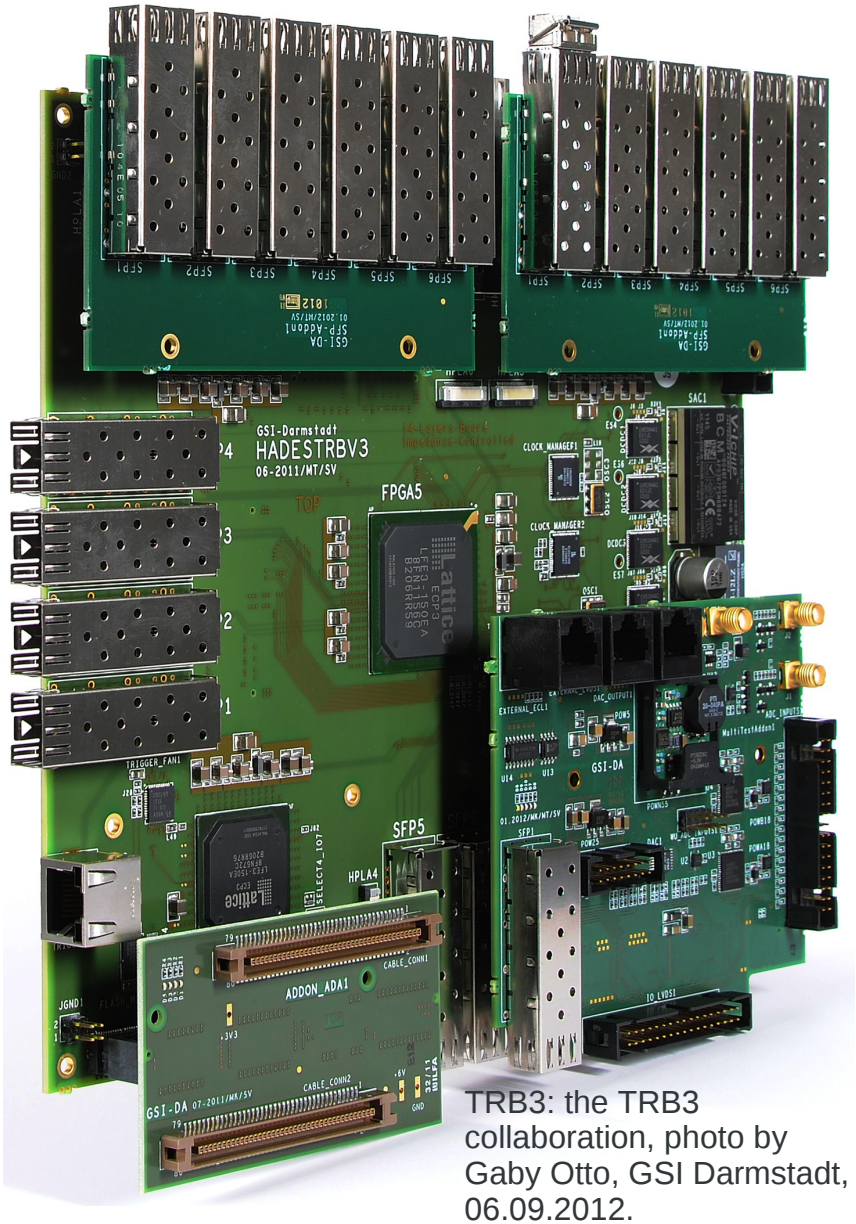
TDC in FPGA: status

- TDC architecture is very powerful
  - 3.6 ps RMS time precision
  - no cut on tails
- Tradeoff for number of channels, time precision and dead time can be adjusted to the needs of the application
  - 64 TDC channels in a FPGA
  - ~10 ps RMS time precision [RMS]
- From an idea (2 years ago) to a working product.....



Published IEEE 2011, E.Bayer et al.

TRB3: Capabilities / Datasheet



TRB3: the TRB3 collaboration, photo by Gaby Otto, GSI Darmstadt, 06.09.2012.

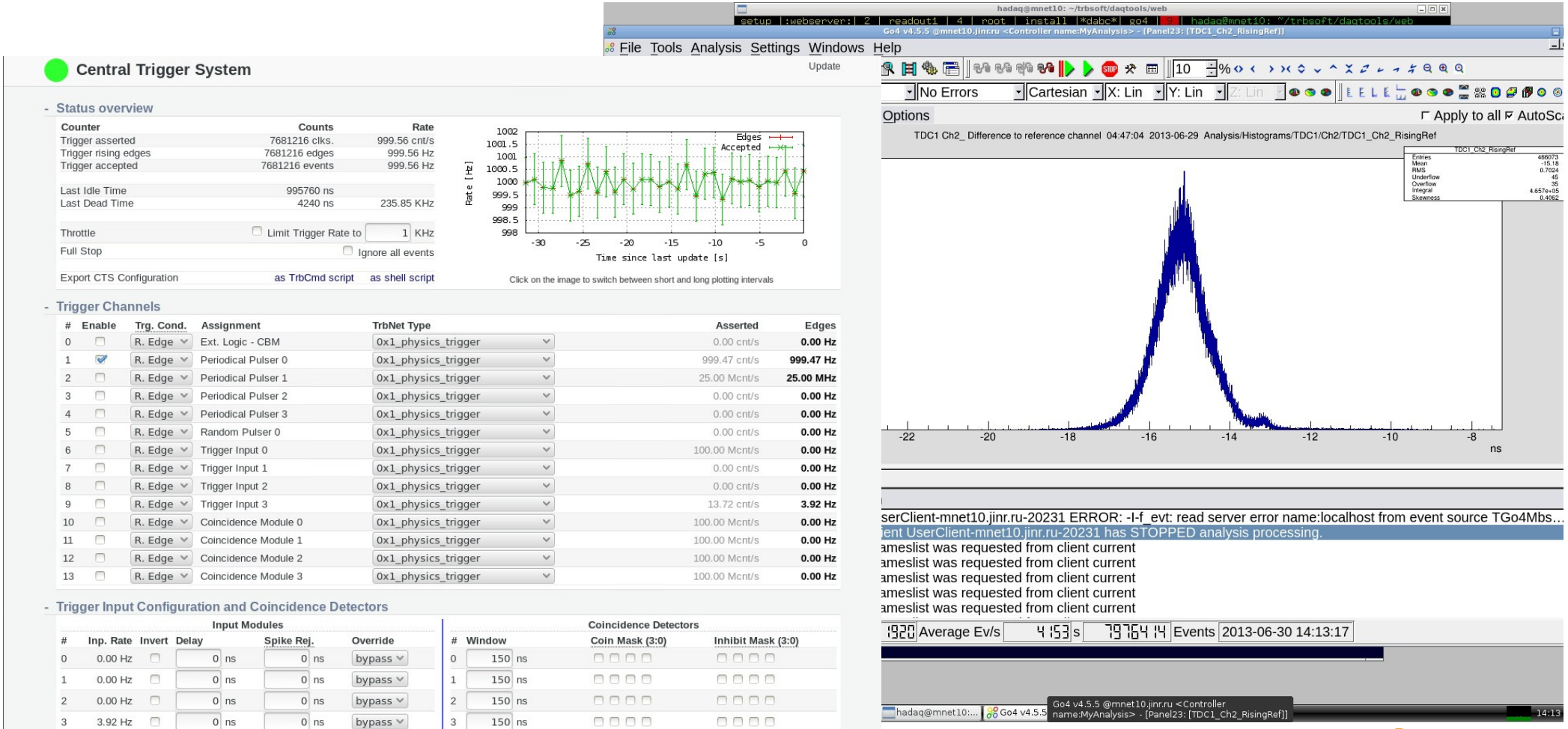
- 5 Lattice ECP3-150EA FPGAs
- 4 peripheral FPGAs as TDCs with 256+4 channels
- The central FPGA acts as Central Trigger System (CTS), 4 channels TDC and GbE controller
- Direct GbE connection for data and slow control; no CPU on board, all implemented in the FPGA
- typical ~10 ps RMS time precision and <20 ps RMS time precision on all channels
- Minimum pulse width <500ps
- 67 MHz max. hit rate per channel
- 700 KHz max. data readout trigger rate
- TrbNetwork for internal communication
- Usable for large system as well as stand alone system: just 48V and GbE are needed to take data
- Can be used as a pure digital board, e.g. as a data collector module or as a TRBNetwork-hub
- Applications: Leading edge and pulse width measurements of discriminated signals from FEE

TRB3: Advantages for the User

- All the connectivity and data transport issues are solved and proven to work reliably:
  - Many years of development of the internal network protocol TRBNet
  - GbE as data transport and SlowControl interface
  - Eventbuilding software for large systems is included (HADES)
  - Analysis software is available, even online software
  - SlowControl interfaces for the TRB, the CTS and the FEE are prepared
  - In several hours of configuration a system is up and taking data

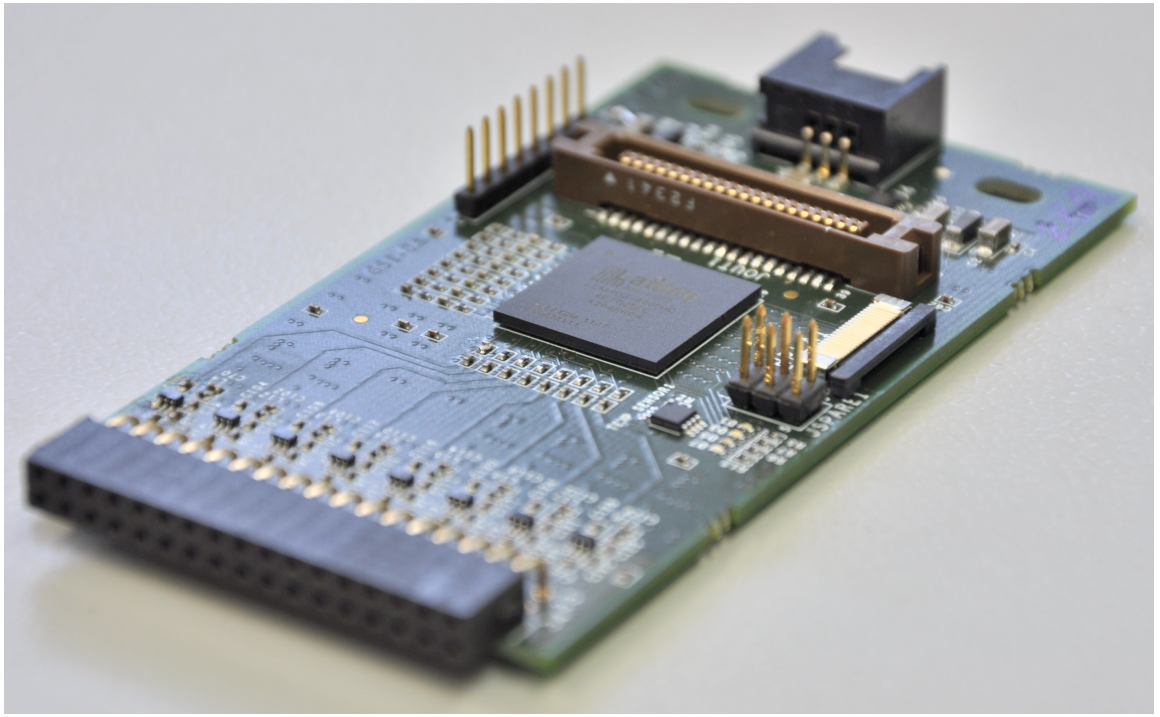
TRB3: Features

- Full Control via Web2.0 applications
- DABC and GO4 fully supported, others analysis code available



How to connect to a MCP/PMT for RICH/DIRC applications?

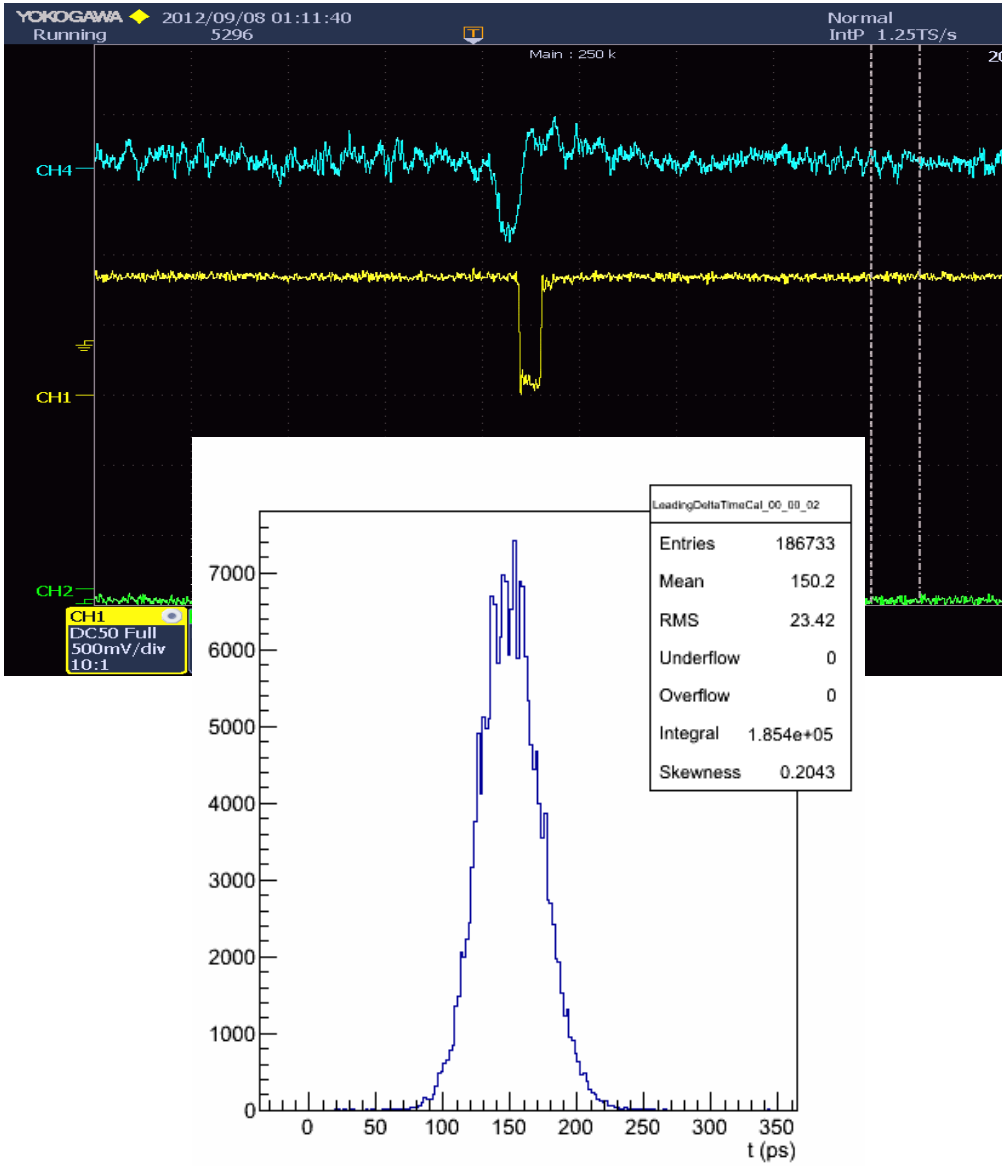
- MCPs/PMTs need amplification and discrimination
- Apply KISS principle: FPGA at the FEE
- The signals from the detector are pre-amplified with commercial amplifiers: MMICs
- Input LVDS buffers in FPGAs are used as discriminators – Lattice MachXO2 is used
- The leading edge time and Time over Threshold is encoded in the digital pulse generated at the output LVDS buffers
- The thresholds are set by using the FPGA as DAC via PWM and low pass filter



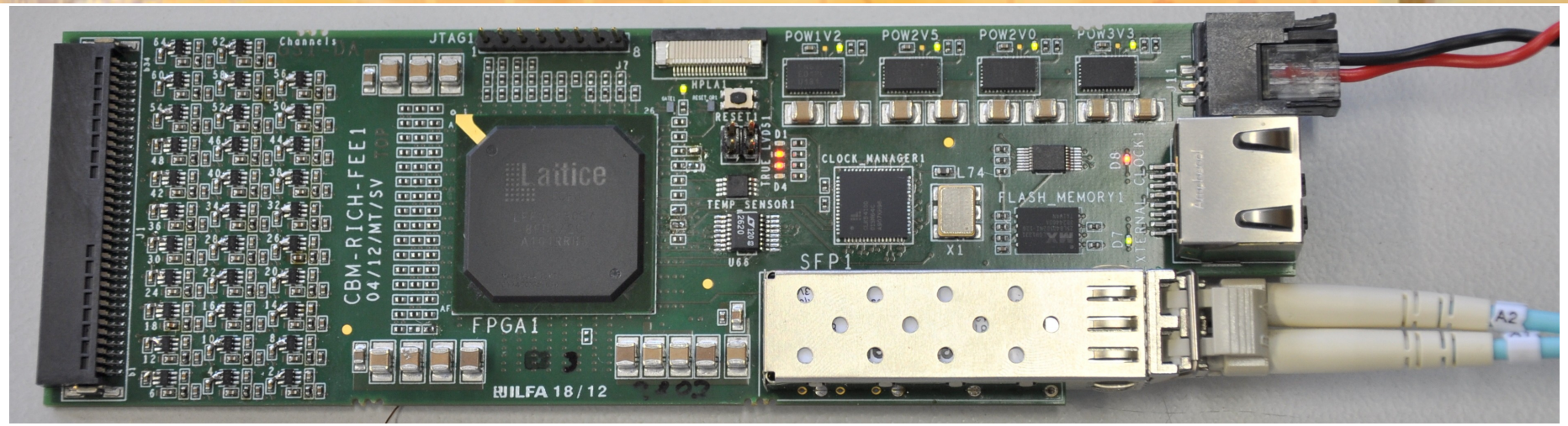
- All the FEE is directly at the detector and only digital signals is are sent out for measurement
- For precise time measurements of the digital pulse the TRB3 is used

FEE: Lab Results

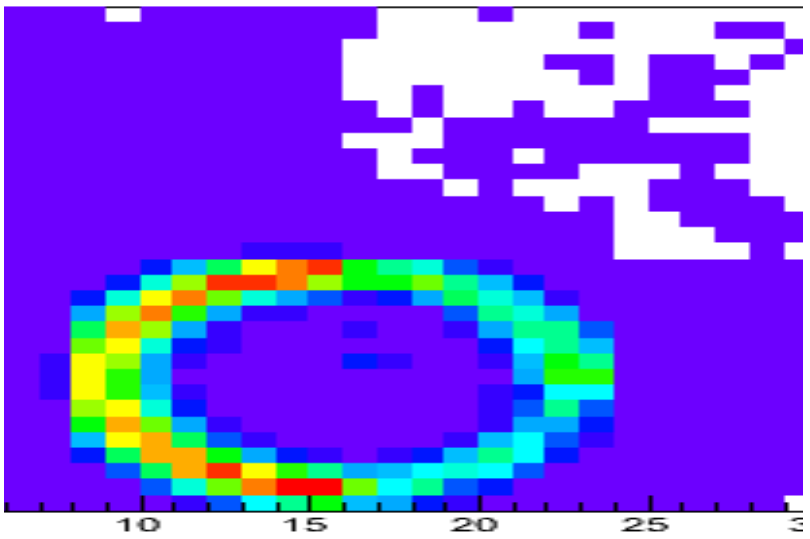
- 500 µV, 6 ns width, analogue signal as input to PCB
- Amplified by factor 40, discriminated at the FPGA-LVDS receiver and sent out to TRB3 as nice LVDS signal
- Threshold is set on the reference LVDS input via a PWM + low-pass with a resolution of <100 µV
- FEE cost (without PCB+connectors) per channel only 0,56€ (16 channel version)
- First tested at the PANDA DIRC beam time in Jülich with 2400 channels PMT/MCP-PMT: Adrian Schmidt: “Cherenkov Rings”
- Specialized versions (connectors) have been built for Barrel-DIRC MCP and BM@N
- Recently tested during the PANDA-DIRC-beam-time in Mainz
  - Result: Operation was fine but need to understand the single photon response in the lab first



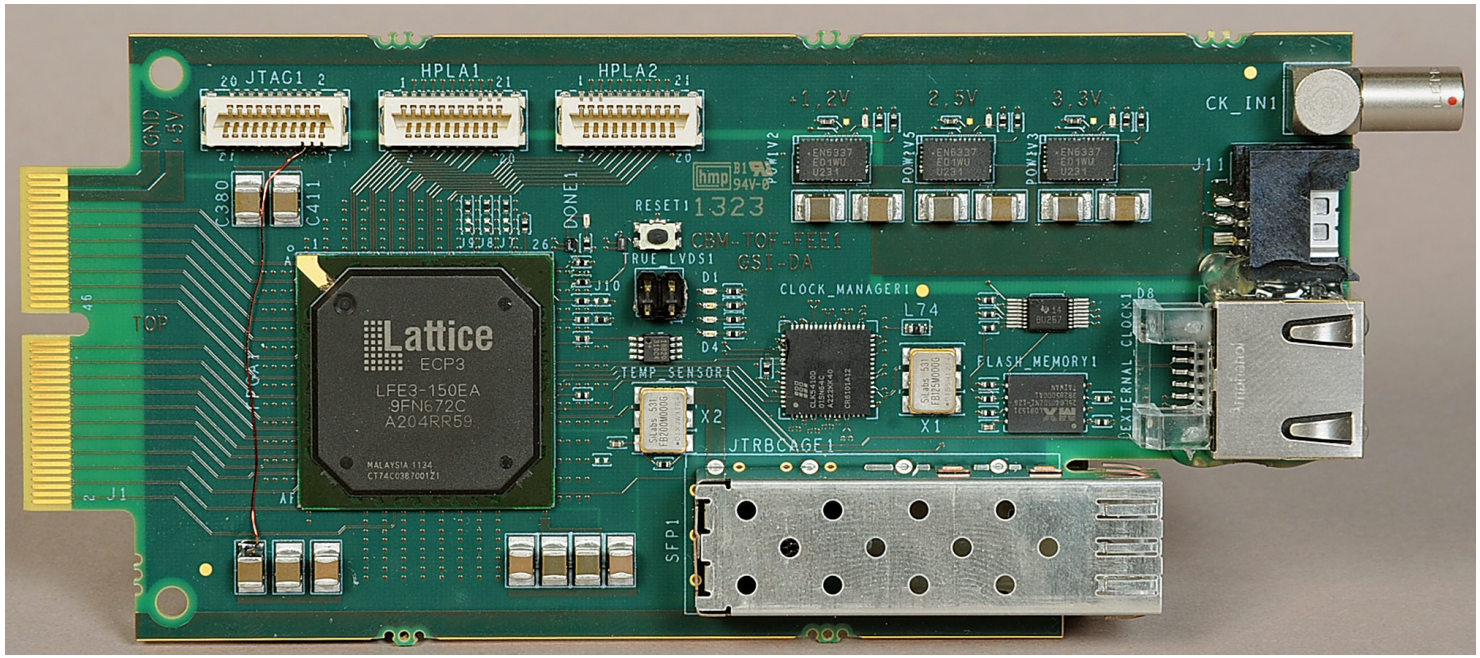
More FEE



- Principle driven to the limit for CBM-RICH
  - 64 channes on 5cmx16cm
  - All analogue (amplification, thresholds, discrimination) + digital (TDCs and DAQ) electronics included
  - Tested during the CBM October 2012 test beam
  - Results are not very good, amplifiers tend to oscillate



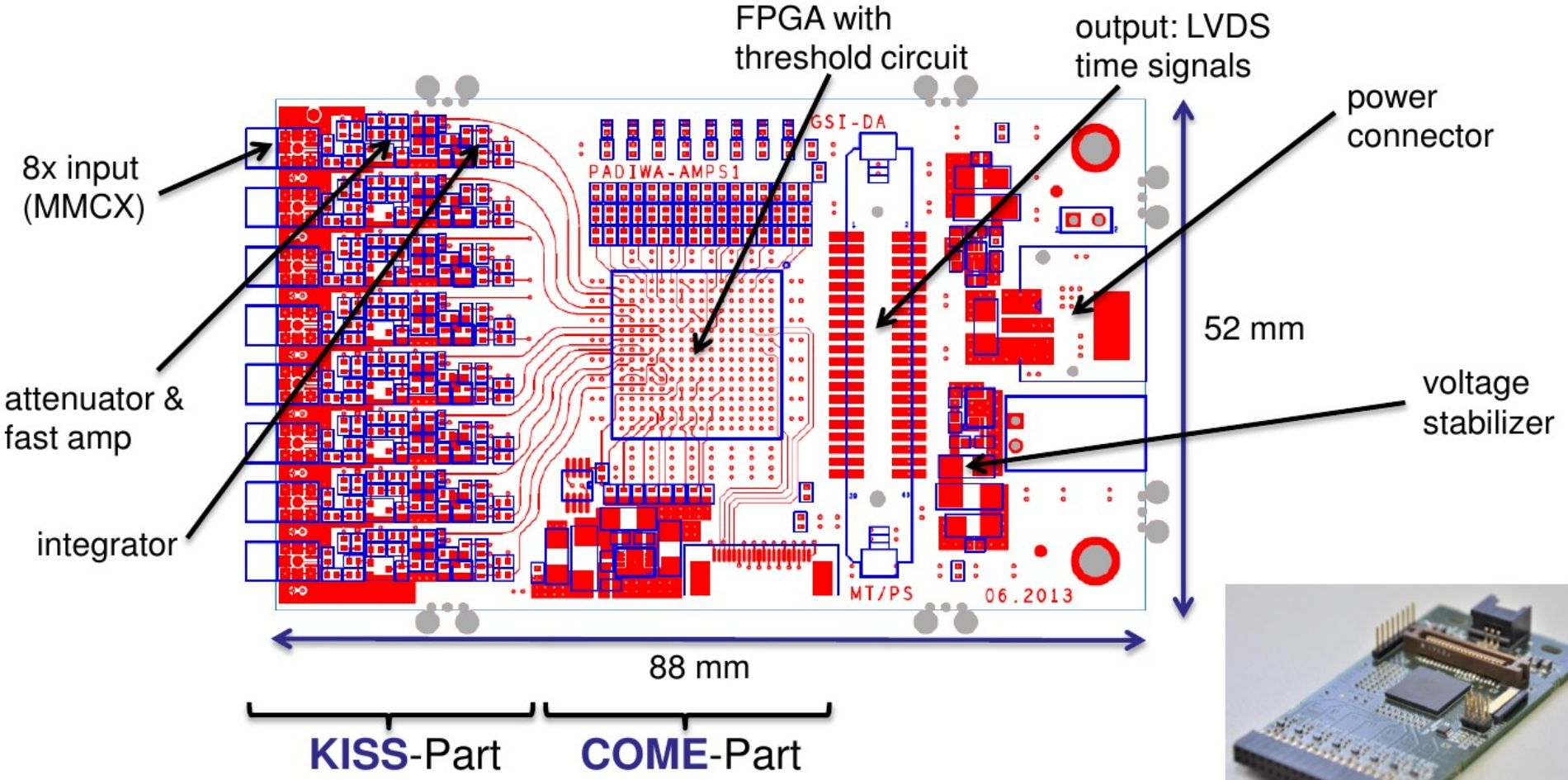
More TRB/FEE Applications



- The TRB3 has not the right form factor for some applications
  - Example: CBM-TOF
  - ¼ of the TRB3, no analogue part
- Animal PET application: 52 channel ADC AddOn in design phase → 208 channels per TRB3
- Many more small adapter boards

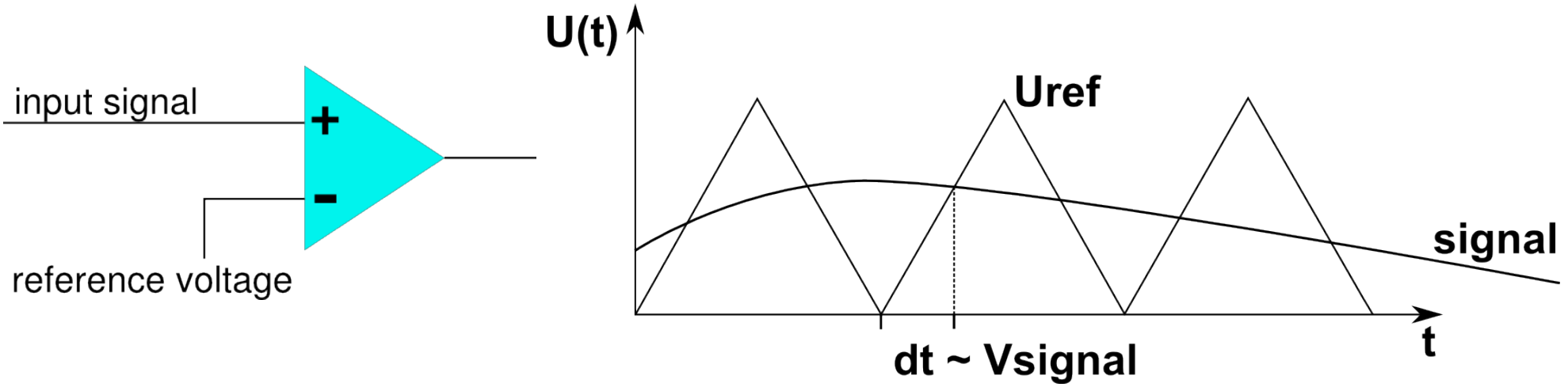
TRB3 FEE: Padiwa-AMPS

- FEE with precise (~0.2%) charge measurement: ECAL + PSD



Basis: PaDiWa front-end board for TRBv3

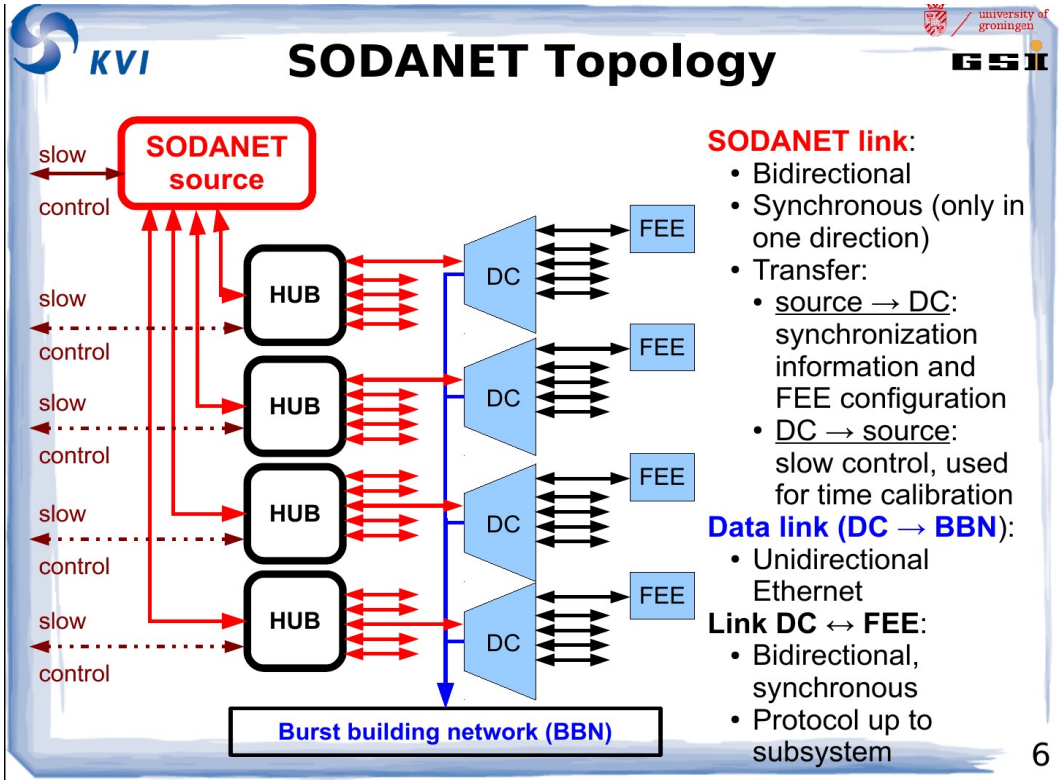
More Analogue Applications



- Multichannel ADC
  - generate ramp on reference pin, measure time until ref. crosses signal
  - Proof of principle done, but no working design available
  - Performance: 64 channel, 10 bit resolution, 20-40MSPS ADC seems possible

Other Digital Applications

- The PANDA Time and Trigger Distribution Network (SODA) is currently developed on the basis of the TRB3
  - All data transport protocol is already finished (TRBNet)
  - The Deterministic Latency messages will be added to the network protocol



From PANDA-FEE/DAQ Meeting in April 2013
Myroslav Kavatsyuk

TRB Readout Platform: Status

- TRB3 produced nearly 100 times
- TRB3 TDC + DAQ and SlowControl functionality established and proven to work reliably in many different locations, also during several beam times
- Development has not ended!
  - Bugfixes
  - Improving performance
  - GbE to 100MBytes/s (currently 50MBytes/s)
  - Currently 256 channels for one edge only
  - KISS-FEE is working but not proven to be as good as the solution with dedicated ASICs: Only the experiment groups can tell
  - Tasks: QDC-FEE and ADC-in-FPGA
- Main Task: Deploying system in many different locations and learn where the deficiencies are and how we can improve: ~25 setups (mainly labs)
  - Main emphasis are PANDA-DIRC and CBM-RICH

TRB3 collaboration

- Main Members: developers
  - Cahit Ugur
  - Jan Michel
  - Grzegorz Korcyl
  - Ludwig Maier
  - Manuel Penschuck
  - Joern Adamczewski-Musch
  - Sergey Linev
  - Matthias Hoeck
  - Andreas Neiser
  - Marek Palka
  - Michael Traxler

- Main Users: bug finders!
  - PANDA DIRC group in Mainz and at GSI
  - CBM-RICH: Christian Pauly (Wuppertal)
  - PANDA-DIRC-WASA: Adrian Schmidt (Erlangen)
  - Many more with small setups:
    - USA, Russia, Israel, etc.

Conclusion

- From the idea 2 years ago with a lot of enthusiasm and manpower involved:
  - TRB3: TDC + DAQ are well established and usable in production
  - Deployment is straight forward

  - KISS-FEE for MCPs/PMTs was built and works in the lab perfectly, but not fully approved up to now by the experiments
  - New FEE is constantly developed as requested
  - Still many things to improve on!
  - A large and motivated team (includes users) keeps the project alive

Thank you for your attention!