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Endoscopic TOFPET & Ultrasound

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The TOFPET ASIC

A Time-Based Readout for Radiation Detectors

André Goerres (FZ Jülich) on behalf of Angelo Rivetti (INFN Torino)

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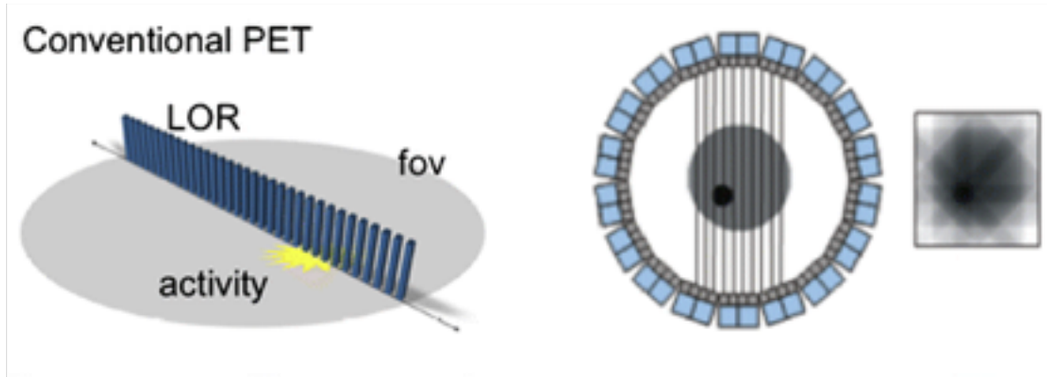
DIRC Workshop, Castle Rauischholzhausen

Overview

- Description of TOFPET and the ASIC
  - The TOFPET experiment
  - Concept of the chip
  - Specifications of the TOFPET ASIC
  - Results of first tests
- Application of TOFPET in PANDA
  - MVD silicon strip readout
- Current status of development

Motivation for using Time-of-Flight in PET

PET: **P**ositron **E**mission **T**omography



Normal PET operation

- Introduce positron-emitting radionuclide (β^+ decay) into patients body, detect annihilation gamma rays.
- Position of annihilation somewhere along the line of response (LOR).
- 2D information by superimposing different LORs.

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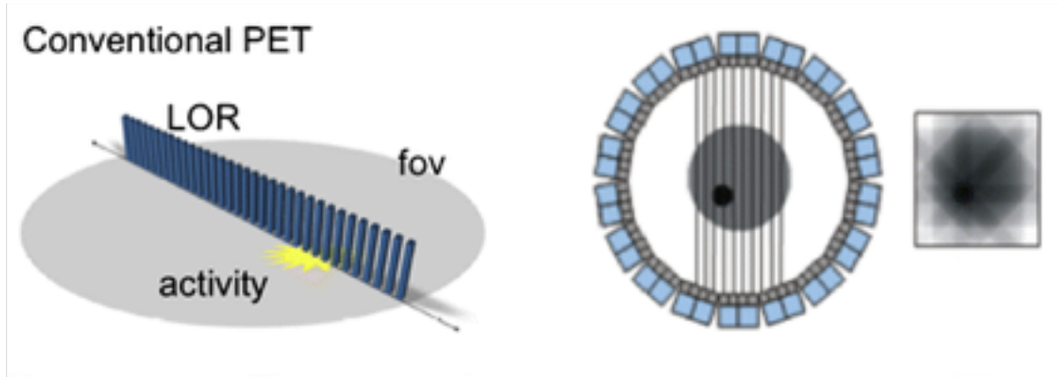

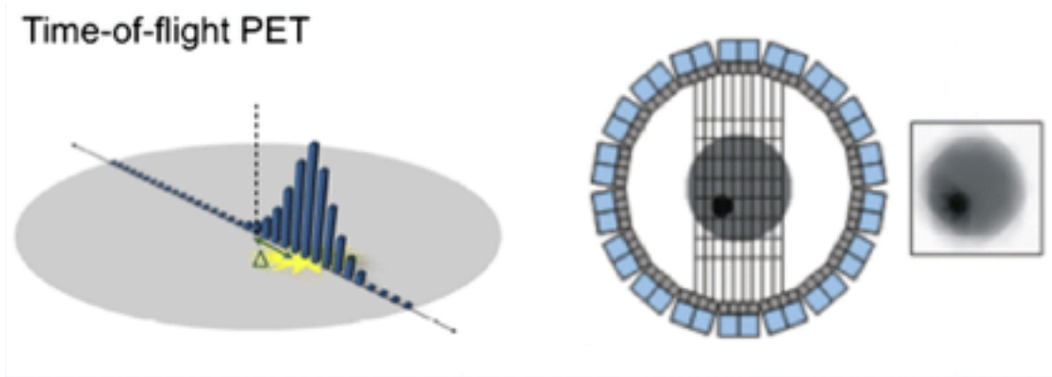

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PET using Time-of-Flight (TOF)

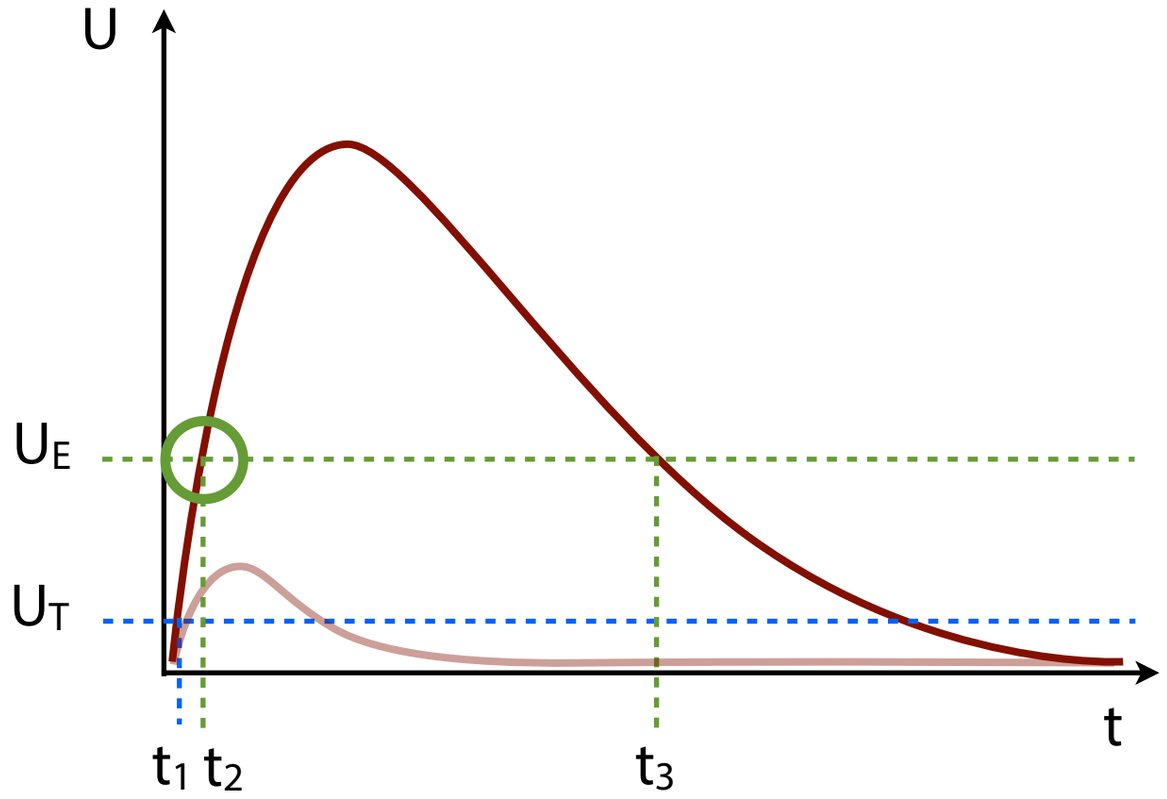
- Again, β^+ radionuclide in body.
- Measure time difference of arriving photons (accuracy ~200 ps ⇒ 3 cm).
- Additional position information alongside LOR.

⇒
- Higher SNR of reconstructed image
- Shorter exam time *and* reduced injected dose

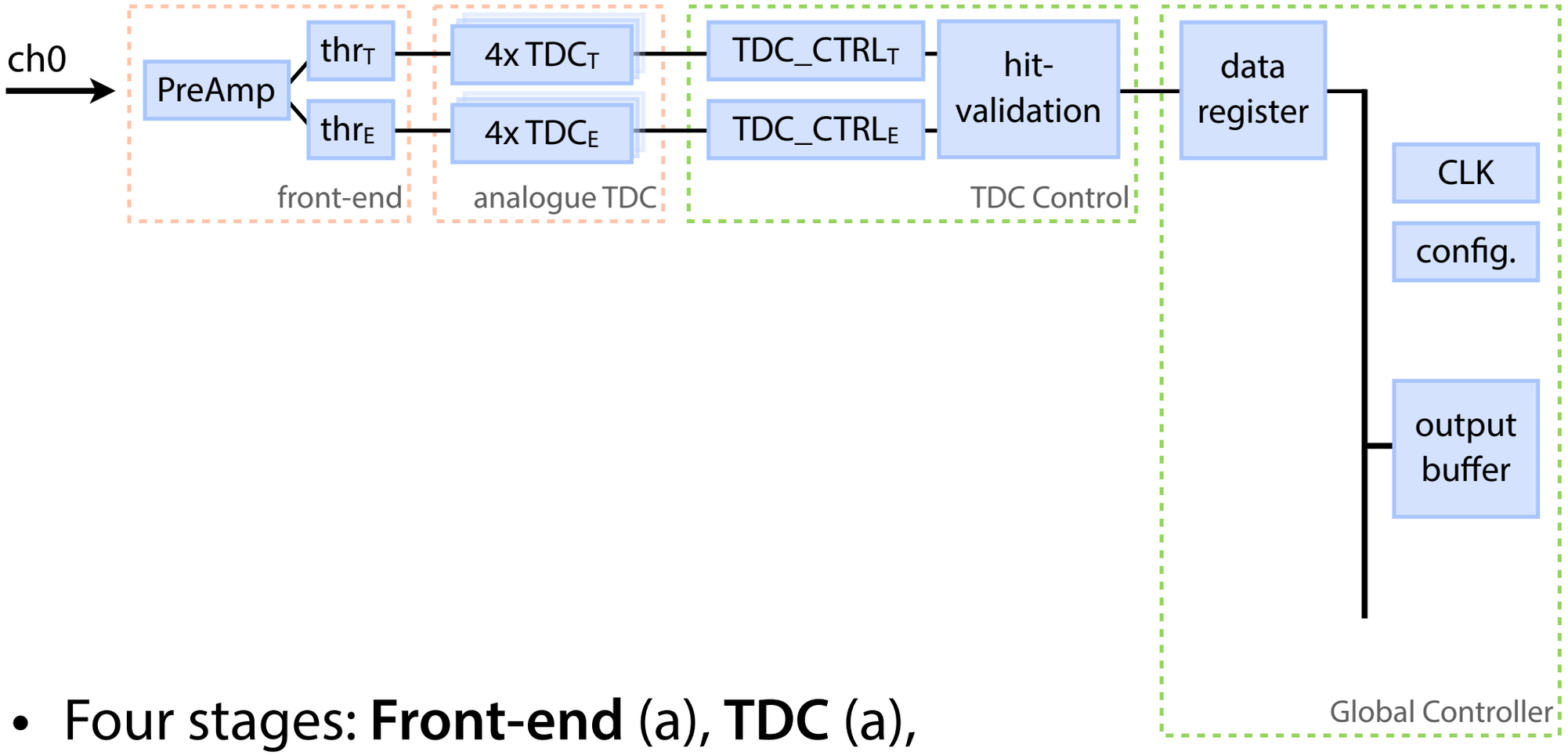
TOFPET ASIC developed by LIP Lisbon in the FP7/EndoTOFPET-US project

Concept of the ASIC

- Readout SiPM, achieve:
  - High time resolution and reduce dark count rate
- Two TDCs per channel
  - Time and energy branch
    (low and high threshold)
  - Energy trigger (t_2)
    validates time trigger (t_1)
- Charge by time-over-threshold (ToT)
  - ToT measurement: t_3 - t_1
  - Time binning: 50 ps (25 ps optional)

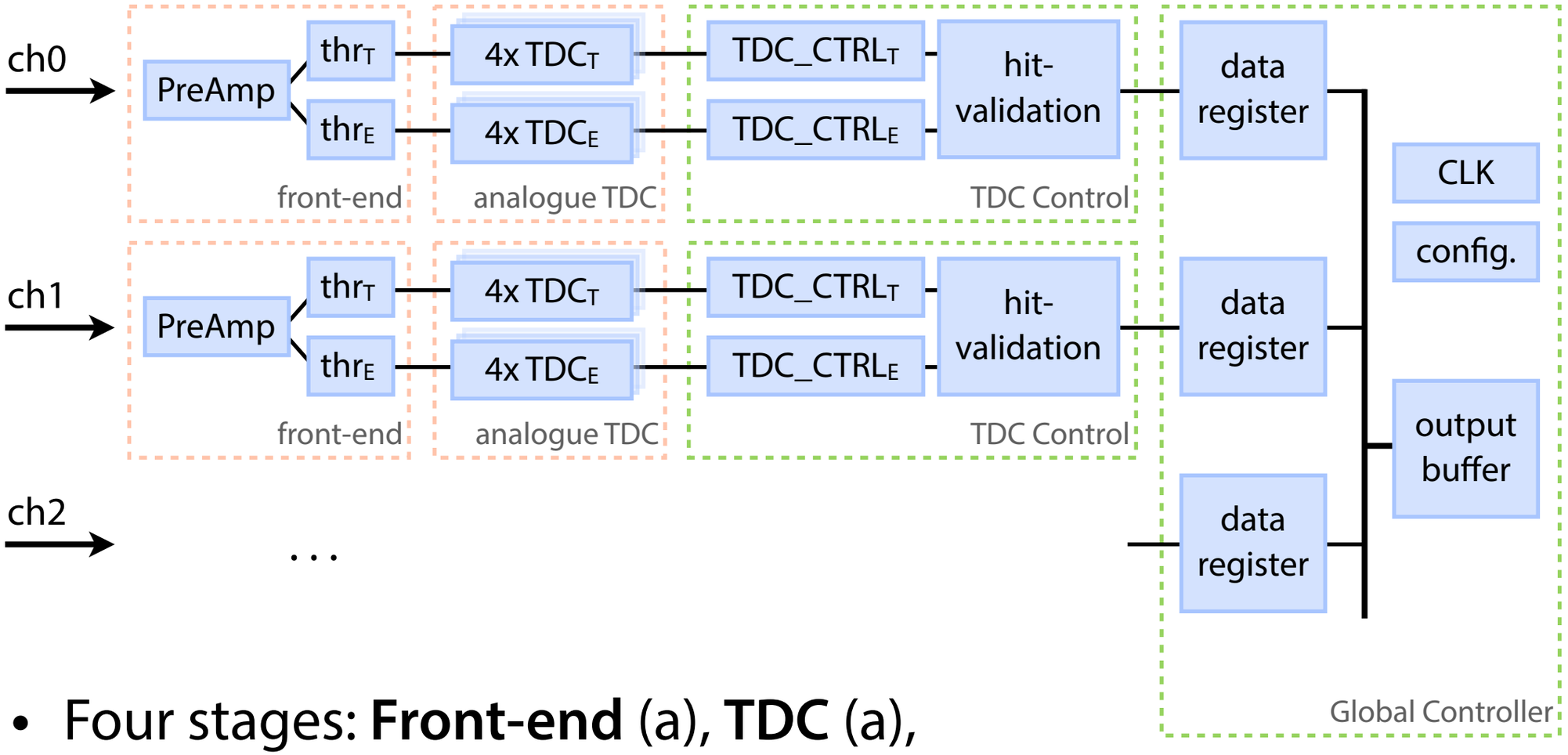


Concept of the ASIC



- Four stages: **Front-end** (a), **TDC** (a),
  TDC Control (d), **Global Controller** (d)

Concept of the ASIC



- Four stages: **Front-end** (a), **TDC** (a),
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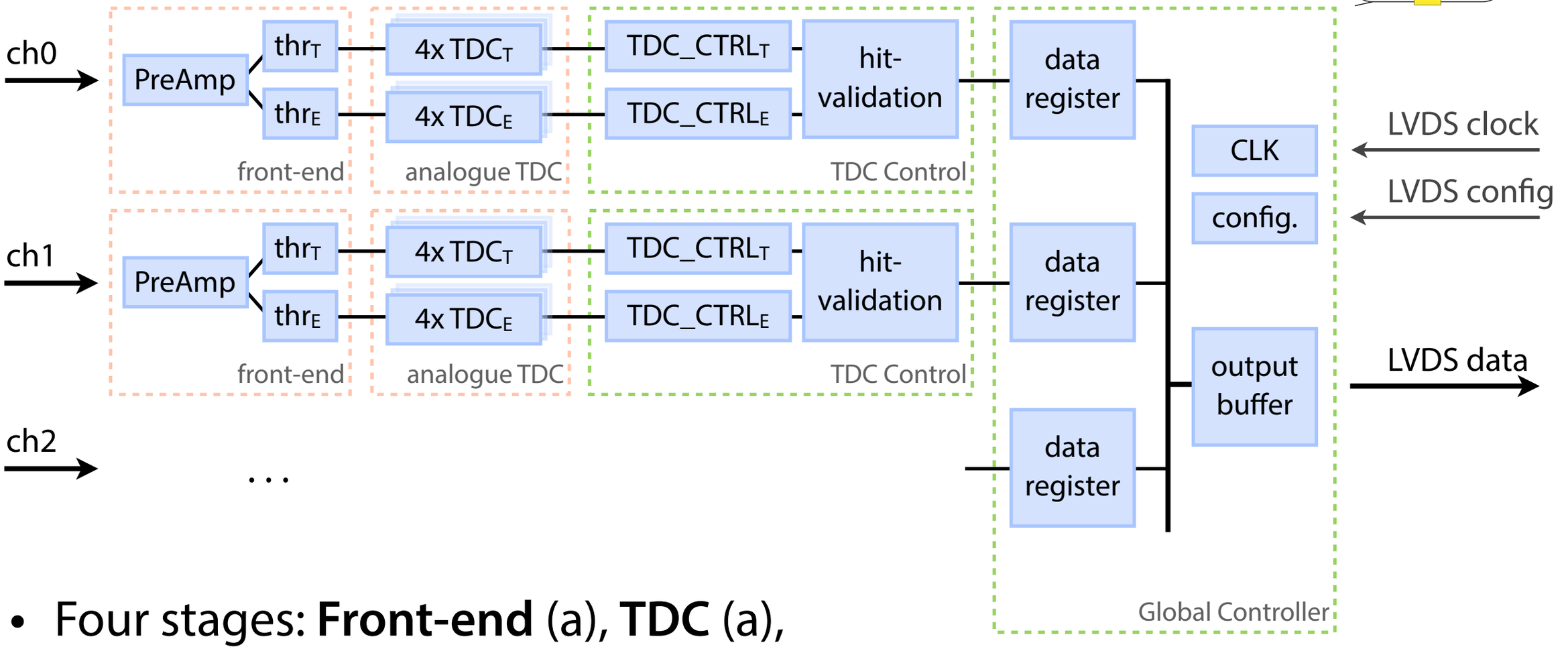
- 64 channels with on-chip DACs

Concept of the ASIC



- Four stages: **Front-end** (a), **TDC** (a),
  TDC Control (d), **Global Controller** (d)
- 64 channels with on-chip DACs
- 160-640 Mbps data output (signals in LVDS standard)
  - One event: 5 bytes (*compressed*) or 10 bytes (*uncompressed*)
- 10 MHz SPI configuration link (LVDS) for bias/channel settings

Analogue front-end

- Pre-amplifier
  - Low Z_{in} pre-amplifier, two polarities
  - Two independent TIA branches for time and energy

TIA: transimpedance amplifier

- Two individual comparators for time and energy
- Fine adjustment of the HV bias of the SiPM
  - 6 bit over 500 mV range
- Selectable delay line for time branch signal
  - Range: 1-6 ns
- Connection to next stage (TDC) via AC coupling
  - Reduces noise in processing

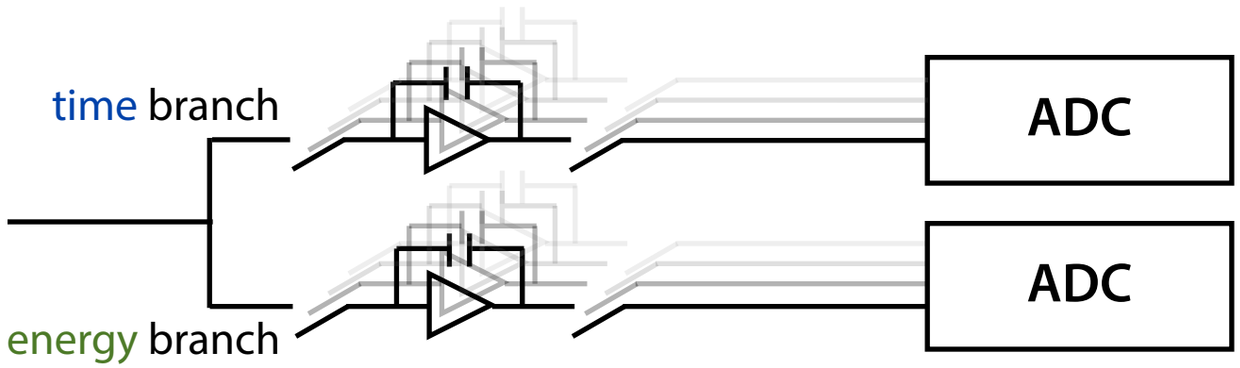
stage 1
front-end

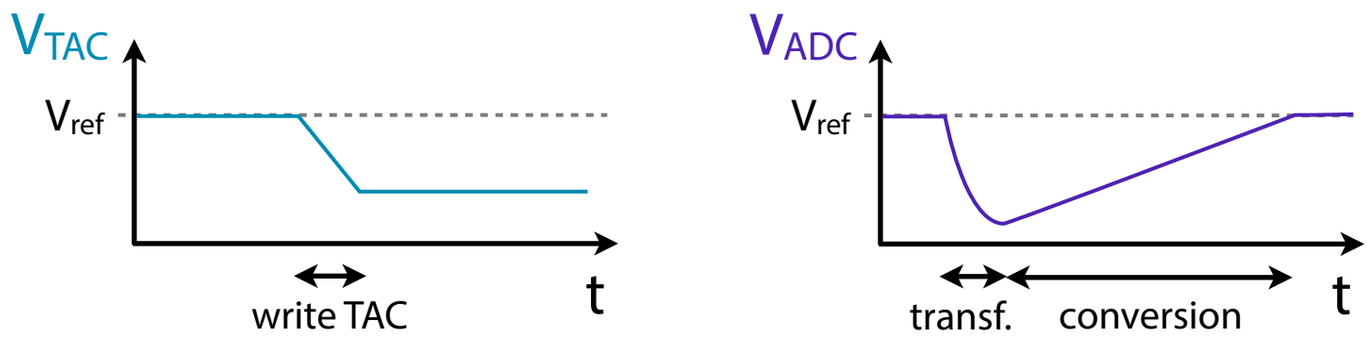
stage 2
analogue TDC

stage 3
TDC CTRL

stage 4
global CTRL

Analogue Time-to-Digital Converter





- Two stages: buffer and convert signal
  - Buffering: discharge a capacitor (TAC)
    - Start: threshold; End: rising edge of clock*
  - Transfer to 4x larger capacitor, linearly recharge with 32/64x smaller current (Wilkinson ADC)
- Increase time resolution by 128/256x (50/25 ps @ 160 MHz)
  - Conversion takes ~ 3 µs (@128x) → buffer multiplicity of 4

ADC: Analogue to Digital Converter
TAC: Time to Analogue Converter

*: Dynamic range 1-3 clock cycles

stage 1
front-end

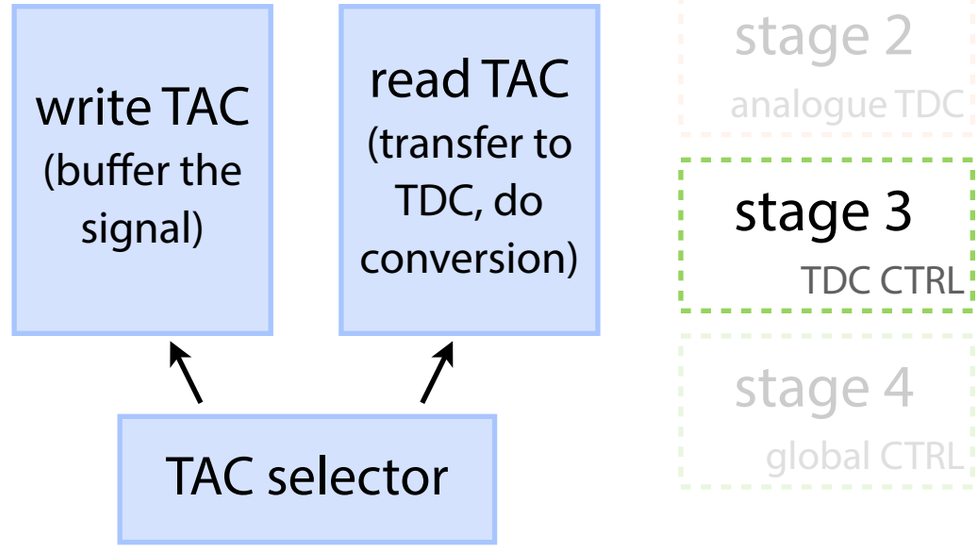
stage 2
analogue TDC

stage 3
TDC CTRL

stage 4
global CTRL

Digital TDC Control (TDC CTRL)

- Controls:
  - Hit validation (discard dark hits)
  - Charging processes:
    - Write TAC: discharging TAC
    - Read TAC: charge transfer
      re-charging TDC capacitor
    - Reset of TAC & TDC
      - Incl. reset of a TAC that was idle for too long
  - Select TAC based on queues
  - Issuing signals for time buffering



- Hit validation in two modes:
  - Synchronous: store with time trigger, discard if energy doesn‘t come
  - Prediction: time delayed, storing with energy trigger

Digital Global Controller (GCTRL)

- Distributes
  - Clock and clock enable signals,
  - Channel / bias settings
- Time buffering
  - Convert counter to grey code (time stamps)
  - Stores 5 x 10 bit time stamps for each channel
    - 2x coarse time (time & energy),
      1x start of conversion (same for time & energy),
      2x end of conversion (time & energy)
- Collects event data and sends it out
- All digital I/O: LVDS

Specifications of TOFPET ASIC

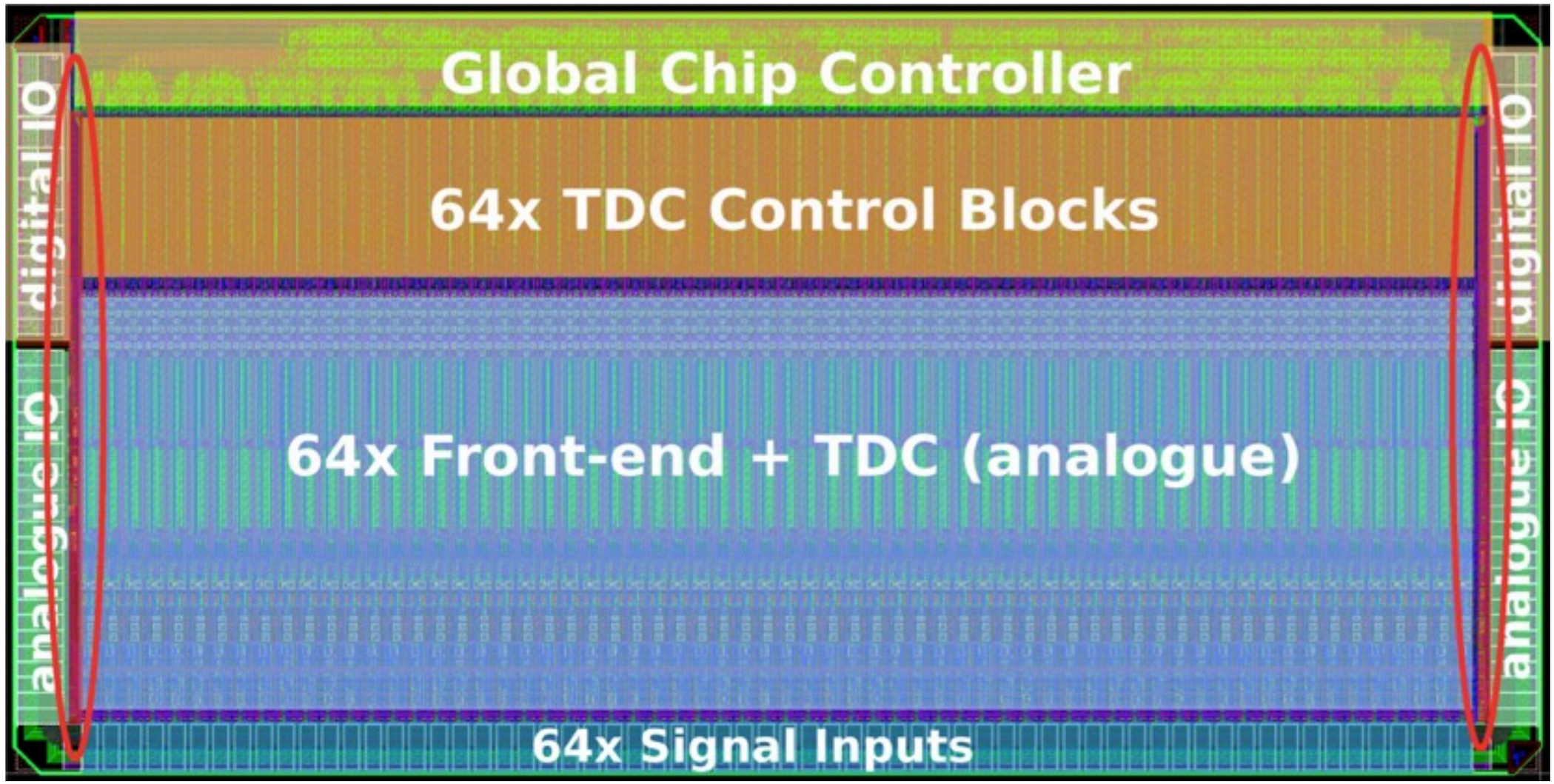
Parameter	Value (version 1)
Area	7.1 x 3.5 mm^2
Number of channels	64, pitch: 102 µm
Channel masking	programmable
Clock frequency	80-160 MHz
Dynamic range of input charge	**300 pC**
SiPM capacitance	70-320 pF
SiPM dark count rate	up to 2 MHz
Max. channel hit rate	**100 kHz**
SiPM fine gain adjustment	500 mV (6 bits)
SNR (Q_{in} = 100 fC)	> 20-25 dB
Amplifier noise (in total jitter)	< 25 ps (FWHM)
TDC time binning	**50 ps** / 25 ps*
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. output data rate	320 Mb/s (DDR: 640 Mb/s)
Power	**7-8 mW per channel**

*: Optionally decrease charging current by factor 2

Note on power:
Bug: pos. & neg. input stages powered
Fix will save ~2 mW/ch

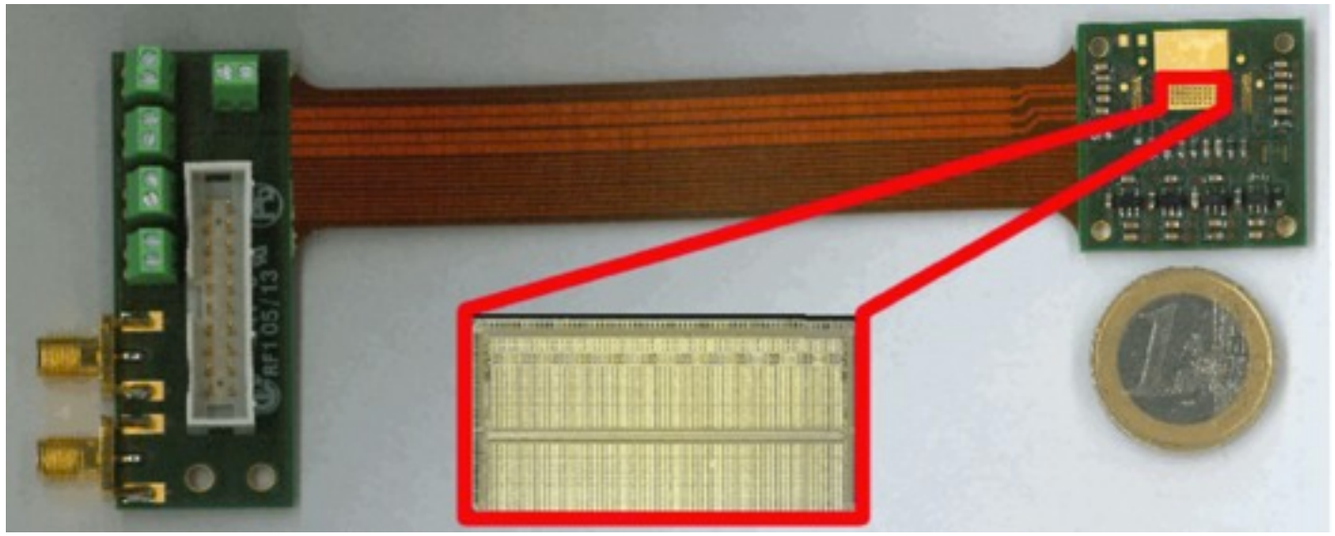
Floorplan of TOFPET ASIC v1

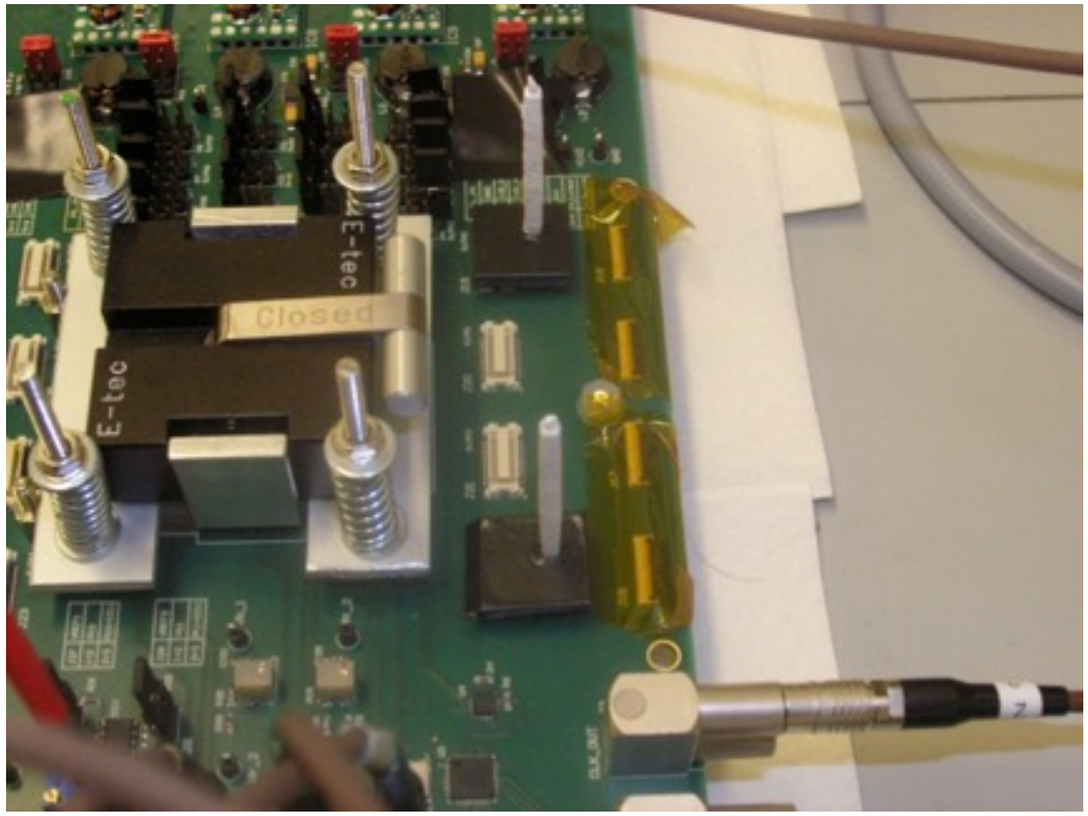
- CMOS 130 nm (IBM), 64 channels on 25 mm^2
- One pad-free edge to attribute two twin chips back-to-back



Highlighted areas: bias and calibration circuitry

Testing the chip in Torino and Lisbon

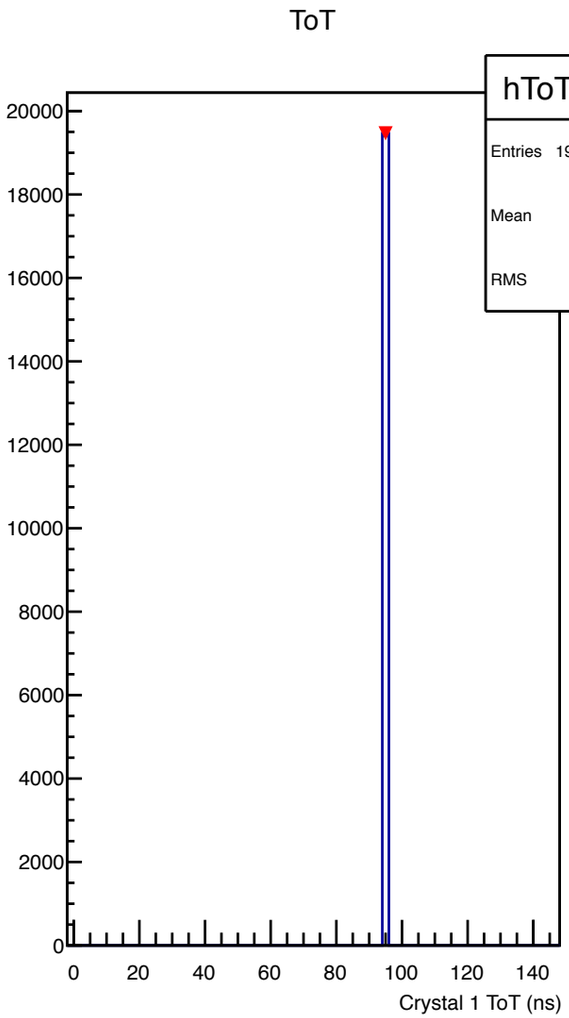


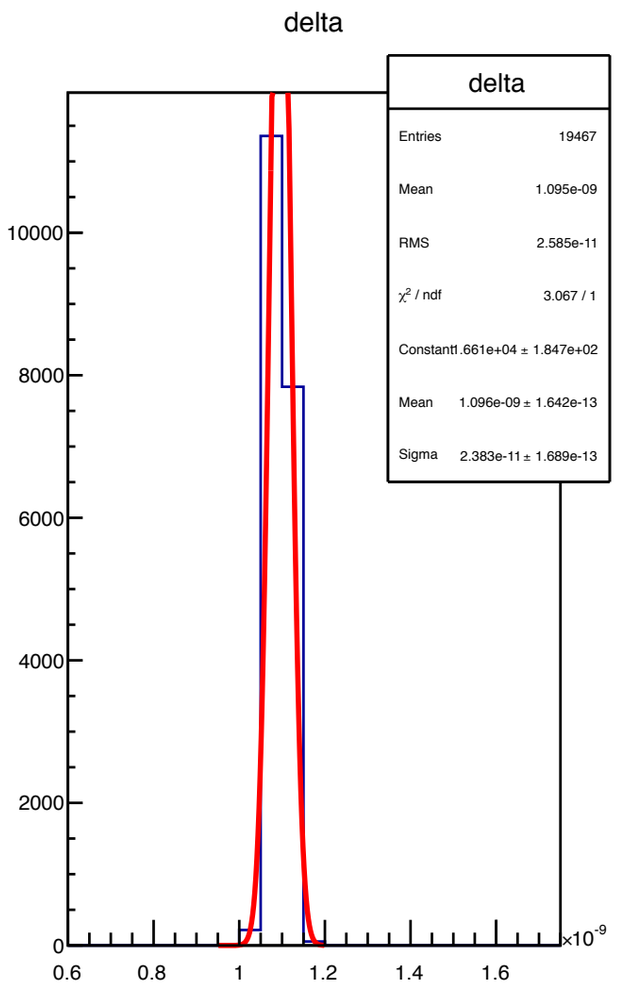


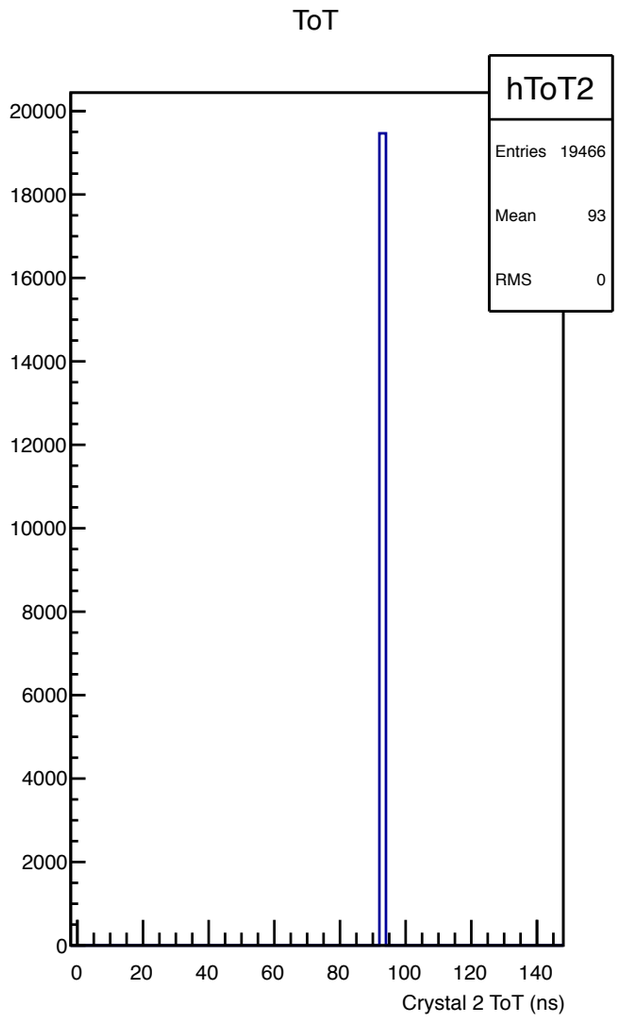
Top: Torino test board, 64 channels
Right: Lisbon test board, 2x64 ch. (back-to-back)

- External pulse and readout via Xilinx ML605
- Tests running since February 2013

Time resolution tests



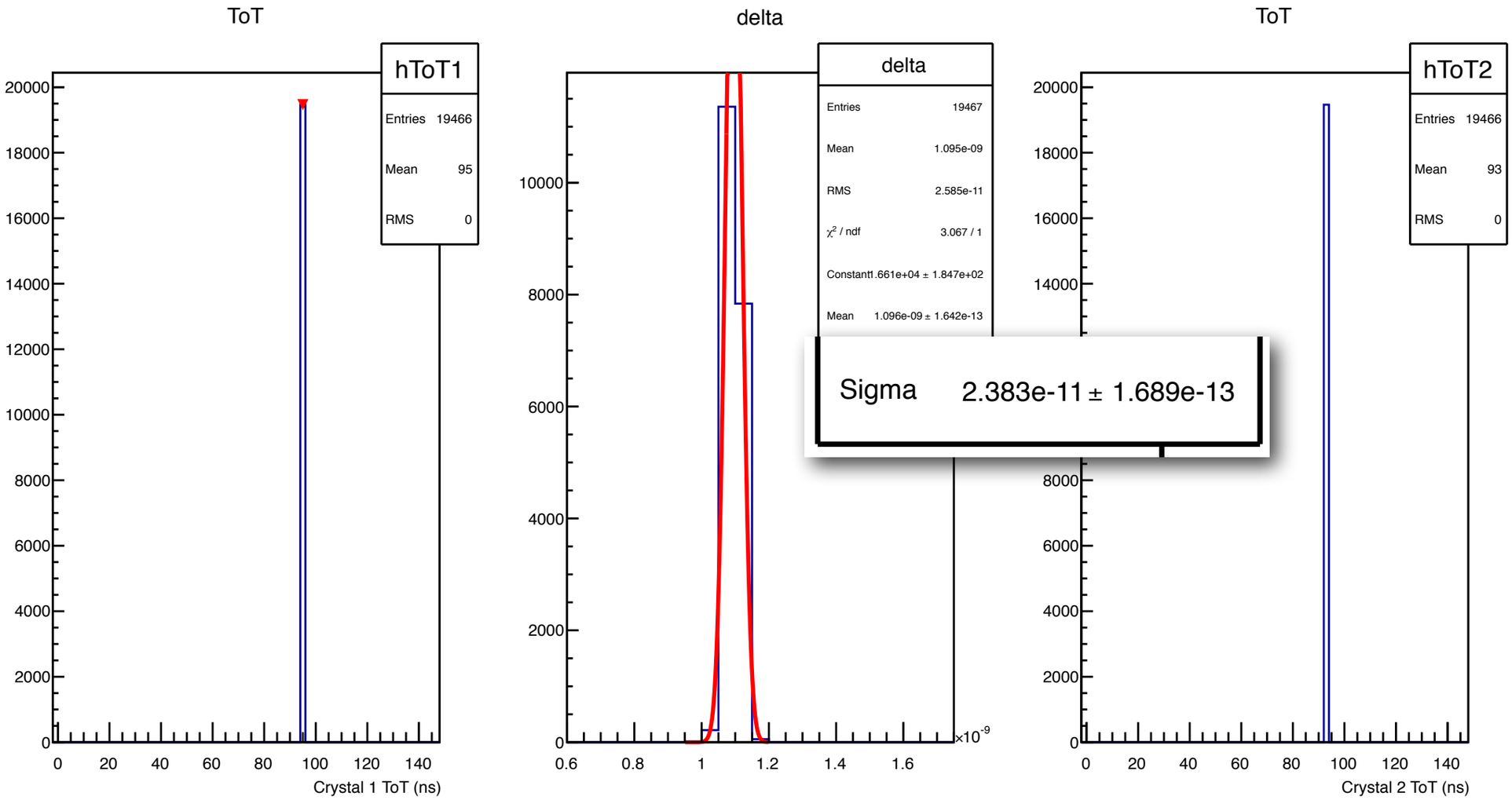




Tests done
at LIP Lisbon

- ToT measurement for test pulses (~ 95 ns)
  - Side plots: ToT values for coincident pairs of channels
  - Center plot: coincidence time histogram
- Sigma of coincidence variation (time resolution): **24 ps**

Time resolution tests



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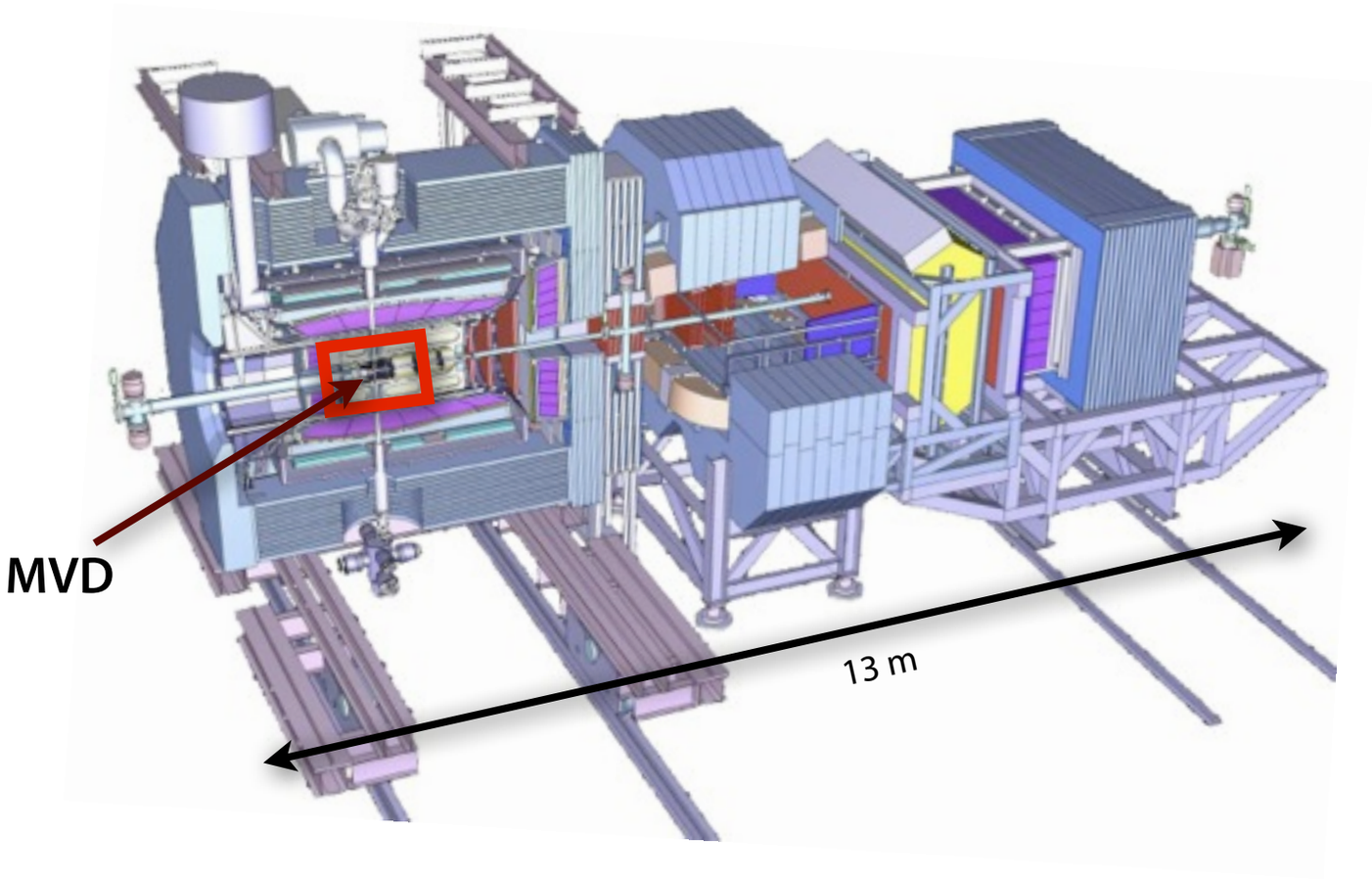
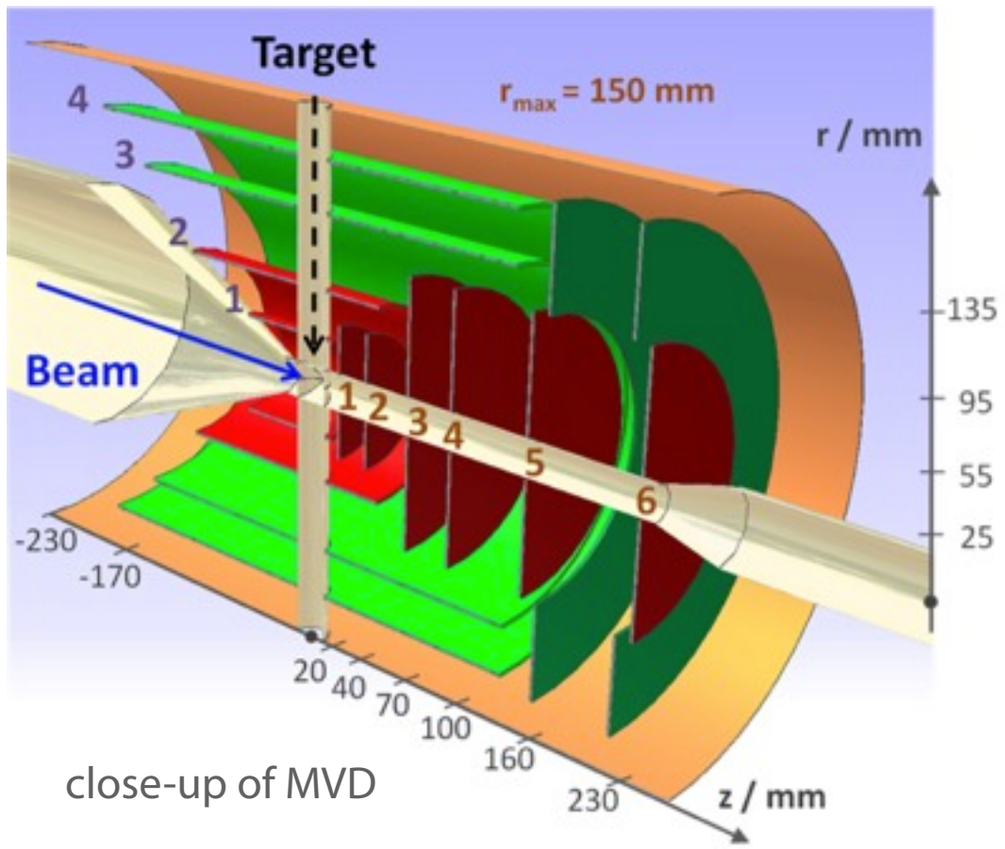
Known issues with TOFPET ASIC

- Power bug: both input stages are powered
  - Solution: power off the unused one
- Non-linearity between time over threshold and energy
  - Will be solved in next version
- Density of digital part very high (TDC CTRL: ~85%)
  - Change to area optimized technology
  - Optimize code structure

} more later

Application of TOFPET chip: PANDA MVD





close-up of MVD

- PANDA: particle detector, p^+-p^- collisions with 1.5-15 GeV
- MVD: **M**icro **V**ertex **D**etector, innermost tracker
  - Two parts: silicon pixel ($10.5 \cdot 10^6$ ch.) and strip ($1.6 \cdot 10^5$ ch.)
  - Readout of MVD strips with modified TOFPET ASIC

Readout of MVD Silicon Strips

- General parameters match the MVD requirements

	Area	Ch. pitch	Hit rate	Time bin.	CLK	Deadtime	Power
TOFPET	7.1 x 3.5 mm²	102 µm	< 100 kHz	50 ps	80-160 MHz	~ 20-40 ns	7-8 mW/ch
MVD req.	< 8 x 8 mm²	≈ 50 µm	< 40 kHz	< 20 ns	155.56 MHz	< 6 µs	< 8 mW/ch*

*newer simulations: < 4 mW/ch

- Differences to solve:
  - Signal shape / capacitance ⇒ redesign analogue part
  - Channel pitch ⇒ try to make a bit smaller, rest with FE layout
  - Power consumption ⇒
    - Slower clock (40 MHz?), clock gating
    - Redesign digital TDC control
    - Tune analogue part

Ongoing changes for MVD version

- Change of technology (IBM 130 nm → UMC 110 nm)
- Redesign of analogue part
  - Different signal shape/height from silicon strips
  - Matching the amplifiers, new comparators, …
- Work on digital part (mostly common enhancements)
  - Redesign TDC CTRL (code structure much clearer & simpler)
  - Protect for Single Event Upsets (SEU)
  - Hit validation also from neighboring channels
  - Bug fixing

Current status of development

- TOFPET ASIC v2:
  - Common enhancements in digital part with MVD development
  - Analogue part works (only non-linearity and power bug)
  - Common form factor needs to be decided

- PASTA v1:
  PANDA **St**rip **A**SIC
  - Changes in design started in beginning of 2013
    - Finish expected in December 2013
    - Submission of first version planned for March 2014
  - Analogue part:
    - Front-end: Concept for redesign ready, start with layout soon
    - TDC: Switched to UMC, add minor details

Current status of development

- PASTA v1: cont.
  - Digital part:
    - Redesigned code: TDC CTRL ~60%, GCTRL 0% *
    - Switch to UMC: TDC CTRL 100%, GCTRL 0%
    - SEU protection: TDC CTRL was ~90%, then decision to redesign code

*: only time stamp buffers

  - **Preliminary** enhancement from redesigning:
    - Power and area occupation down to ~10-20% of values before

  - Formal collaborative agreement between PASTA and TOFPET/LIP has to be established soon

Conclusion

- TOFPET ASIC designed for readout of SiPM
  - max. hit rate: 100 kHz, dead time: ~ 20-40 ns
  - time binning: 50 ps, 25 ps optional (@ 160 MHz)
  - power: currently 7-8 mW/ch
- Application in PANDA MVD
  - Adapt to silicon strips instead of SiPM (analogue part)
  - Include SEU protection, switch technology
- More discussions @ PANDA meeting next week
  - Angelo Rivetti, rivetti@to.infn.it

Thank you!

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People involved in TOFPET ASIC and PASTA:

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[3]: INFN - Istituto Nazionale di Fisica Nucleare sez. Torino

Image resources

- p. 2: The future of hybrid imaging, Thomas Bayer et al. (2011) http://link.springer.com/article/10.1007%2Fs13244-011-0069-4/fulltext.html#Fig5
- p. 11: Floorplan, Manuel D. Rolo, LIP Lisboa (2013)
- p. 12: Test benches for chip characterization, Manuel D. Rolo, LIP Lisboa (2013)
- p. 13: Time resolution test results, Manuel D. Rolo, LIP Lisboa (2013)
- p. 15: PANDA Technical Design Report for the Micro Vertex Detector, PANDA Collaboration (2013)

Endoscopic TOFPET & Ultrasound

Combined TOF-PET (200 ps time resolution), ultrasound imaging and endoscopic biopsy

PET components:
- dSiPM/crystal endoscopic probe
- aSiPM/crystal external plate

ENDO TOFPET US
Endoscopic TOFPET & Ultrasound

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