DIRC2013

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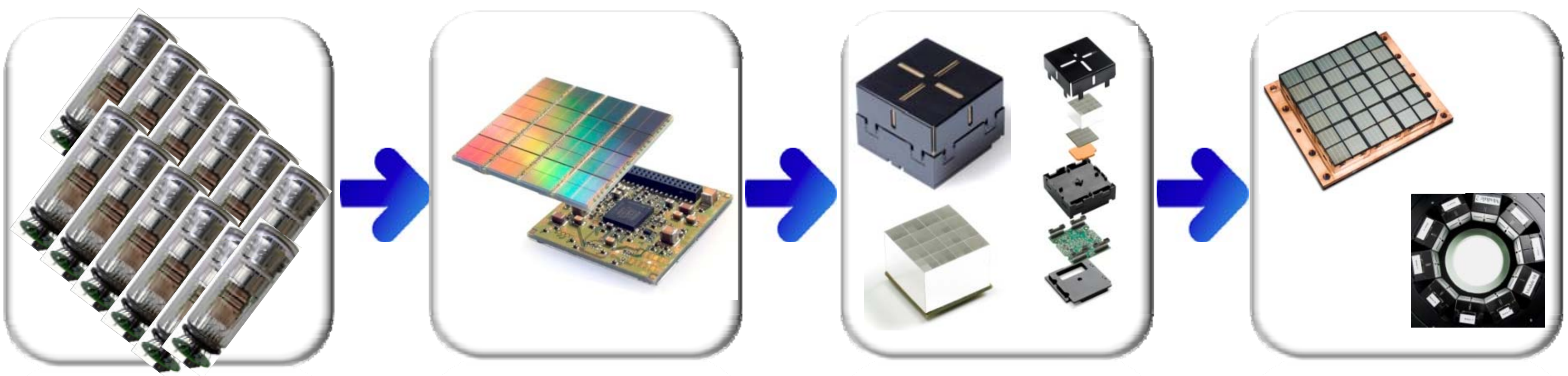
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Digital Photon Counting (DPC) – a scalable light detection technology with high temporal resolution

Dr. York Haemisch, Senior Director, Philips Group Innovation
Philips Digital Photon Counting, Aachen, Germany



OUTLINE

- **DPC represents industry trend(s)**
- **SiPM: analog vs. digital**
- **Benefits of DPC technology**
- **First POC's: PET & FARICH**
- **DPC technology concept & market approach**
- **Future Developments**

Trends: Solid State, Digitization & Integration

Transistor

Television

Photography

Telephony

+ SOFTWARE !

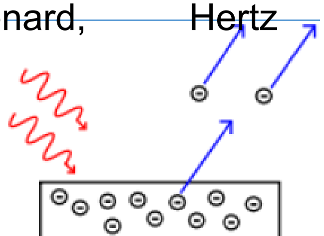
X-Ray imaging

Next?: Light Detection

> 100 years of light detection: From **Photomultiplier Tubes** (PMTs) to **Photodiodes** (PDs), **Avalanche Photodiodes** (APDs) to Arrays of Geiger-Mode APDs (**Silicon Photomultipliers** (SiPMs)

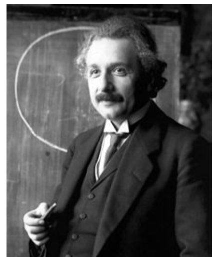
1887

Lenard, Hertz



Photoelectric Effect

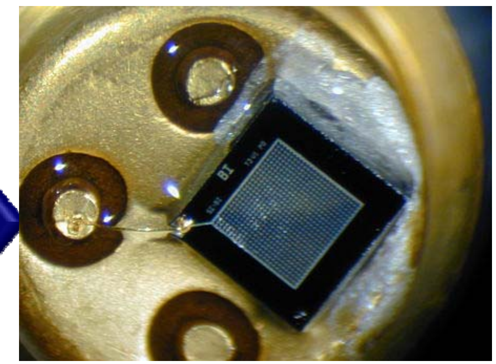
1905

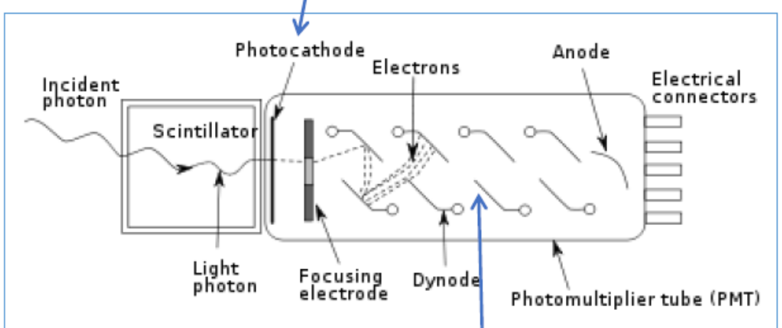


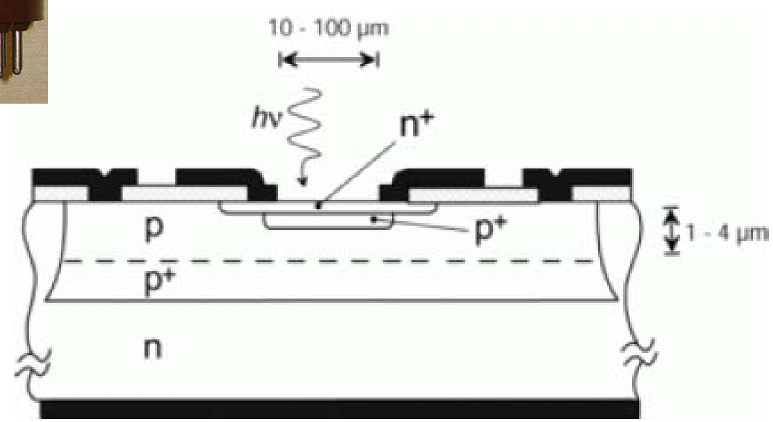
1934

1980's

Saveliev & colleagues



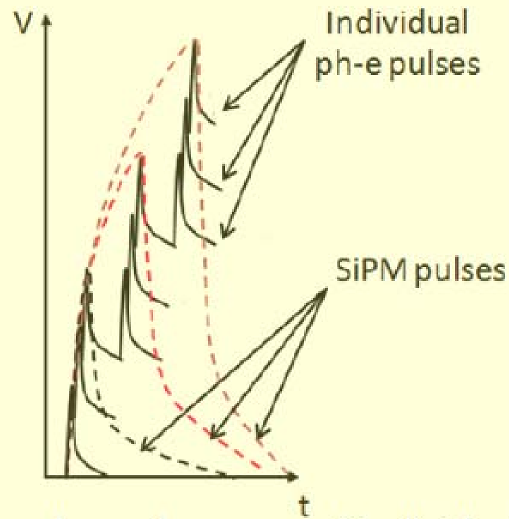




Secondary electron emission

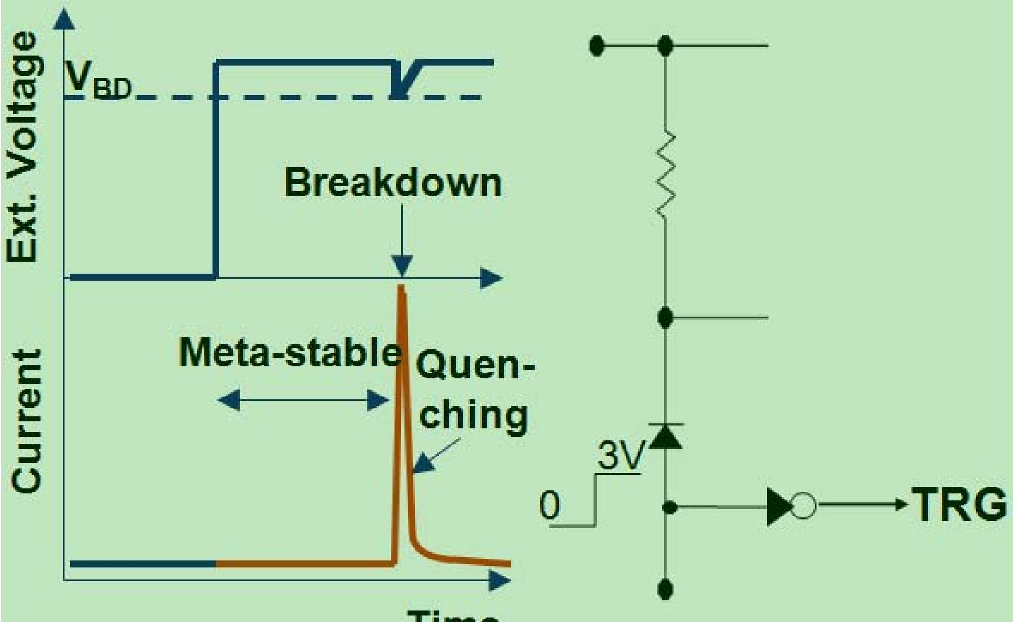
The DPC Takes Advantage of the Binary Nature of the Geiger-Mode APD

Analog SiPM



- Signal: analog sum of individual pulse amplitudes
- amplitudes depend on gain
- gains depend on temperature
- temperature drifts: 2-8%/K

Digital Photon Counter (DPC)

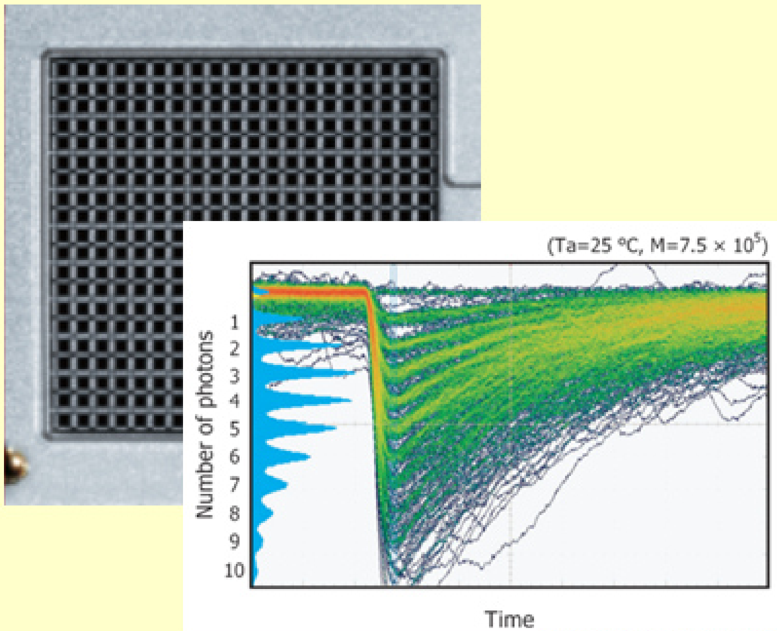


- Signal: digital sum of trigger bins & digital time stamp from TDC
- amplitudes are not relevant
- no gain dependency, reduced temp. drift: 0.33%/K

"Therefore, while the APD is a linear amplifier for the input optical signal with limited gain, the SPAD is a trigger device so the gain concept is meaningless."
(source: Wikipedia)

DPC: Front-end Digitization by Integration of SPAD & CMOS Electronics

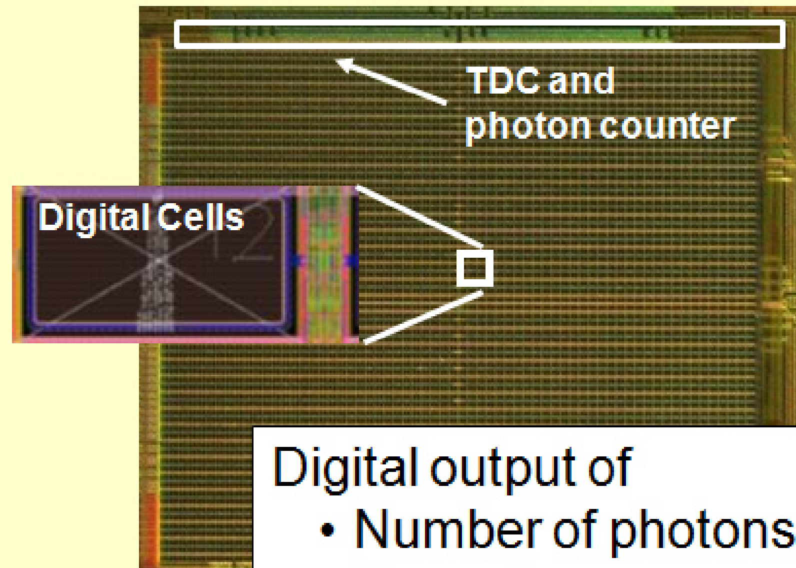
analog SiPM



www.hamamatsu.com

Summing all cell outputs leads to an analog output signal and limited performance

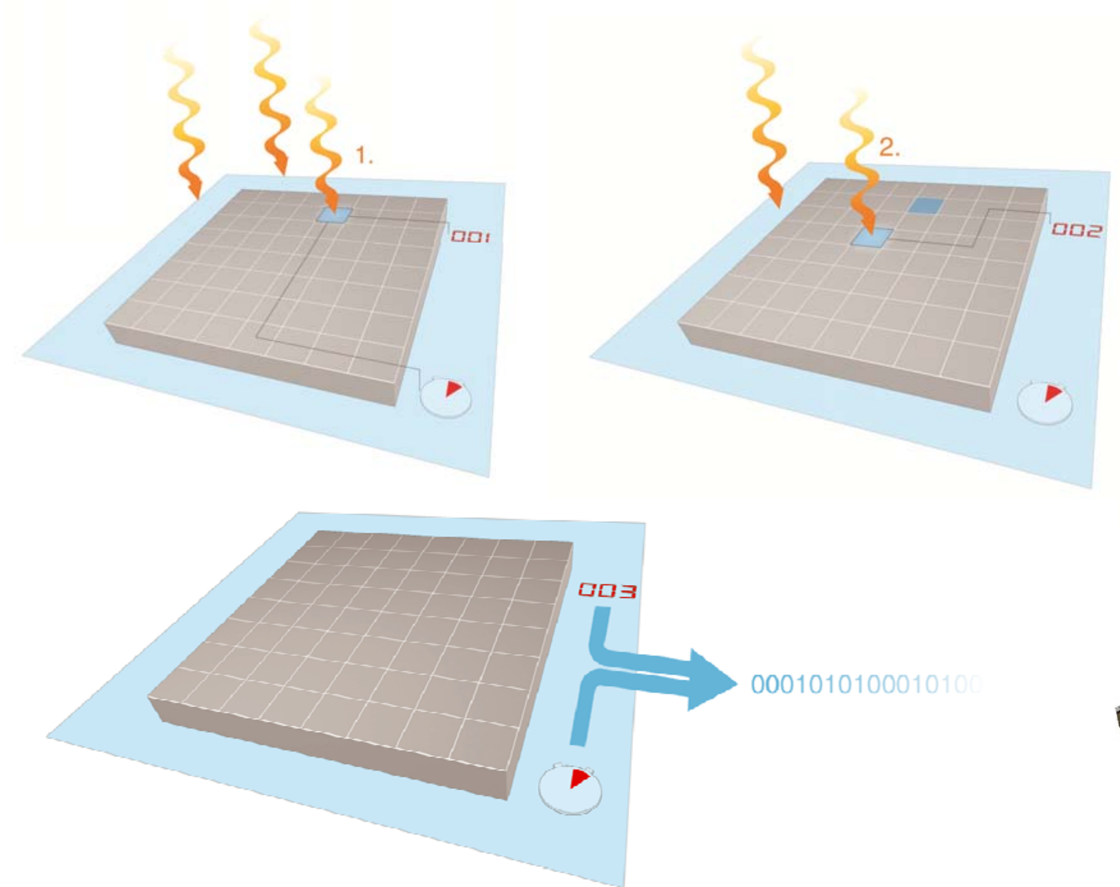
Digital Photon Counter (DPC)

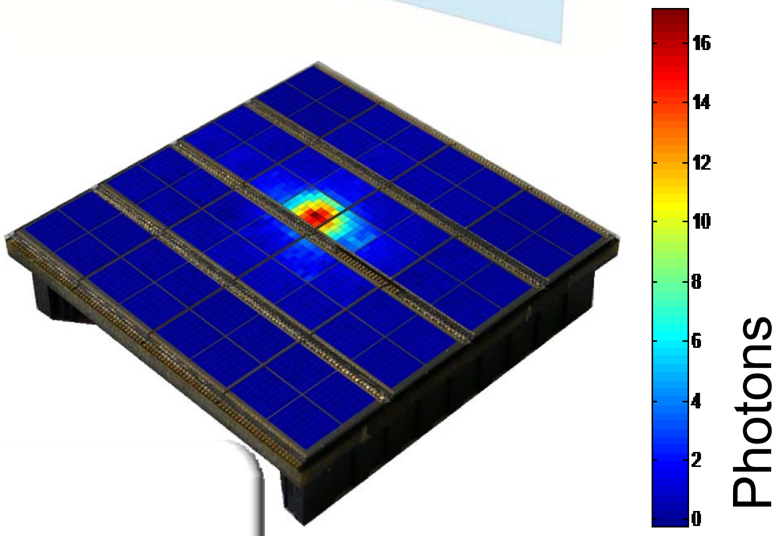


Digital output of
- Number of photons
- Time-stamp

Integrated readout electronics is the key element to superior detector performance

DPC: Now Photons are Counted Directly

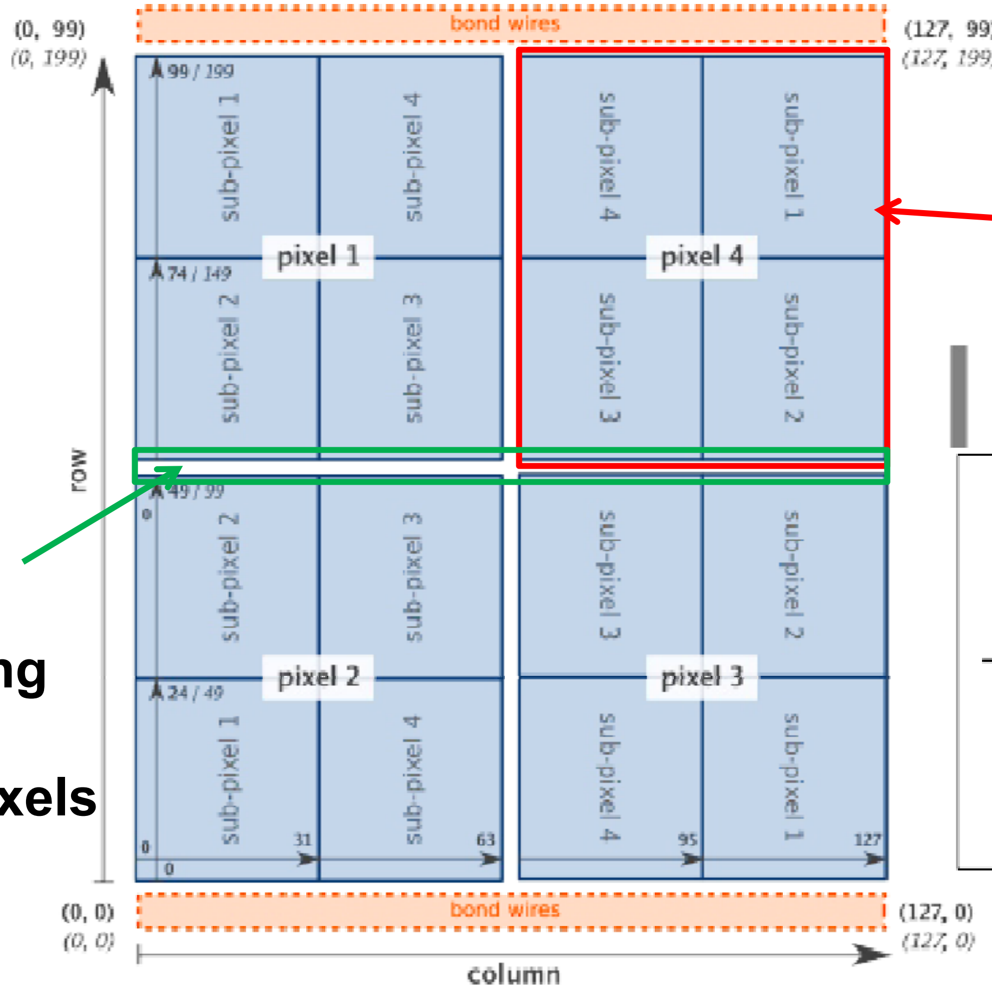




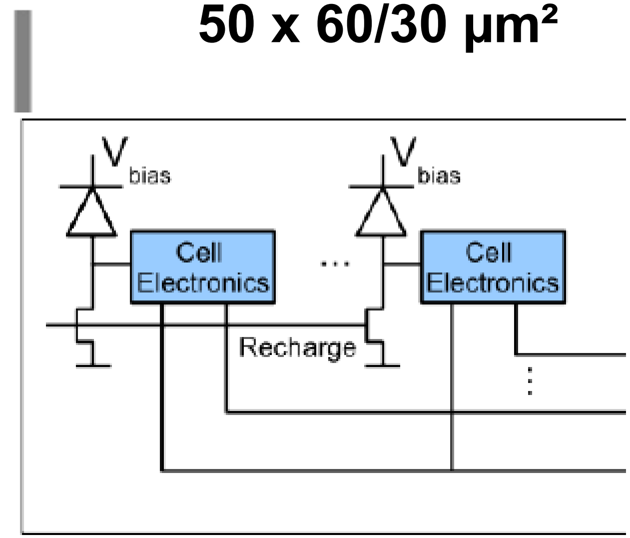
Output: > no. of photons
> time stamp(s)

No analog post-processing necessary!

DPC: Die structure

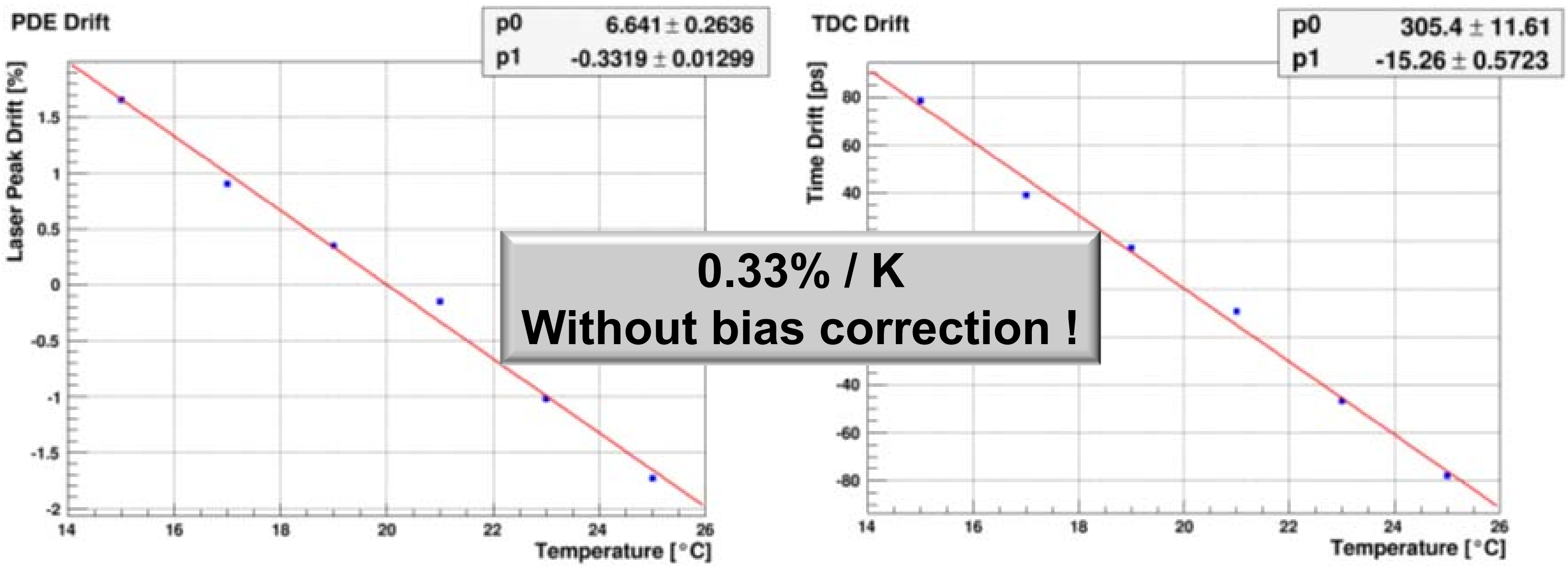


Per Pixel:
3200/6400 SPAD's
50 x 60/30 µm²



1 Line-TDC:
19.5 ps timing resolution
Serving 4 pixels

DPC: Front End Digitization Significantly Reduces Temperature Sensitivity

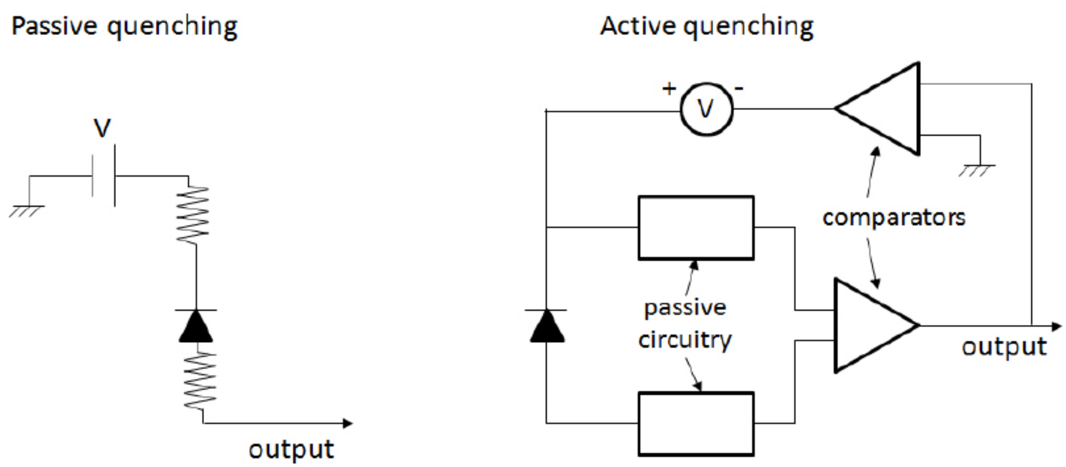


- **24 ps** full-width at half-maximum timing resolution of ps-laser
- Photopeak changes **0.33%** per degree C due to changing PDE **(values of analog SiPM's are ranging from 2-8%)**
- Time changes **15.3 ps** per degree C (TDC + trigger network drift)

DPC: CMOS Integration Enables Active Quenching

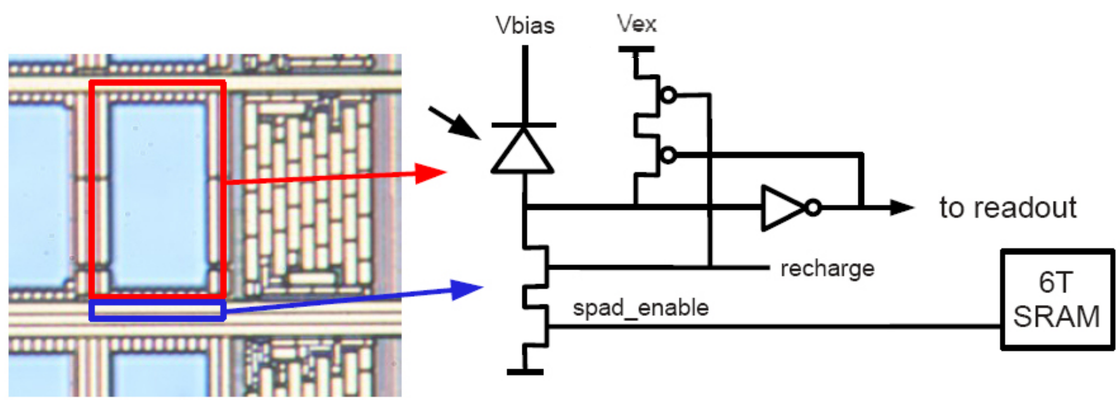
Figure 11. Generic schematics of a passive (left) and an active (right) quenching circuit employed at the micro-cell level (the micro-cell is represented by the diode symbol).

Graphics from Spanoudaki & Levin, Stanford, in: Sensors (10), 2010

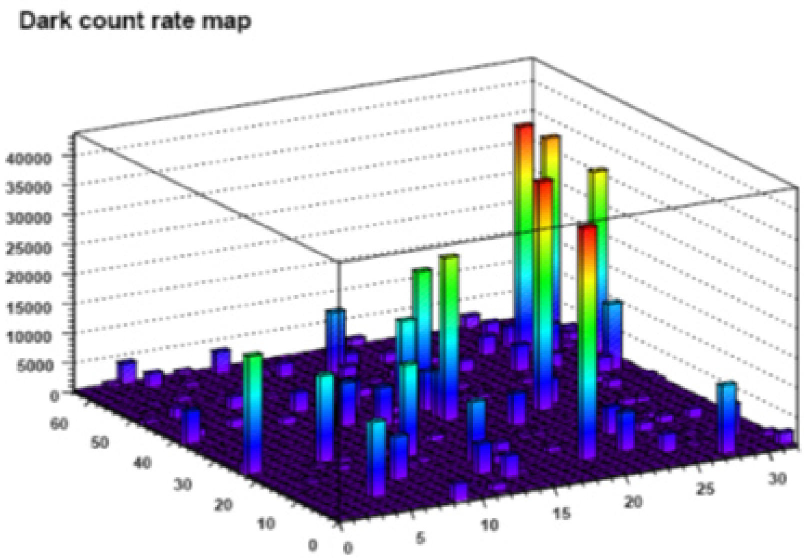


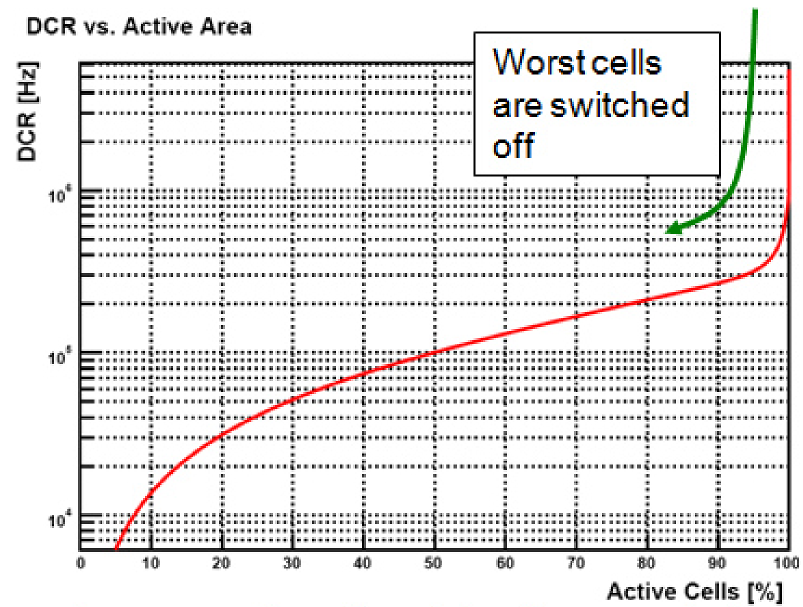
Digital SiPMs show reduced afterpulsing (0.3%) and crosstalk.

Cell layout of Digital SiPM cells:
Digital electronics take up only 3-6% of active area.



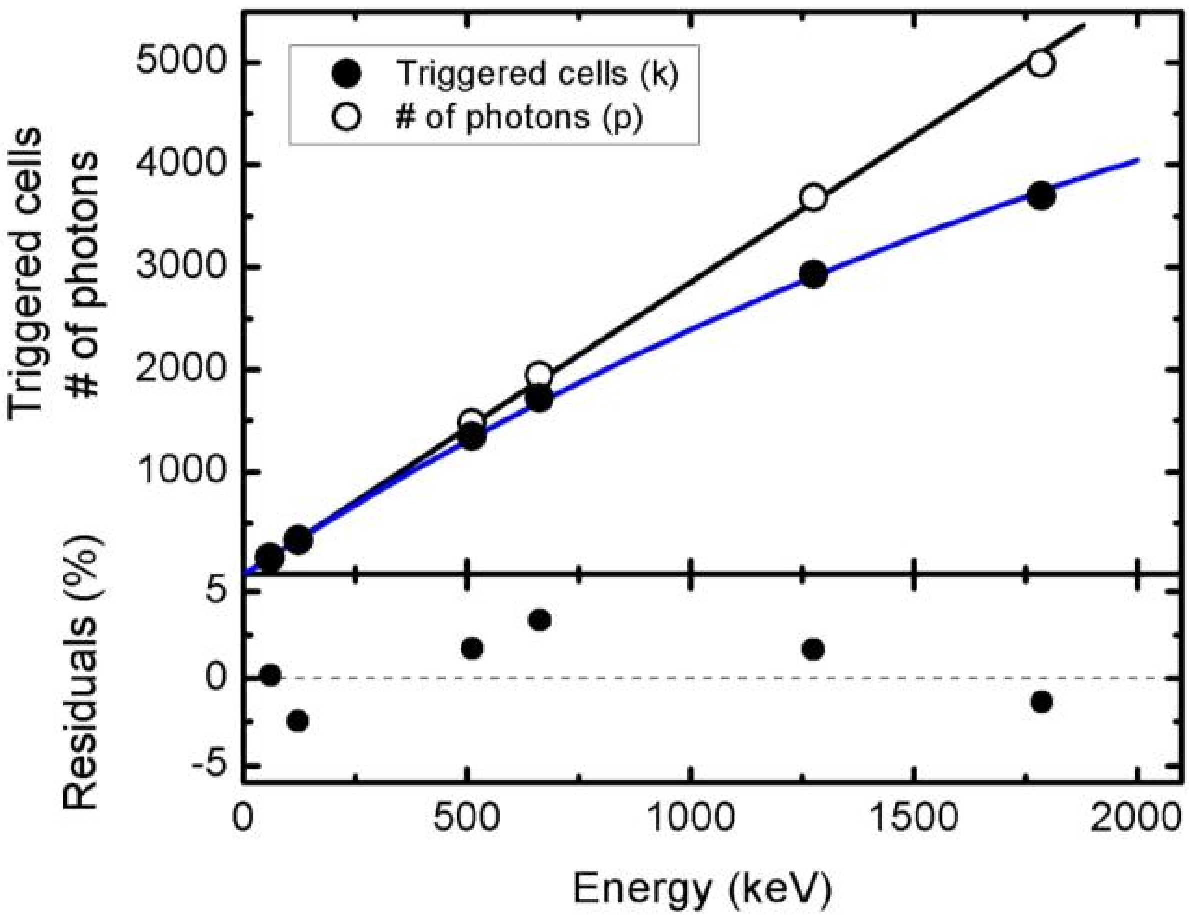
DPC: CMOS Integration Allows Active Control of Dark Count Rate (DCR)





- Silicon based light sensors have background noise (dark counts), varying with temperature.
- In digital SiPMs every cell can be addressed individually.
- Cells with high dark counts can be switched off.
- A few cells switched off (1-5%) reduces dark count levels by orders of magnitude.

DPC: Enables Easy Linearity Correction

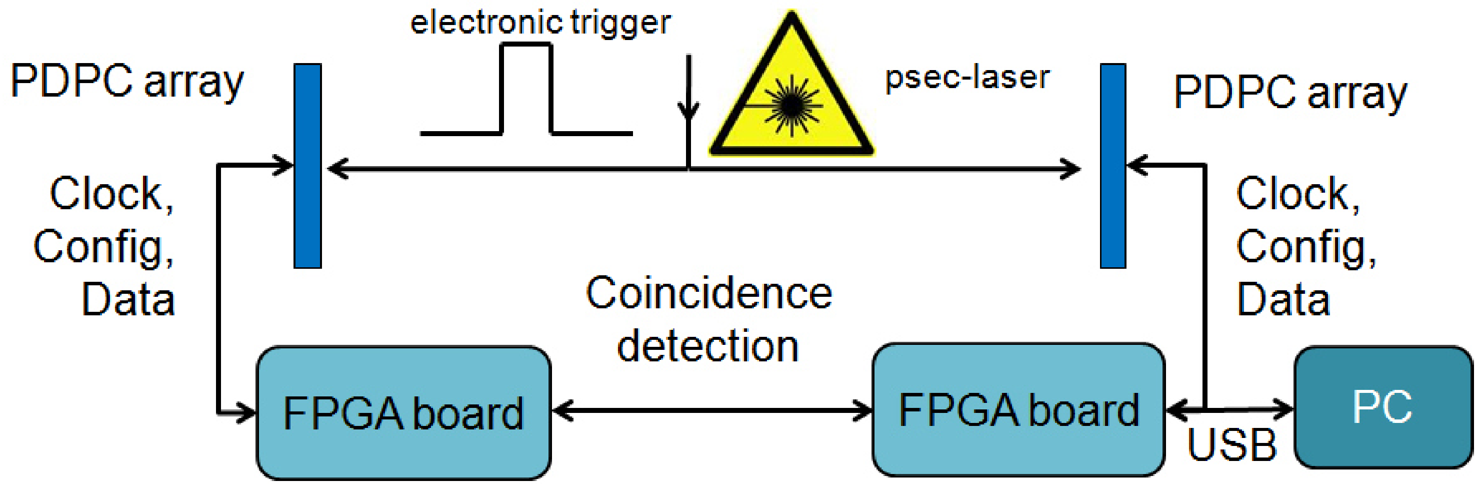


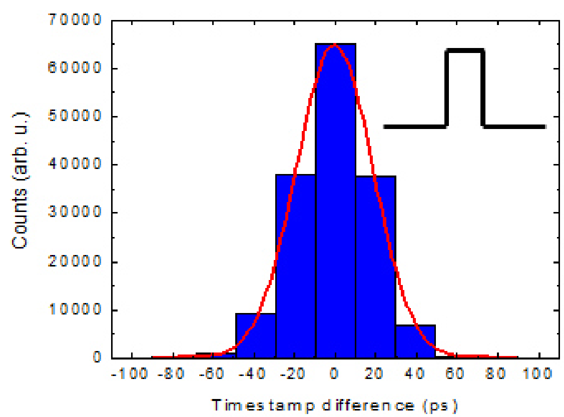
$$p = -N \cdot \ln\left(1 - k/N\right)$$

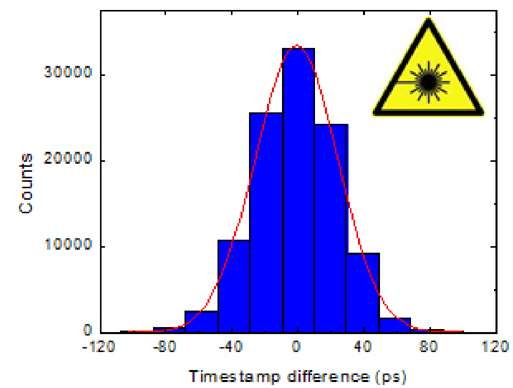
N: active cells (6400)
k: triggered cells
p: # of photons

- Experiments taken at room temperature
- No temperature stabilization
- **Correction more difficult with analog SiPMs**

DPC: Integration of TDC on Chip Provides Superior Timing Across Whole Arrays





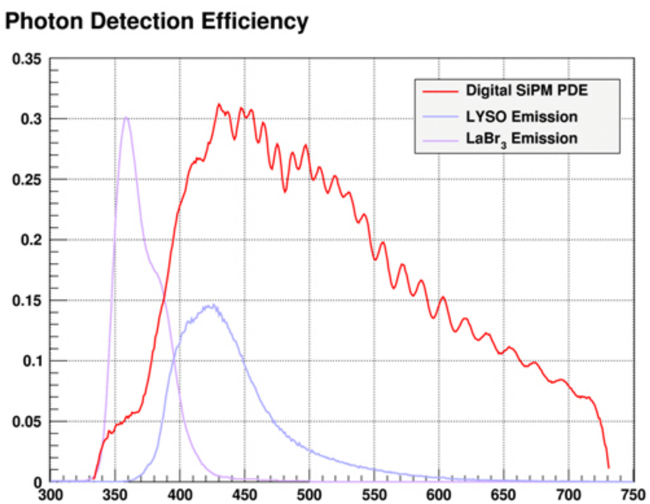


Timing jitter: **44 ps FWHM** **59 ps FWHM**

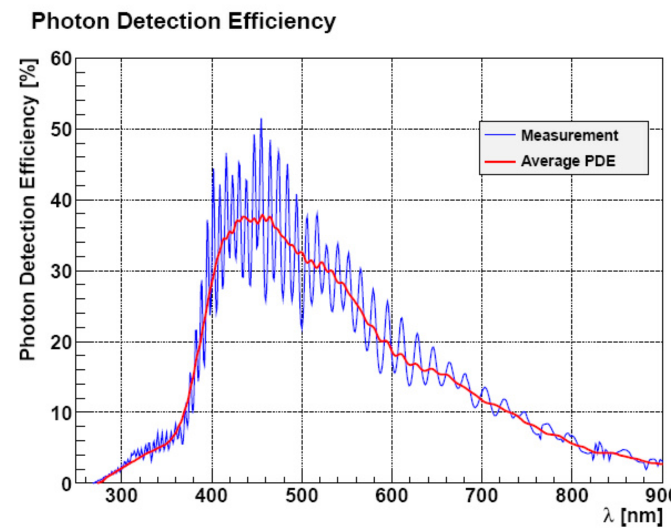
Contribution of: **TDC network** **TDC network + diodes**

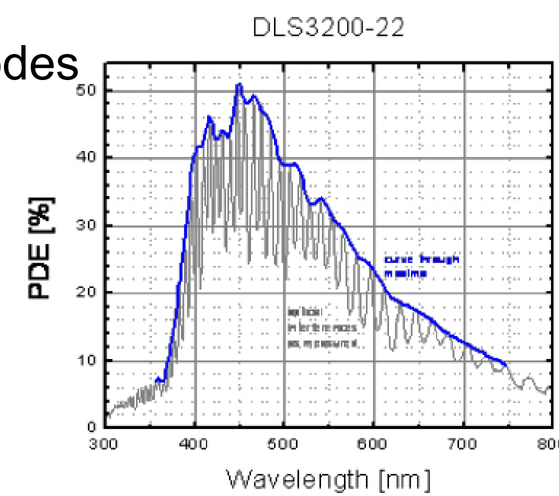
DPC: Higher PDE than PMT is Possible

DPC6400-22-44



DPC3200-22-44

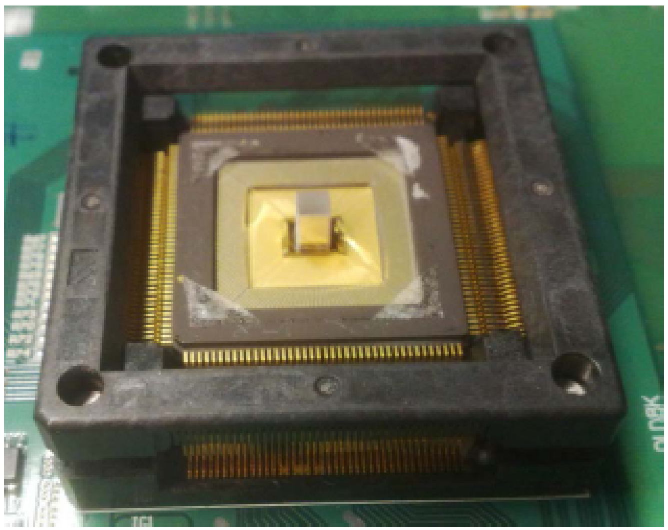




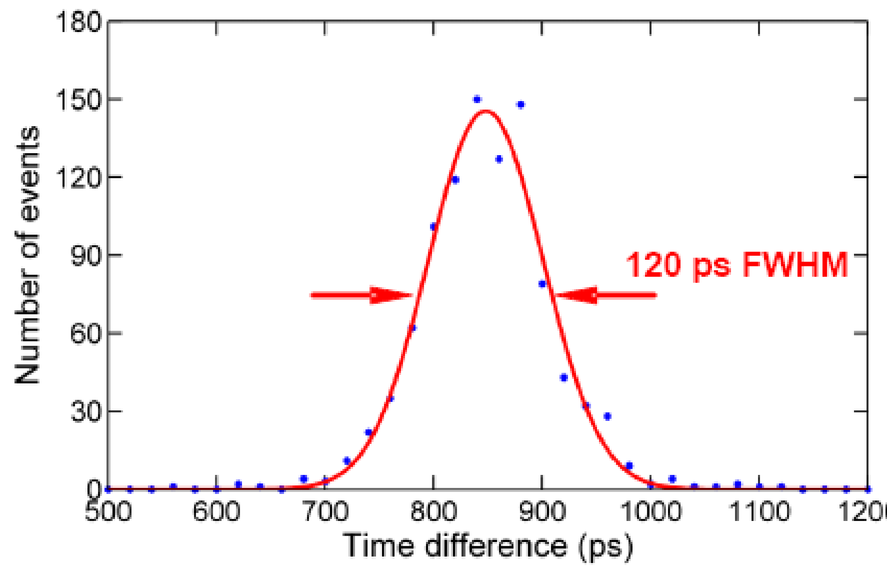
- 3.3V excess voltage, -20°C, randomly selected diodes
- Measured one diode at a time, 50 cm slit
- Parallel measurement with PIN photodiode
- Transmission window not optimized yet → strong decline towards dark blue/UV
- no ARC → strong interference patterns

DPC: Timing Resolution with Single Short LSO:Ca Crystal

3 mm x 3 mm x 5 mm Ca co-doped LSO:Ce on PDPC demonstrator chip



Photograph of Ca co-doped LSO:Ce crystal mounted on dSiPM demonstrator chip

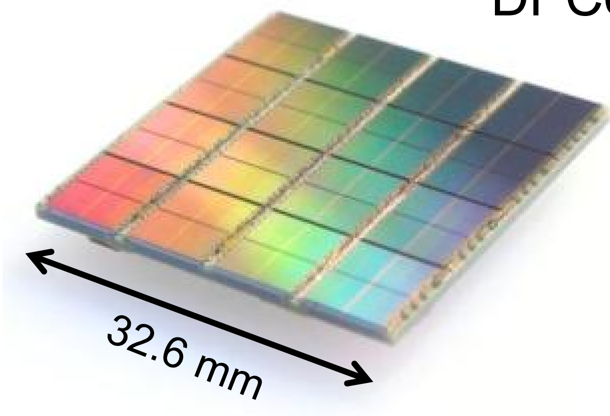


- Time difference spectrum measured with a Na-22 point source
- CRT = 120 ps FWHM (for two detectors in coincidence) at room temperature

TUDelft *D.R. Schaart et al, NSS-MIC 2011, MIC15.S-137* 11

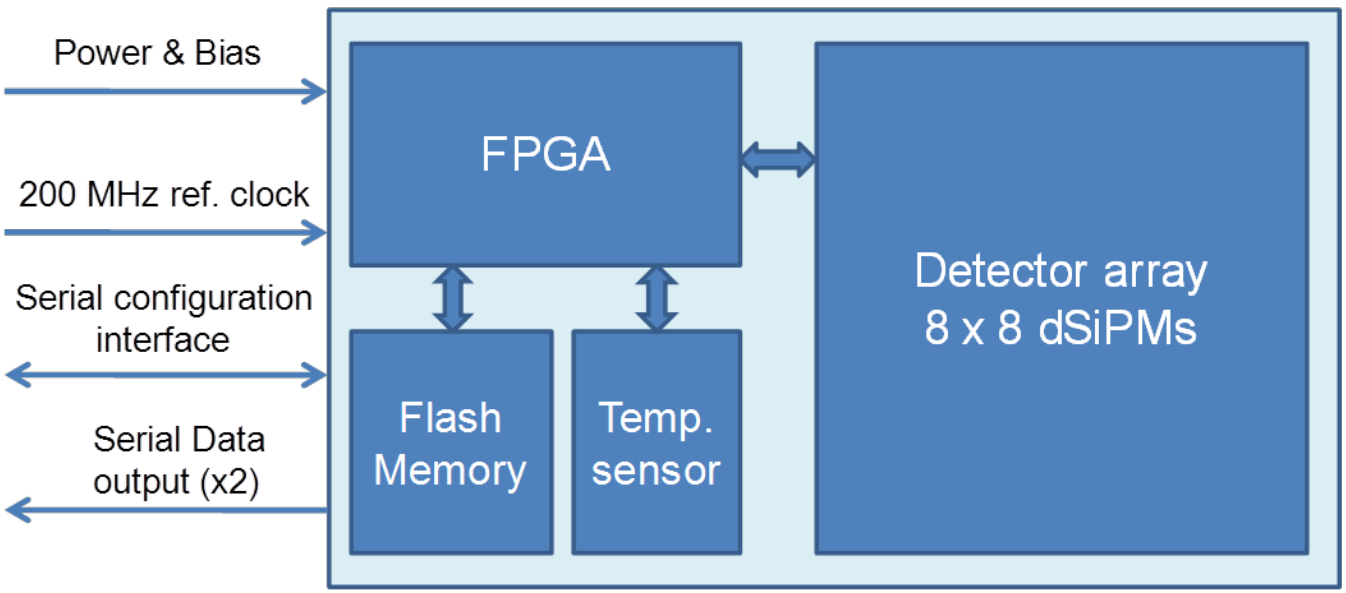
DPC is an Integrated "Intelligent" Sensor

DPC3200-22-44
DPC6400-22-44

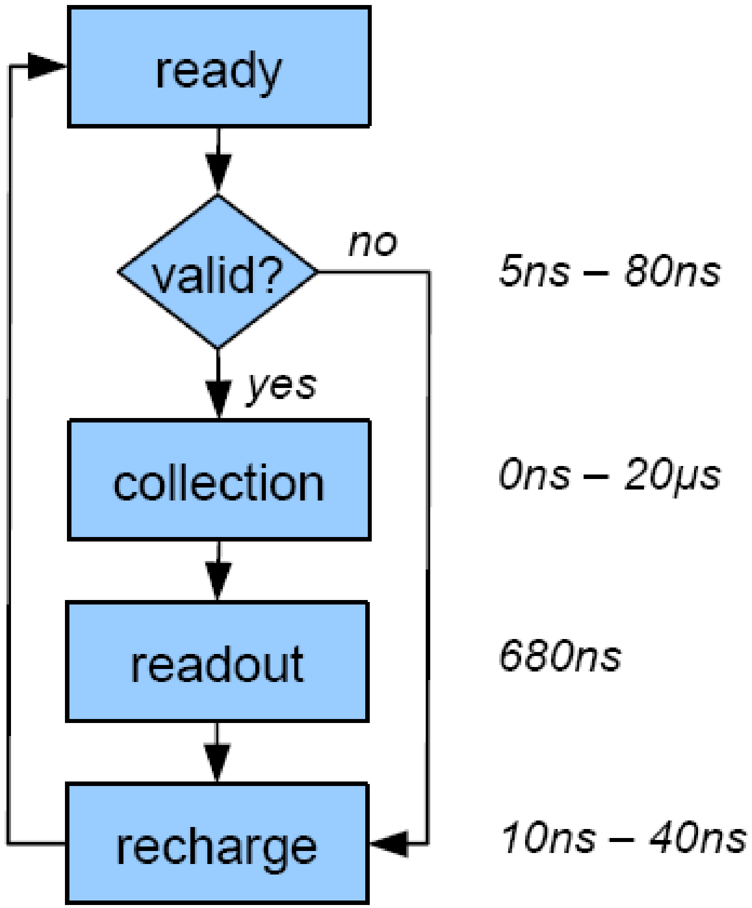


FPGA
- Clock distribution
- Data collection/concentration
- TDC linearization
- Saturation correction
- Skew correction

Flash
- FPGA firmware
- Configuration
- Inhibit memory maps



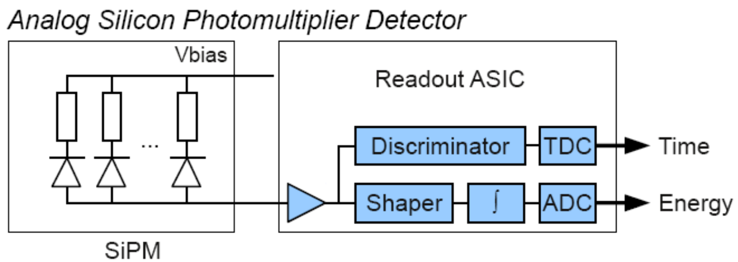
DPC: Typical Acquisition Sequence (example)



- 200MHz (5ns) system clock
- Variable light collection time up to 20µs
- 20ns min. dark count recovery
- dark counts => sensor dead-time
- data output parallel to the acquisition of the next event (no dead time)
- Trigger at 1, ≥2, ≥3 and ≥4 photons
- Validate at ≥4 ... ≥64 photons (possible to bypass event validation completely)

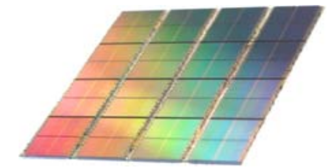
DPC is an Integrated, Scalable Solution

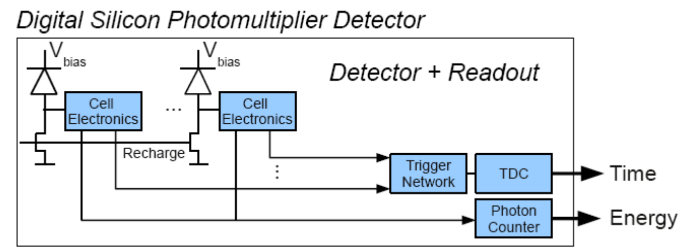
Analog SiPM



- discrete, limited integration
- analog signals to be digitized
- dedicated ASIC needed
- difficult to scale

Digital SiPM

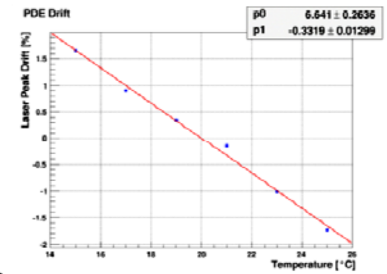


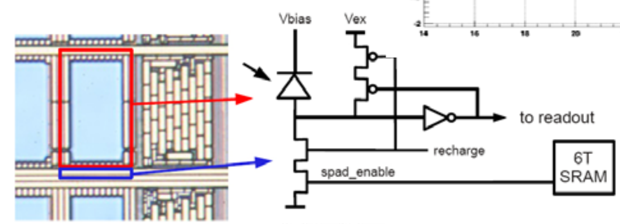


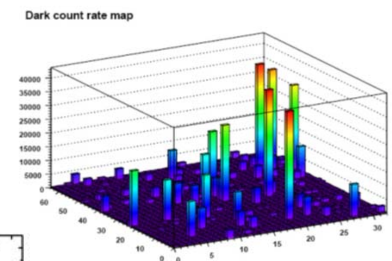
- fully integrated
- fully digital signals
- no ASIC needed
- fully scalable

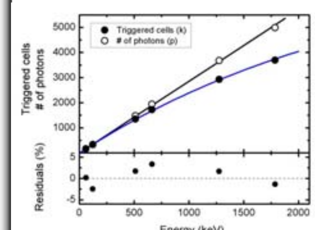
Sub-Summary: Advantages of Philips' DPCs

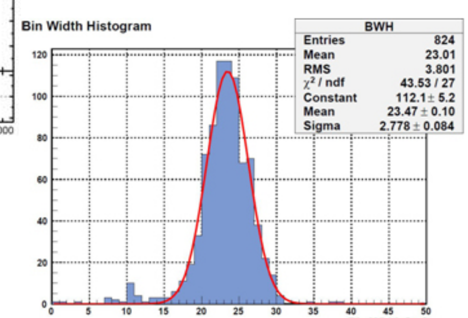
- significantly reduced temperature sensitivity (~10^{-1})
- active quenching reduces afterpulsing & crosstalk (~10^{-1})
- individually addressable cells enable DC control (~10^{-2})
- better linearity (&correction)
- better intrinsic timing resolution due to integrated TDCs (~ factor 5)
- no analog electronics, no ADCs, no ASICs





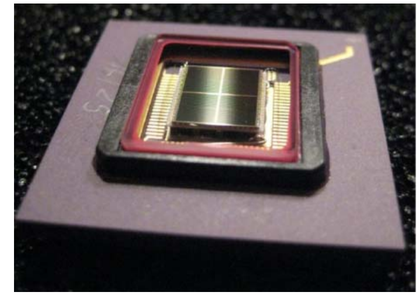






DPC technology is SCALABLE

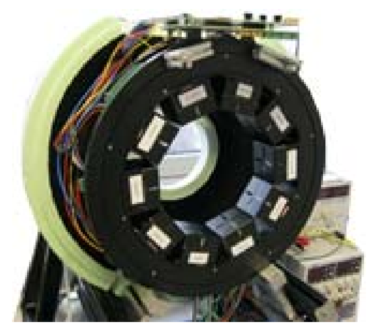
2 x 2 pixels in ceramic package
with Peltier Cooling



8 x 8 pixels in frames

Coolable Detector Modules (256 pixels)

Coolable Detector Rings/Areas
(any number of pixels)

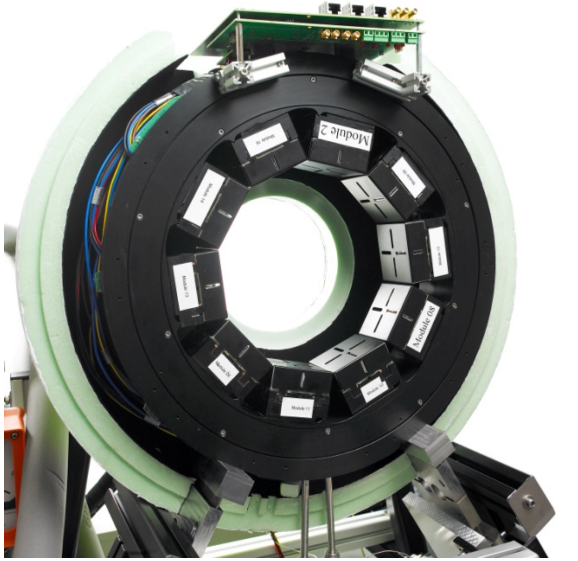


Philips DPC Technology: Detector Modules

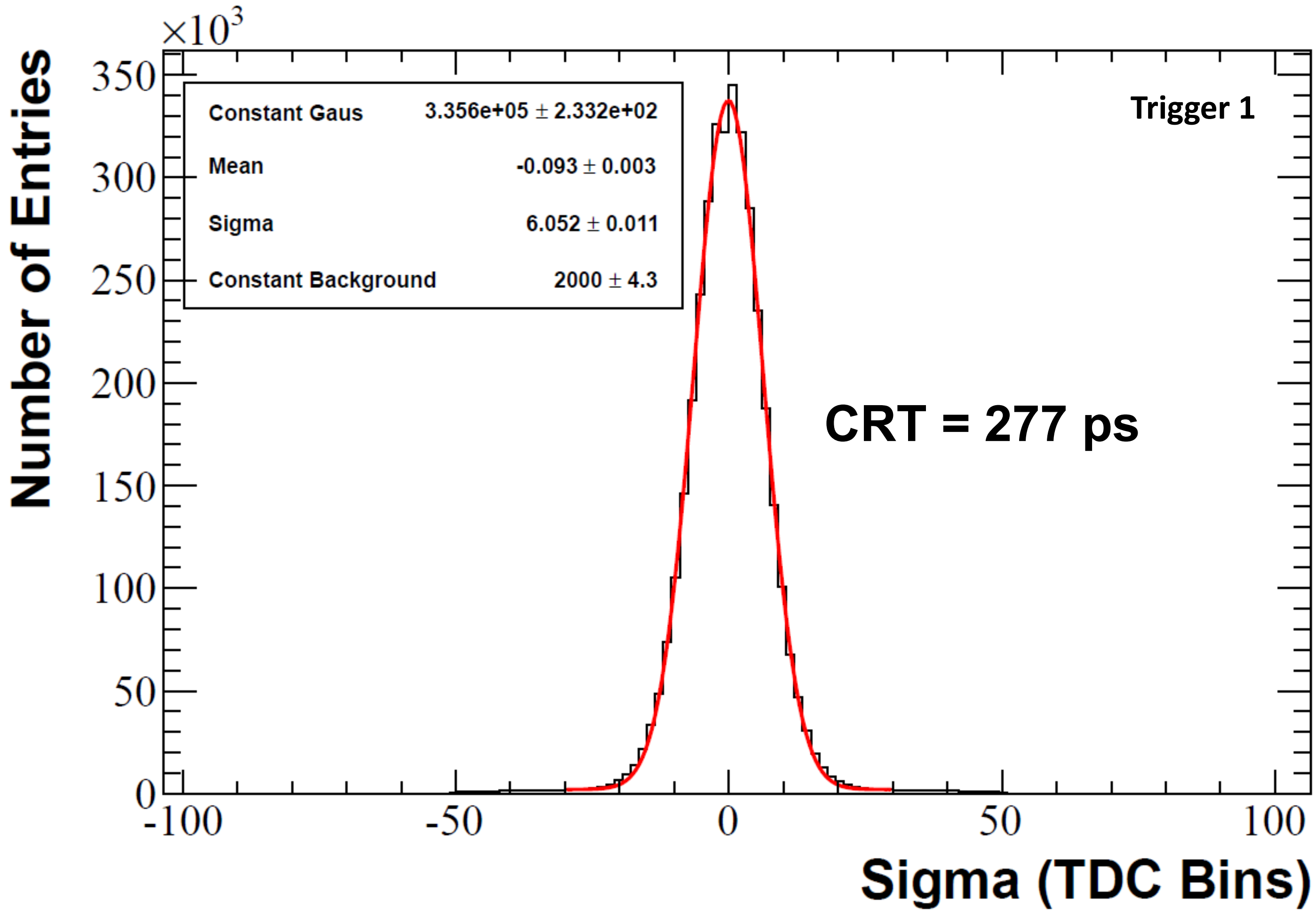
- 4 DPC sensor arrays (tiles)
- ~ 6.6 x 6.6 cm^2
- usable with or w/o scintillator crystals
- variable scintillator geometries
- Module board with FPGA, pre-processing capability & simple interface
- experimentally cooled to - 40°C

PDPC Technology: Test PET-Ring (@FZ Juelich)

- Inner Diameter (face-to-face): 20 cm
- 10 modules a 4 sensors
- LYSO 4 x 4 x 22 mm²
- Coolable down to 0°C
- Sensor temp. : ~ 5-10°C



Timing Coincidence Resolution



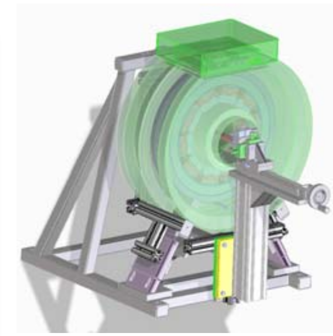
0x00 validation setting

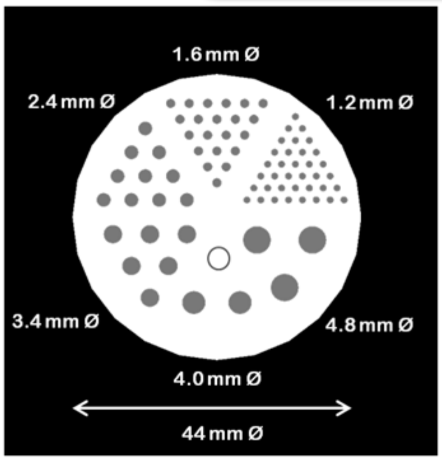
CRT (Trigger 1, CPI array) ~277 ps
CRT (Trigger 2, CPI array) ~362 ps

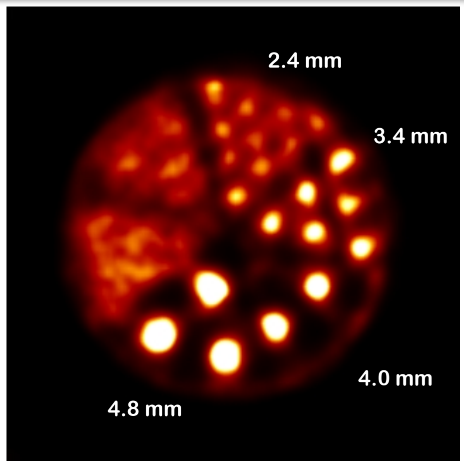
PHILIPS

Image Quality Overview

- Fillable rods (44 mm diam. / 34 mm length)
- 90 min acquisition (25 MBq of 18F)
- Trigger 2 at 7-9°C (internal tile temperature)
- Energy (ER 13% & clustering) and time (TR 390 ps) calibrations applied
- Energy window of [440;660] keV and time window of 3 ns [-1.5;1.5]







PURE/OSEM (0.5 mm voxels), no norm., no decay time, all corrections applied.
15.2% randoms, 5.0% scatters

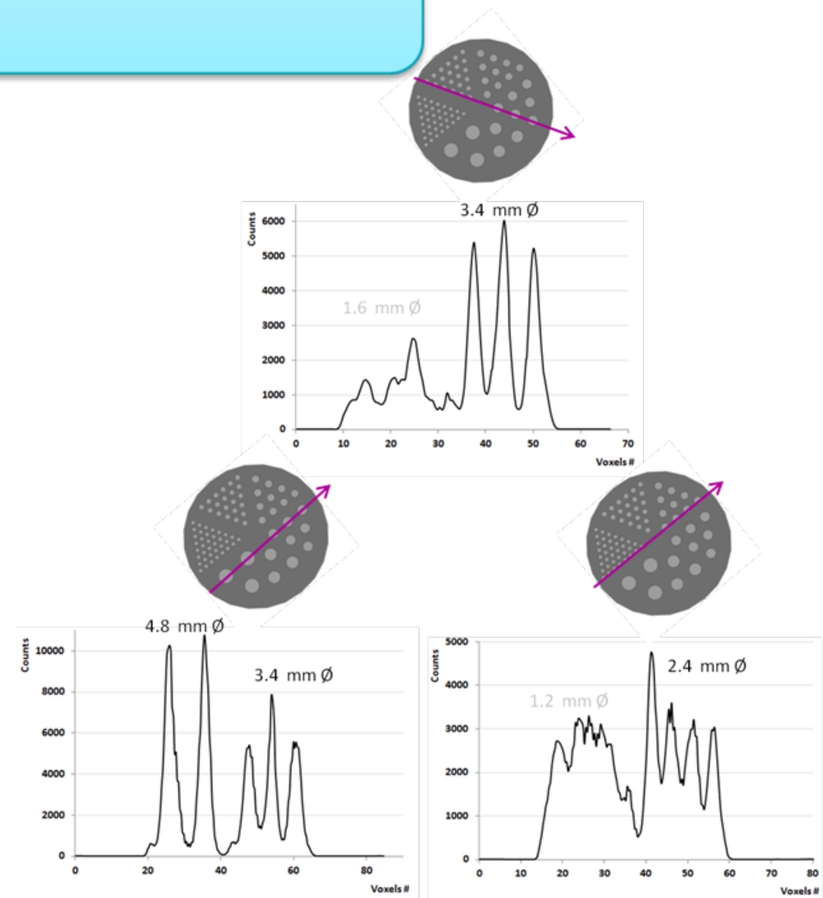
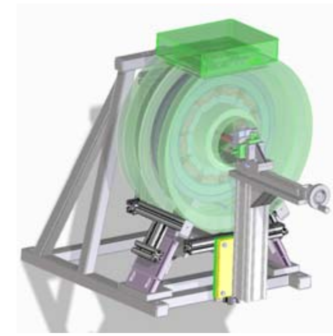
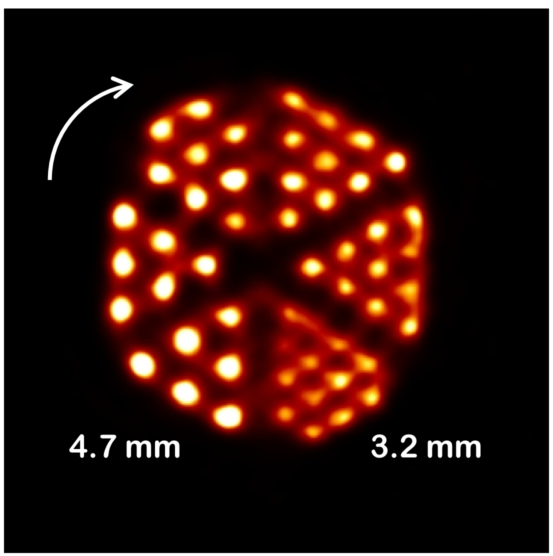


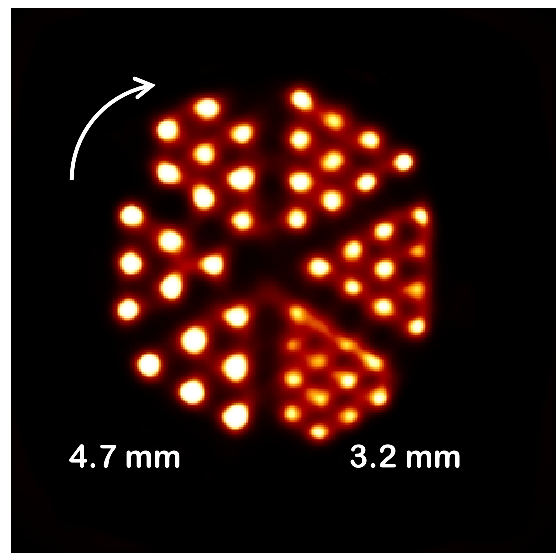
Image Quality Overview

- Hot rod phantom (**70 mm diameter**)
- 1h data acquisition (10-15 MBq ^{18}F)
- Trigger 2 at 7-9°C (internal tile temperature)
- Energy (RE 13% & clustering) and time (TR 390 ps) calibrations applied
- Energy window of [440;660] keV and time window of 3 ns [-1.5;1.5]



Without TOF | **With TOF (266 ps)**





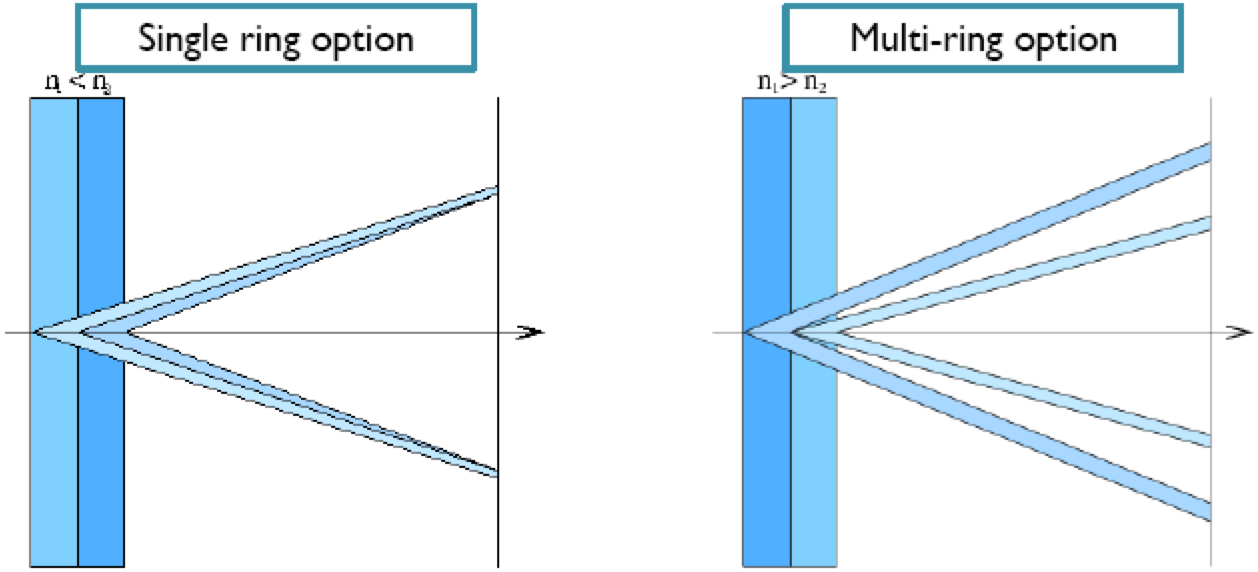
PURE/OSEM (0.5 mm voxels), no norm., no decay time, all other corrections applied.

DPC in High Energy Physics: FARICH Detector

FARICH concept

Focusing Aerogel RICH – FARICH

Improves proximity focusing design by reducing radiator thickness contribution into the Cherenkov angle resolution



T.Iijima et al., NIM A548 (2005) 383
A.Yu.Barnyakov et al., NIM A553 (2005) 70

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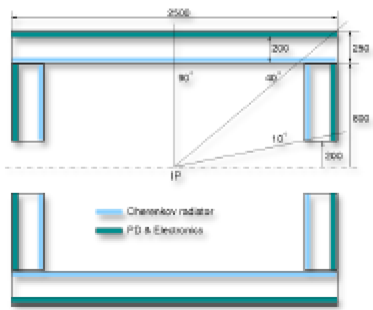
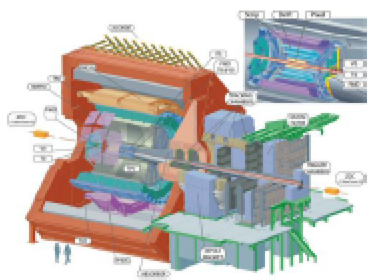
DPC in High Energy Physics: FARICH Detector

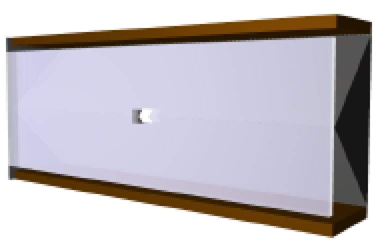
FARICH projects and proposals



FARICH for Super Charm-Tau Factory (Novosibirsk)
Particle ID: μ/π up to 1.7 GeV/c
$21 m^2$ detector area (SiPMs)
~1M channels



FARICH for ALICE HMPID upgrade
Particle ID: π/K up to 10 GeV/c, K/p up to 15 GeV/c
$3 m^2$ detector area (SiPMs)



Forward Spectrometer RICH for PANDA
Particle ID: π/K/p up to 10 GeV/c
$3 m^2$ detector area (MaPMTs or SiPMs)

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First test of DPC in High Energy Physics: FARICH Detector @ CERN, June 2012

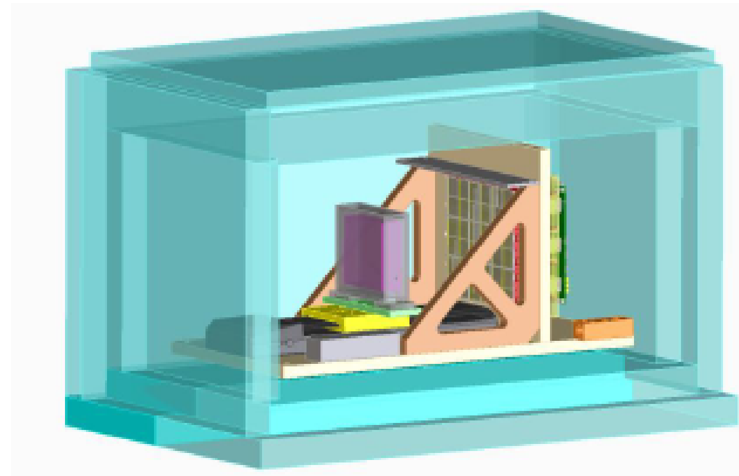
Main objective:

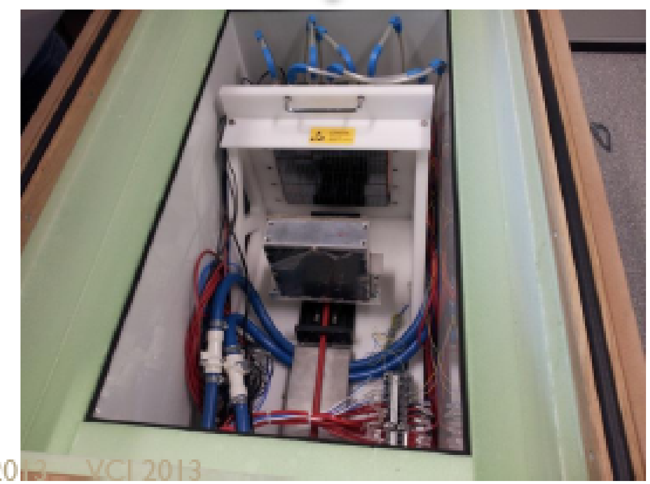
Proof of concept: full Cherenkov ring detection with DPC array

Timeline:

- Started to envisage: **28/02/12**
- Requirements for the FARICH prototype test setup fixed: **30/04/12**
- Prototype operational @ Aachen Labs: **03/06/12**
- Installed @ CERN: **12/06/12**
- Subsequent beam runs for 12 days until **25/06/12** with smooth setup operation

Fast prototyping!

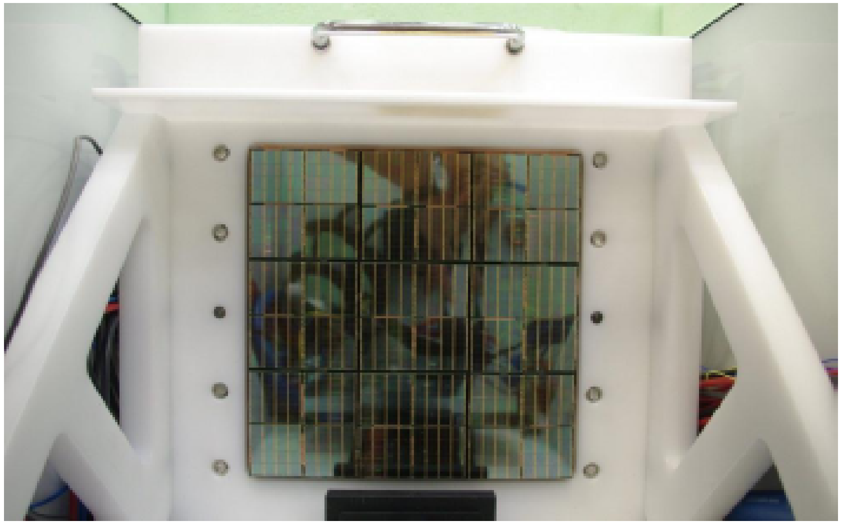




FARICH prototype with DPC…

4-layer aerogel

- n_{max} = 1.046
- Thickness 37.5 mm
- Calculated focal distance 200 mm
- Hermetic container with plexiglass window to avoid moisture condensation on aerogel

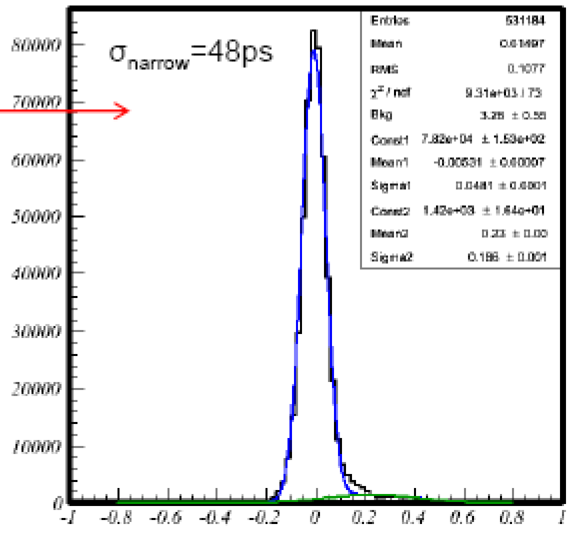


Square matrix 20x20 cm²

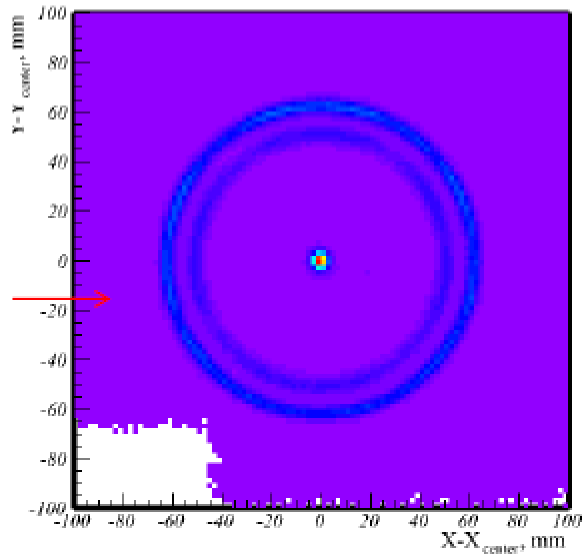
- Sensors: DPC3200-22-44
- 3x3 modules = 6x6 tiles = 24x24 dies = 48x48 pixels in total
- 576 time channels
- 2304 amplitude (position) channels
- 4 levels of FPGA readout: tiles, modules, bus boards, test board

Preliminary results from FARICH Detector Prototype @ CERN

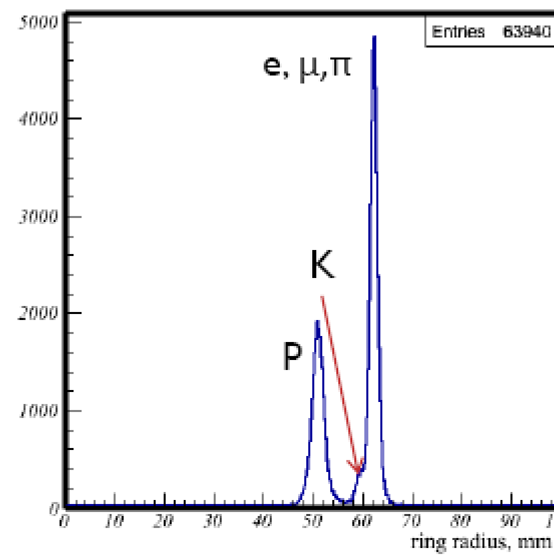
Intrinsic timing



Hit positions



Event distribution on radius

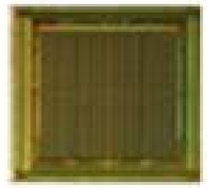


- Intrinsic timing resolution of full (20 x 20 cm²) detector: **σ = 48 ps**
- Discrimination of protons, kaons and pions with high angular resolution
- Curable damage of sensor at primary beam spot

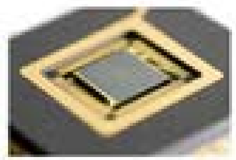
Scalable Technology Maintains Intrinsic Performance

DEMONSTRATOR:
single pixel

CRT ~ 270 ps*



CHIP:
2 x 2 = 4 pixels



CRT ~ 270 ps*

ARRAYS (TILES):
8 x 8 = 64 pixels

CRT ~ 270 ps*

MODULES:
256 pixels

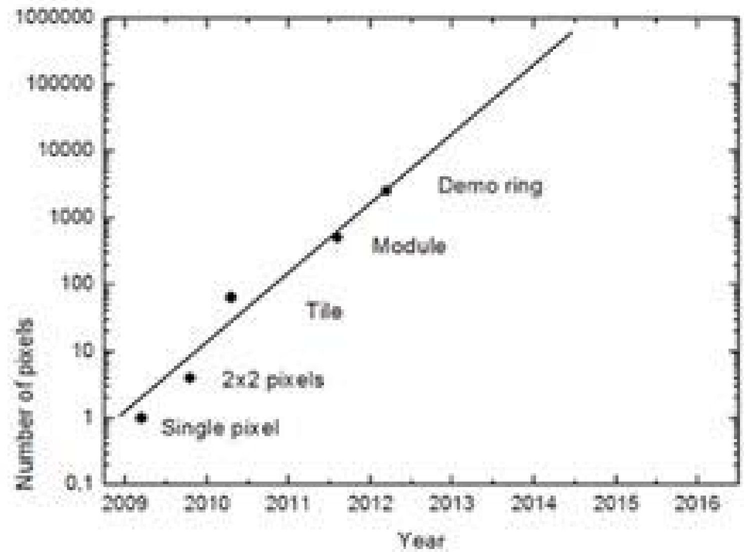
CRT ~ 270 ps*

DEMO RING:
2560 pixels

CRT ~ 270 ps*

Many first time rights

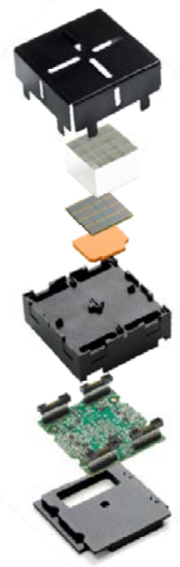
PDPC-Moore's law



* Using 4x4x22 mm³ LYSO crystals !!

PDPC technology to business approach

Integration

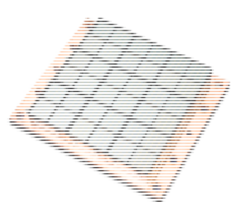
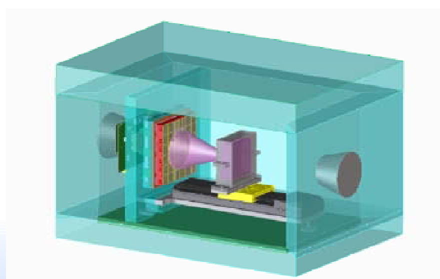
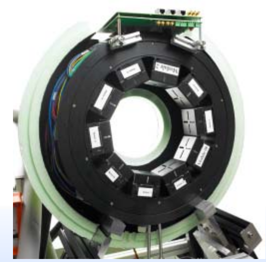


TEK 1 - POP (tile TEK)

POP - proof of principle

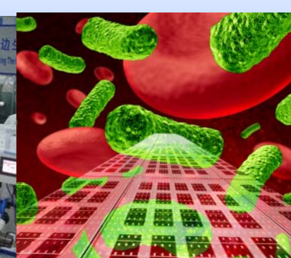

TEK 2 - POC (module TEK)

POC - proof of concept

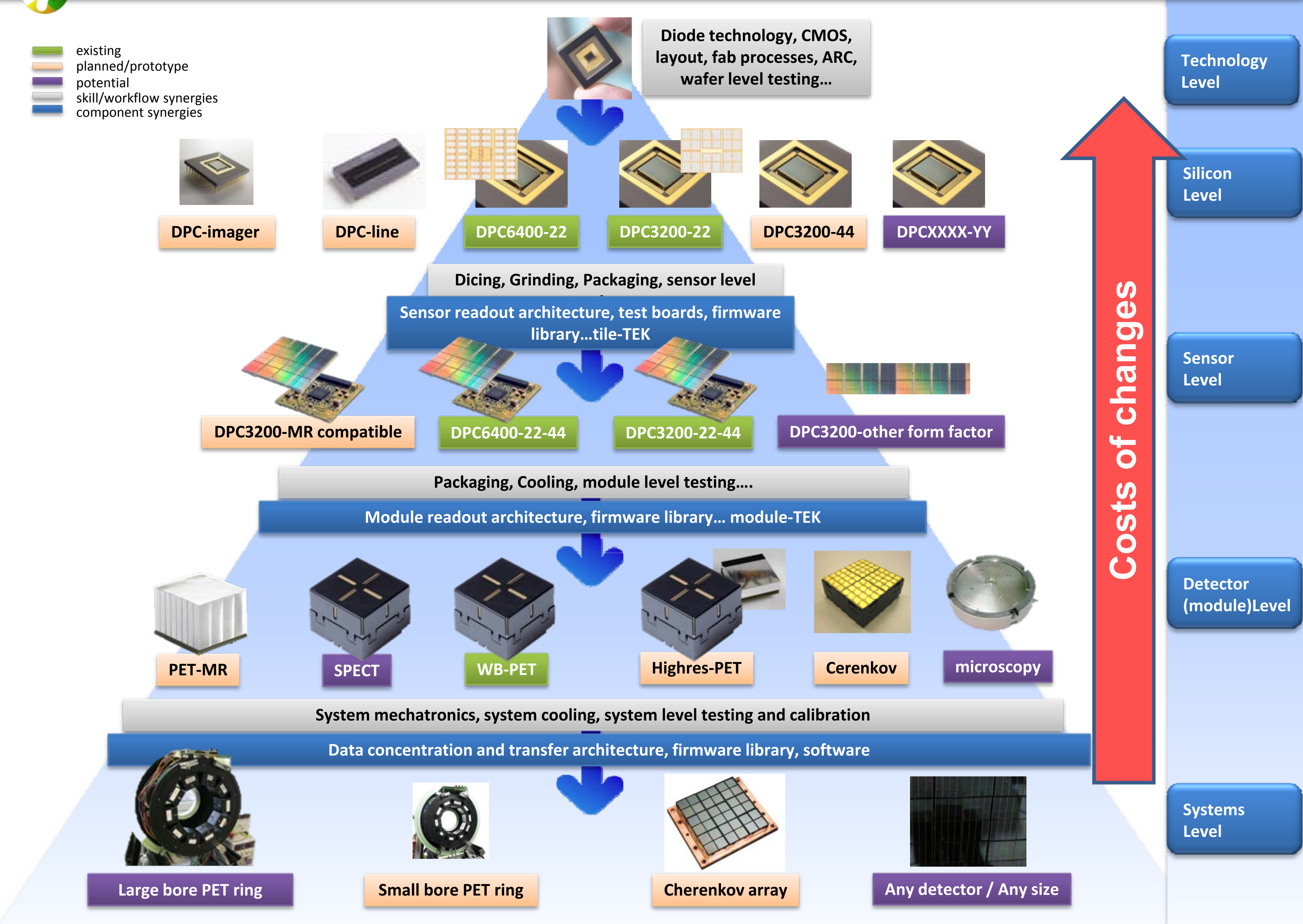
Rapid prototyping





Application Business

The Philips tree of scalable DPC technology

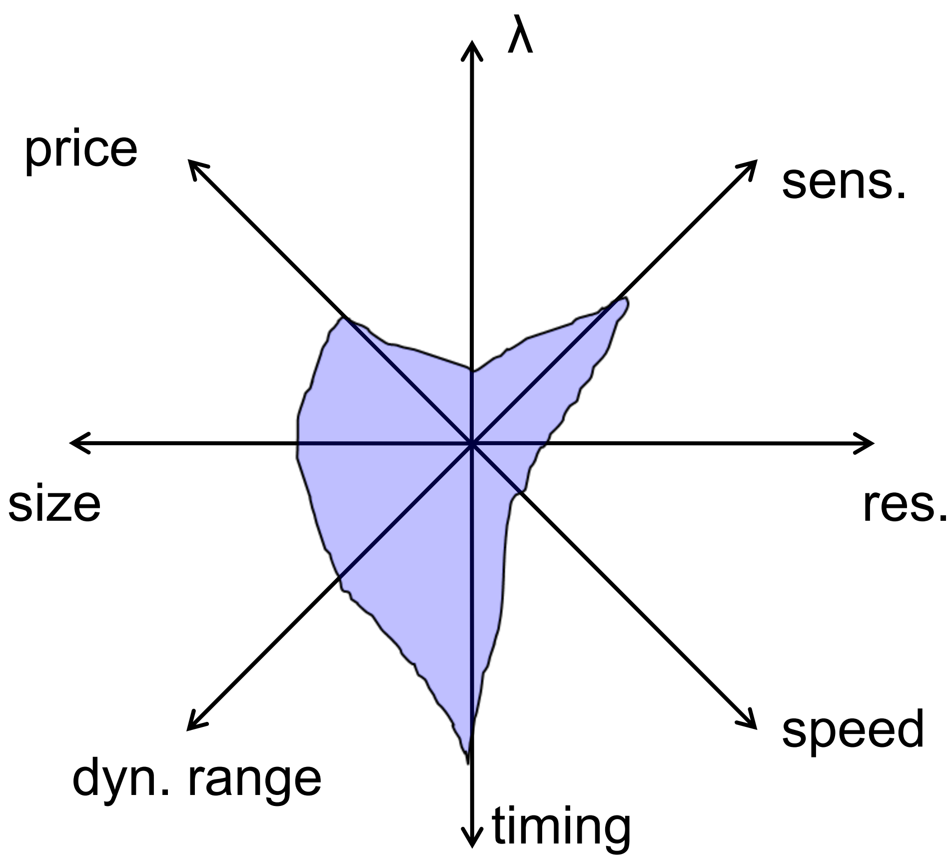


PDPC Technology Evaluation Kit (TEK)

> 30 kits installed so far

The future: what direction to go?

DPC: current parameters are optimized for TOF-PET



Summary

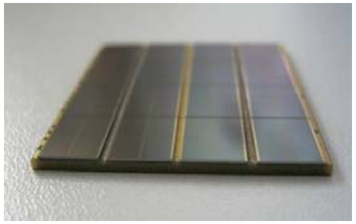
- **DPC is a disruptive technology that will induce changes in applications.**
- **DPC development was triggered by ToF-PET abut can be expanded to other applications.**
- **DPC has shown superior performance and ease of use vs. analog SiPM technology (> 15 papers & posters @ IEEE2013).**
- **DPC demonstrated scalability of technology in maintaining intrinsic performance over larger systems:**

  - PDPC PET test ring

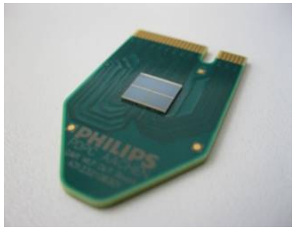
  - FARICH detector prototype
- **As a CMOS based technology DPC needs volume to succeed, therefore a systems architecture concept was developed.**
- **New application areas for DPC are explored by adapted designs.**

Outlook

- **Expansion of Scale of technology:**
  - ***detectors with larger number of pixels***
  - ***additional building blocks of scalable architecture***

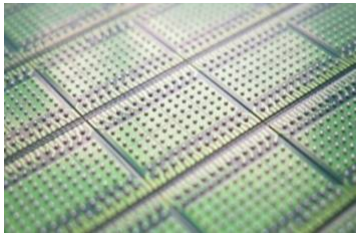


- **Improved performance of DPCs (2nd generation):**
  - ***higher PDE***
  - ***less dead time***
  - ***better intrinsic timing resolution***
  - ***sub-pixel (2 mm²) readout***
  - ***radiation hardness improvements***



- **New designs for new applications**
  - ***line- and image sensors (FLIM, Spectroscopy)***

- **New technologies/materials are under investigation**
  - ***TSV***
  - ***WLP***
  - ***ARC***
  - ***3D technologies***
  - ***Graphene and other 2D materials (further out)***



http://www.youtube.com/watch?feature=player_embedded&v=dTSnnIITsVg

Thank you very much for your attention!

Thanks also to:

PET

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Torsten Solf
Andre Salomon

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Siegfried Jahnke
Gerhard Roeb
Simone Beer
Matthias Streun
Marco Dautzenberg

FARICH

Budker Institute of Nuclear Physics, Novosibirsk
A.Yu.Barnyakov
M.Yu.Barnyakov
V.S.Bobrovnikov
A.R.Buzykaev
V.V.Gulevich
S.A.Kononov
E.A.Kravchenko
I.A.Kuyanov
A.P.Onuchin
I.V.Ovtin
A.A.Talyshev

Boreskov Institute, Novosibirsk
A.F. Danilyuk

Institute of Nuclear Research RAS, Moscow
A,I.Berlev
D.A.Finogeev
T.L.Karavicheva
E.V.Karpechev
A.B.Kurepin
A.N.Kurepin
A.I.Maevskaya
Yu.V.Musienko
V.I.Razin
A.I.Reshetin
N.S.Topilskaya
E.A.Usenko

www.philips.com/digitalphotoncounting

york.haemisch@philips.com