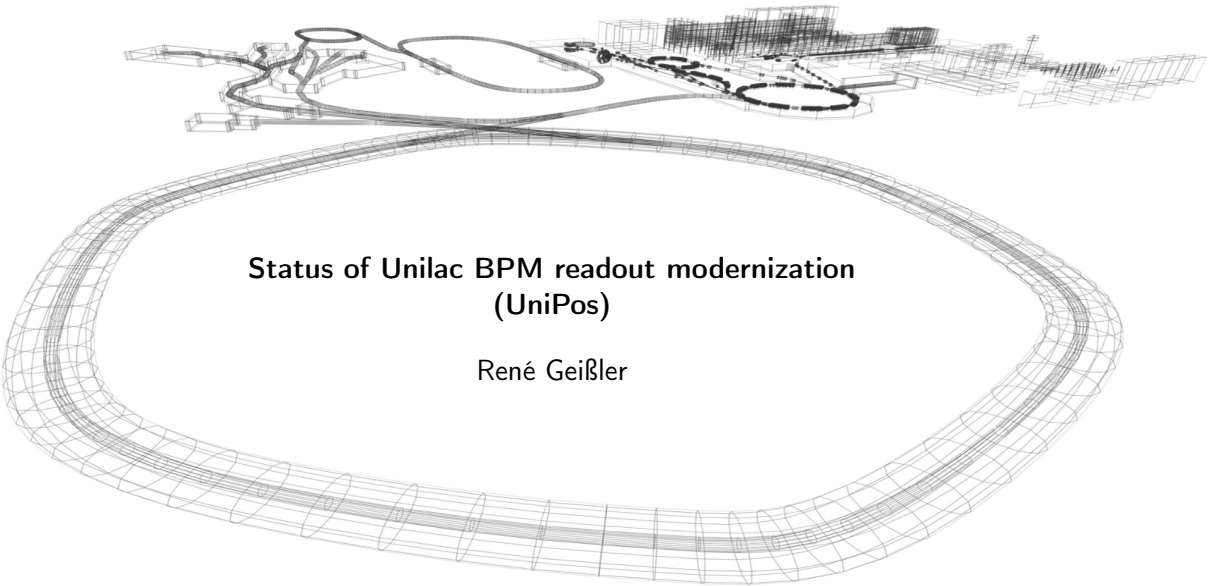


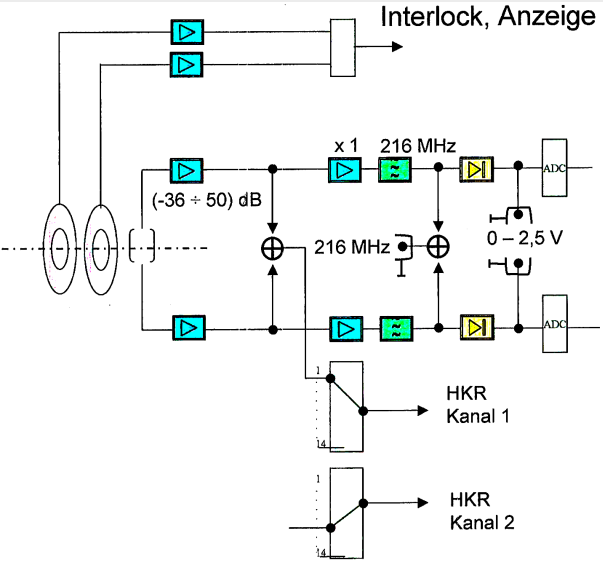
Status of Unilac BPM readout modernization (UniPos)

René Geißler

Previous UI


links
X
rechts
oben
Y
unten
Monovolt
PK60
OVPact
Vact
Limit
Blende
UH3/2
UH4/3
US1/1
US2/2
US4/7
US4/9
UA1/1
UA2/2
UA3/3
UA4/4
UT1/0
UT1/2
UT2/Y
UY2/2
TK1/1
TK2/2
TK2/4
TK3/3
TKD/6
TK3/5
TK4/1
TK4/2
TK5/2
TK6/1
TK7/3
SV/12A

BPM Electronics Schematic



Analog signal processing:

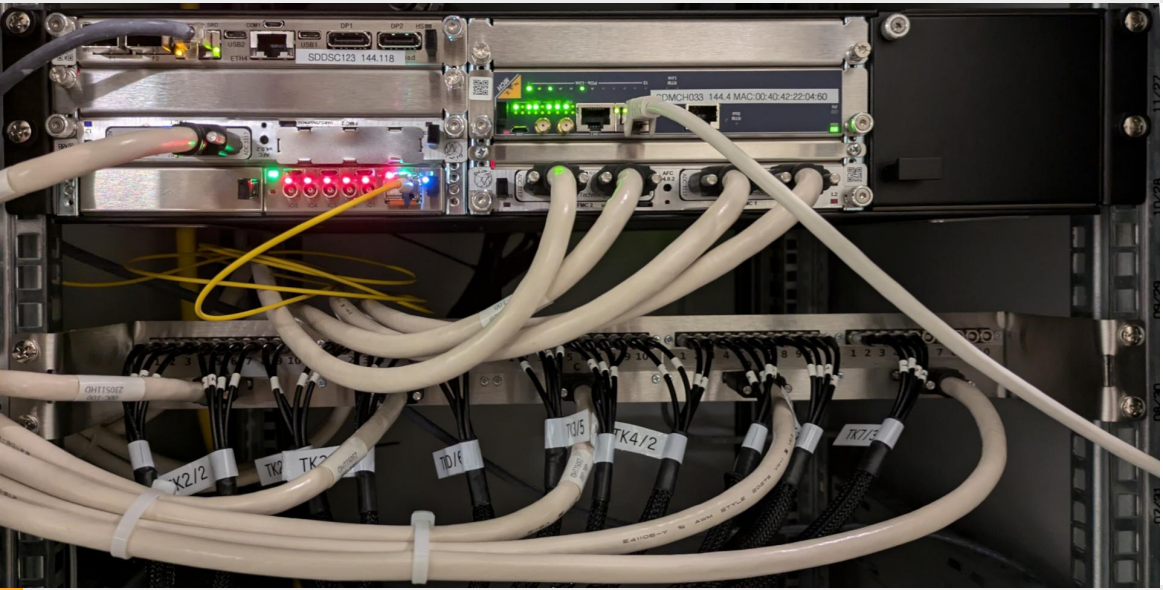
- amplification
- filtering
- demodulation of the 216.8 MHz component using a diode
  $\rightarrow$ nonlinearity correction required

Previous Rack Setup

Current Rack Setup

Current Rack Setup - Detail

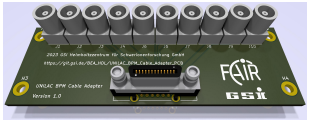
MicroTCA Crate



New Hardware

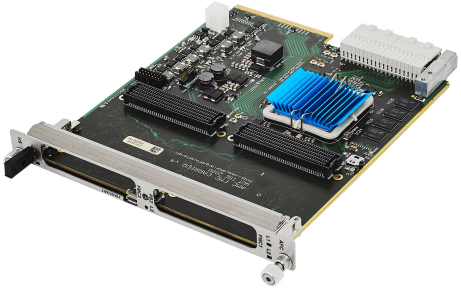
location	BPMs	ADC channels
LSB2 (Prestripper)	4	16
LSB4 (Poststripper)	11	44
EH-Basement (TK)	11	44
in total	26	104

3 x MTCA Crate



12 x Cable Adapter

3 x Adapter Case



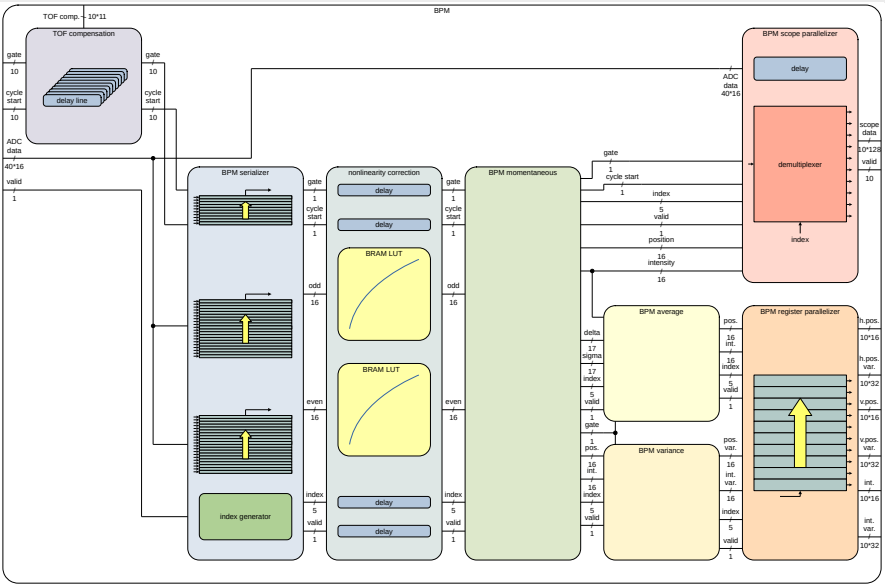
5 x AFC FMC Carrier (FPGA)

7 x IOxOS ADC_3117
(20 channels, 5 MHz)

Newly Developed Software

- FPGA gateware
- FESA class
- GUI

FPGA Gateware



parallel implementation does not fit into FPGA

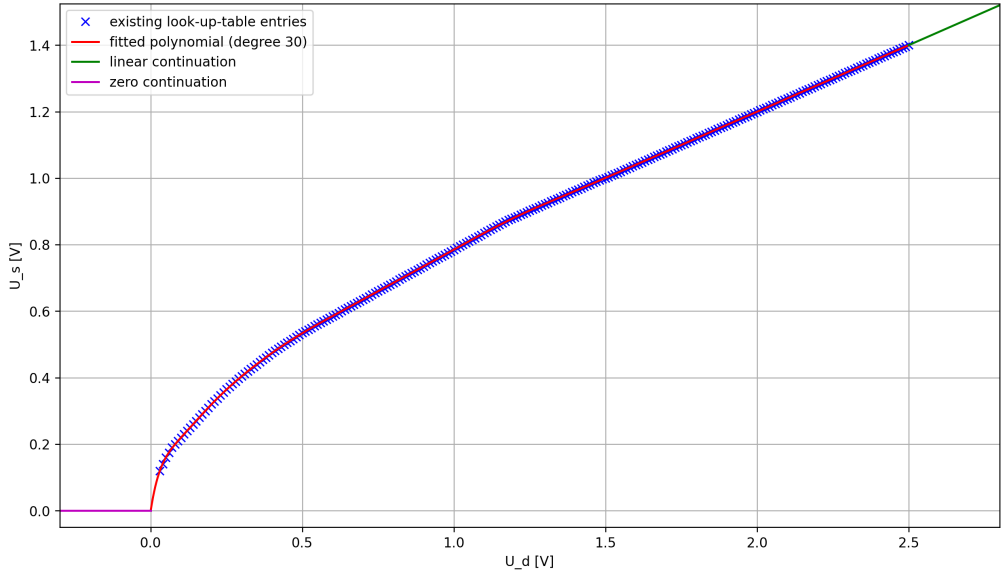
Resource Sharing implementation:

20 channel pairs @ 5 MHz

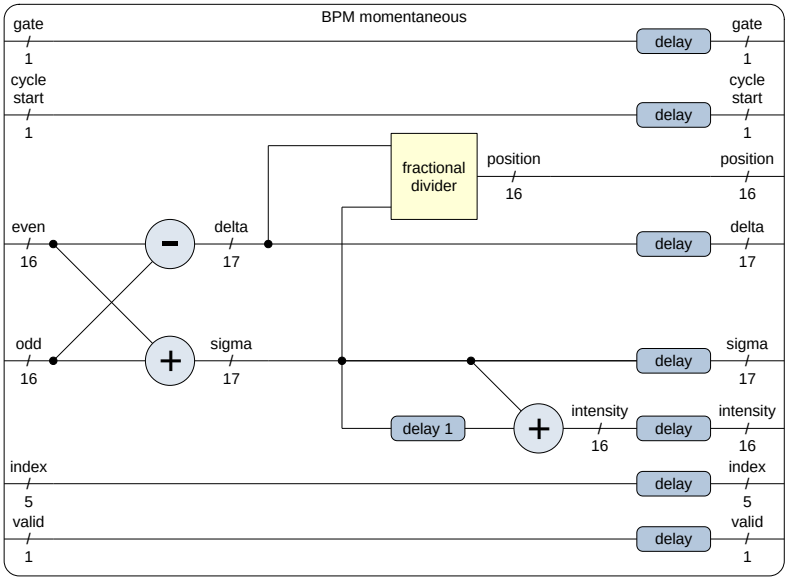
→

1 processing path @ 100 MHz interleaved

Demodulator Nonlinearity Correction



Momentaneous Position Calculation

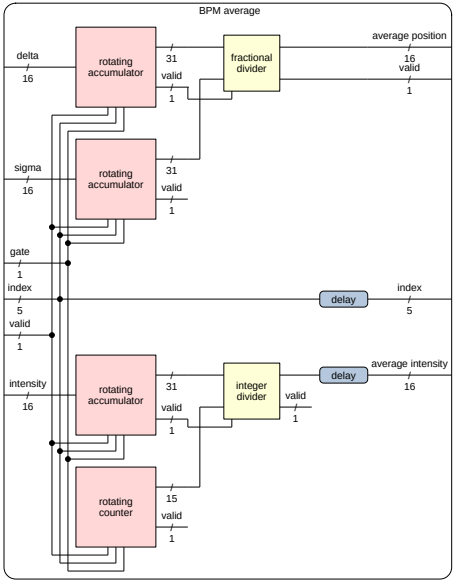


$$x = r \cdot \frac{\delta}{\sigma} = r \cdot \frac{U_R - U_L}{U_R + U_L}$$

with $r = 25$ mm
(BPM radius)

$$I = \xi \cdot \sigma' =$$
$$\xi \cdot (U_R + U_L + U_T + U_B)$$

Average Position Calculation



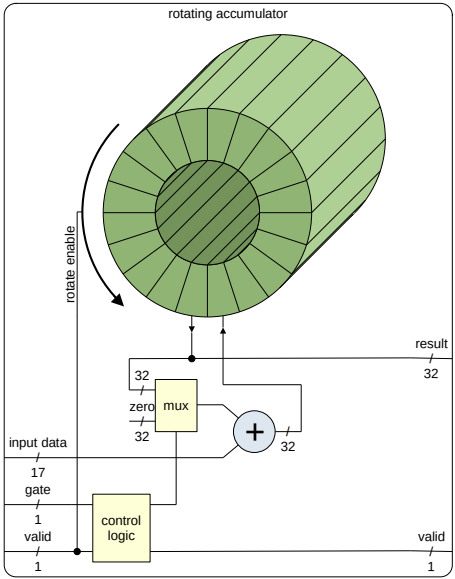
$$x_a = r \cdot \frac{\overline{\delta}}{\overline{\sigma}} = r \cdot \frac{\overline{U_R} - \overline{U_L}}{\overline{U_R} + \overline{U_L}}$$

with $\overline{U_R} = \frac{\sum_{i=1}^{N} U_{R,i}}{N}$ and $\overline{U_L} = \frac{\sum_{i=1}^{N} U_{L,i}}{N}$

(arithmetic means of the voltages over a macro pulse)

$$I_a = \overline{I} = \frac{\sum_{i=1}^{N} I_i}{N}$$

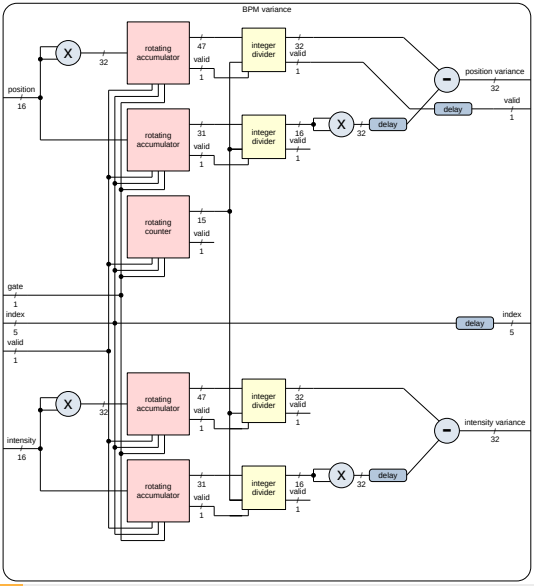
Resource Sharing Implementation - Detail



Averaging breaks the pipelining concept:

- while the rest of the algorithm is independent from the number of channels, averaging requires one storage element per channel
- implemented here as a rotating set of registers

Variance Calculation



$$Var(x) = \overline{x^2} - \overline{x}^2$$

$$Var(I) = \overline{I^2} - \overline{I}^2$$

Averaging Algorithm - Possible Improvement

Algorithm e.g. used in the Cryring BPM gateware:

- linear least squares fitting with an unknown offset
- evaluated in a paper by A. Reiter, R. Singh, 2017
- automatic offset compensation

$$\frac{x}{\kappa} = \frac{N\sum_i \sigma_i\delta_i - (\sum_i \sigma_i)(\sum_i \delta_i)}{N\sum_i \sigma_i^2 - (\sum_i \sigma_i)^2}$$

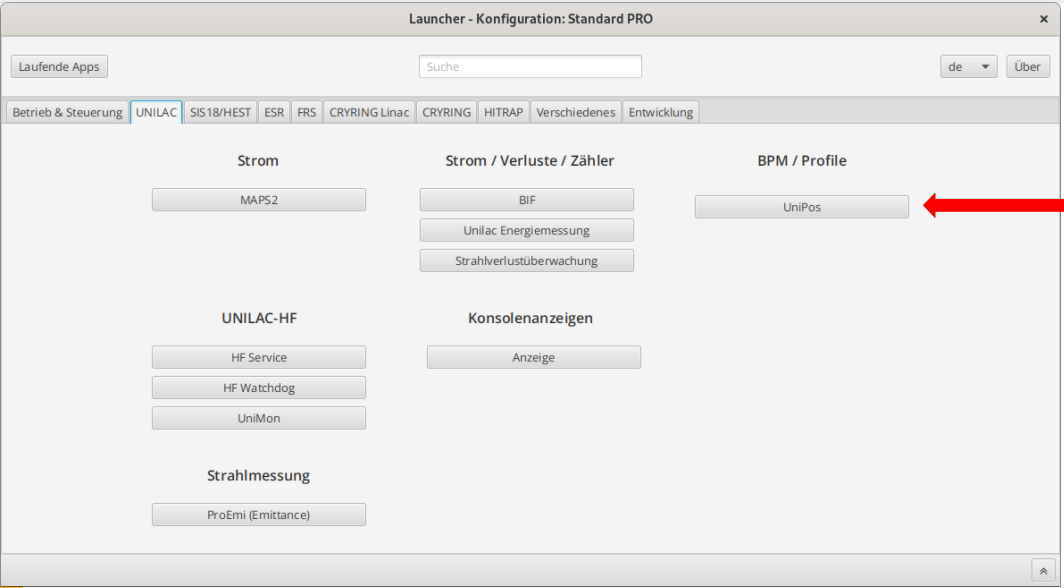
Challenges:

- needs varying amplitudes to work, e.g. by including data from outside of macro pulse
- variable macro pulse length $\rightarrow$ varying window optimal
- information by Wolfgang: serious interferences possible outside of macro pulse

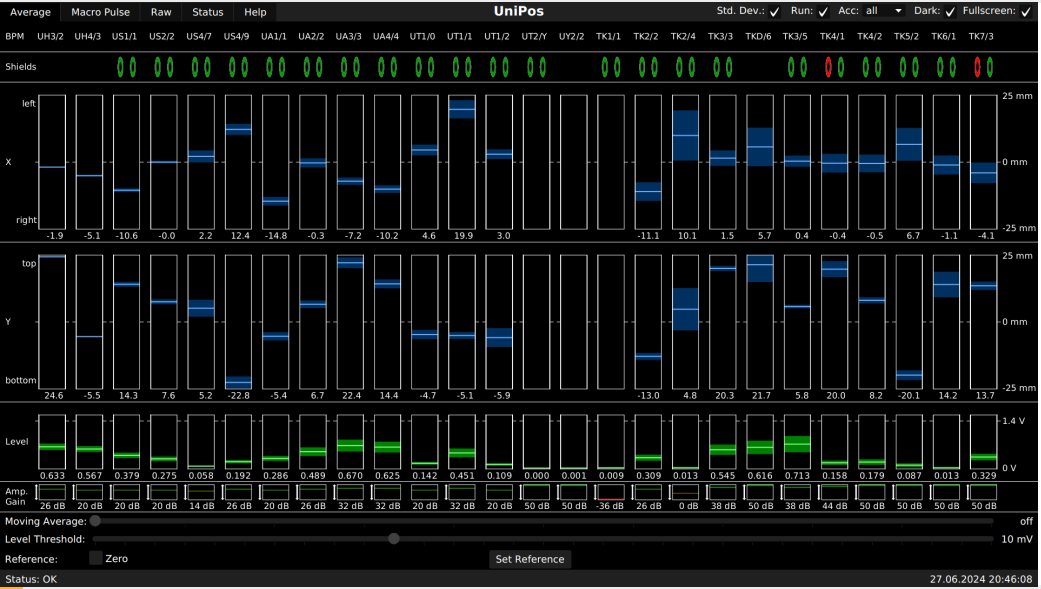
Additional Averaging in GUI

→ Hopefully no more "Lichtorgel"!

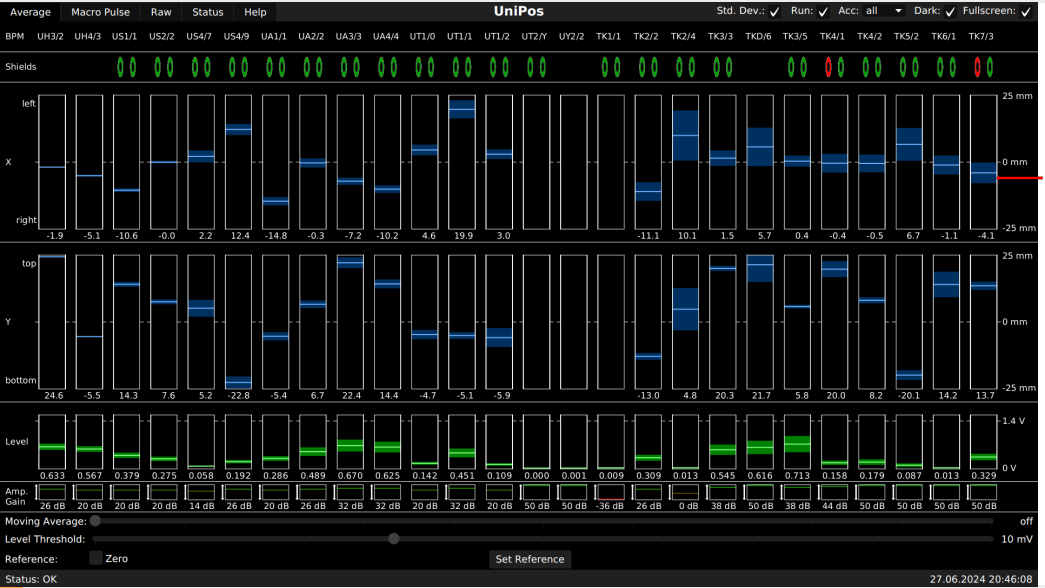
How to start in HKR



Average Tab

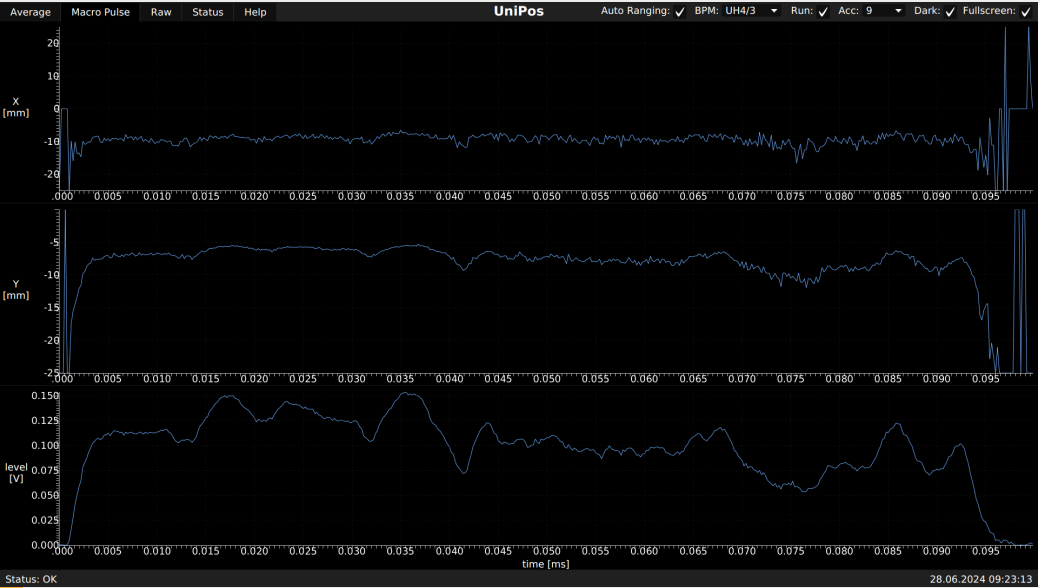

Average
Macro Pulse
Raw
Status
Help
UniPos
Std. Dev.:
Run:
Acc: all
Dark:
Fullscreen:
BPM UH3/2 UH4/3 US1/1 US2/2 US4/7 US4/9 UA1/1 UA2/2 UA3/3 UA4/4 UT1/0 UT1/1 UT1/2 UT2/Y UY2/2 TK1/1 TK2/2 TK2/4 TK3/3 TKD/6 TK3/5 TK4/1 TK4/2 TK5/2 TK6/1 TK7/3
Shields
left
X
right
25 mm
0 mm
-25 mm
-1.9 -5.1 -10.6 -0.0 2.2 12.4 -14.8 -0.3 -7.2 -10.2 4.6 19.9 3.0 -11.1 10.1 1.5 5.7 0.4 -0.4 -0.5 6.7 -1.1 -4.1
top
Y
bottom
25 mm
0 mm
-25 mm
24.6 -5.5 14.3 7.6 5.2 -22.8 -5.4 6.7 22.4 14.4 -4.7 -5.1 -5.9 -13.0 4.8 20.3 21.7 5.8 20.0 8.2 -20.1 14.2 13.7
Level
1.4 V
0 V
0.633 0.567 0.379 0.275 0.058 0.192 0.286 0.489 0.670 0.625 0.142 0.451 0.109 0.000 0.001 0.009 0.309 0.013 0.545 0.616 0.713 0.158 0.179 0.087 0.013 0.329
Amp. Gain
26 dB 20 dB 20 dB 20 dB 14 dB 26 dB 20 dB 26 dB 32 dB 32 dB 20 dB 32 dB 20 dB 50 dB 50 dB -36 dB 26 dB 0 dB 38 dB 50 dB 38 dB 44 dB 50 dB 50 dB 50 dB 50 dB
Moving Average:
off
Level Threshold:
10 mV
Reference:
Zero
Set Reference
Status: OK
27.06.2024 20:46:08

Standard Deviation Interpretation

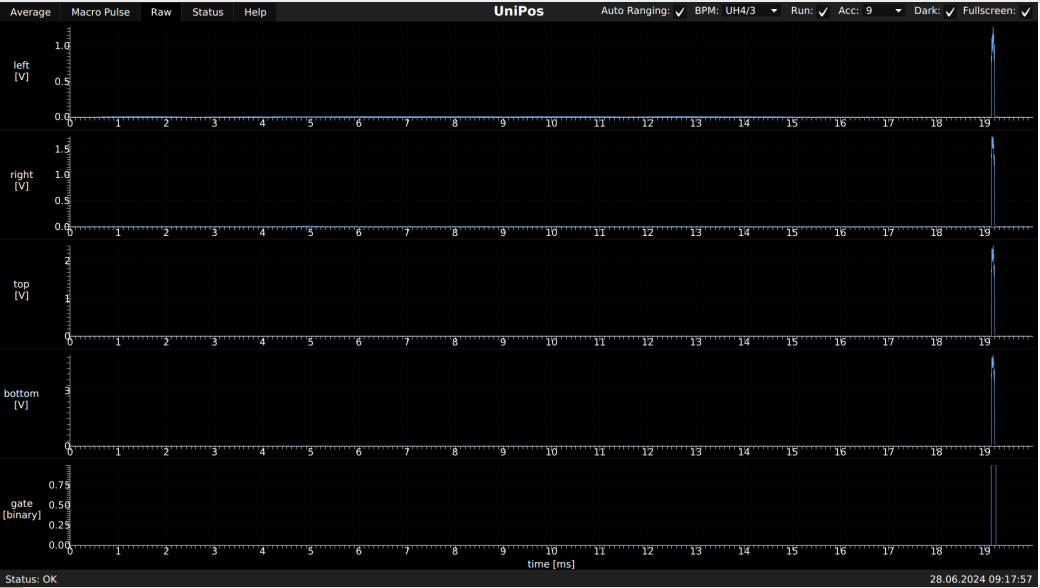


The standard deviation should not be understood as error bars, but in most cases is dominated by the variation of the position during a macro pulse.

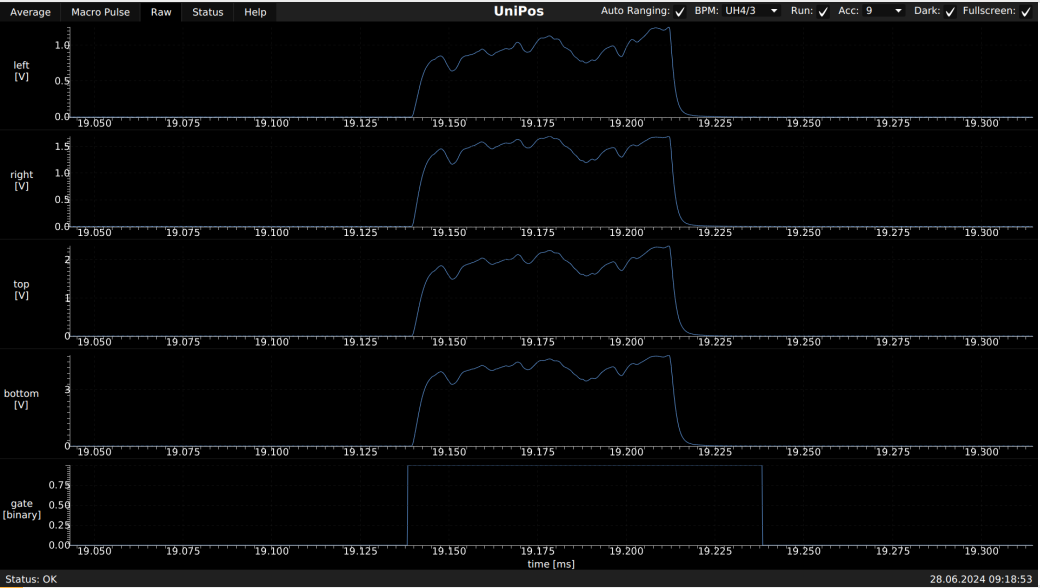
Macro Pulse Tab



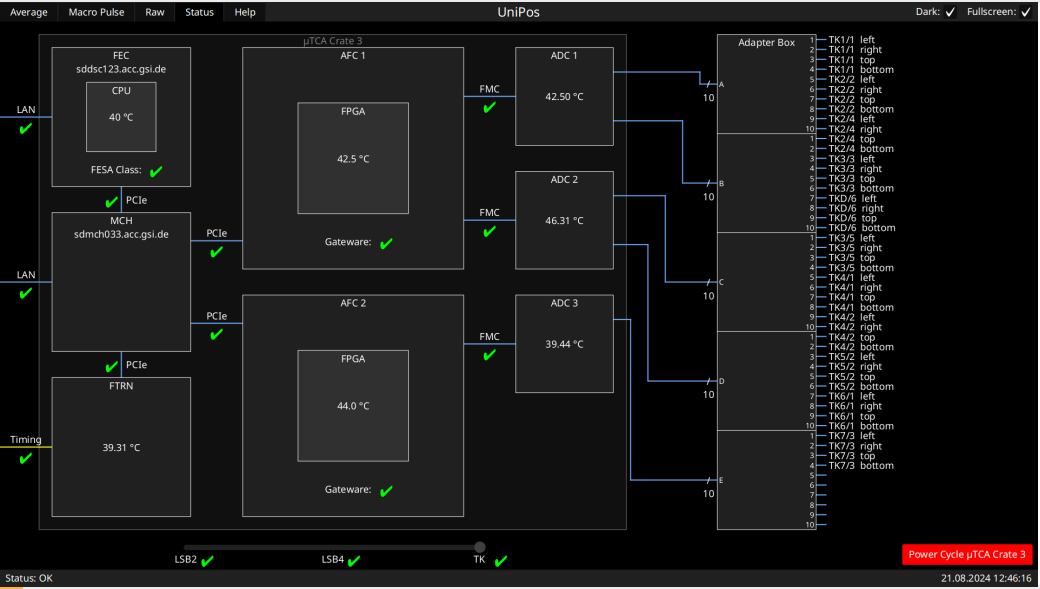
Raw Tab


Average
Macro Pulse
Raw
Status
Help
UniPos
Auto Ranging:
BPM: UH4/3
Run:
Acc: 9
Dark:
Fullscreen:
left [V]
right [V]
top [V]
bottom [V]
gate [binary]
time [ms]
Status: OK
28.06.2024 09:17:57

Raw Tab - Detail



Status Tab


Average
Macro Pulse
Raw
Status
Help
UniPos
Dark:
Fullscreen:
µTCA Crate 3
FEC
sddsc123.acc.gsi.de
CPU
40 °C
FESA Class:
LAN
PCIe
MCH
sdmch033.acc.gsi.de
LAN
PCIe
PCIe
FTRN
39.31 °C
Timing
AFC 1
FPGA
42.5 °C
Gateware:
AFC 2
FPGA
44.0 °C
Gateware:
FMC
FMC
FMC
ADC 1
42.50 °C
ADC 2
46.31 °C
ADC 3
39.44 °C
Adapter Box
A
B
C
D
E
10
TK1/1 left
TK1/1 right
TK1/1 top
TK1/1 bottom
TK2/2 left
TK2/2 right
TK2/2 top
TK2/2 bottom
TK2/4 left
TK2/4 right
TK2/4 top
TK2/4 bottom
TK3/3 left
TK3/3 right
TK3/3 top
TK3/3 bottom
TKD/6 left
TKD/6 right
TKD/6 top
TKD/6 bottom
TK3/5 left
TK3/5 right
TK3/5 top
TK3/5 bottom
TK4/1 left
TK4/1 right
TK4/1 top
TK4/1 bottom
TK4/2 left
TK4/2 right
TK4/2 top
TK4/2 bottom
TK5/2 left
TK5/2 right
TK5/2 top
TK5/2 bottom
TK6/1 left
TK6/1 right
TK6/1 top
TK6/1 bottom
TK7/3 left
TK7/3 right
TK7/3 top
TK7/3 bottom
LSB2
LSB4
TK
Power Cycle µTCA Crate 3
Status: OK
21.08.2024 12:46:16

Open Tasks

Support (Wolfgang and/or Operators + beam) required:

- checking of the 104 channels
- offset and gain calibration of 104 channels
- time of flight calibration
- comparison of positions to "Gitter"results

Open Tasks (not me, e.g. Kajetan Fuchsberger)

- A central service for all *Device Access* accesses
- Unification of applications:
  - Phasensondenansteuerung (PHAS)
  - Unilac-Energiemessung (via TOF)
  - UniPos

Known Issues

- 11 of the 104 channels seem the be dead $\rightarrow$ corroded LEMOs or electronic defects?
- suspiciously small signals on multiple other channels
- when switching the amplifier gain, some position results change $\rightarrow$ different nonlinearity?
- all *Device Access* accesses (amplifier gain, shields): Readout to slow or not working when there are competing accesses.

Feel free to test it!
But don't rely on any results!

Thank you!