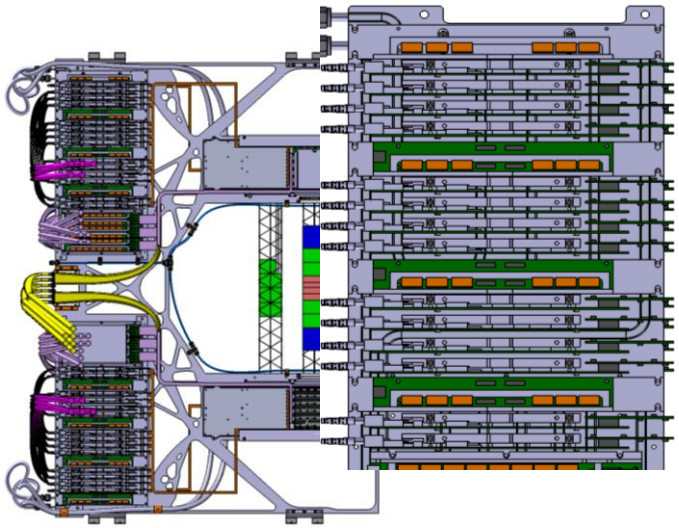
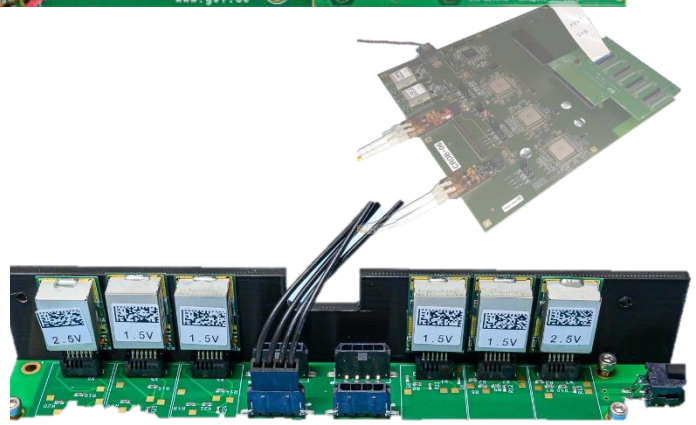
STS Readout Developments

Final Boards for STS Integration: STS-ROB, RPOB, FPOB



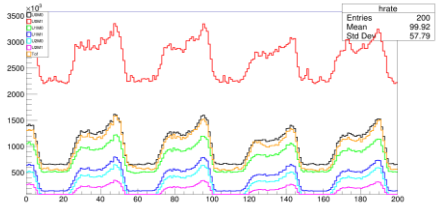


J. Lehnert,
R. Kapell, P. Semeniuk

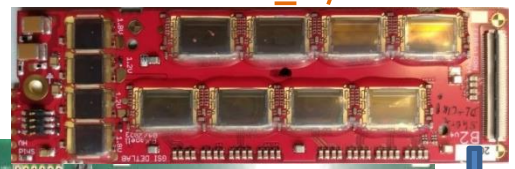
46th CBM Collaboration Meeting
Tue. 21.10.2025

From CROB to STS-ROB

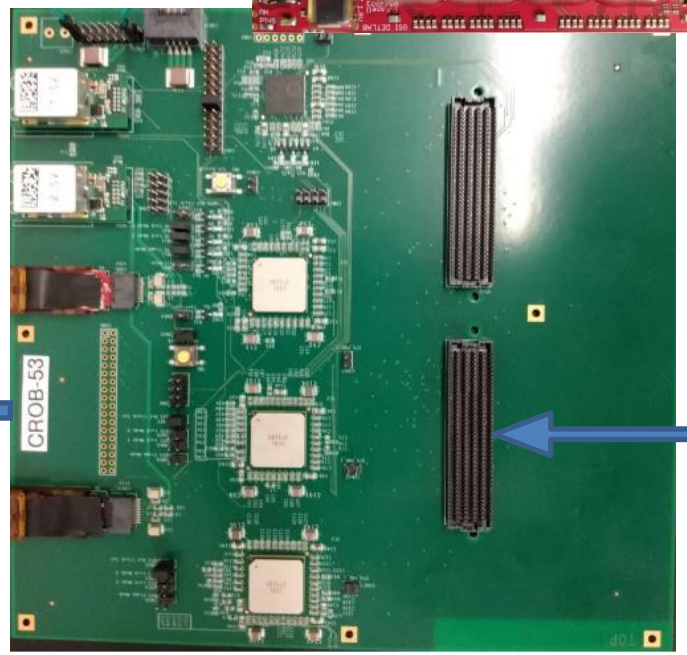
mSTS Data Rates



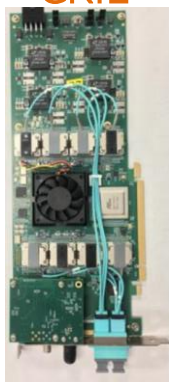
FEB8_1/2



CROB

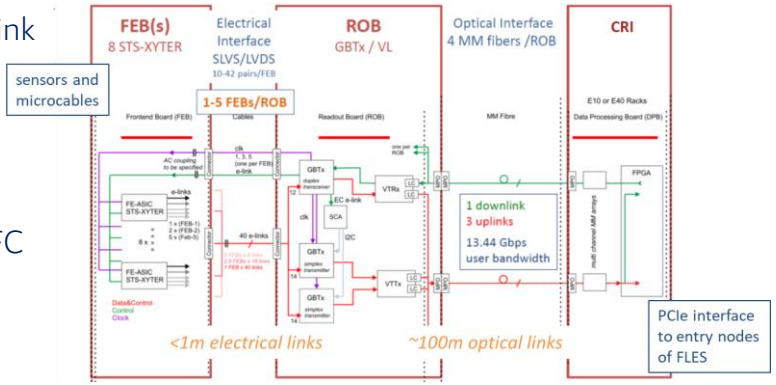


CRI1



STS Readout Chain

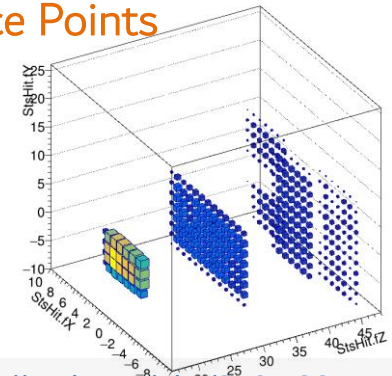
- **1752** FEB8 with 8 SMX ASICs
  - 1-5 uplinks 320 Mbps uplinks (9.4-47 MHits/s/link; 73-367 kHits/s/channel)
  - common clock and downlink
- **576** ROB3
  - data aggregation from 40 uplinks (1-5 FEB8)
- **76** CRI (8 ROB3 each)
  - data readout, controls, TFC



significantly smaller form factor

STS-ROB

mSTS Reconstructed Space Points

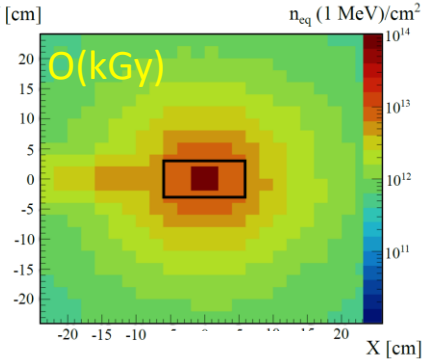


Common Readout Board (CROB)

- full required ROB3 functionality for STS
- in use **since 2018** (mCBM and test setups)
  - up to 7 boards in mSTS
  - also mMUCH, mTRD1D, (mTRD2D), mMVD

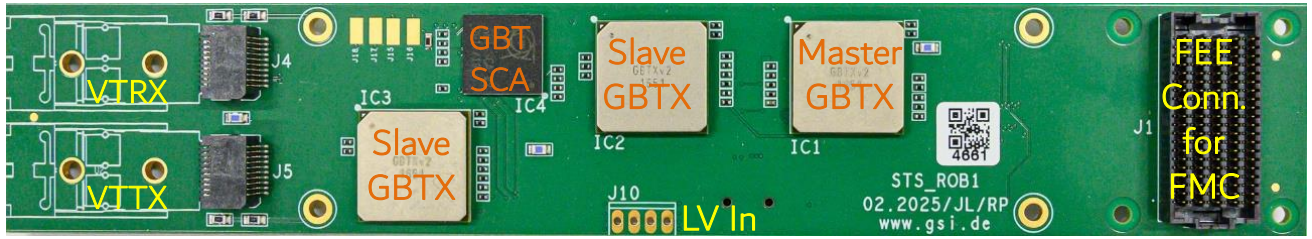
Rad. Hard GBTX and VTRX

Irradiation at 1st STS station



https://arxiv.org/abs/2505.20517

STS-ROB Design



Assembled STS-ROB

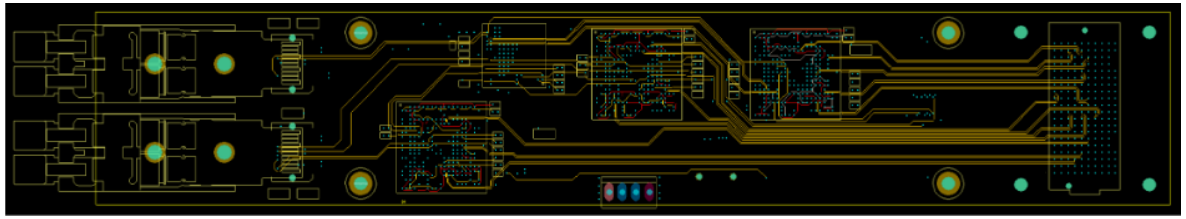
STS Readout Board

- same GBTX/VL functionality as CROB
- size: 201 mm x 36 mm (CROB: 208 mm x 199 mm)
- powering: FEAST_MP off-board
- commissioning: configuration and monitoring off-board
- hardwired configuration pins
- re-arrangement of GBTX/VL locations
- FEE connector: 200pin
  - Samtec SEAF-20-05.0-S-10-2-A-K-TR
  - elinks required for STS, MVD
  - custom pinout

STS-ROB PCB

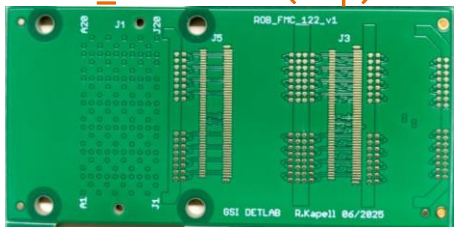
- 14 layer design
- components on top and bottom layer
- 5 inner signal layers
  - impedance controlled (100 ohm differential)
- elinks between master(25), slave GBTX(17) and FEE connector

Inner Signal Layer



Layout: R.Pursch (GSI/EE)

FMC_122 PCB (Top)



FMCs

- addon board for various FEE connectivity
  - ZIF connectors for each FEB8
- first type FMC_11111 (5 x FEB8_1)
  - used for full FEE connectivity tests
- 7 types in total (no readout cable crossing)
  - FMC_11111
  - FMC_122 and FMC_221
  - FMC_1112 and FMC_2111
  - FMC_5(t) and FMC_5(b)

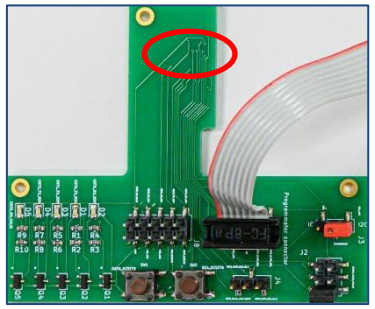
Assembled STS-ROB with VTXx and FMC

STS-ROB Testing

STS-ROB Testing and Characterization

- extensive evaluation of operational functionality and data transmission
- focus on features modified wrt CROB
  - layout related
- optimization of selected components

STS-ROB Testing



Addon Board for Commisioning

- I2C
- efusing
- monitoring

No relevant issues observed

External Power Supply

- voltage drops
- operational V range
- stability

VCC_1V5 [V]	I(1V5) [A]	Status FEC
1.60	1.431	OK, no issues
1.50	1.30	OK, no issues
1.40	1.17	OK, no issues
1.32	1.04	OK, no issues
1.28	0.963	**FEC unstable**

Operation at var. VDD

Efuse Configuration

Transmission Error Rates

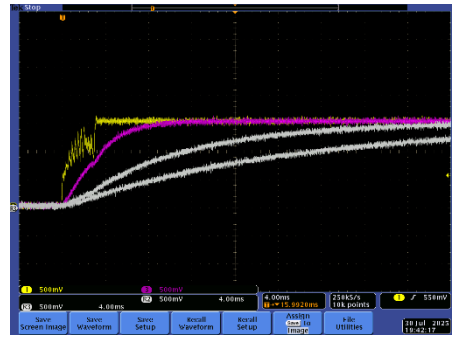
Elinks

Metric	Short run	Long run
Transactions executed	28 000	1 162 400
Elapsed time	119.0 s	5 399.0 s
Avg transaction	235.3 /s	215.3 /s
Uplinks executed	40 / 40	

Optical links

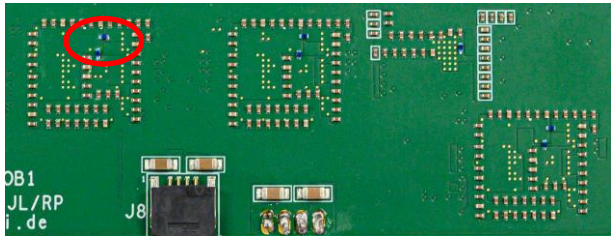
BER < 1×10^{-13}

Powerup/Startup/Reset



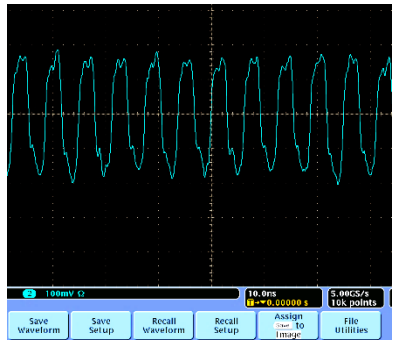
Startup: 1.5V and various ResetB settings

Onboard LV Filtering

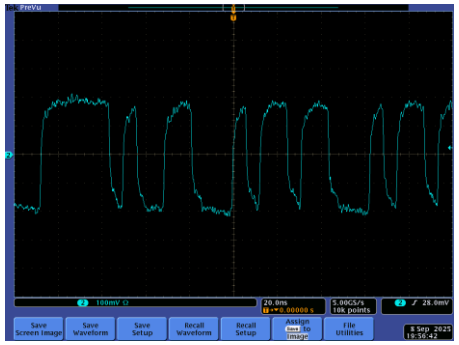


VDDRx/VDDTx Inductances

Signal Integrity

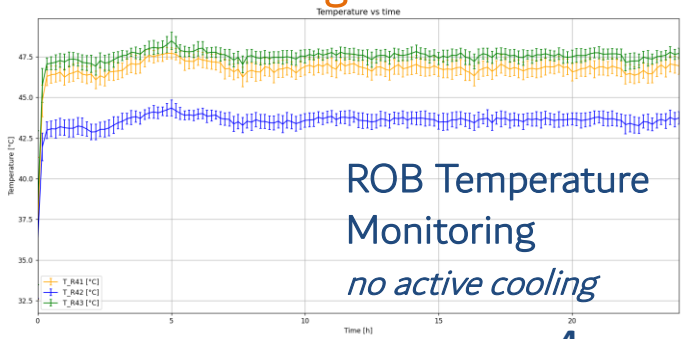


FEE Clock



FEE Downlink

SCA Monitoring



ROB Temperature Monitoring

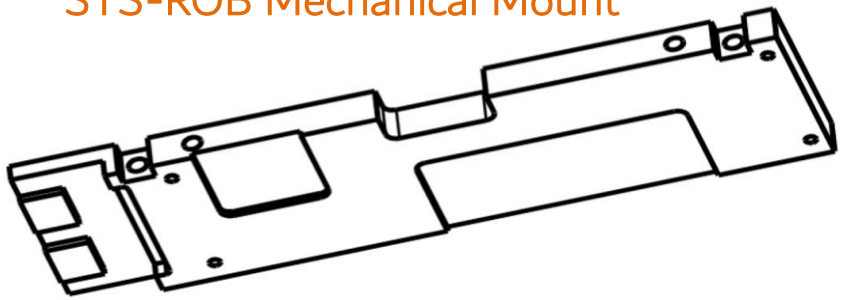
no active cooling

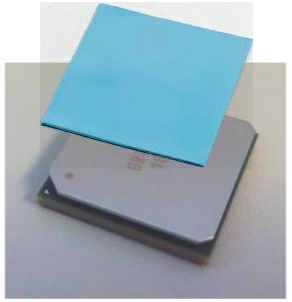
STS-ROB Integration

Mechanical Mount and Cooling

- STS-ROB PCB screwed to mechanical support fin
  - components towards fin
- interface with thermal pads to all power dissipating devices
  - structured surface to accommodate height differences
- dissipated power ~5W
  → factor 4 lower than on FEB8 fin

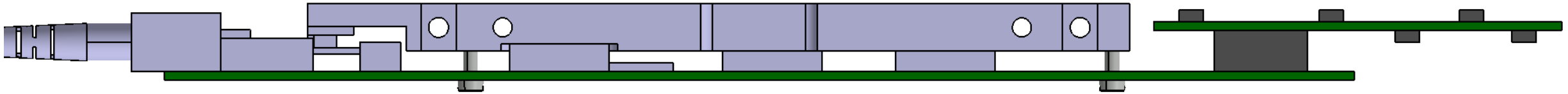
STS-ROB Mechanical Mount





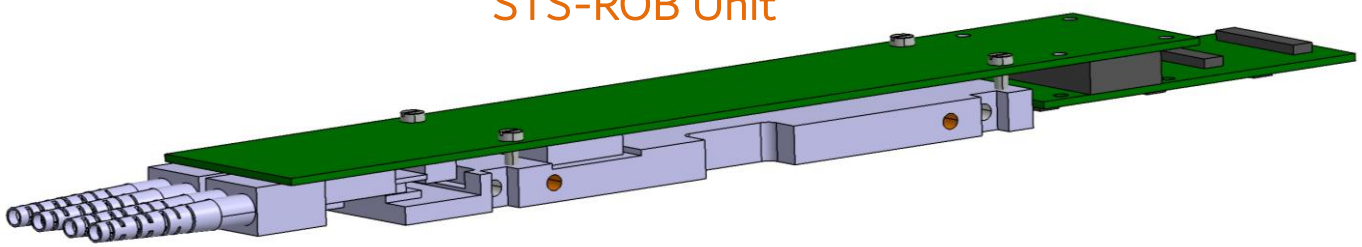
GBTX ASIC with Cooling Interface and Thermal Pad

Side View of STS-ROB Unit with Mech. Mount, FMC and VTXx



Power Dissipation and Temperature (Uncooled!)

STS-ROB Unit



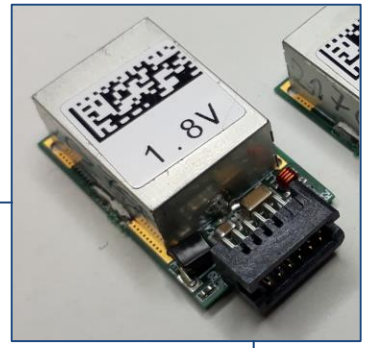
mechanics designs: O. Vasiliev (GSI/DTL)

FPOB and RPOB Powering

Powering for STS Frontend Boards and Readout Boards

- radiation tolerant FEAST_MP (CERN) DCDC converter
  - custom CBM form factor
- installed on dedicated Powering Board (PoB)

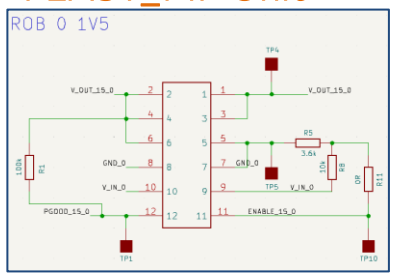
FEAST_MP
CBM form factor



Frontend Board Powering

- 8 FEB8 per FPOB
- 1 x 2.4V and 1x 3.0V FEAST_MP per FEB8
- LDOs on FEB for 1.2V and 1.8V
- each FEB8 and its FEAST_MP on corresponding sensor bias potential up to +/- 250V
- used in mSTS

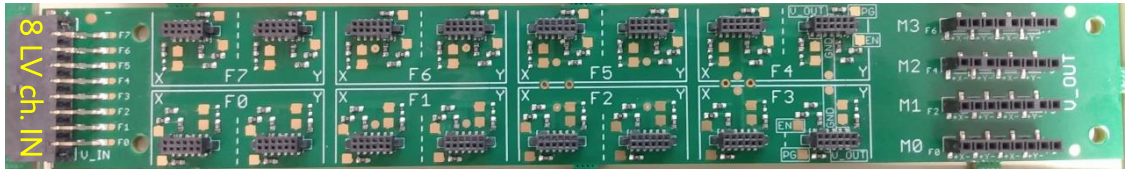
Schematics
FEAST_MP Unit



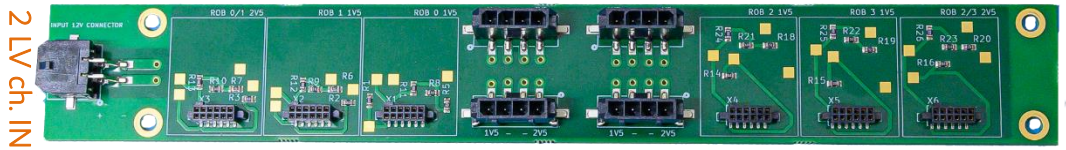
Readout Board Powering

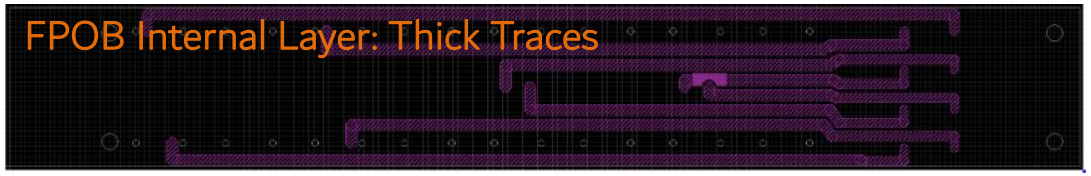
- 1 x 1.5V FEAST_MP per ROB
- 1 x 2.5V FEAST_MP per 2 ROB
- 1 LV channel per 3 ROB
- 4 ROB per RPOB
- short (4-8cm) LV cables
- all RPOB and ROB on common GND

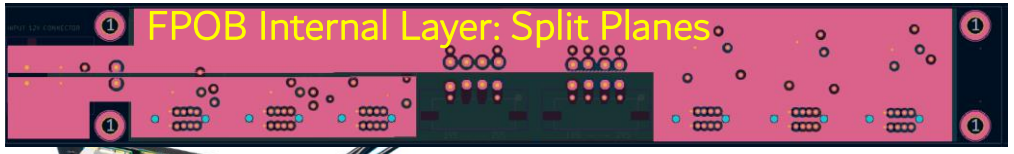
Assembled FPOB



Assembled RPOB

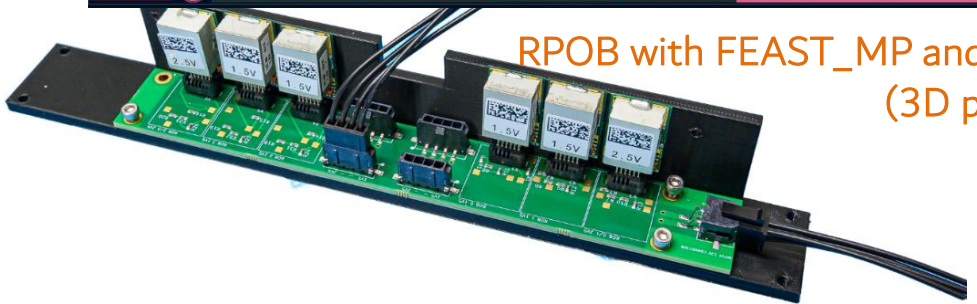






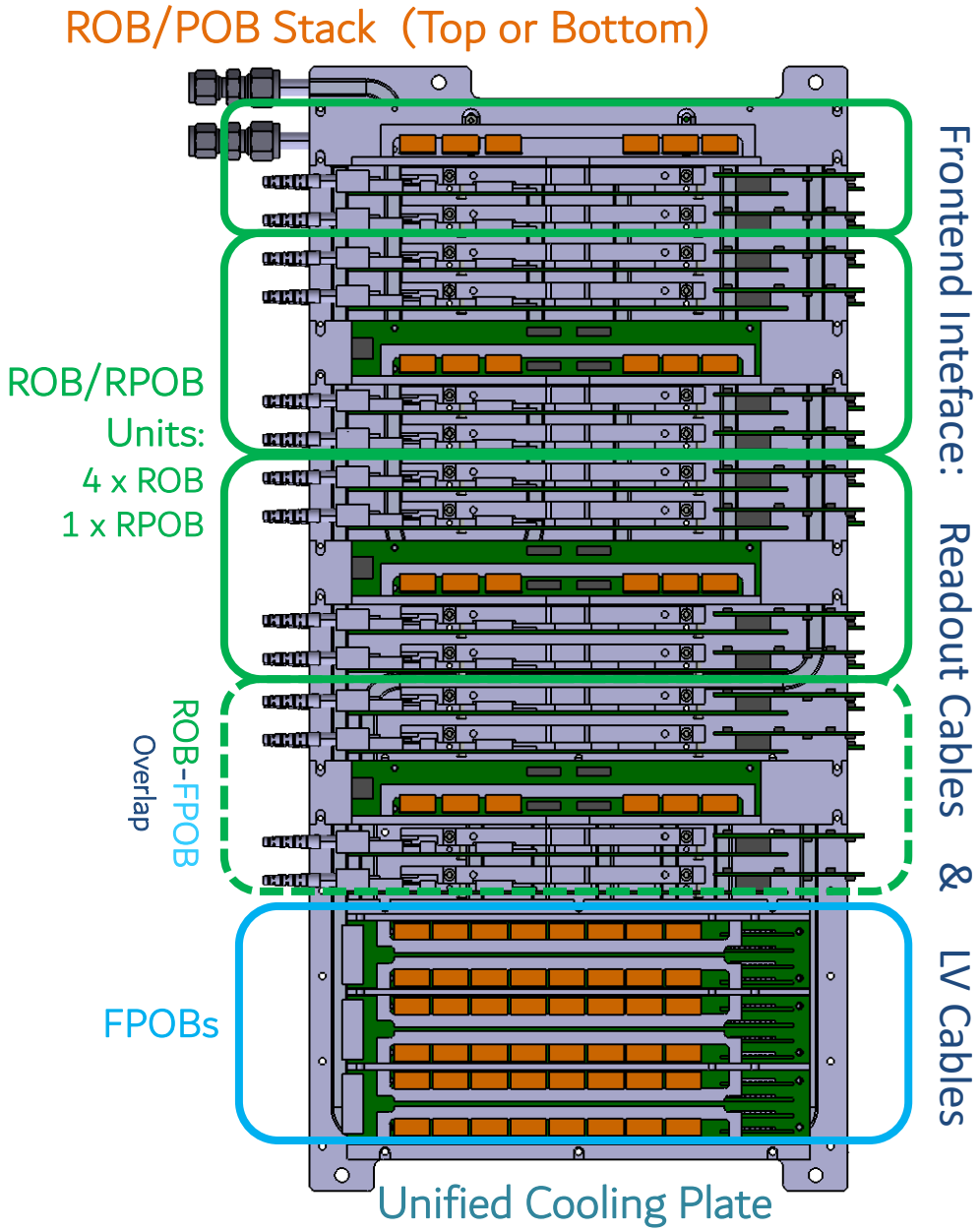
FPOB Isolation Test 500V

FPOB with Sumida LV cables to FEBs



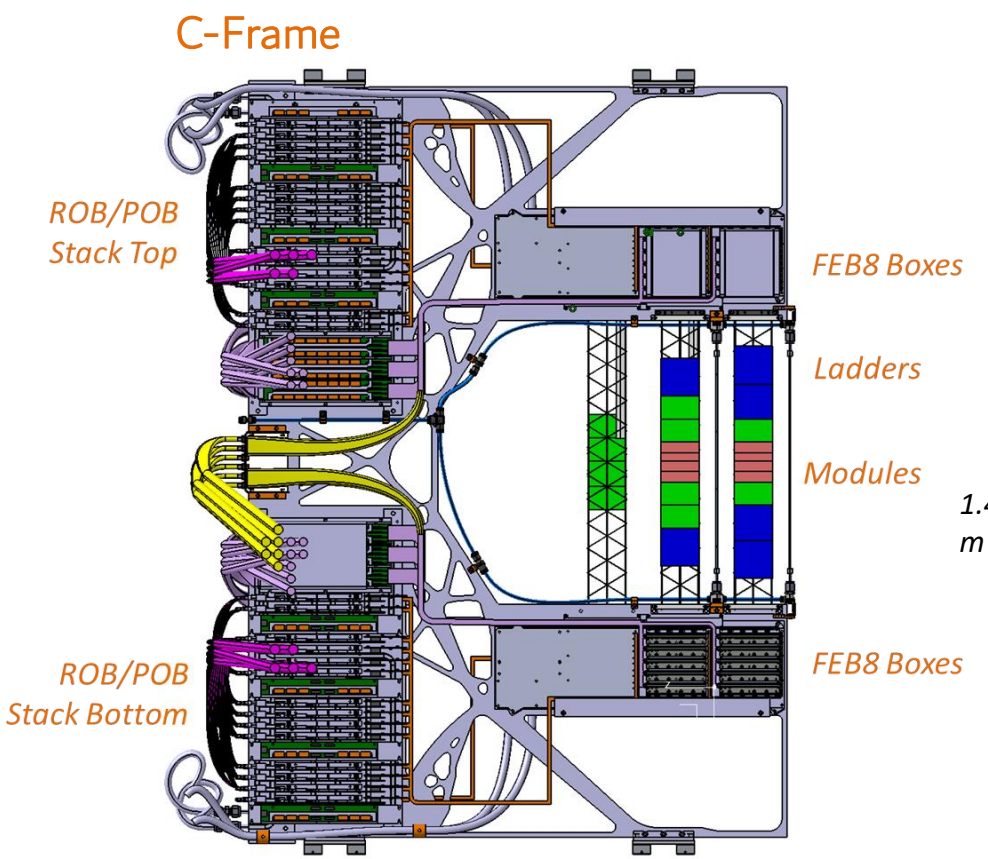
RPOB with FEAST_MP and L-Cooling Fin
(3D printed mockup)

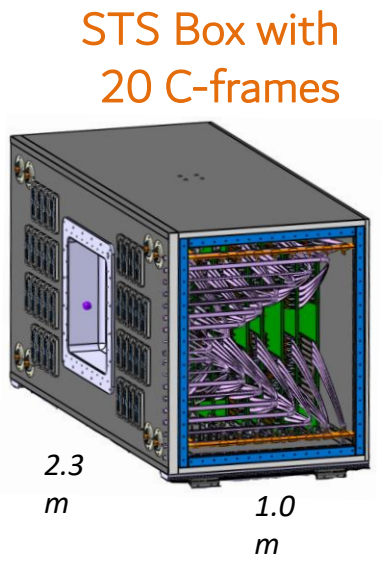
The ROB/POB Stack



STS-ROB on ROB/POB Stack

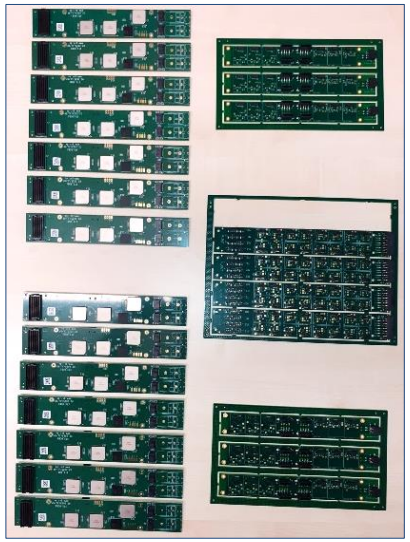
- ROB mounted on top or bottom of fin
  - only one ROB version (no symmetric twin needed)
- ROB-FMC with ZIF connectors on top/bottom
  - two cable types (same/opposite side contacts)





Status

- components for full STS readout and powering **developed, built, tested**
  - STS-ROB, RPOBs, FPOBs, FMC_11111 (FMC_122 in the next days)
- sufficient boards **available for integration of first C-Frame**
- when mechanics components available
  - characterization of cooling performance
  - assembly of first ROB/POB stack
- some additional characterization work
  - extended BER tests
- Rev.2 with minor modifications
  - mostly optimizations for series assembly and testing
- **Production Readiness Review** for STS-ROB and RPOB, FPOB
  - successfully done last Thu. 16.10.25
  - *https://indico.gsi.de/event/23248/*



ROB and POB devices
for first C-frame