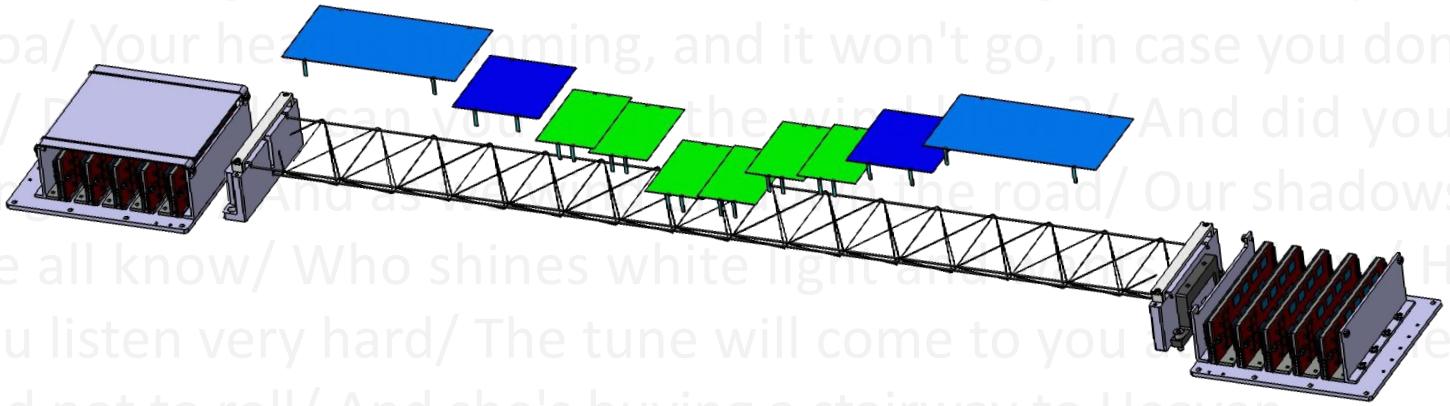
Stairways to heaven:🎶 the STS Ladder

46th CBM Collaboration meeting

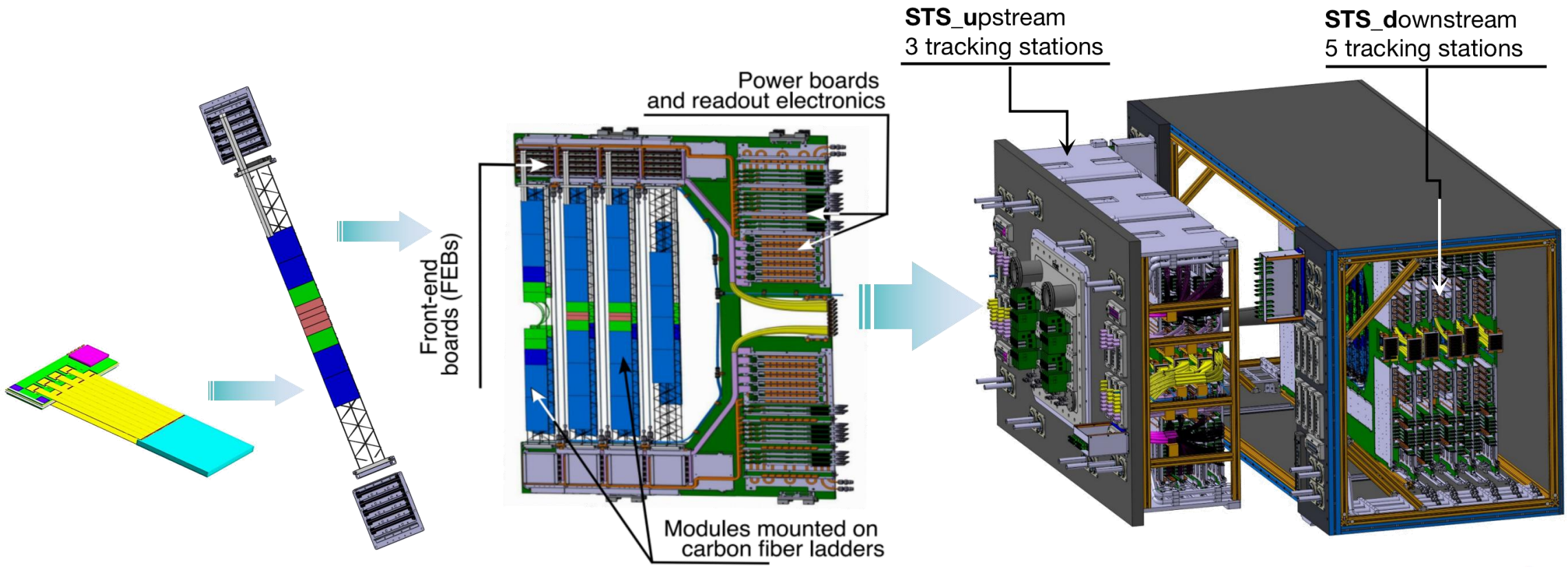
L.M. Collazo Sánchez *for the STS team*



October 24th , 2025

Lanzhou, China

BRIEF INTRODUCTION TO THE SILICON TRACKING SYSTEM OF CBM



876 modules
160 different modules
~1.8 million channels

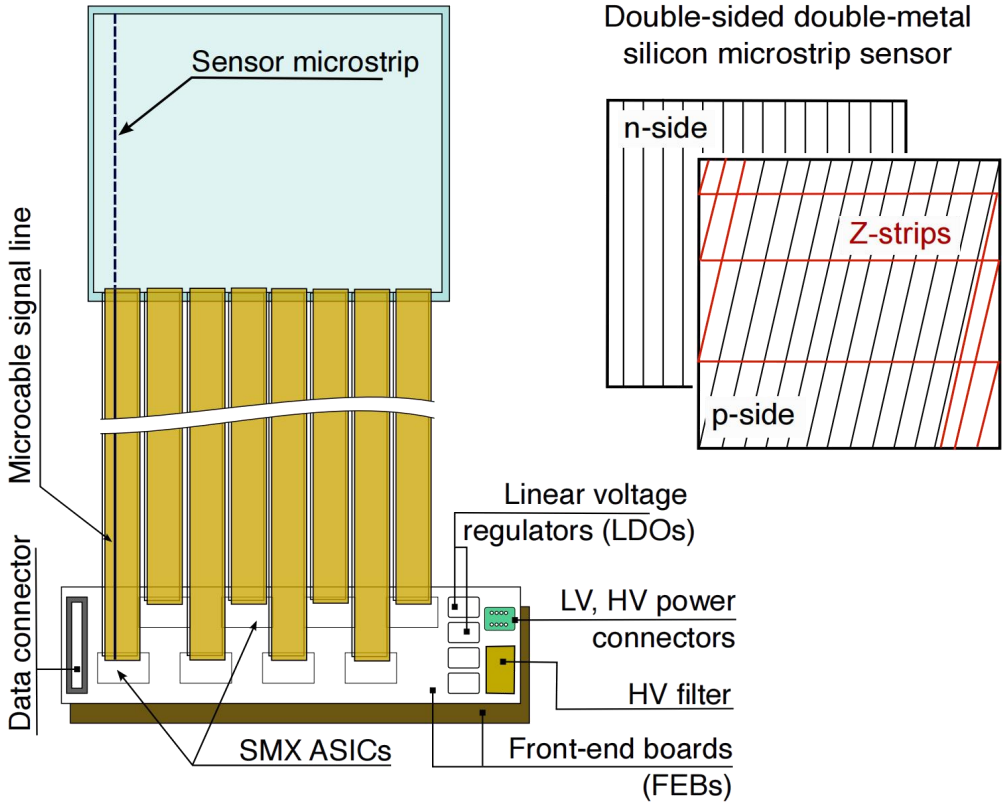
106 ladders
41 different form factors
2 - **10** modules

20 half-units

STS: 8 Tracking stations
3 **STS_u** + 5 **STS_d**

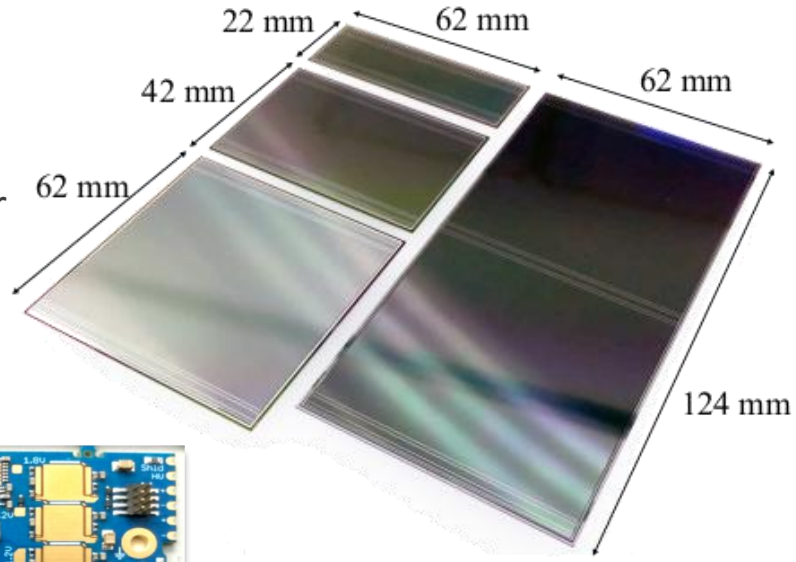
WHAT IS THE STS MODULE?

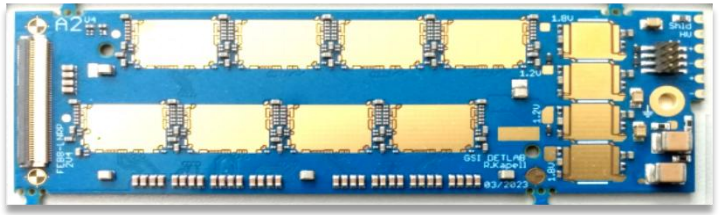
- 876 modules for STS
- 160 module variants (sensor + microcables)



Schematics of the STS detector module and its main components

- Thickness: 320 µm
- 1024 strips per side
- Pitch: 58 µm
- Double metalization layer in p-side
- 32 microcable stacks



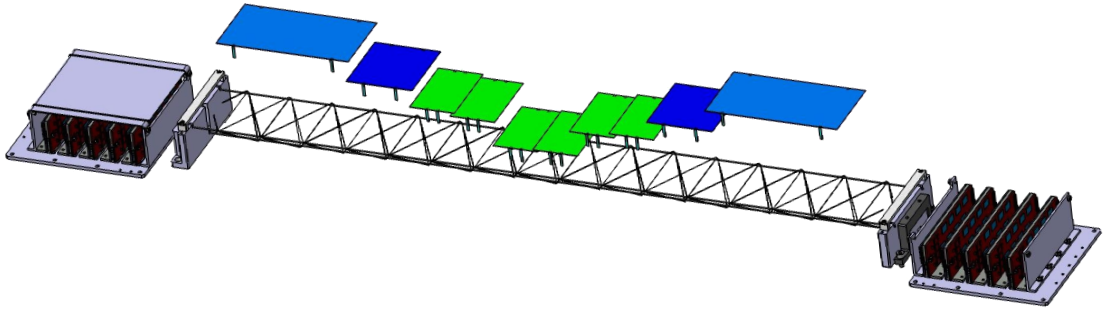


- 8 custom-design ASICs per Fornt-End Board (FEB)
- 128 channels per ASIC

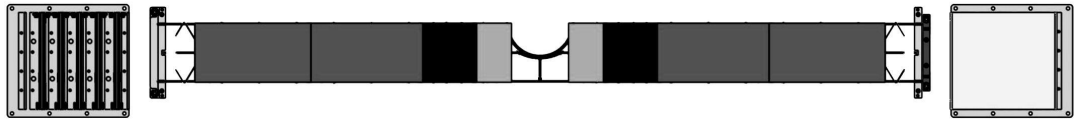
STS module before the shielding layers are soldered

A. Rodriguez Rodiguez et al. (2023), NIM A 1058 168813, DOI 10.1016/j.nima.2023.168813
M. Teklishyn et al. (2024), JINST 19 C07002, DOI 10.1088/1748-0221/19/07/C07002

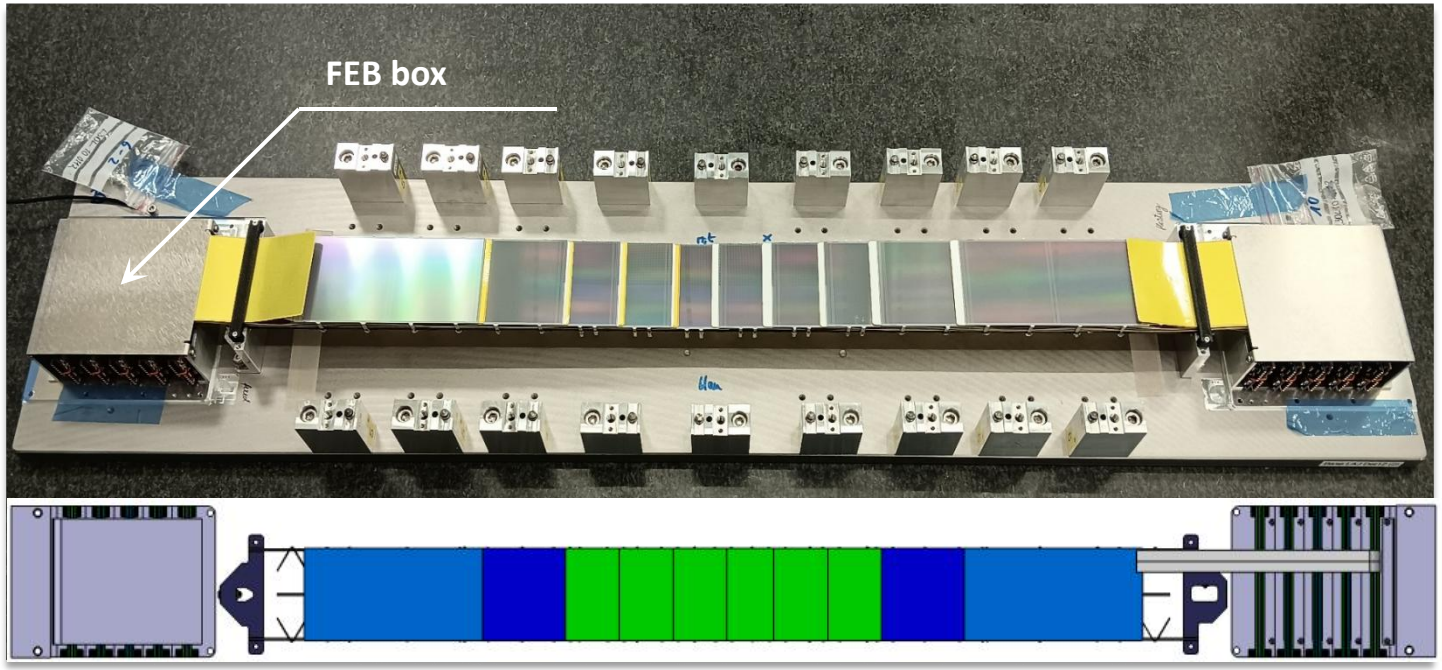
WHAT ARE STS LADDERS?



Central ladder



Peripheral ladder



Fully assembled STS ladder carrying 10 modules

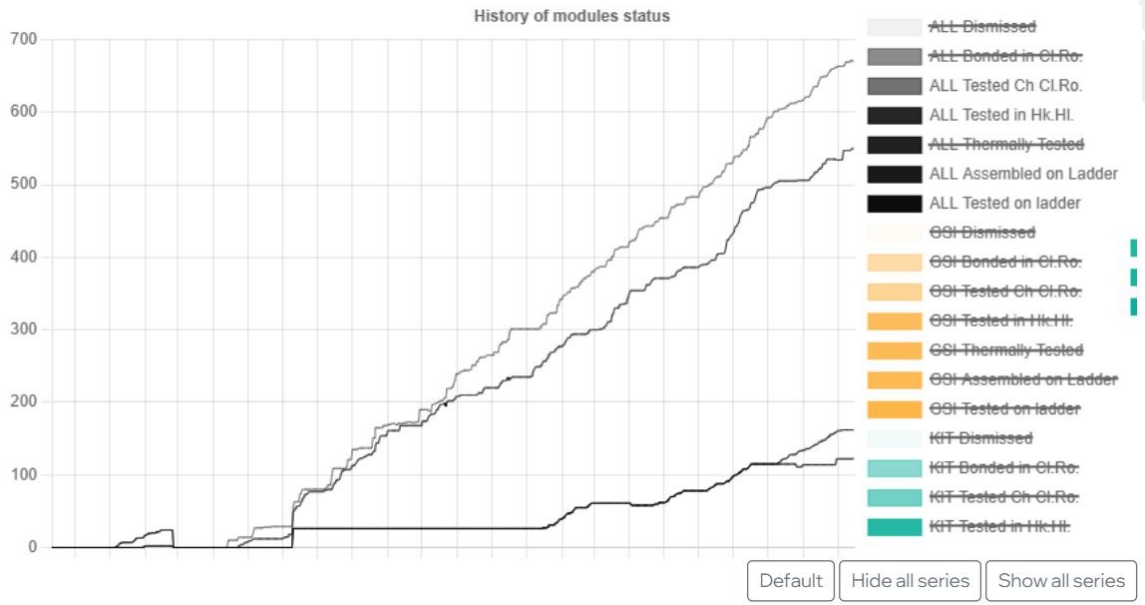
Towards STS full assembly:

- 106 ladders with different form factors (2-10 modules per ladder)

ASSEMBLY & TESTING STATUS

Where is STS today in terms of Assembly and Testing?

- Data/Status can be consulted under: STS database
  - Up to today **672** modules have been PRODUCED (**77%**)
  - **550** modules have been TESTED (**63%**)
  - Already **21** ladders have been BUILT with **162** out of the **550** tested modules (**18%**)
  - From them **15** ladders have been fully TESTED with **122** out of the **162** modules (**14%**)



Module statuses - All (GSI, KIT)

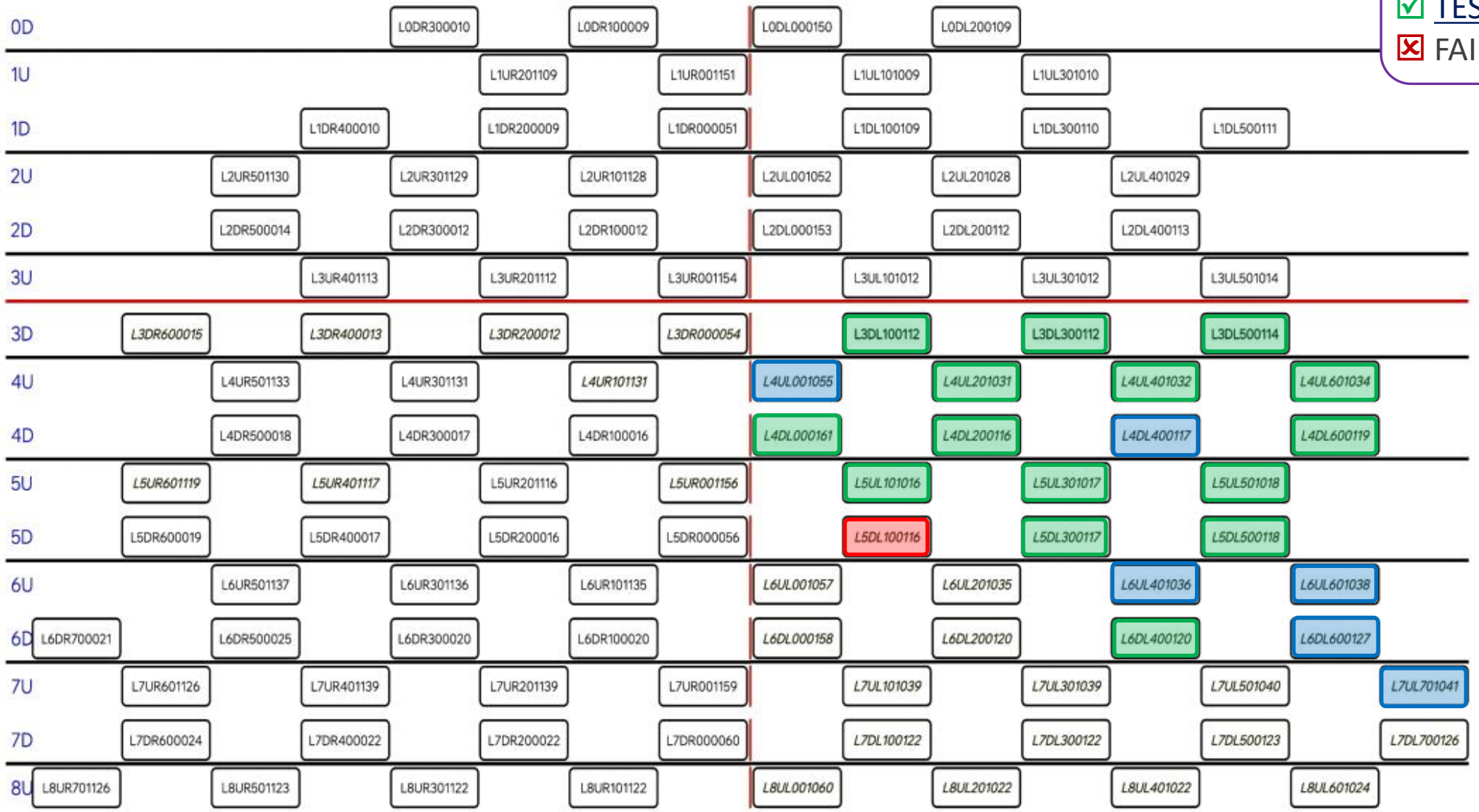
Total		GSI		KIT		
#	%	#	%	#	%	
122	14	99	80	23	20	Tested on ladder
162	18	125	80	37	20	Assembled on Ladder
550	63	367	70	183	30	Tested in Hk.Hl.
552	63	367	70	185	30	Undef. status at Hk.Hl.
582	66	394	70	188	30	Test started in Hk.Hl.
582	66	394	70	188	30	Tested HV in Cl.Ro.
672	77	448	70	224	30	Tested Ch Cl.Ro.
675	77	448	70	227	30	Bonded in Cl.Ro.
6	1	1	20	5	80	Wrongly built
34	4					Rebuilt modules
197	22	53	30	144	70	Reserved

ASSEMBLY & TESTING STATUS

Ladders

- ☑ ASSEMBLED: **21**
- ☑ TESTED: **15**
- ☒ FAILED: **1**

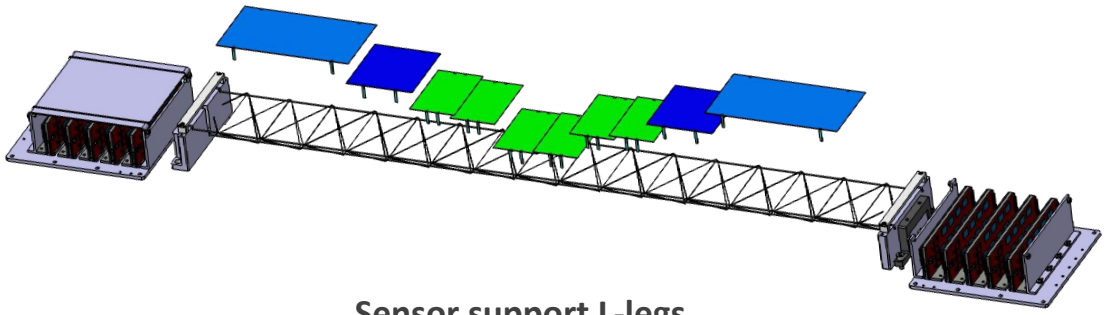
How do they distribute in STS?

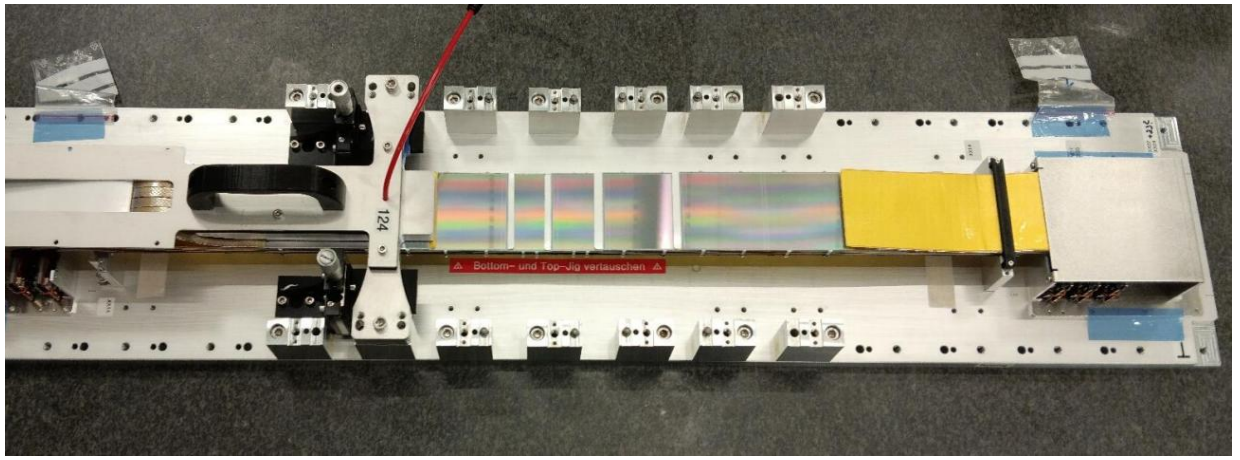


OUTLINE

- LADDER ASSEMBLY & METROLOGY
- LADDER TESTING SETUPS
- TESTING PROTOCOL
- OVERALL RESULTS
- ENCOUNTERED ISSUES & SOLUTIONS
- SUMMARY & OUTLOOK

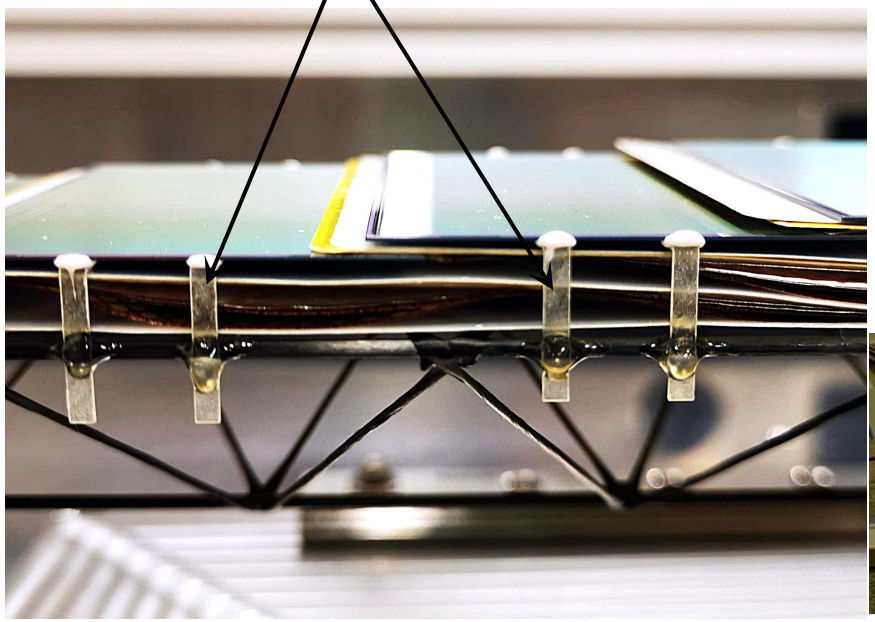
LADDER ASSEMBLY



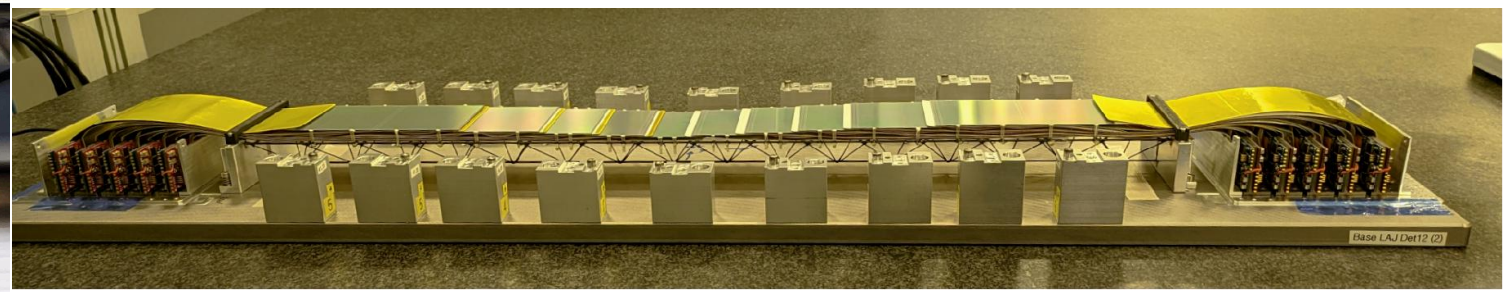


Fully assembled STS ladder carrying 10 modules

Sensor support L-legs



Detail of an assembled ladder, where sensors can be seen glued to the so-called "L-legs"

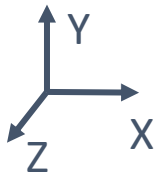


Fully assembled STS ladder carrying 10 modules

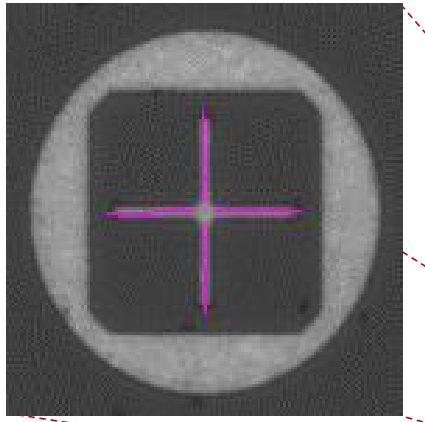
LADDER METROLOGY

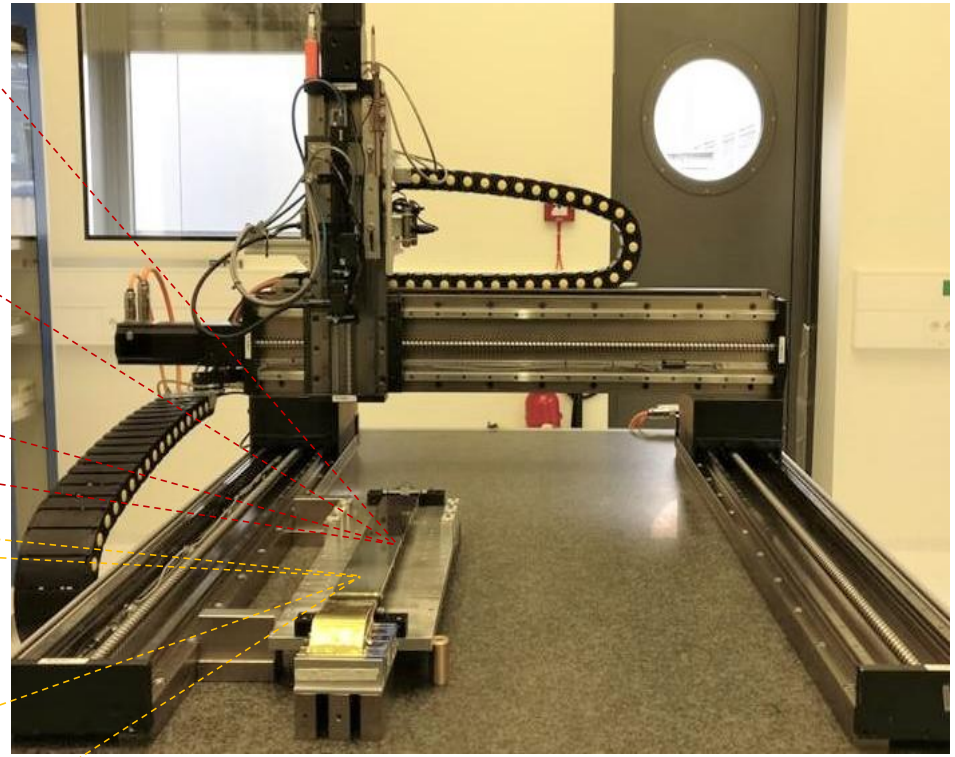
Setup to evaluate ladder assembly based on optical inspection of the sensor surface with precision better than 10 µm

- XY based on pattern recognition
- Z (high) based on focus variation

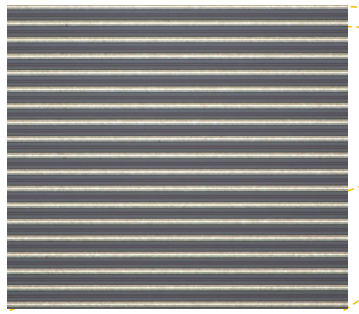


marker on the sensor

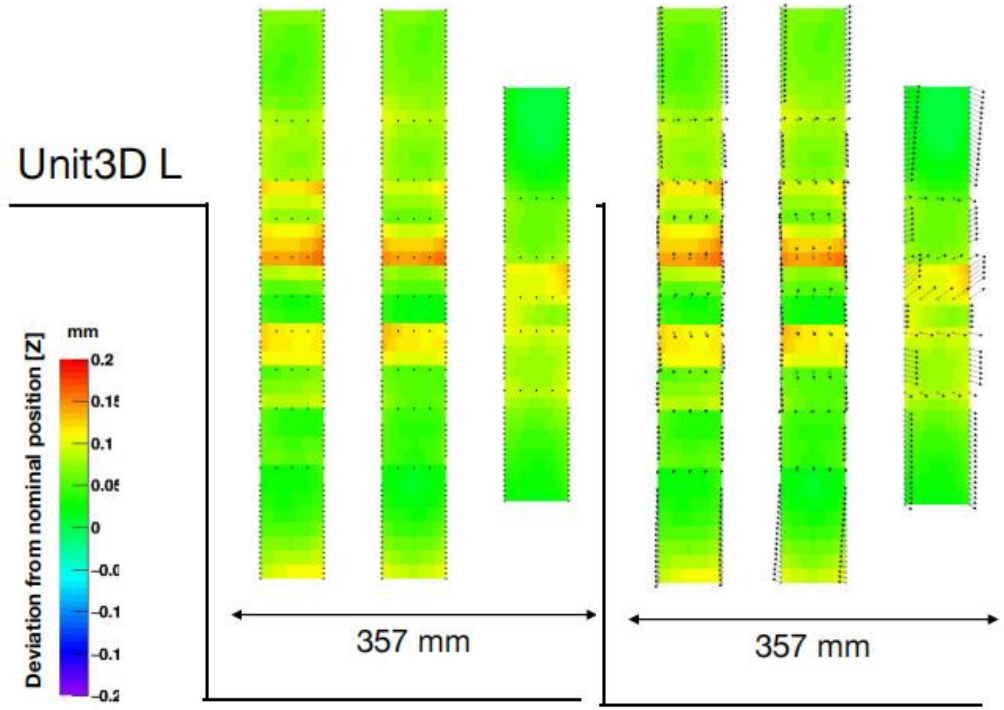




Optical inspection setup



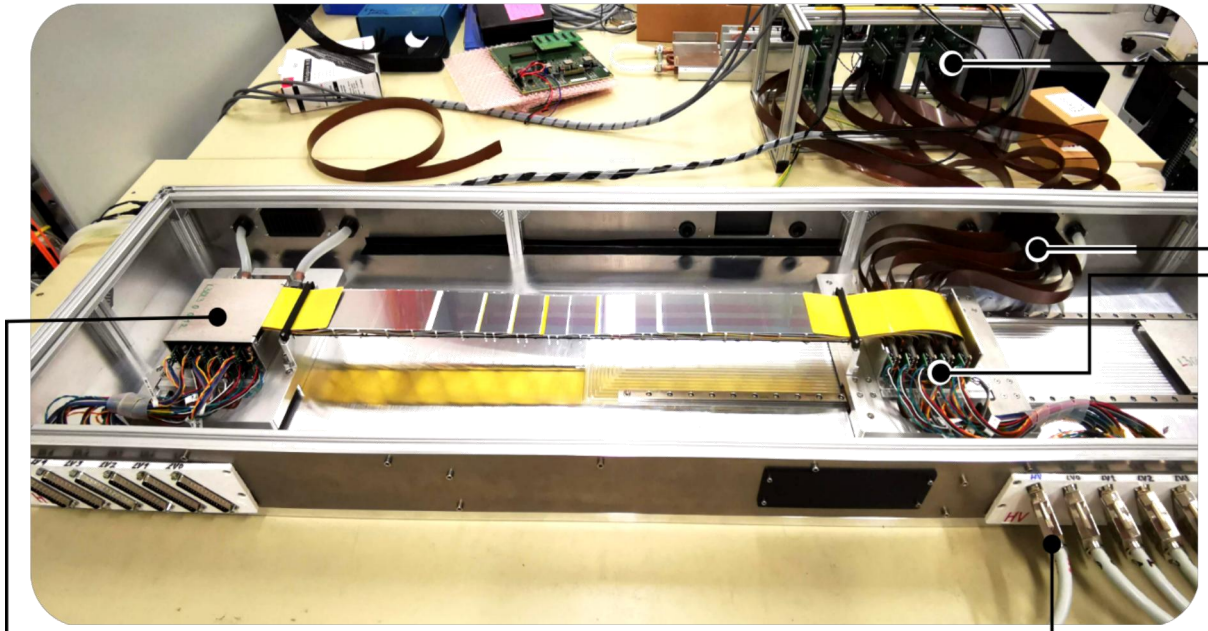
strips on the sensor

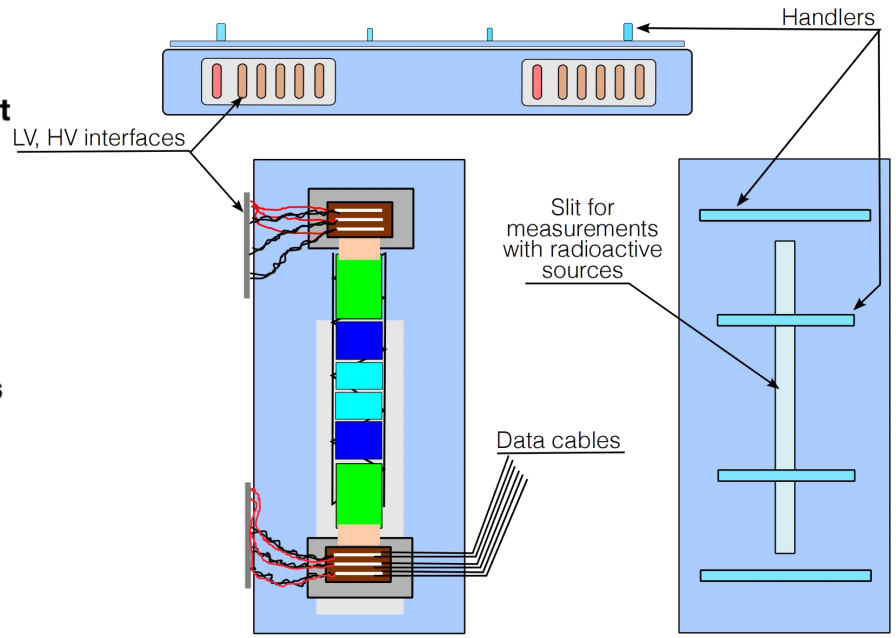


XY deviations enhanced factor 100

Optical inspection confirmed the precise mounting of sensors, meeting the STS requirement of ~100 µm accuracy

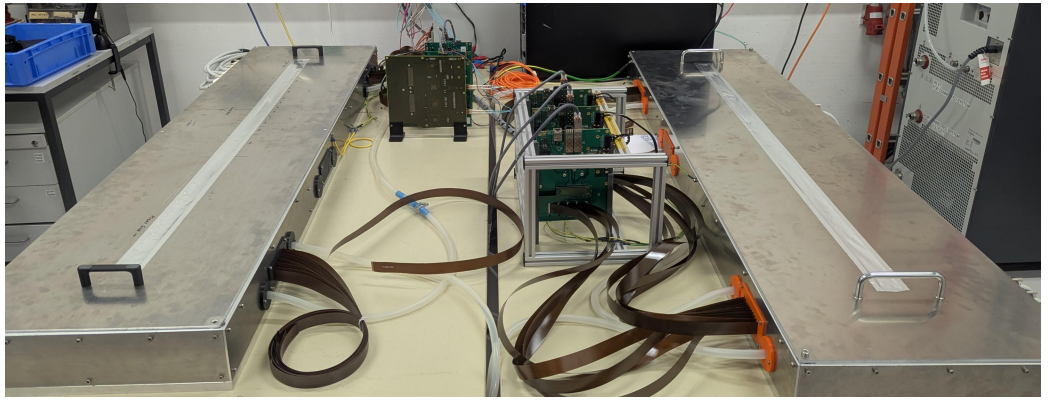
LADDER TESTING SETUPS





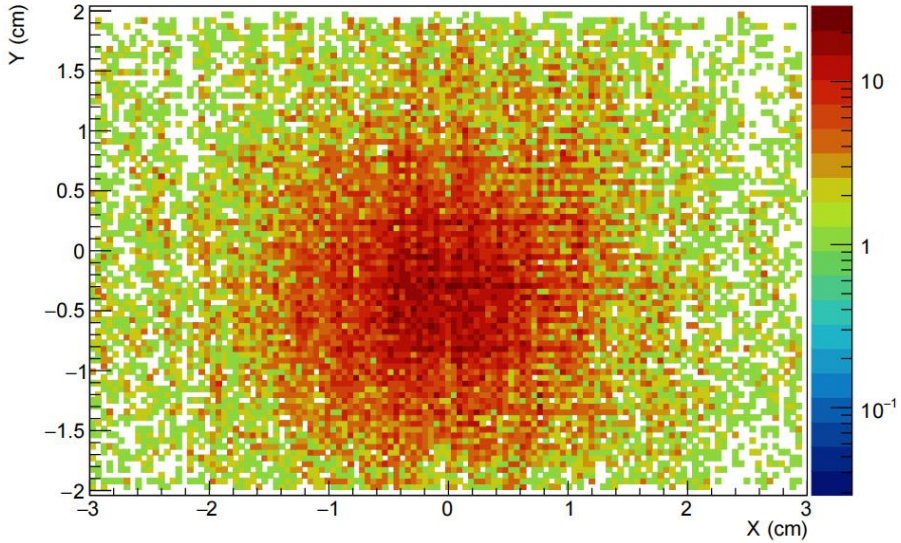
Schematic view of the Ladder test box

- Modular design that can accomodate all ladder types
- All interfaces for operation (LV, HV, data readout, cooling)
- Light tight, EMI protection
- Slit for measurements with radioactive sources
- Two testing stations are used to streamline ladder testing



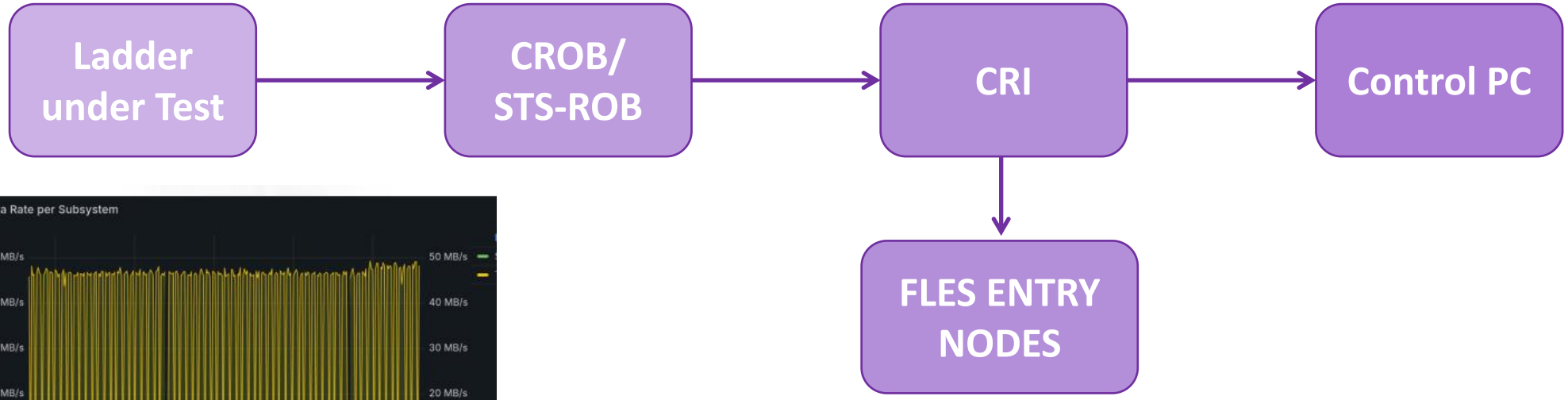
LADDER TESTING SETUPS: READOUT CHAIN

Existing readout chain



^{90}Sr/Y source spot measured with a module of ladder L3DL100112. Channel artefacts linked to the limited readout bandwidth.

New & Final Test readout chain



- Multi-Source real-time monitoring
- Same monitoring functionalities as in mCBM

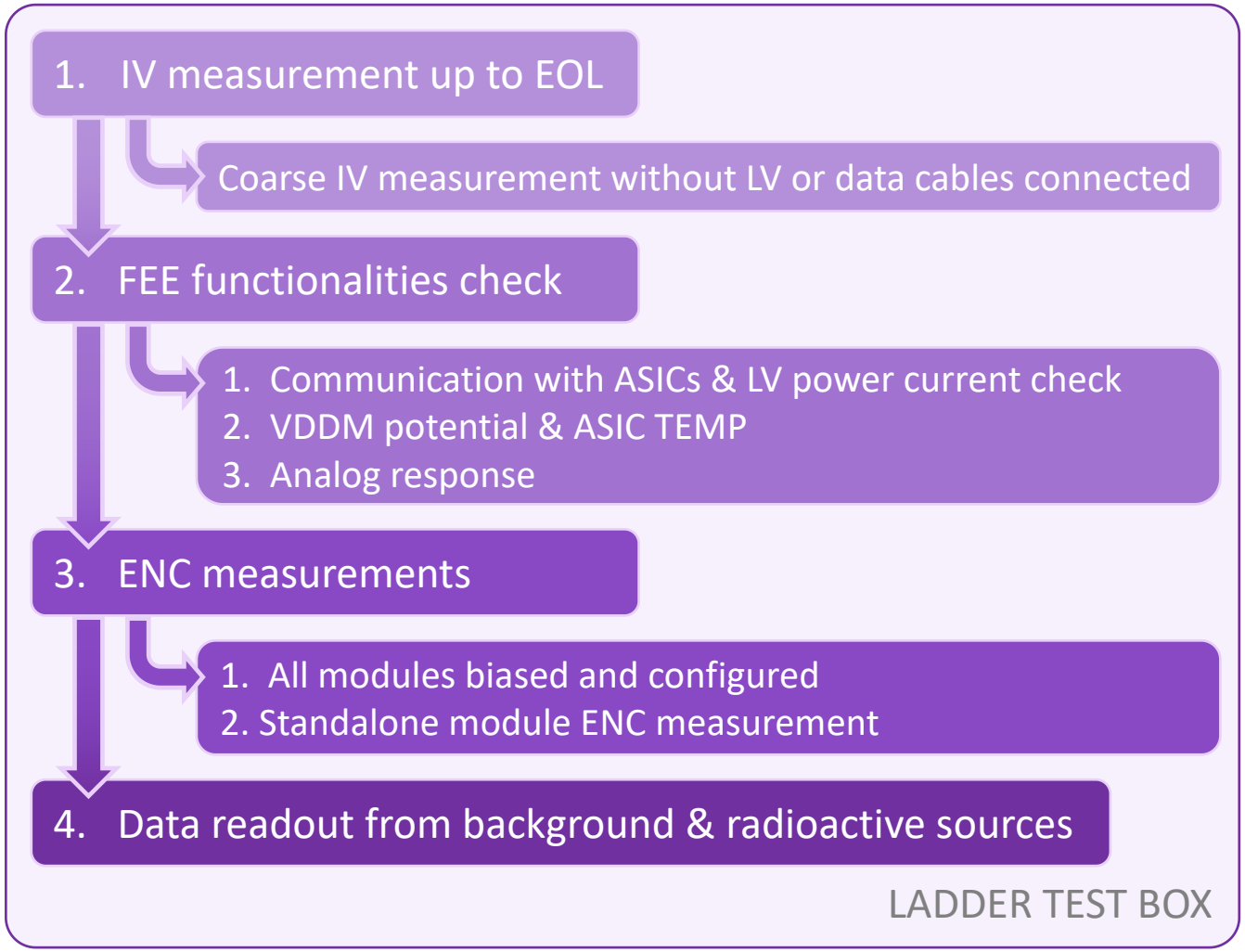
TESTING PROTOCOL

Two main points to address with the assembly and testing of ladders:

- Quality of the assembled laddders
- Functional performance of the modules on the ladders

Simplified protocol for ladder testing:

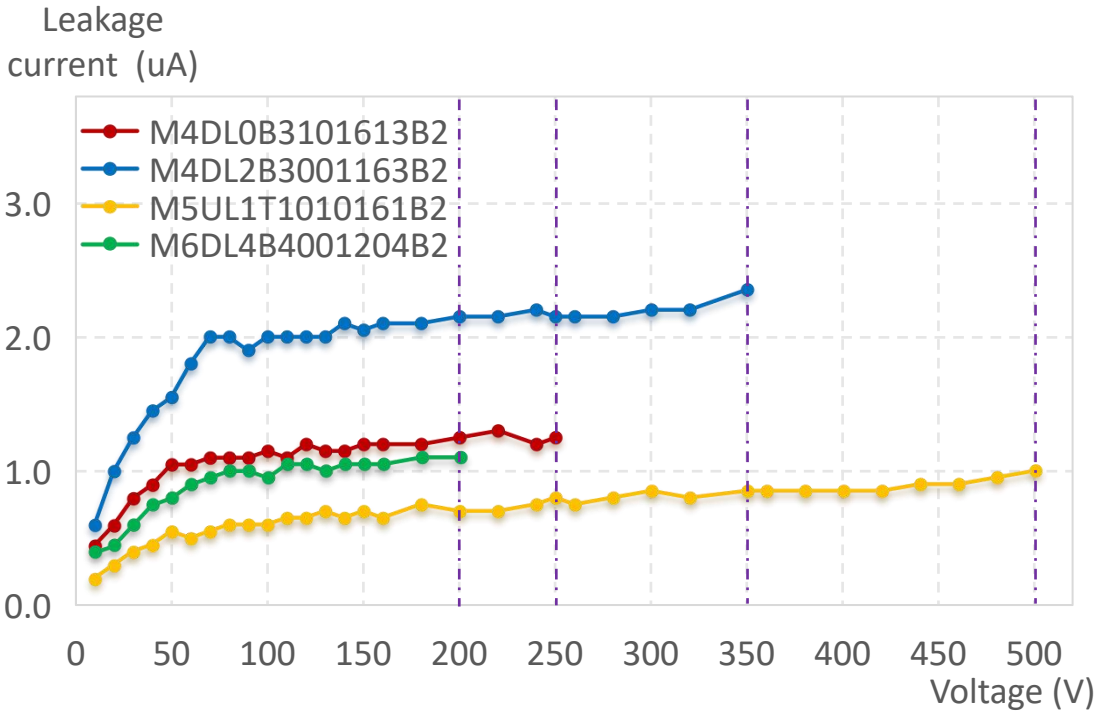
- Derived mostly from the gained experience with module testing.
- For the first-of-series ladders, other tests were also included to study in more detail noise levels and signal response

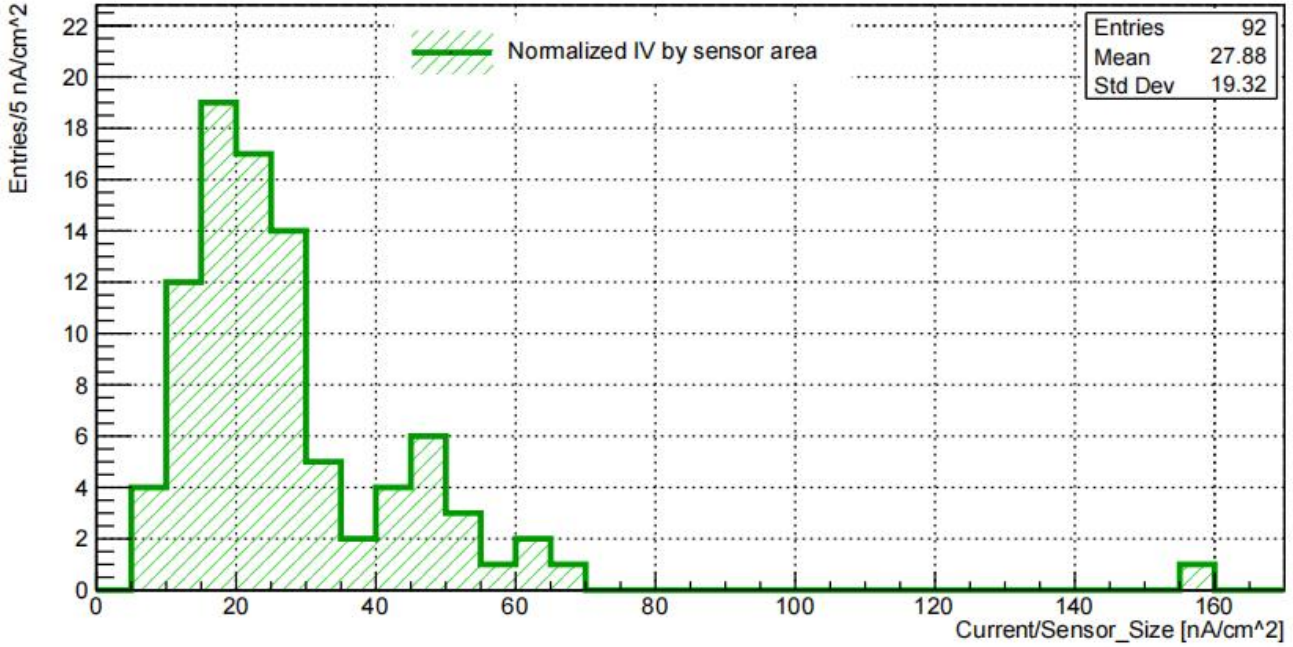


OVERALL RESULTS: IV

IV measurement with low resolution ($0.1\mu A$) HV power supply and LV cables unconnected:

- Up to projected End-of-Life (EOL) based on sensor grade [**A** (500 V), **B** (350 V), **C** (250 V), **D** (200 V)]



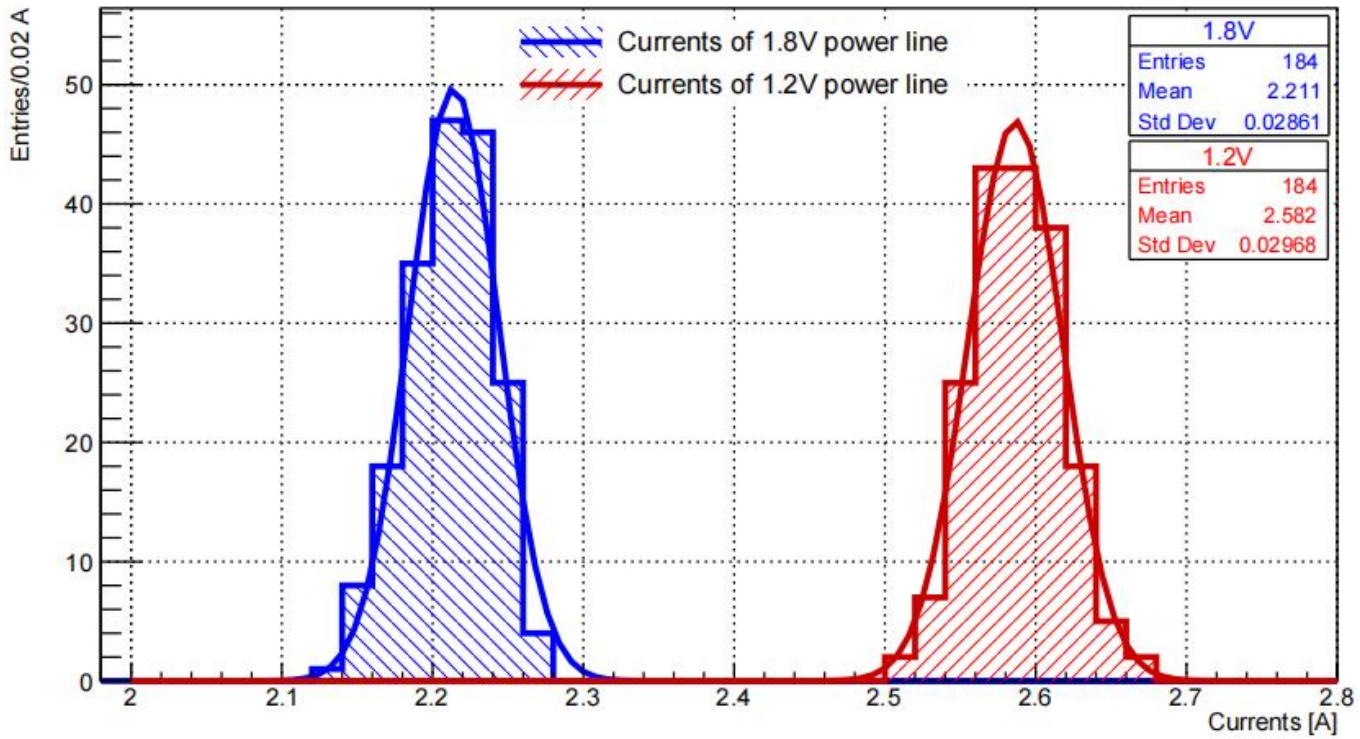


Sensor current measured at 150 V during IV measurements. The values are normalized by sensor area.

FINDINGS: All sensors from the tested ladders can be biased up to the voltage required at EOL

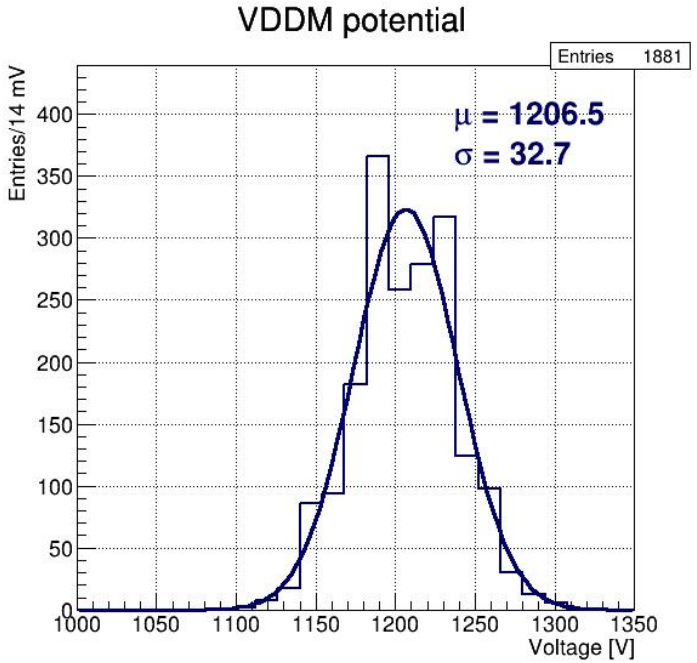
OVERALL RESULTS: FEE FUNCTIONAL TEST

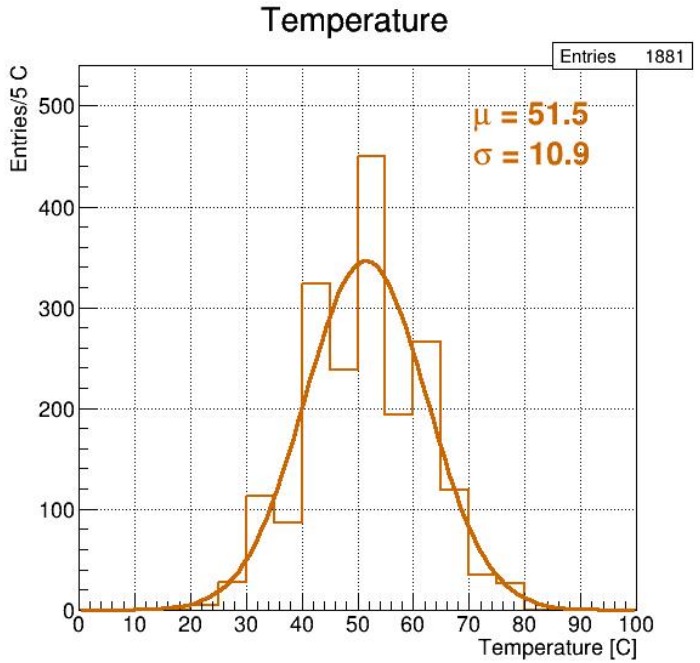
Functional test for all modules on ladders:	
Communication w/ ASICs	1888/1888
Register W/R	☑
LV power current check	2.58 A (1.2 V)/ 2.21 A (1.8 V)
Analog front-end issues	4/1888

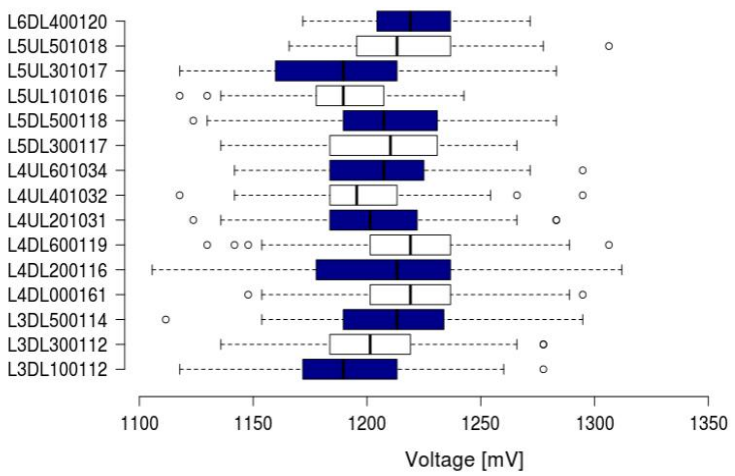


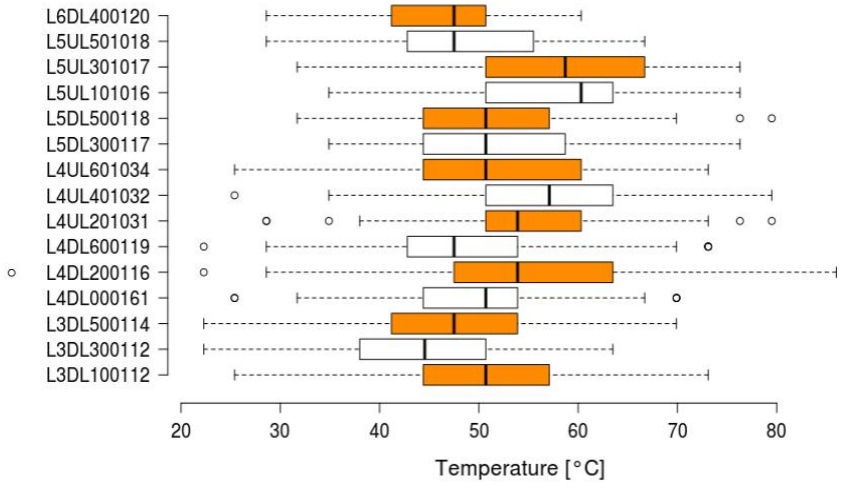
Current consumption measured for the two main power domains of the Front-End Electronics during testing. The red histogram represents the current distribution of the 1.2 V analog power domain, while the blue histogram shows the currents of the 1.8V power line, which combines the analog and digital domains.

OVERALL RESULTS: FEE FUNCTIONAL TEST



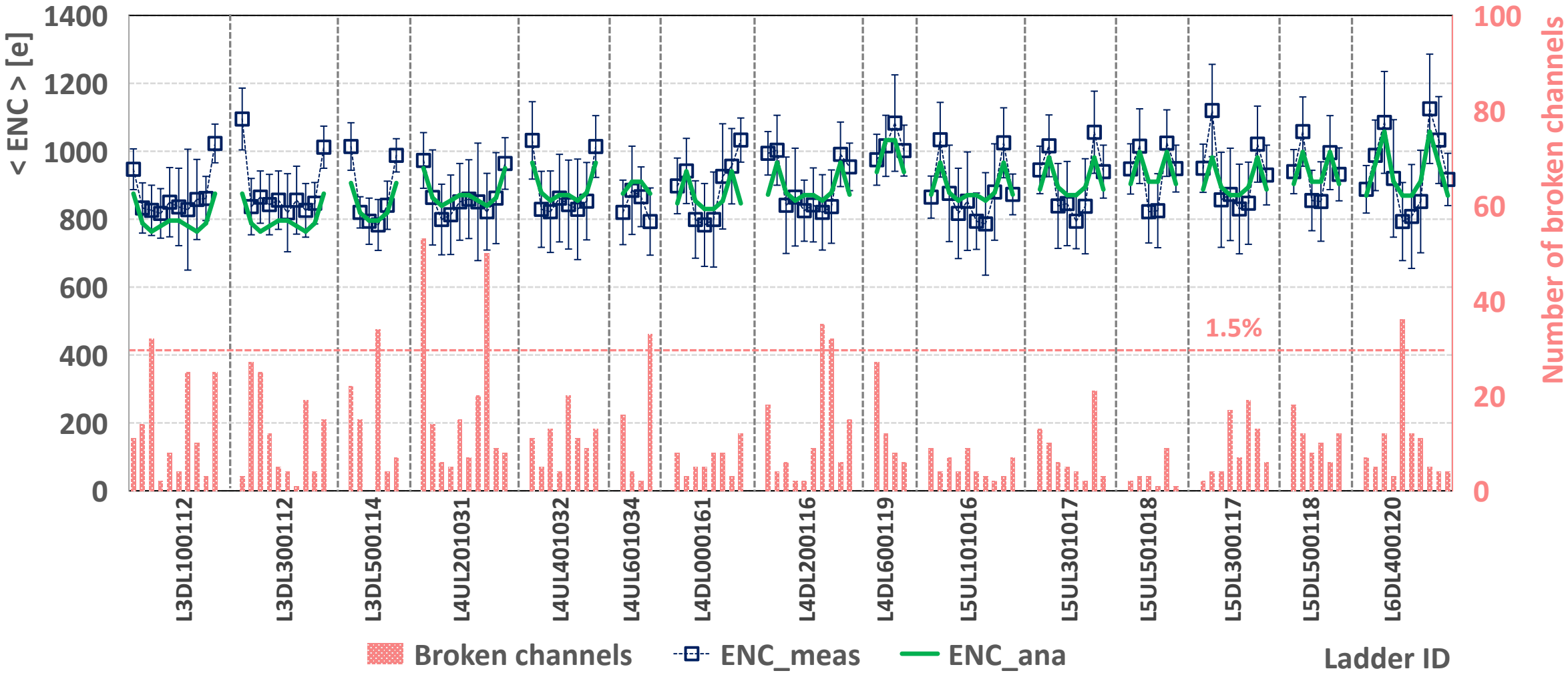






Distributions of ASIC operating potential (VDDM) and ASIC temperatures (TEMP) measured for all modules in ladders.

OVERALL RESULTS: ENC CHARACTERIZATION



Noise values measured for each N-side module mounted on a ladder. All modules were biased at 150 V and fully configured. The average noise behavior is consistent with the ENC parametrisation based on the overall capacitance. Number of broken channels within the guiding lines of STS.

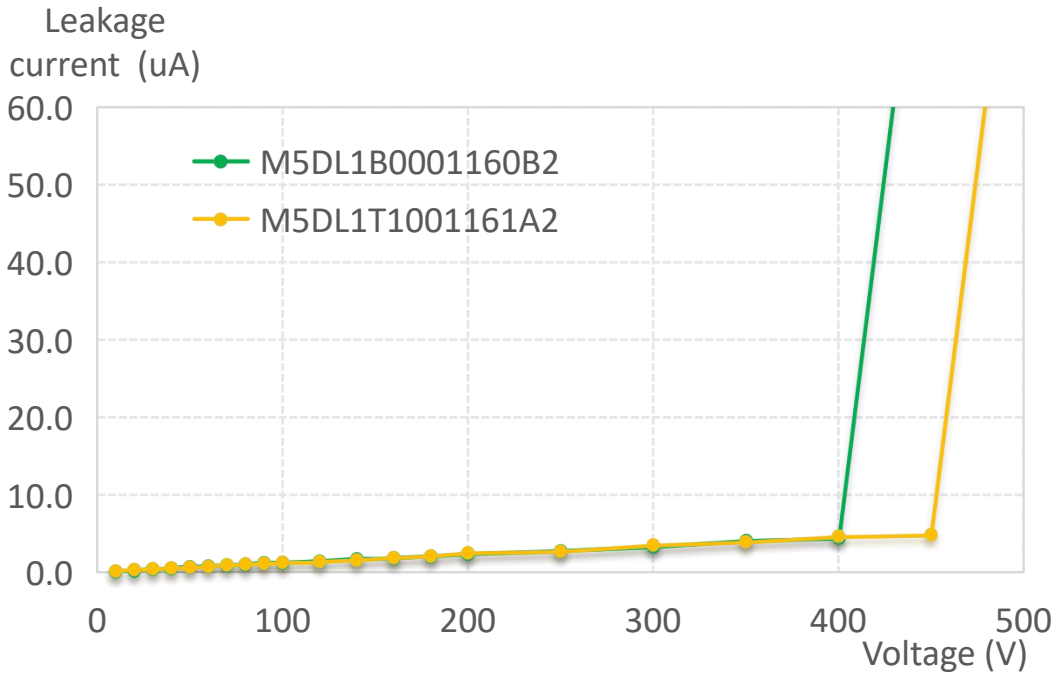
There's a lady who's sure all that glitters is gold 

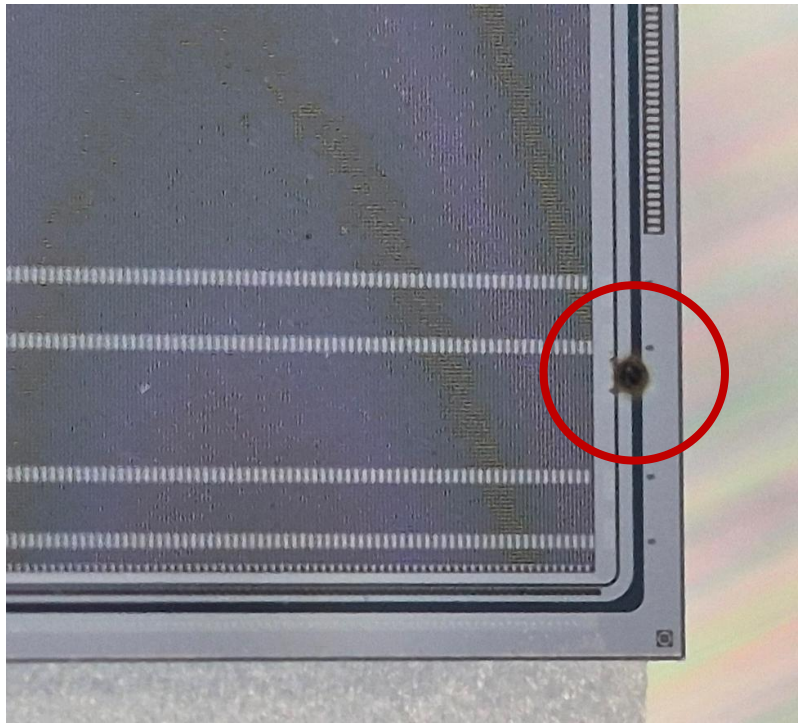
ENCOUNTERED ISSUES & SOLUTIONS

ENCOUNTERED ISSUES & SOLUTIONS

L5DL100116:

- All modules were biased at the same time to measure the IV
- LV and data cables were connected





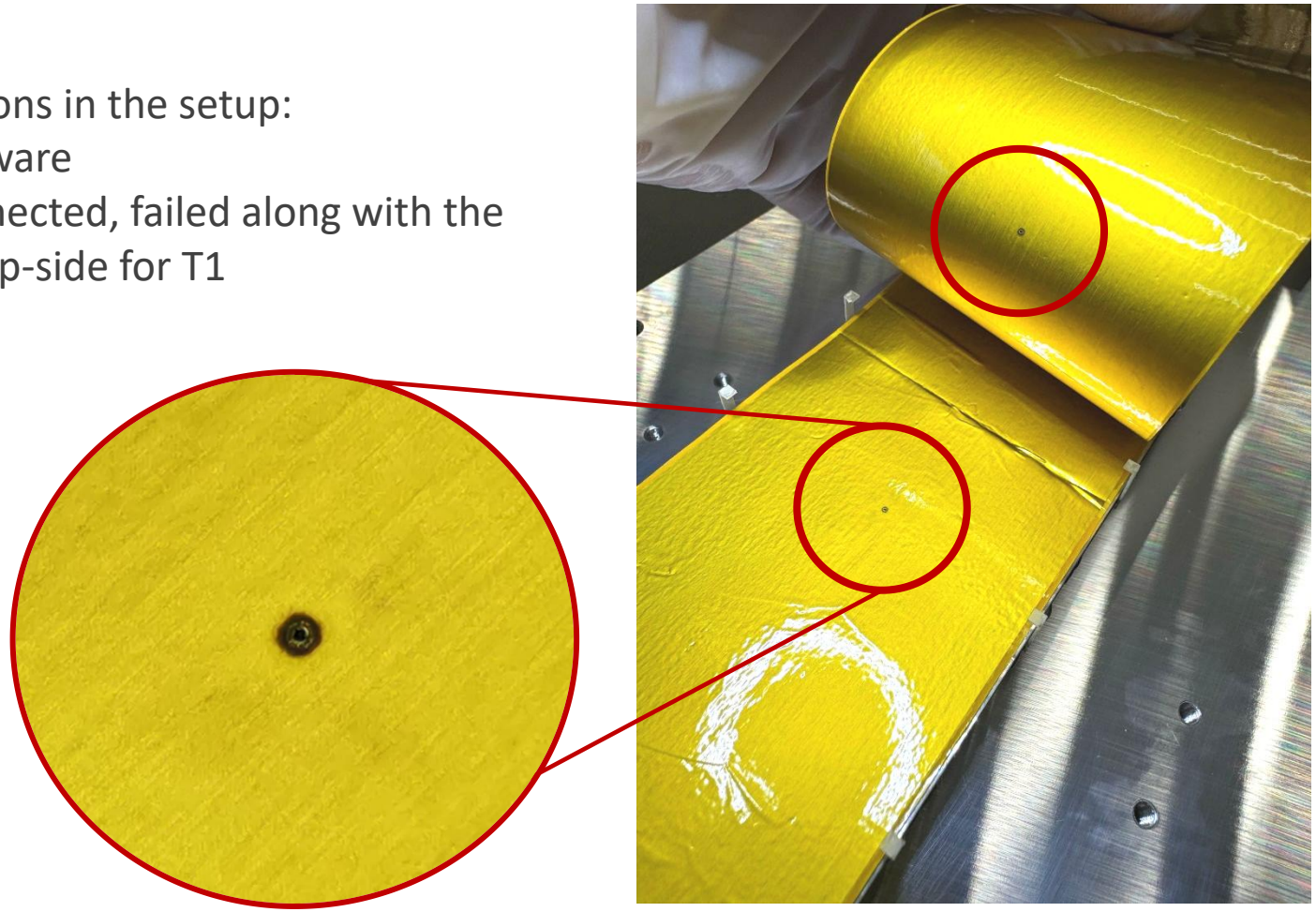
Discharge onto HV-ring of B0 sensor

ENCOUNTERED ISSUES & SOLUTIONS

L5DL100116:

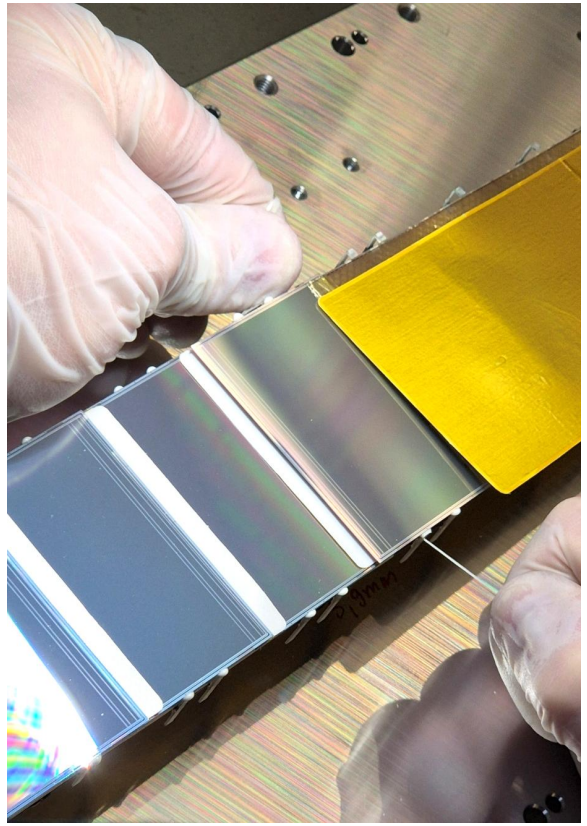
The T1 breakdown triggered multiple malfunctions in the setup:

- The LV PS lost communication with the software
- The EMU board, where T0 and T1 were connected, failed along with the uplink_1 driver on the n-side for T0 and the p-side for T1



RESULT: Three non-functional modules

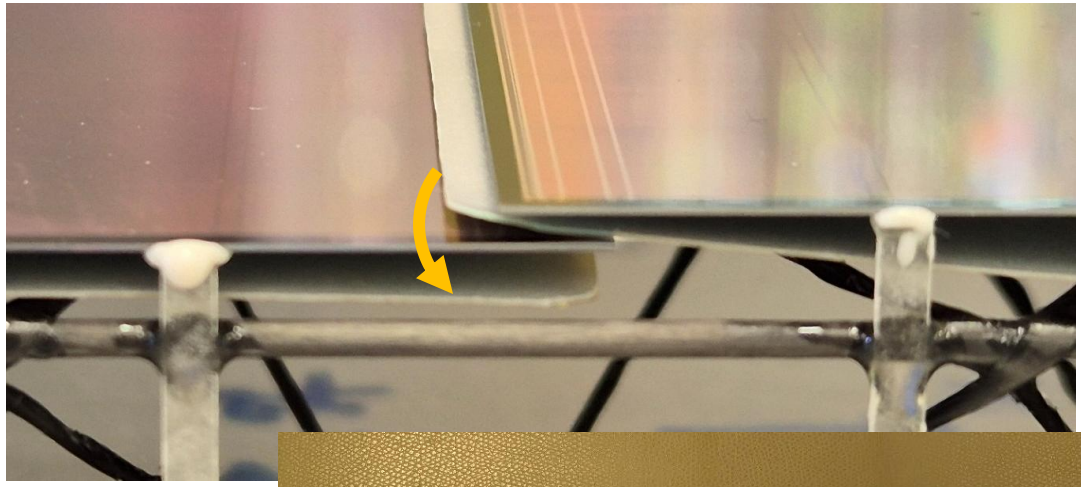
ENCOUNTERED ISSUES & SOLUTIONS



The three non-functional modules:
A procedure was elaborated to dismount modules from an assembled ladder without compromizing function → **This makes everything less monolithic**

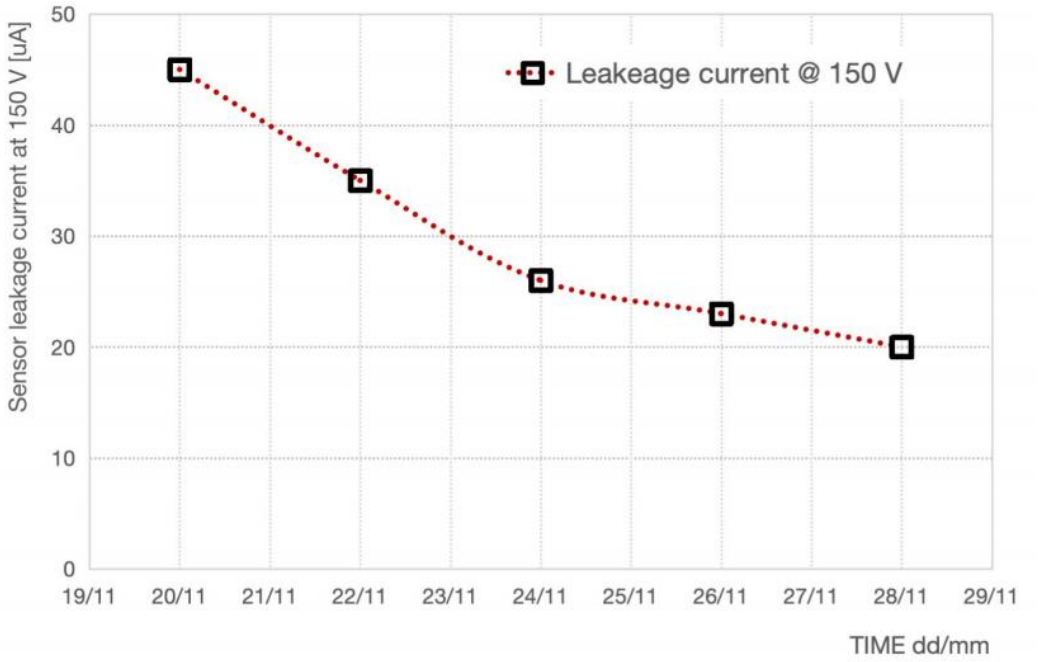
L5DL100116: Solutions

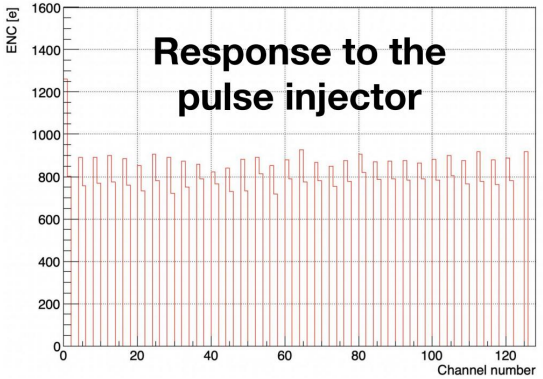
- An extra isolation layer of 7.5 um Polyimide (Kapton) was added to each shileding of modules with grade A (500 V)
- Modifications in the IV measurement procedure: LV and data cables are not connected when measuring IV



ENCOUNTERED ISSUES & SOLUTIONS

A module with a high sensor leakage current may indicate humidity or some form of charge-up.
Solution: Biasing the sensor for several hours, which will allow the leakage current to relax over time.



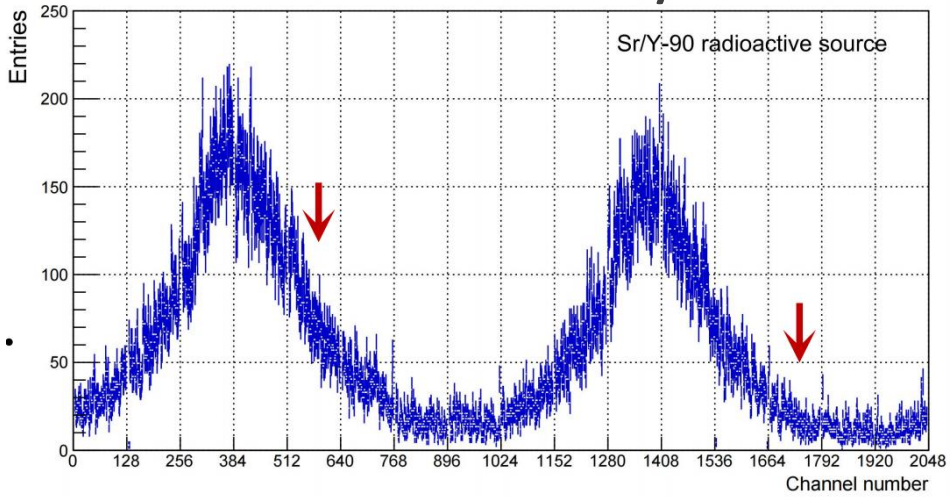


ASIC with problematic analog responses to injected pulses

How to know is not a problematic ASIC?

- Monitoring the noise events in the counter indicates that the AFE of all channels was functioning properly.
- The analog functionalities on the ASICs were verified using ^{90}Sr/Y measurements.

Measurements with ^{90}Sr/Y source

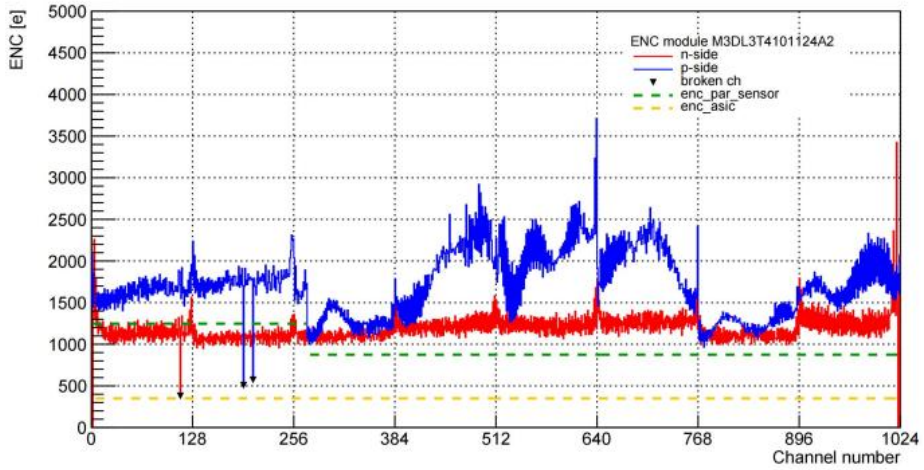


ENCOUNTERED ISSUES & SOLUTIONS

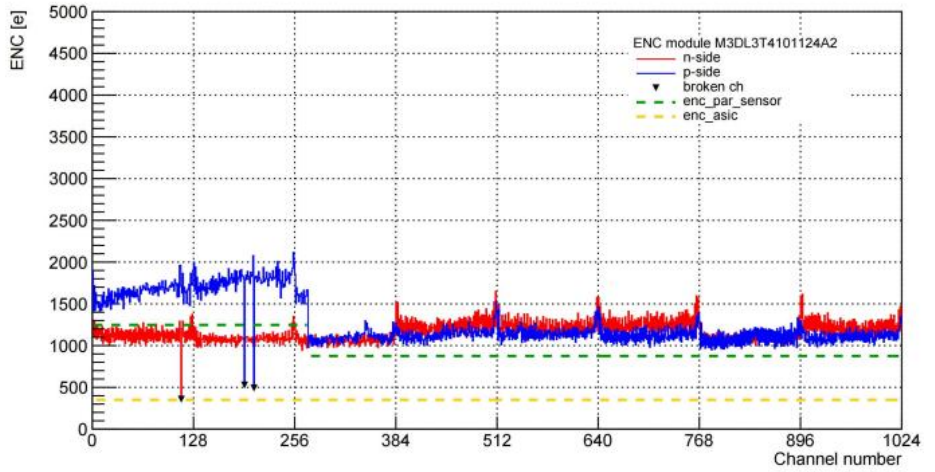
Noise Pattern Characteristics:

- Identified during Ladder Testing
- Also observed in standalone modules
- Up-to-date it has been observed ONLY in p-side.
- Mostly visible in 12 cm sensor modules
- Pattern changes after re-arrengement of the shielding -> (change in C).
- The pattern can be present in all ASICs of p-side.
- Within one ASIC, the pattern has a smooth behaviour (no jumps)
- It is reversible

PATTERN



NO PATTERN



Summary of the measurments and knowledge regarding this issue can be found:

- ENC pattern studies summary on Miro
- STS_retreat: The ENC pattern question

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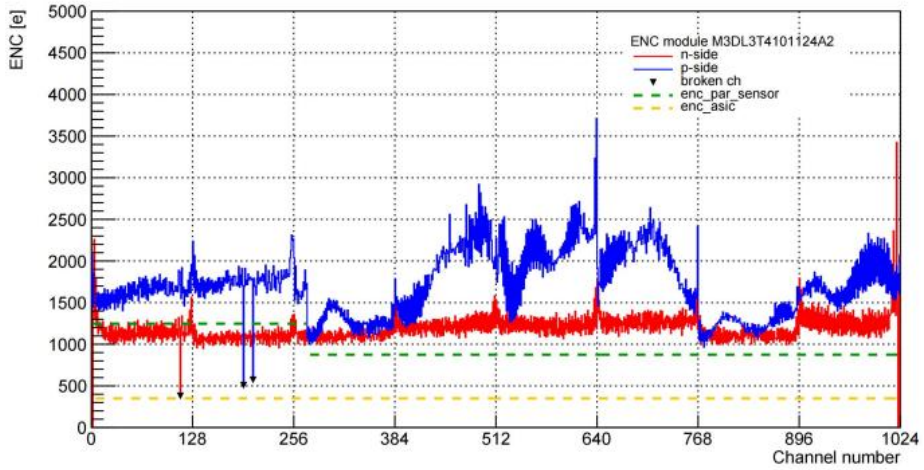
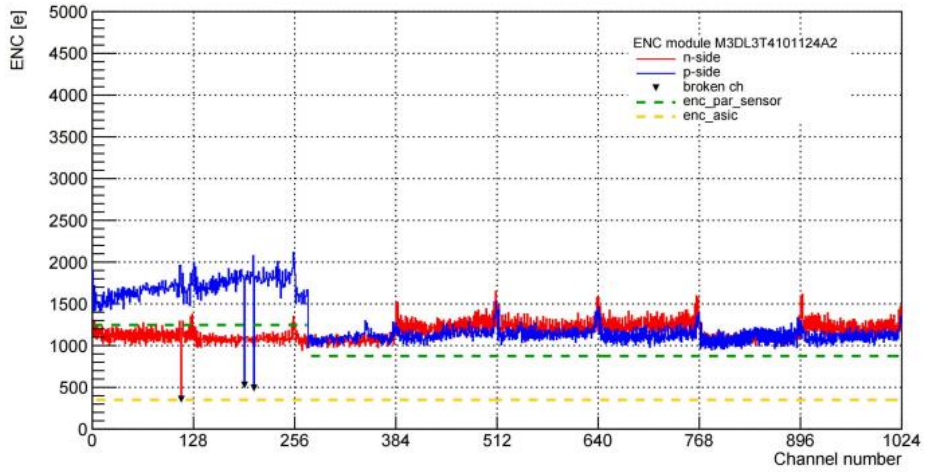
Parameter scan of multiple registers to understand the causes and possible to reduce excess noise:

- Shaping time
- CSA and shaper's current
- Feedback capacitance and resistance
- Power in the 1.8 V LV line
- Different geomtrical arrangement or configurations of microcables, shieldings, clamp and lids....

PATTERN



NO PATTERN



Summary of the measurments and knowledge regarding this issue can be found:

- ENC pattern studies summary on Miro
- STS_retreat: The ENC pattern question

ENCOUNTERED ISSUES & SOLUTIONS

What did we overlooked?

- CSA Buffer and Cascode current **Register: [130,14]**

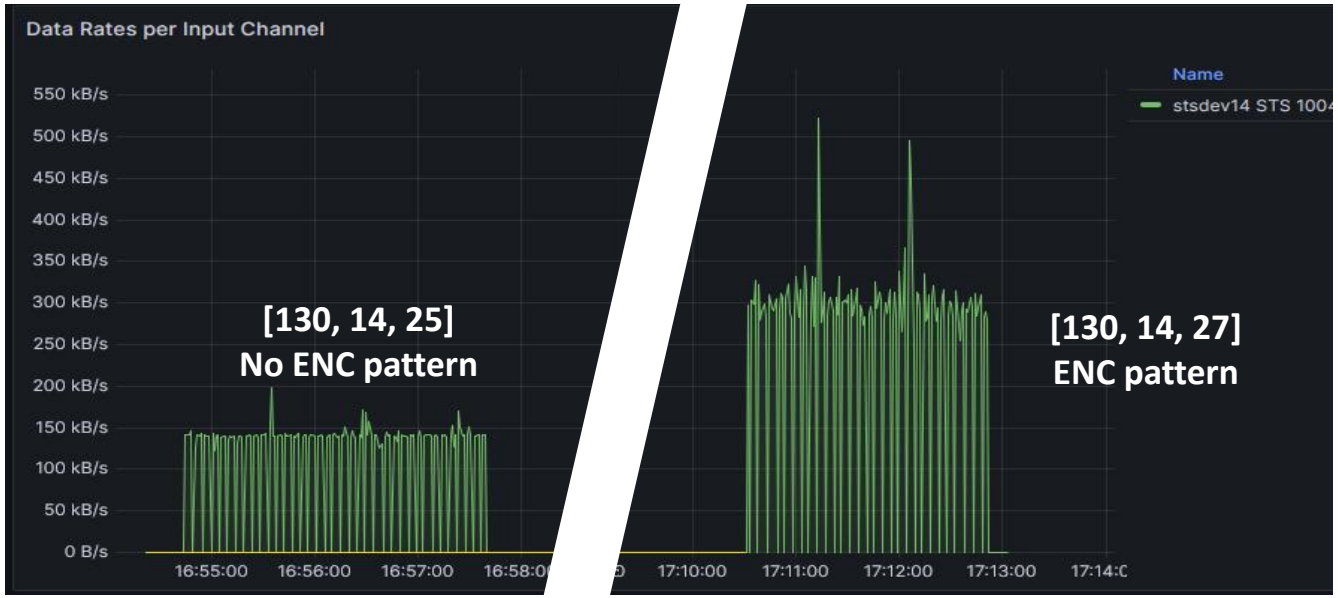
SCAN of the CSA Buffer and Cascode values **Global Register: [130,14] of the SMX_ASIC**

Findings: The **cascode current** plays a fundamental role in suppressing or worsening the ENC pattern.

Large **cascode current** values worsen the ENC levels.

They also induce the first signs of ENC pattern on n-side.

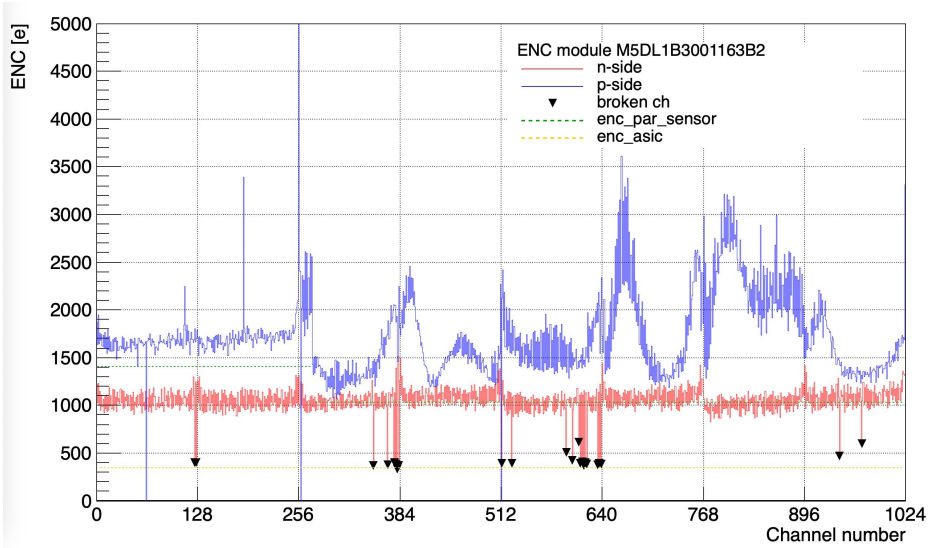
The Buffer cascode contributes very little to the improvement



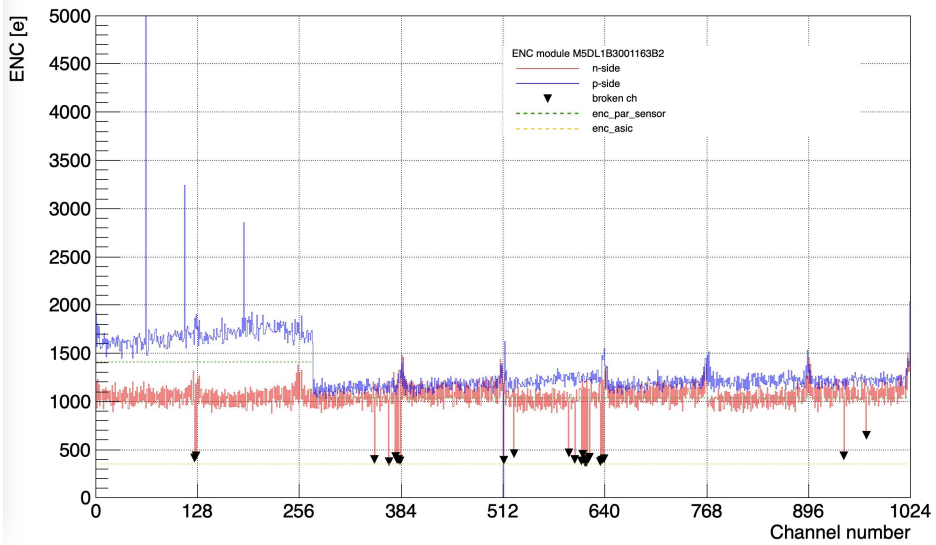
Example of data rates of background measurements at different settings in Grafana. Data rate at high threshold (~10500 e) different settings comparison.

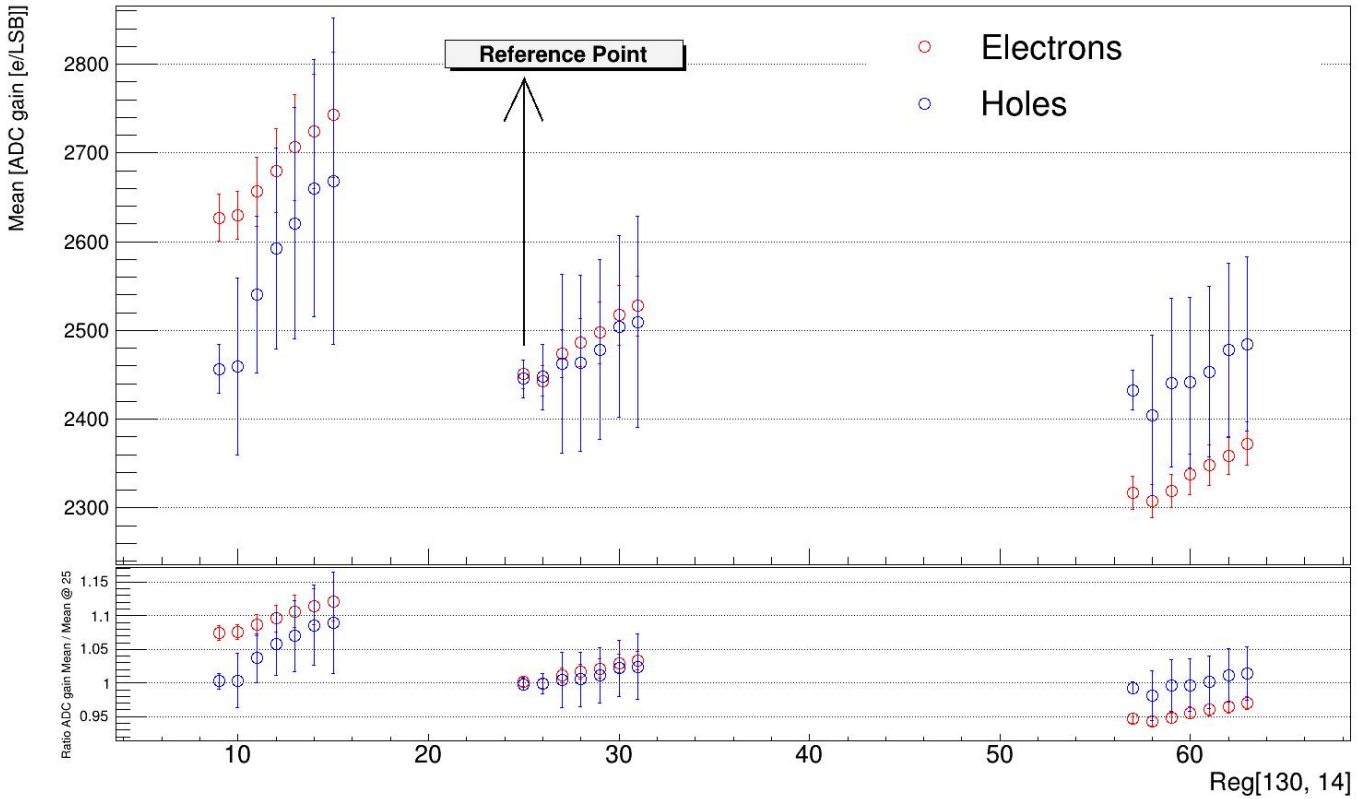
ENCOUNTERED ISSUES & SOLUTIONS

CSA buffer and cascode current = 27 (Default)



CSA buffer and cascode current = 25





Average ADC gain shown for different values of the CSA buffer and cascode current. The former value used was 27 while the new value is 25. The variation of the ADC gain for these two values is minimum.

SUMMARY & OUTLOOK

Ladder assembly and testing are well-established and running procedures from the STS series production:

- All modules have been successfully biased to the projected end-of-life (EOL) specifications.
- Communication has been established with all FEBs, and all ASICs were configured and operated.
- ENC noise levels for all modules, when simultaneously powered and configured, align closely with expectations (~1000 e ENC).
- The number of broken channels complies with the STS guideline, maintaining approximately 1.5% per module.
- Several issues were identified and thoroughly investigated.

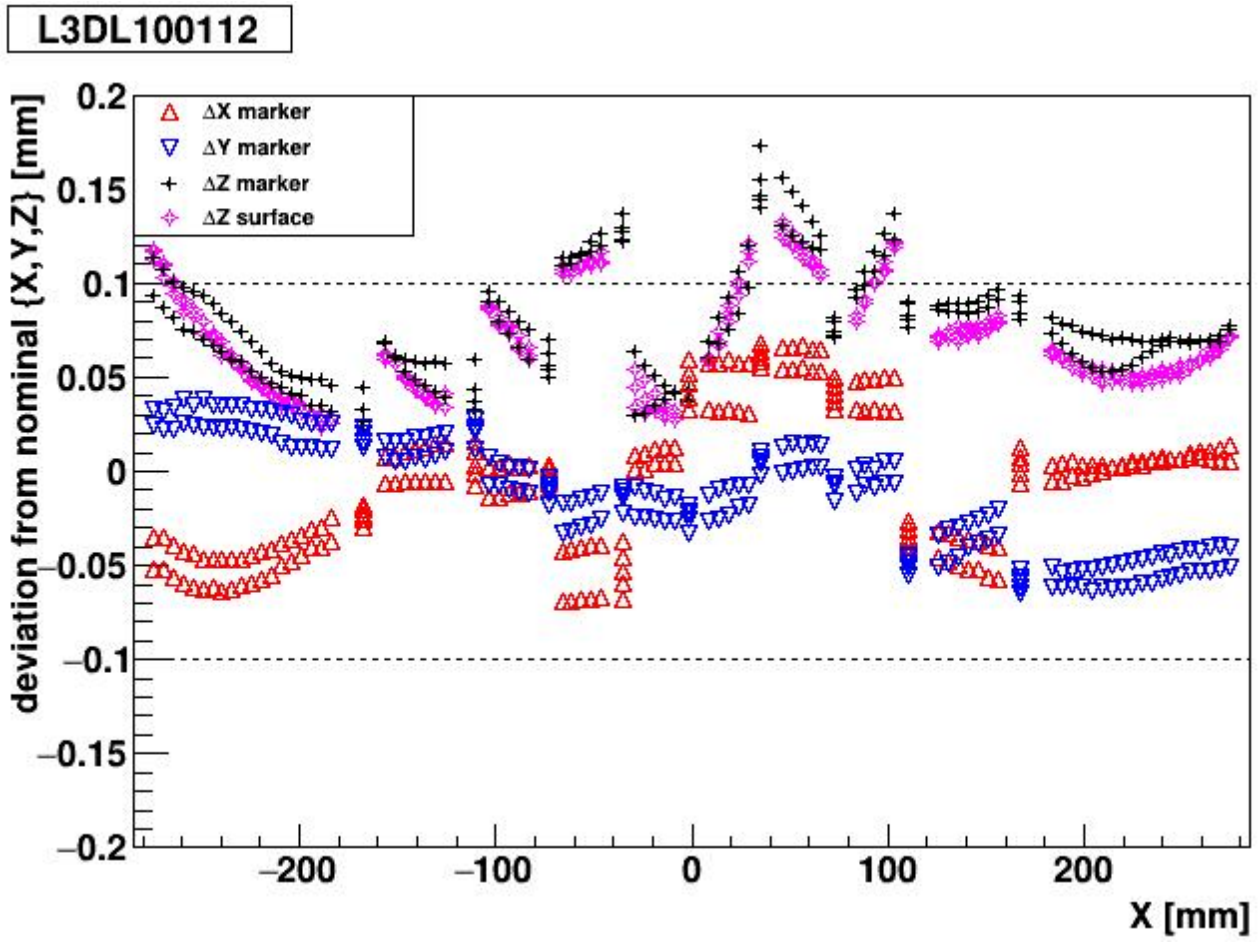
Where do we go?

- CRI Based readout with all the functionalities
- Signal readout to check quantitatively the effect of the cascode current
- Testing the ladders as part of the next integration step "Half-unit". It can be considered as a final test, as the ladders will be mounted in its final position and all final services, LV and HV interfaces, will be in use.

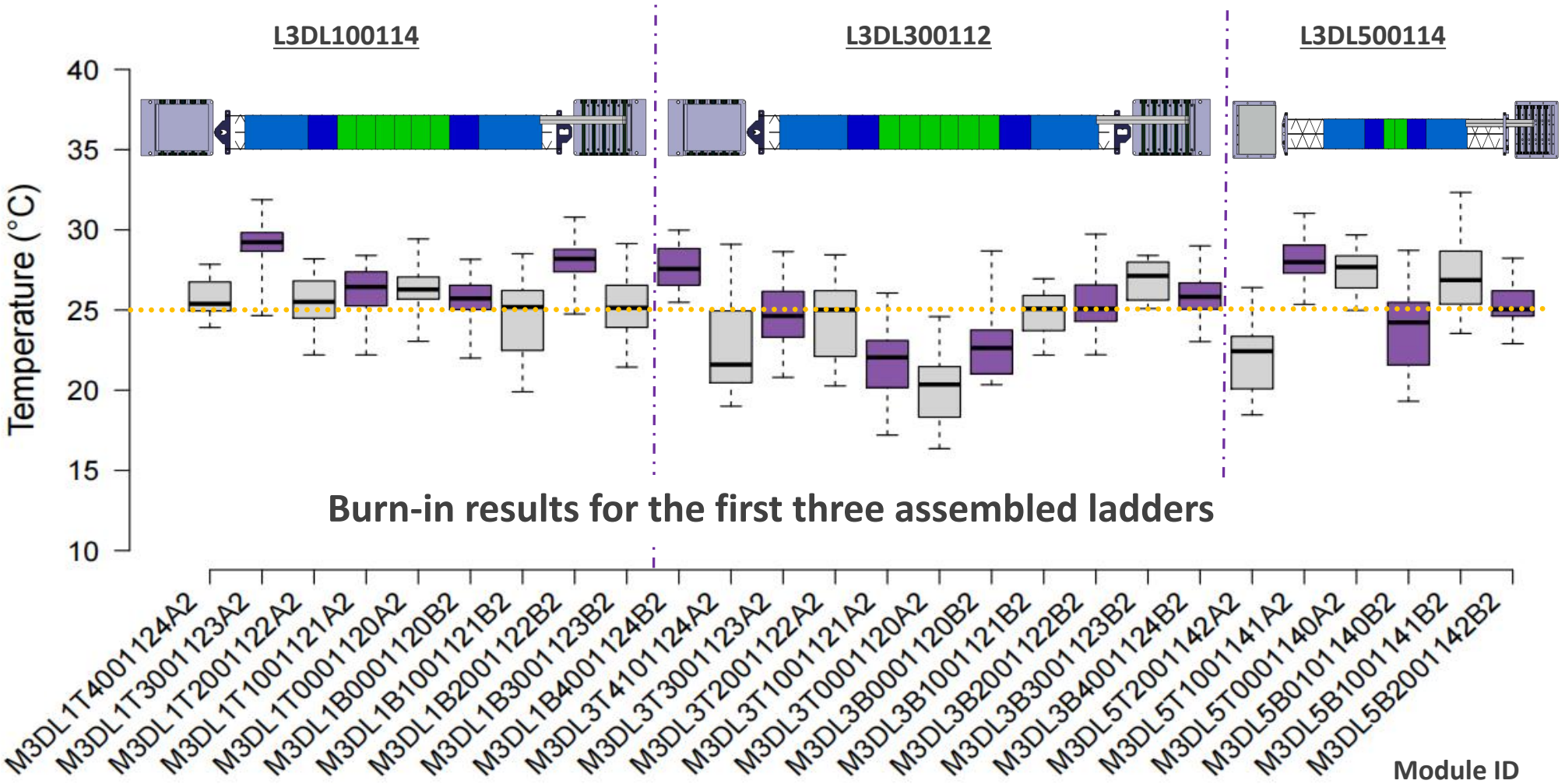
THANK YOU

We’re not buying a **Stairway to Heaven**;
STS is building one, module by module, ladder by ladder.

BACK UP SLIDE

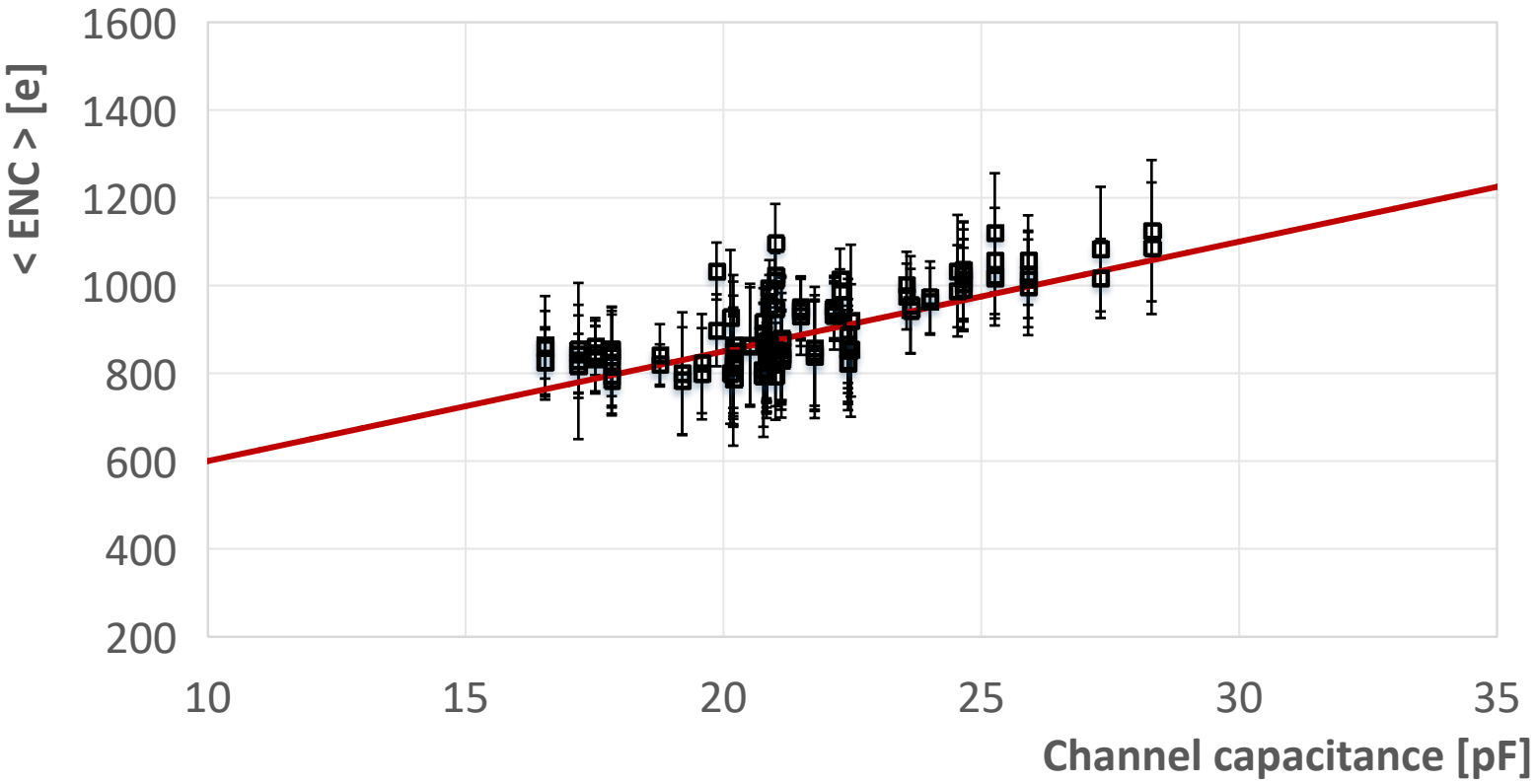


BACK UP SLIDE



Burn-in results for the first three assembled ladders

BACK UP SLIDE



$$ENC = \left[\underbrace{L_{\text{sensor}} \cdot 1.02 \ \frac{\text{pF}}{\text{cm}}}_{\text{sensor}} + \underbrace{L_{\text{cable}} \cdot 0.38 \ \frac{\text{pF}}{\text{cm}}}_{\text{microcable}} \right] \cdot 25 \ \frac{\text{e}}{\text{pF}} + \underbrace{350 \ e}_{\text{ASIC}}$$

Rodríguez, A., Nucl. Instrum. Meth. A 1058 (2024)