# R&D activities on monolithic pixel detectors in TPSCo 65 nm technology

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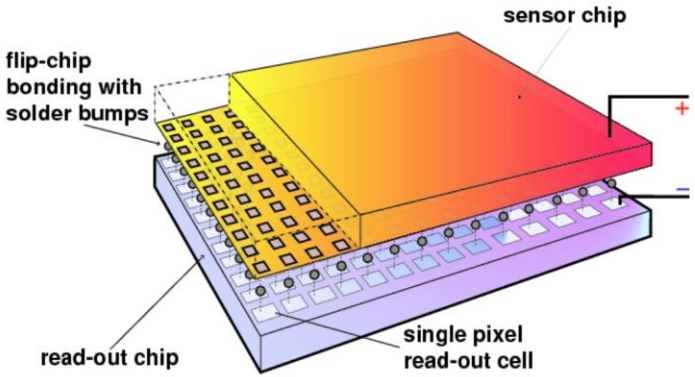
# Overview

1) Introduction
2) TPSCo  65nm ISC technology validation
3) First stitched chips prototypes
4) MOSAIX – full scale, fully functional ALICE ITS3 detector prototype
5) Summary

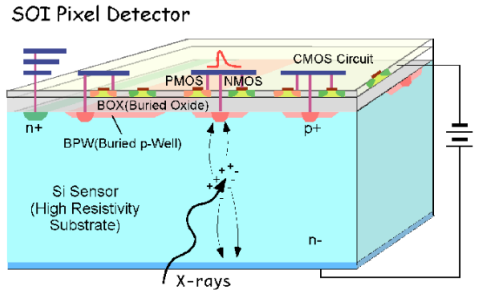
# Pixel detectors classification

## ➢ By fabrication technology:

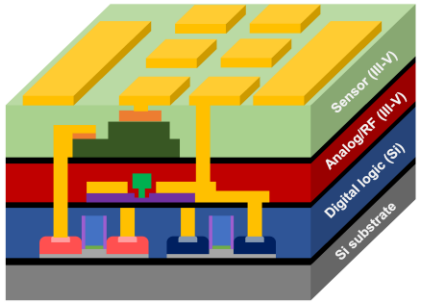
### HYBRID



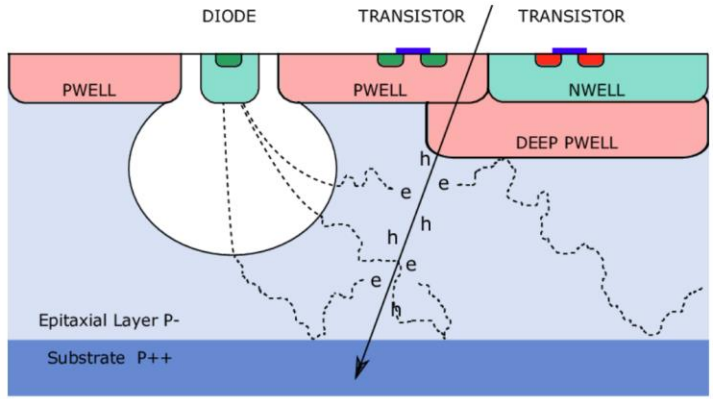

- Sensor and readout produced (optimized) independently
- Most of the currently operating HEP detectors
- Bump-bonding limits the pixel pitch




### 3D-Integration (Wafer stacking, TSV …)




### MONOLITHIC




- Sensor and readout fabricated together
- Lower costs
- Pixel size driven by the in-pixel inteligence
- Lower material budget

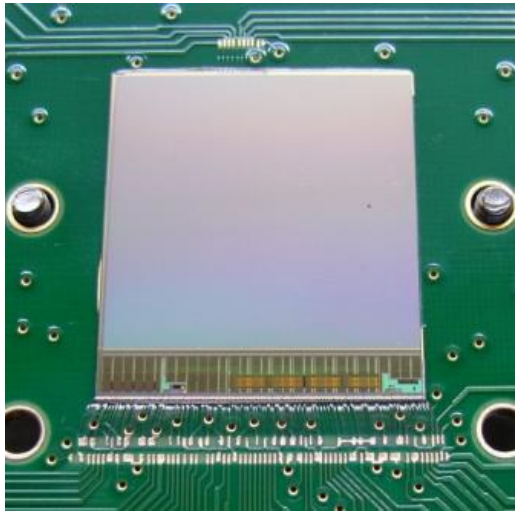
## ➢ By readout architecture:

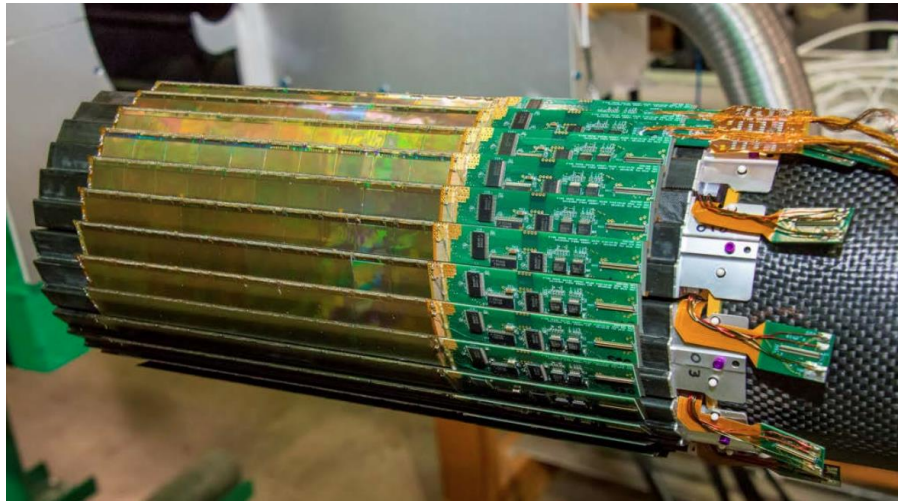
- Event readout --> HEP
- Integrating --> imaging
- Counting --> X-ray imaging

# Monolithic detectors in HEP experiments

➢ **Star PXL detector (MIMOSA28)**

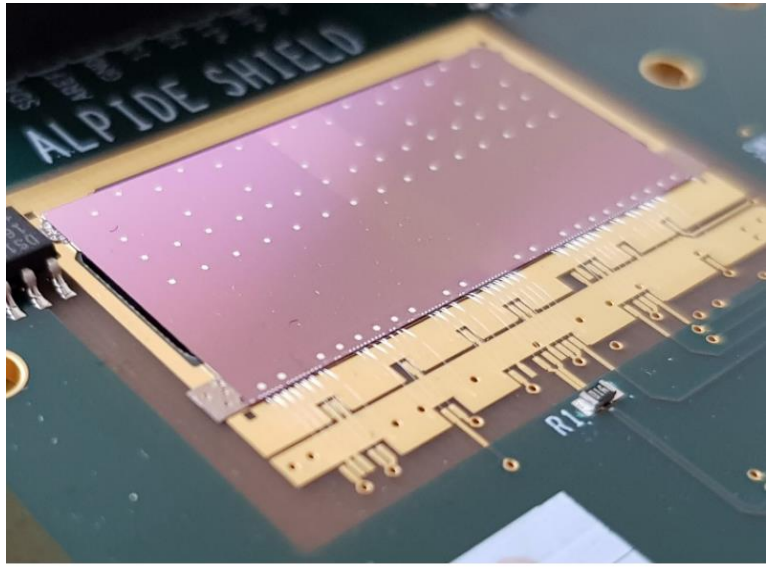
- **Running from 2014**
- Twin well 0.35 µm CMOS (AMS)
- 18.4 µm pitch
- 576x1152 pixels,
- 20.2 x 22.7 mm2
- Rolling shutter readout

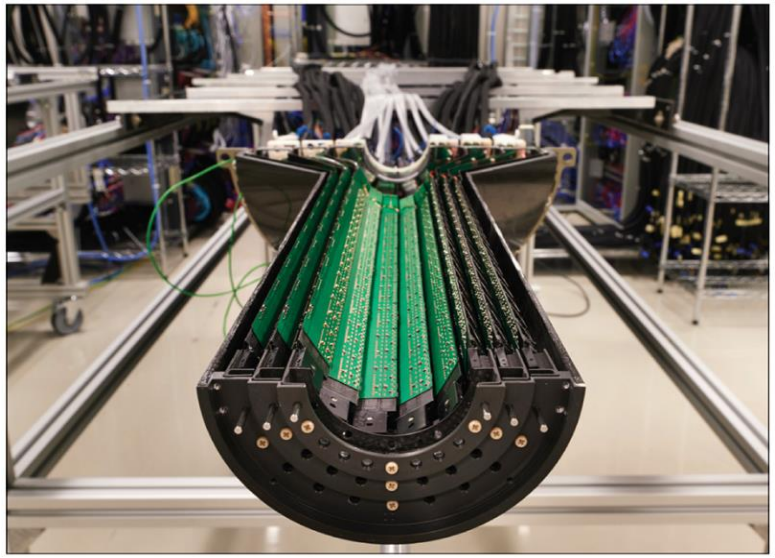




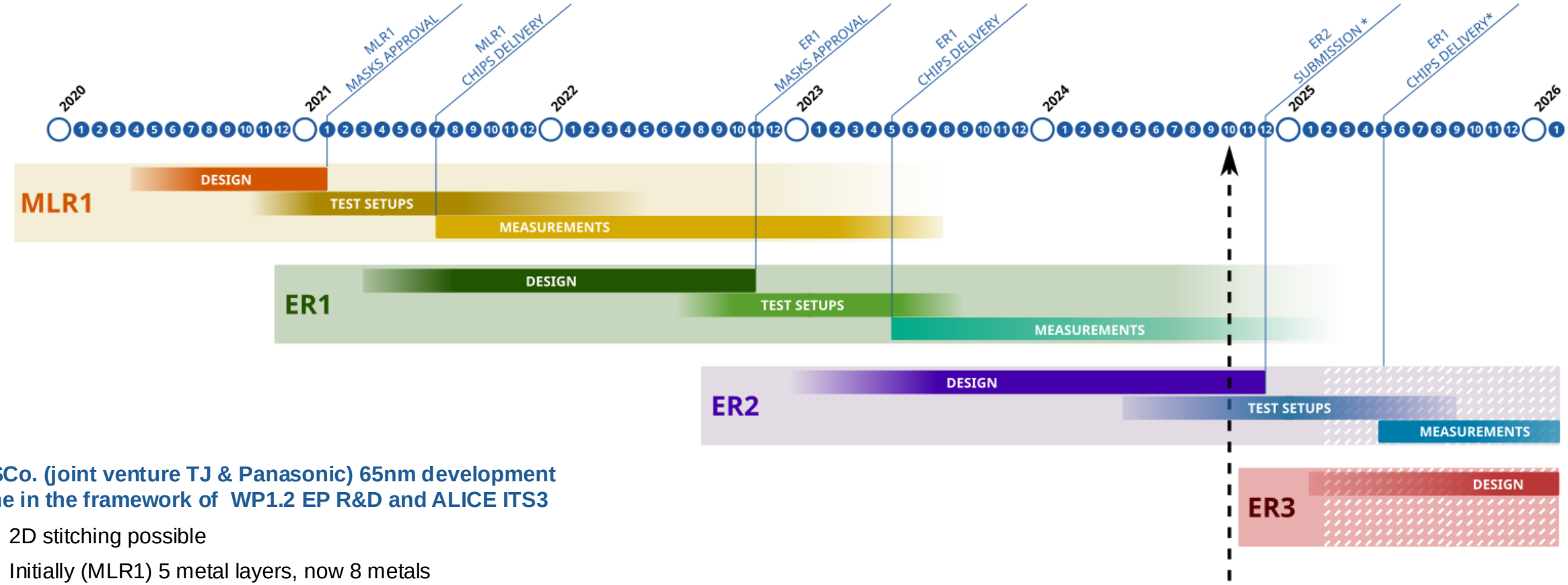
➢ **ALICE ITS2 (ALPIDE)**

- **Running from 2020**
- **TowerJazz CMOS 180nm**
- 27 x 29 µm pitch
- 1024 x 512 pixels,
- 30 x 15 mm2
- Zero-suppressed readout



# Towards 65 nm technology




- **TPSCo. (joint venture TJ & Panasonic) 65nm development done in the framework of WP1.2 EP R&D and ALICE ITS3**
  - 2D stitching possible
  - Initially (MLR1) 5 metal layers, now 8 metals

- **Collaborative effort undertaken by many institutes**
  - **BNL / CERN / CPPM / DESY / IPHC / NIKHEF / RAL / Yonsei / INFN / ...**
  - Coordinated by CERN in the spirit of joint development

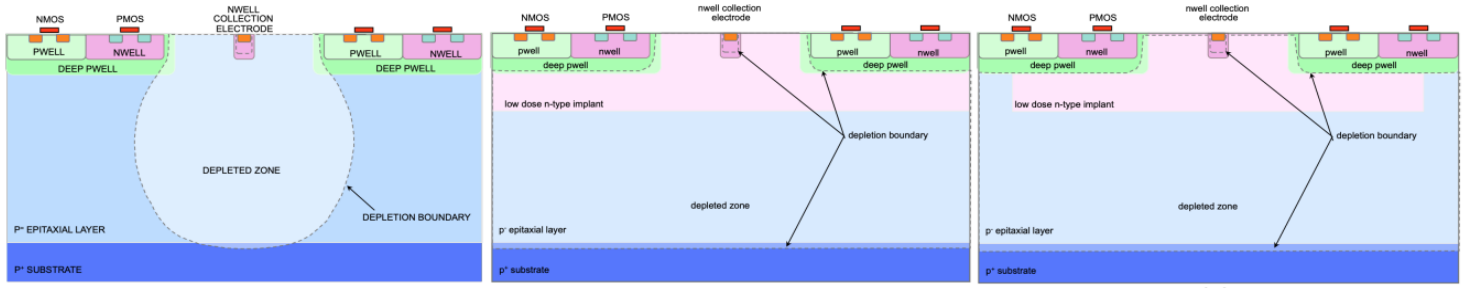
- **Where are we at the moment?**
  - Two submissions taped-out
  - Numerous **(very encouraging!)** measurements results
  - Ongoing activities concentrated around:
    - finising designs for ER2
    - preparing testing infrastructure
  - ER3 – **final sensor for ALICE ITS3** (installation duting LS3)

# First submission (MLR1)

# First submission in TPSCo 65nm (MLR1)

## MLR1 Objectives:

- **Technology validation**
  - transfer 10-year experience from TJ 180nm to 65nm (proces modification: standard / blanket / n-gap)

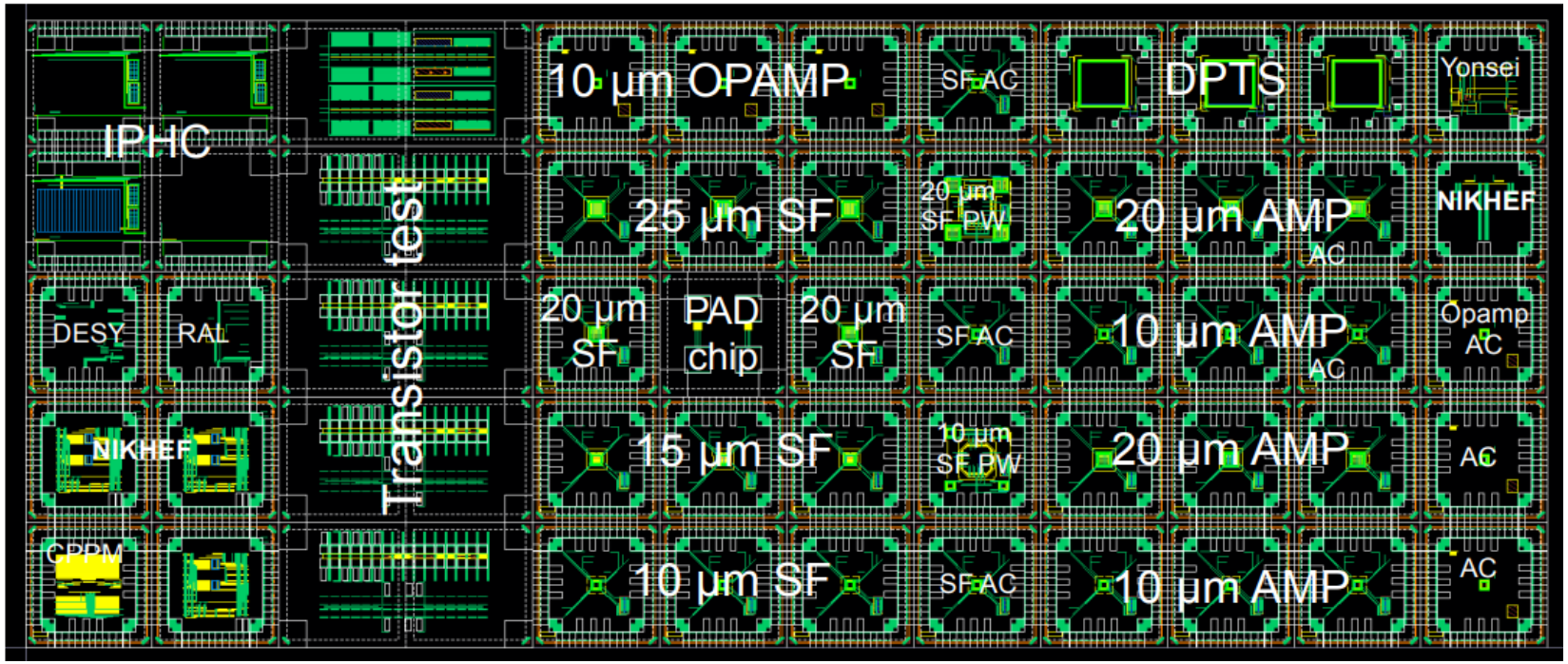



  - detection performance
  - radiation hardness

- **Design know-how**
  - understanding the design kit limitation/features
  - getting familiarity with IO structures

## Submitted Chips:

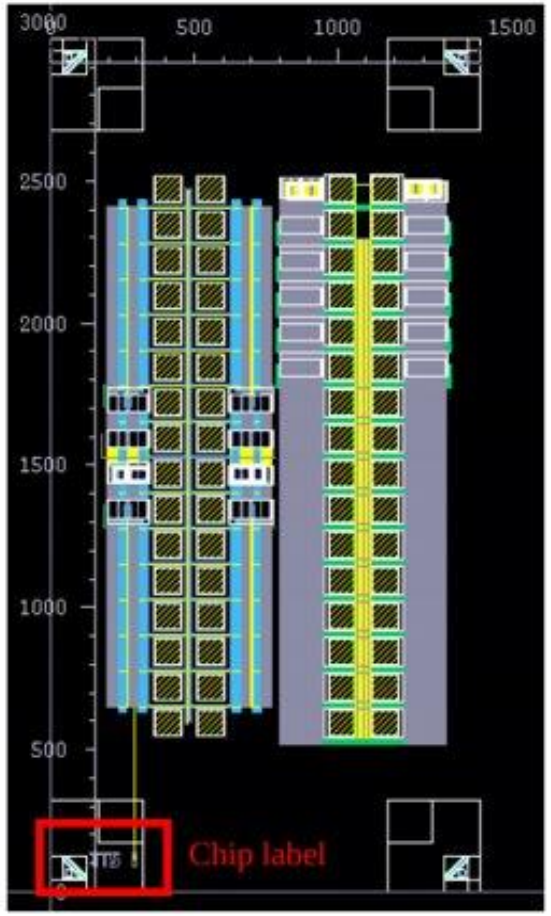
- **Transistor test structures**
- **Pixel test structures**
  - APTS (44)
  - DPTS (3)
  - CE65 (4)
  - CSA Pixel
- **First batch of common functional blocks**
  - Temperature sensor
  - Bandgap's
  - DAC's
  - LVDS/CML
  - ....

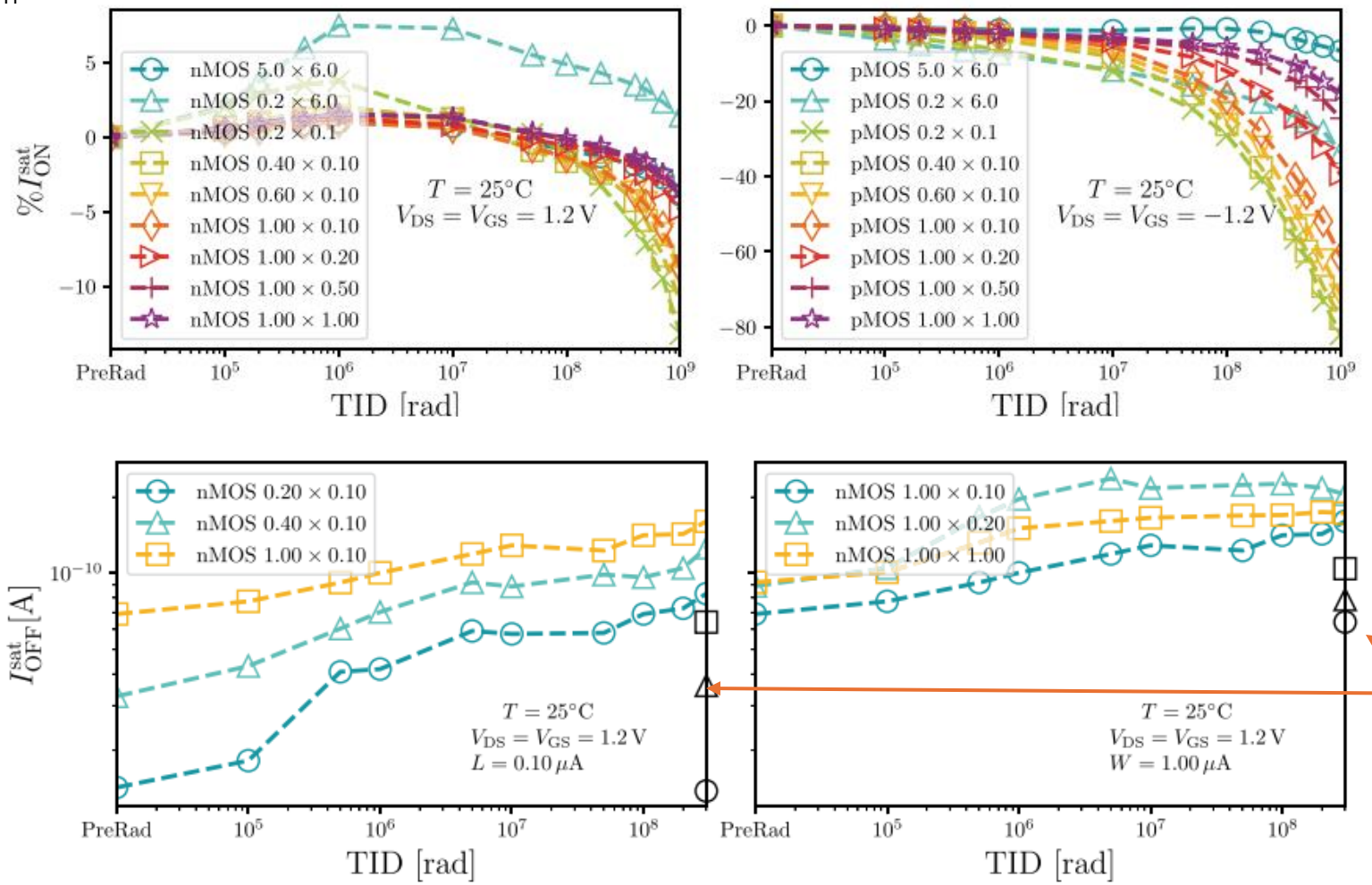


# Transistor Test Structures

## Transistors radiation hadrness:

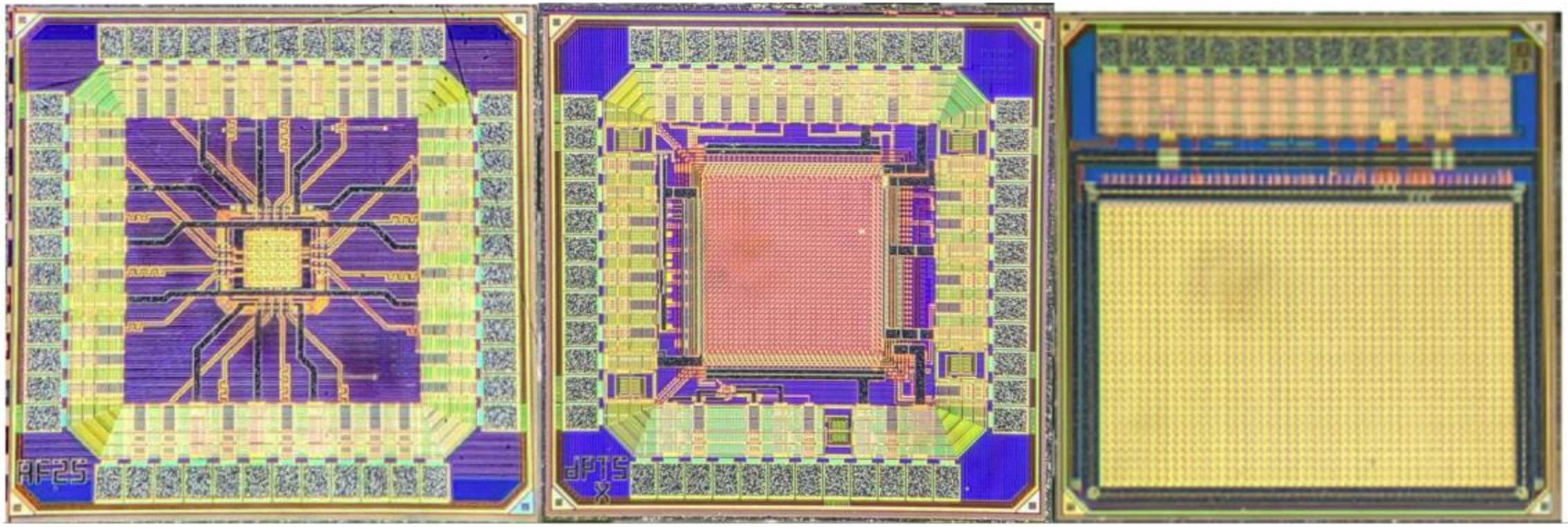
- nMOS transistors works up to 1Grad (15% drop of $I^{SAT}_{ON}$)
- pMOS transistors less resiliant
- Annealing at 100*C recovers the shifts in $V_{TH}$




*„Measurements of total ionizing dose effects in TPSCo 65 nm and influence of NMOS bulk bias" by A. Dorda Martin*

# Pixel Test Structure




- **APTS (Analog pixel test structure)**
  - 4x4 pixel matrix
  - Pixel pitch 15 / 20 / 25 um
  - SF / CSA input stage
  - individually connected to IOs
- **DPTS (Digital pixel test structure)**
  - 32x32 pixel matrix
  - Pixel pitch 15 um
  - CSA + discriminator
  - Time preserving digital readout
- **CE65 (Circuit Exploratoire 65 nm)**
  - 64x32 pixel matrix
  - Pixel pitch 15 / 25 um
  - SF / CSA input stage
  - Rolling-shutter readout

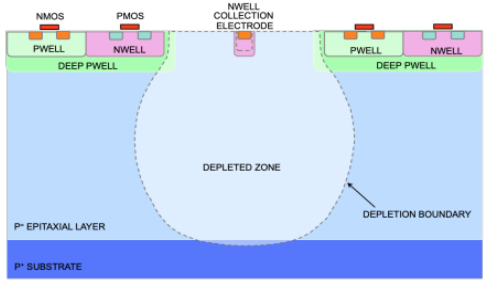
# Pixel Test Structure

## CHARGE COLLECTION:

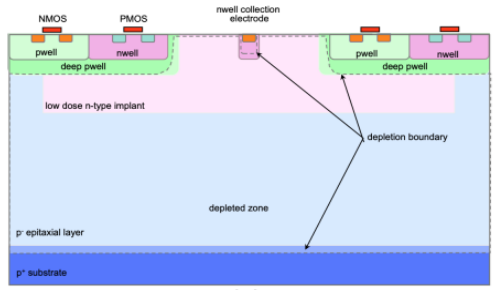
### Charge sharing comparision for different sensor variants

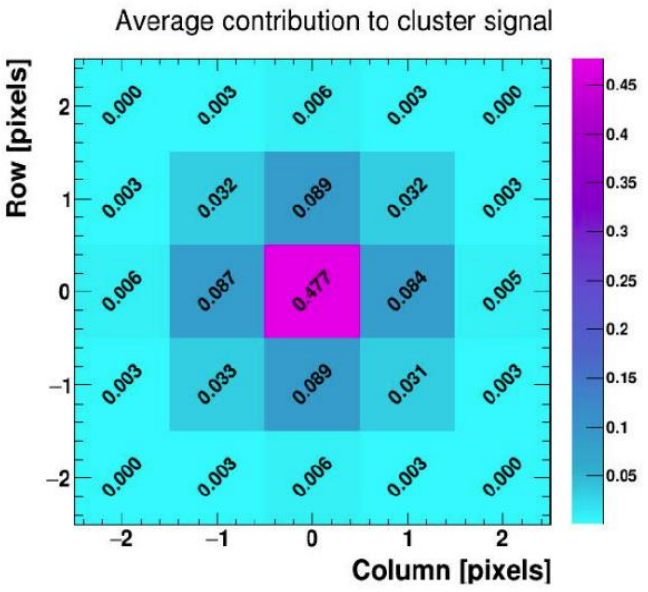
### (based on CE65 results)

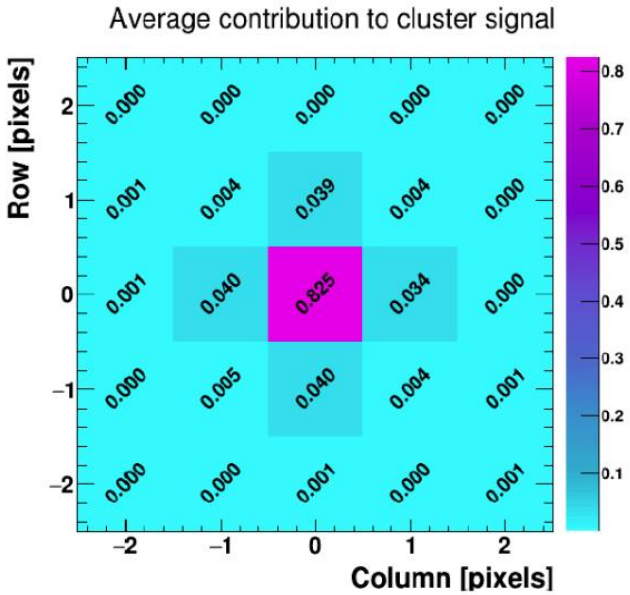
**Standard**



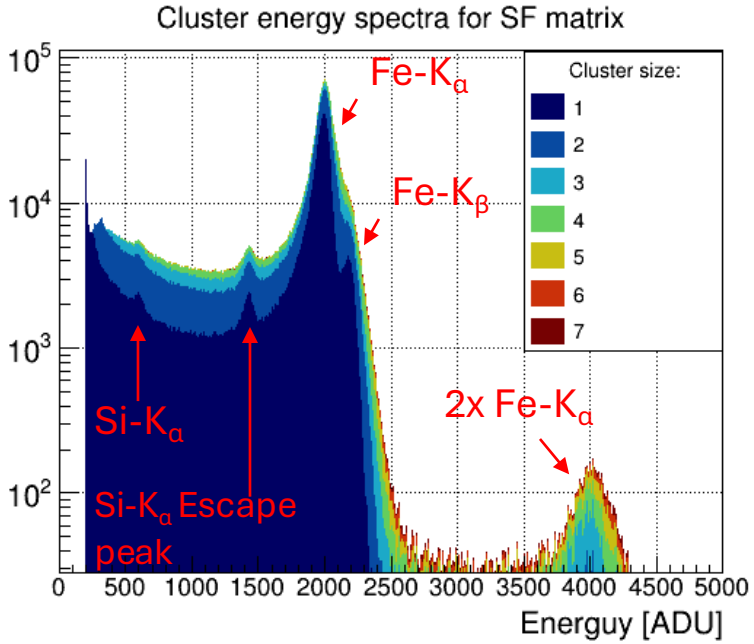

**N-GAP**




**$^{55}$Fe spectra from CE65**

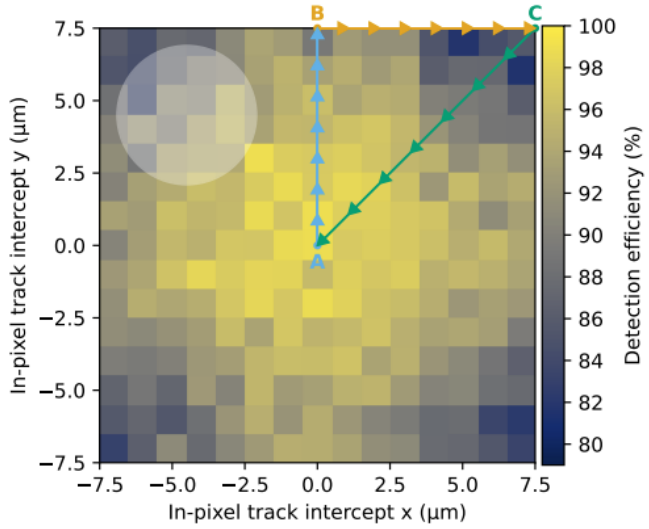


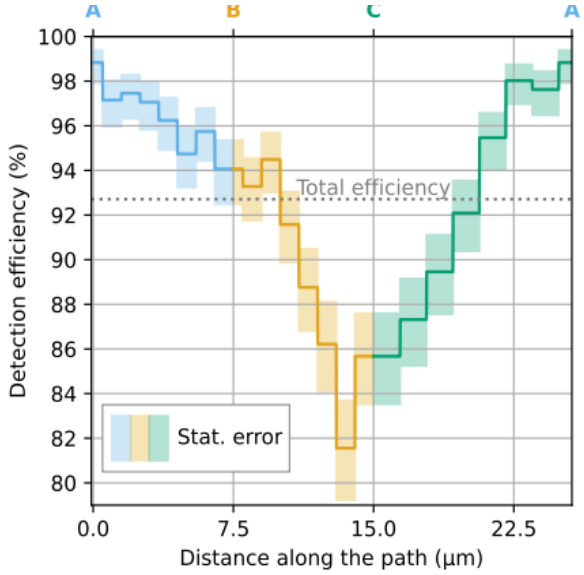

- **5 peaks clearly visible:**
  - Si($K_\alpha$) = 1.74 keV
  - Si($K_\alpha$) escape peak ($FeK_\alpha - SiK_\alpha$= 4.16 keV)
  - Fe($K_\alpha$) = 5.9 keV
  - Fe($K_\beta$) = 6.49 keV
  - 2x Fe($K_\alpha$)= 11.8 keV

*„Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology" by S. Bugiel*

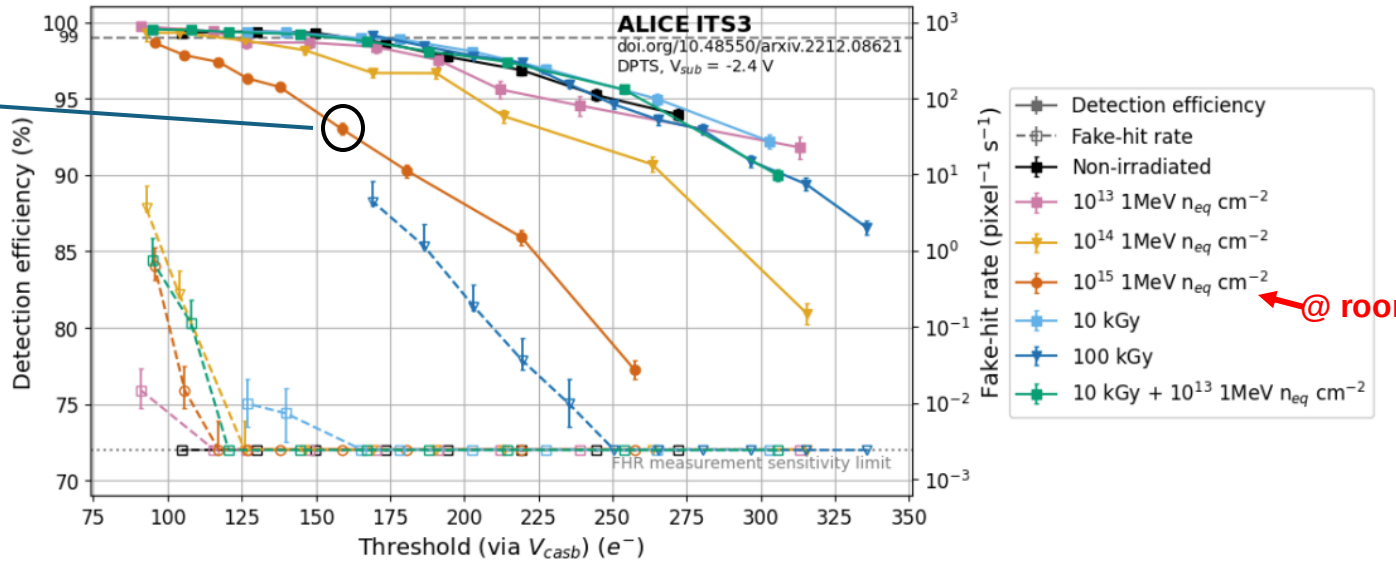
# Pixel Test Structure

## Detection Efficiency:




### DPTS efficiency at different irradiation levels




@ room temp

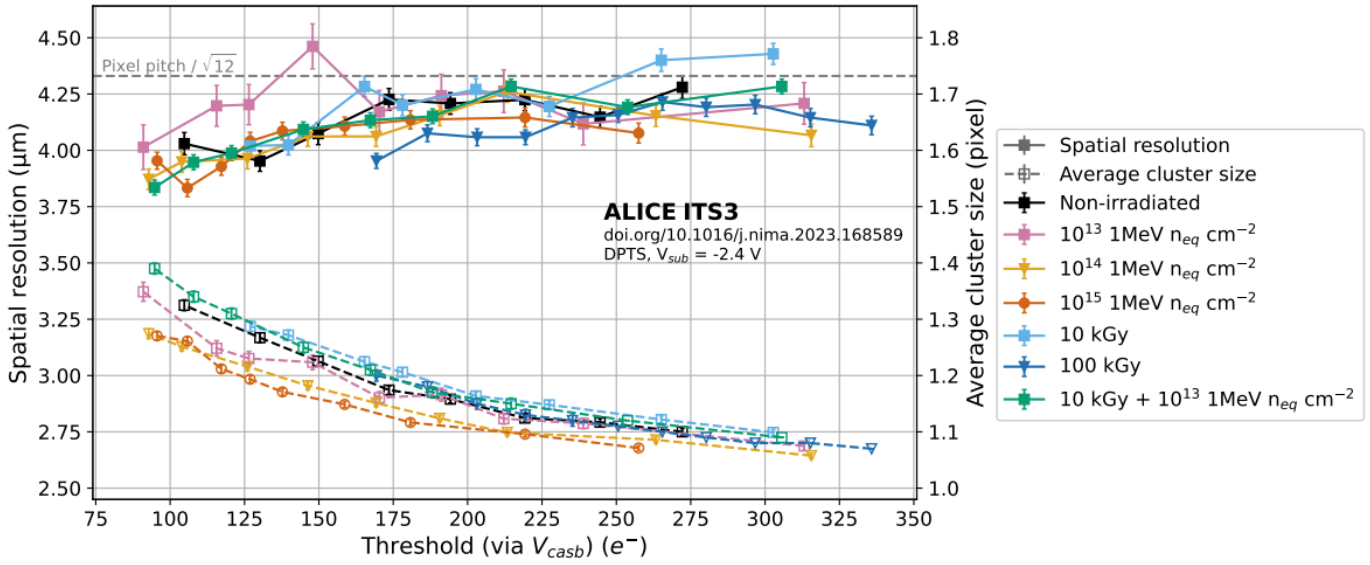
https://arxiv.org/pdf/2212.08621.pdf

*„Digital Pixel Test Structures implemented in a 65 nm CMOS process" by M. Šuljić*

# Pixel Test Structure

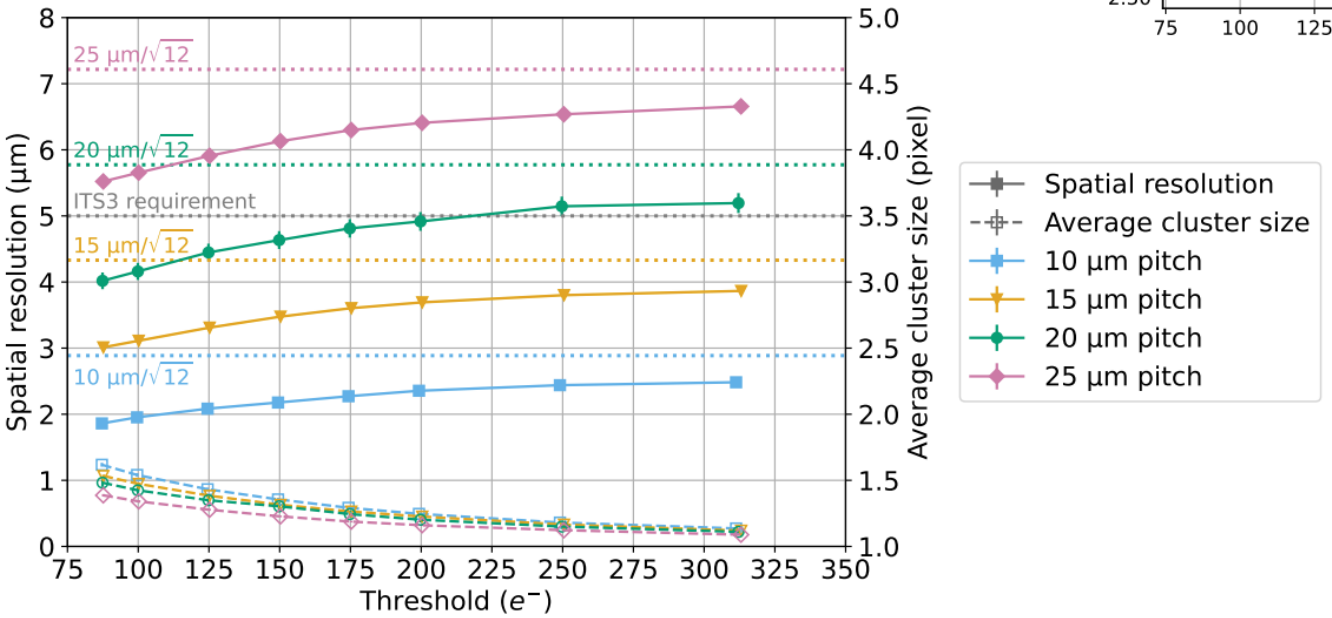
## Spatial resolution:

### DPTS resolution at different irradiation levels




### APTS resolution for different pixel pitch

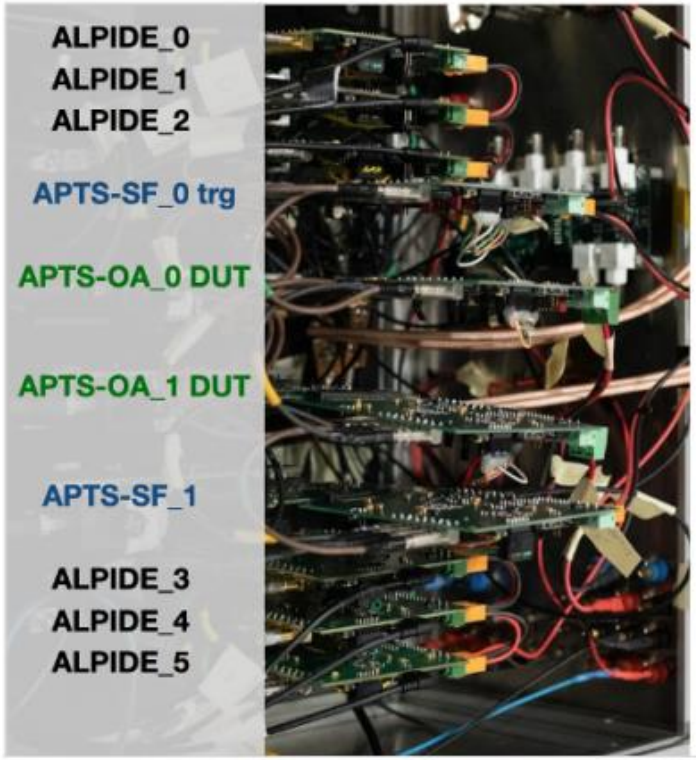
(emulating digital output)

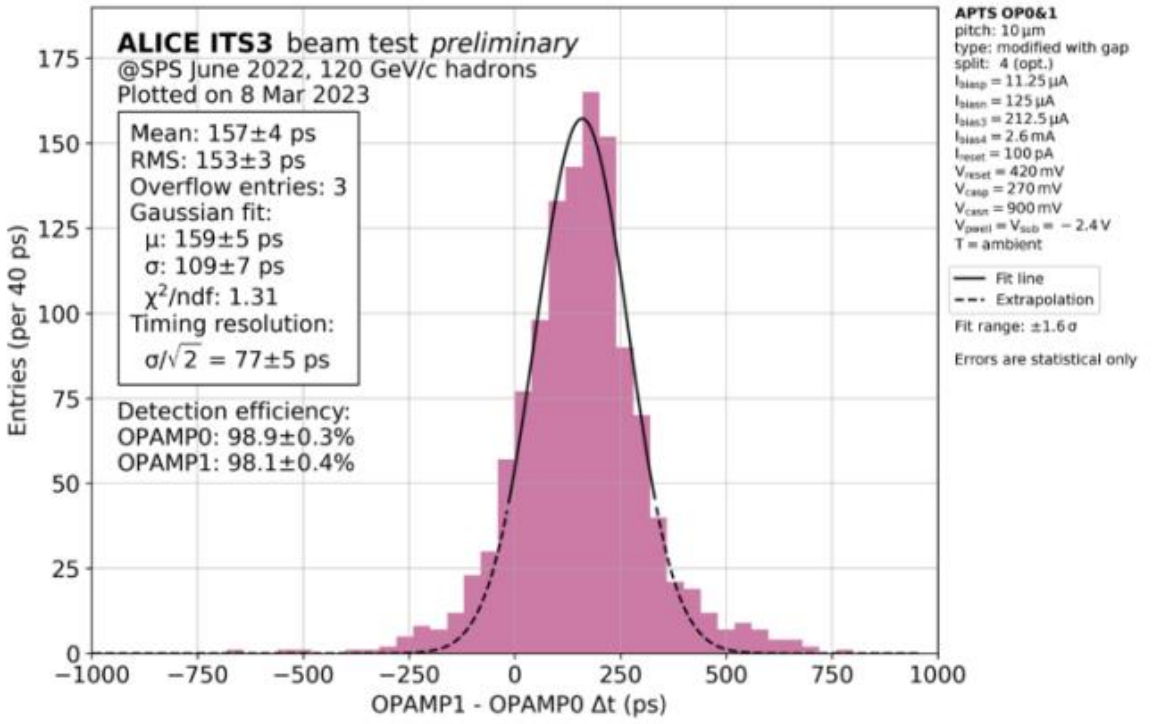


# Pixel Test Structure

## TIME RESOLUTION:

- 110 ps resolution for time difference between two planes
- **~77 ps resolution for a single plane**

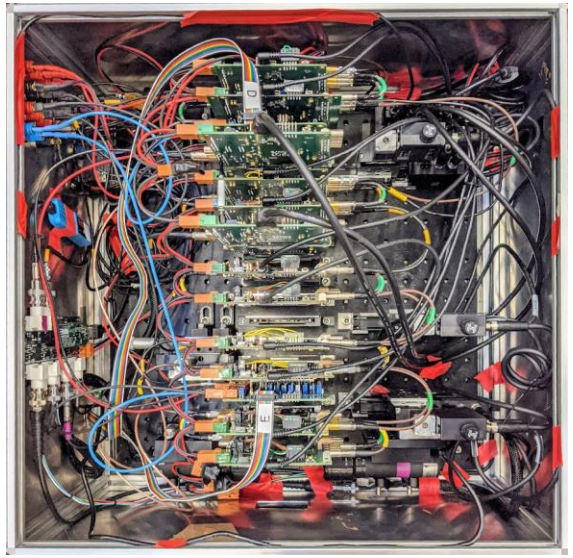


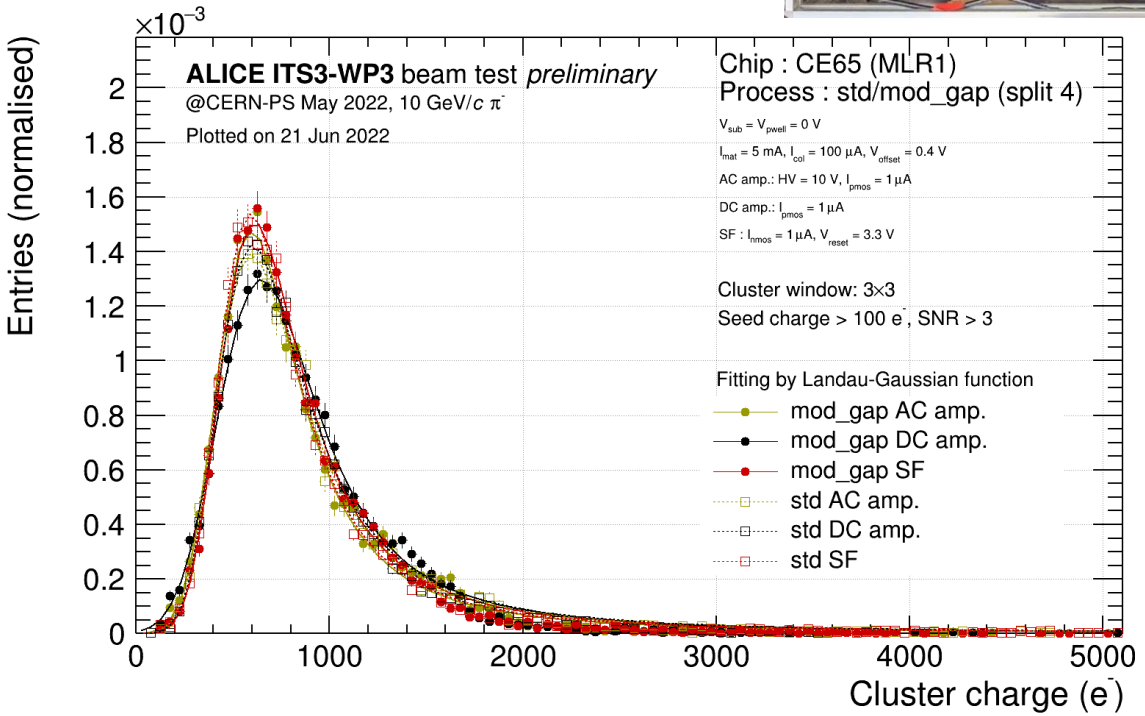



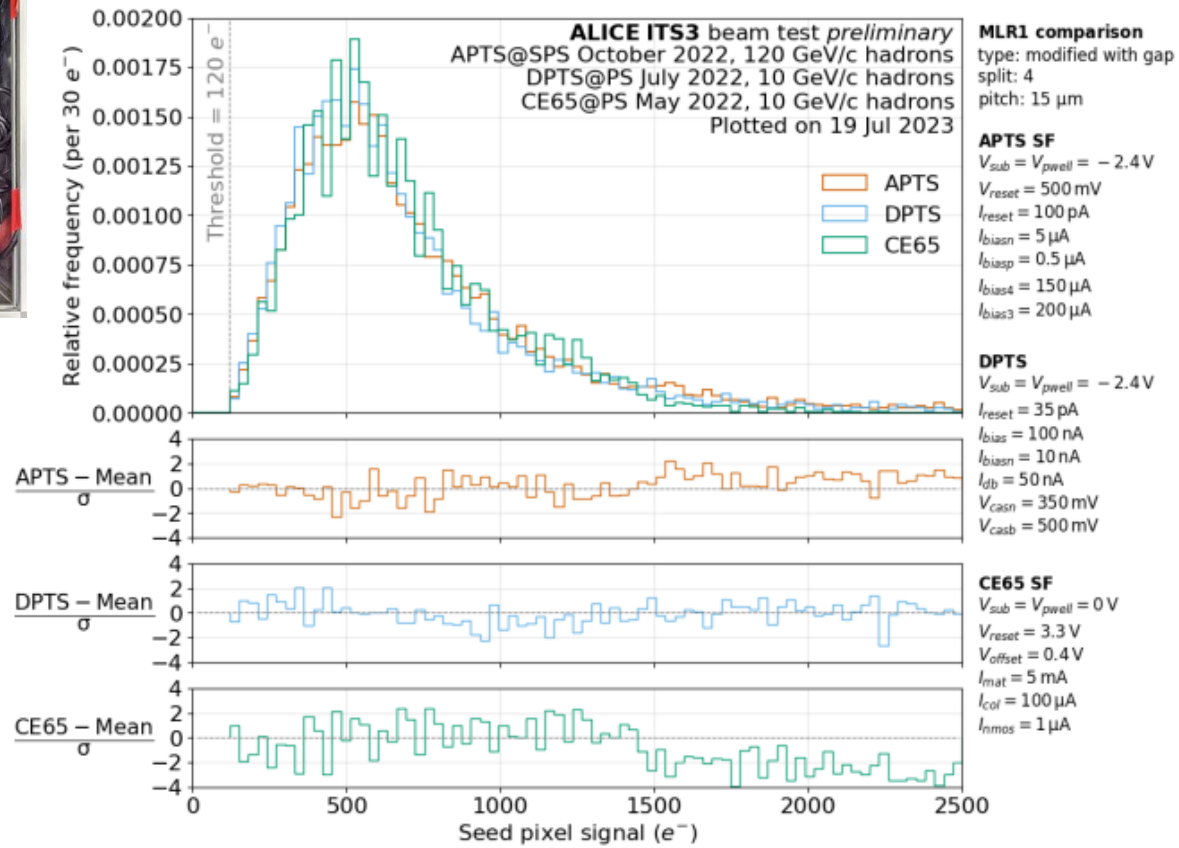
# Pixel Test Structure

## Sensitive volume thickness:

- Cluster charge distribution **MPV around 600e⁻**
  - epi-layer thickness ~11 um
  - well matched accros different test chips





# Second submission (ER1)

# Second submission (ER1)

## ER1 Objectives:

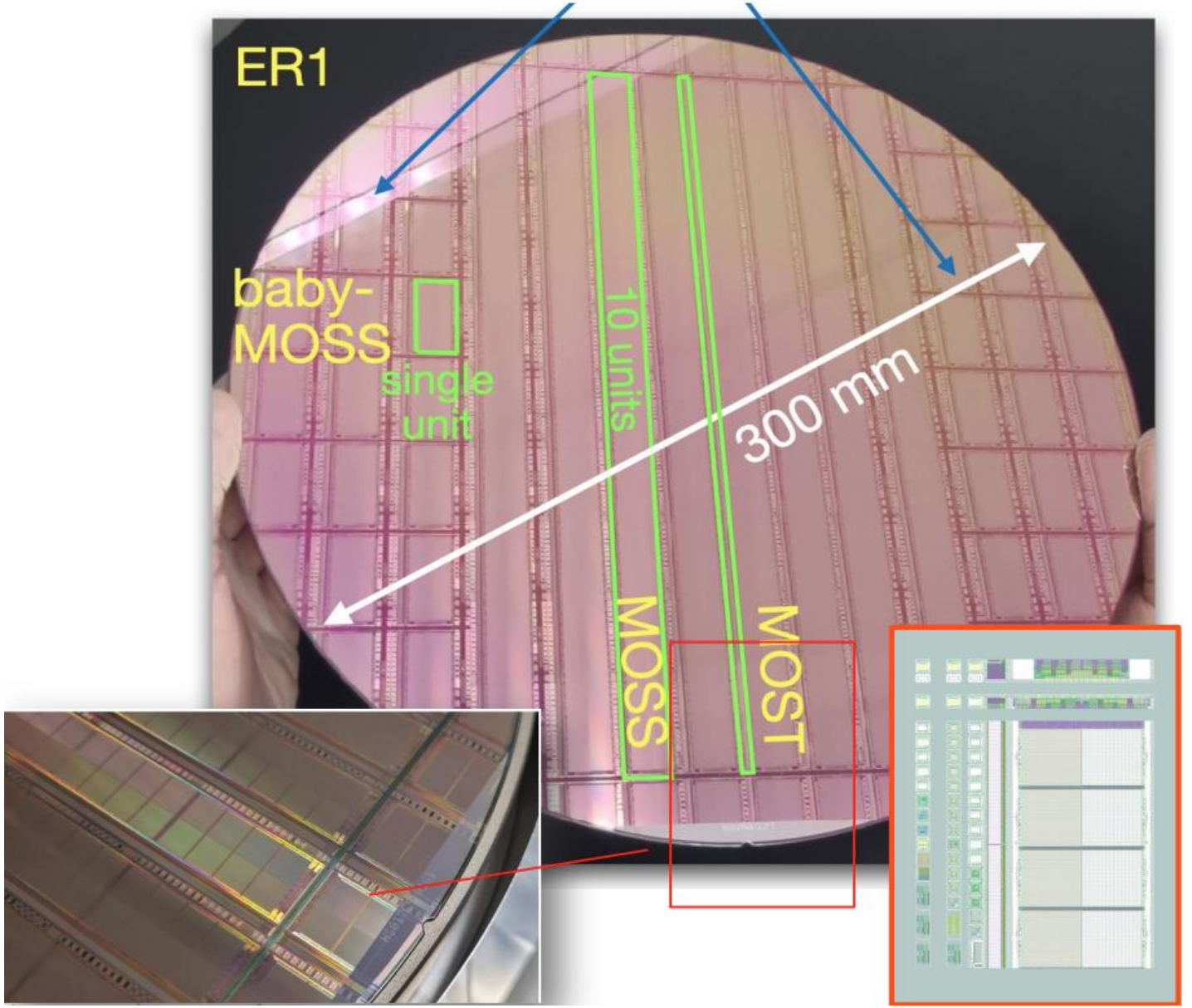
- **Develop stitching know-how**
  - Yield estimate
  - Defects „masking”
  - Power distribution
  - Sensor depletion
  - Waferscale spreads
  - Methodology

  } **MOSS** **MOST**

- **Continue R&D program**
  - Second batch of small exploratory detectors
  - SEU chip

- **Additional set of functional blocks:**
  - PLL
  - LDO
  - DATA LINKS
  - ....

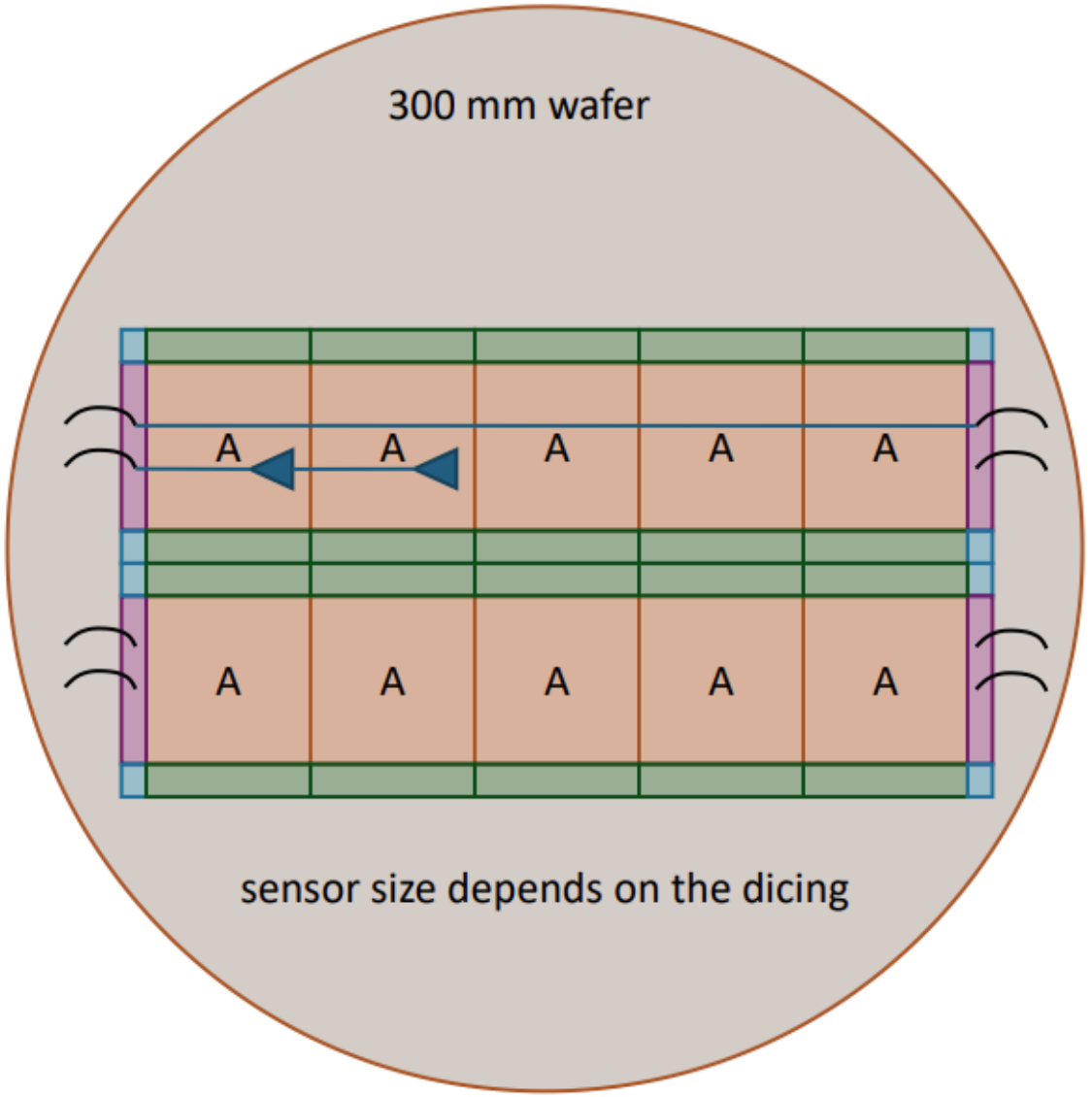
- **Essential input for ER2**



# Stitching technique

- Wafer scale detector? --> Stitching technique
  - Dividing a reticle (typ 2 x 3 cm) into a separate units:

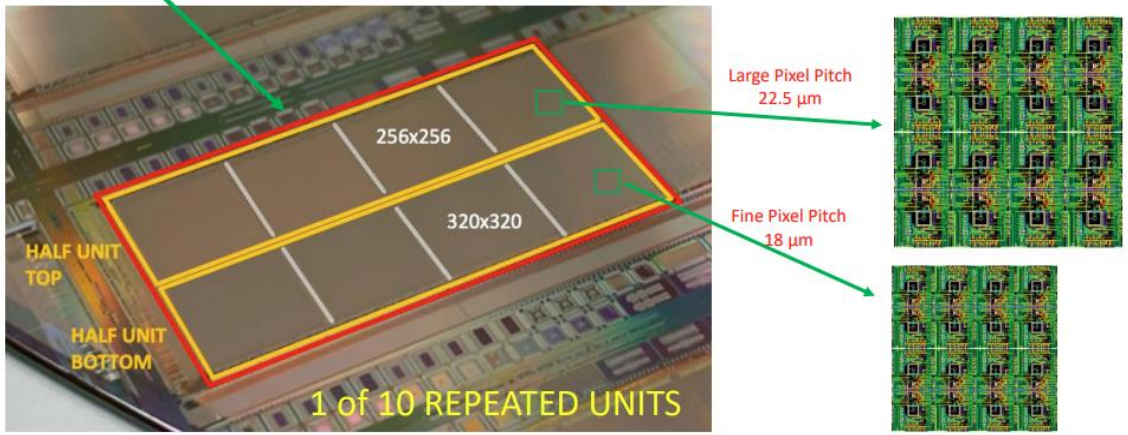

  - Stepping the lithography process with the repeated unit such that the connectivity on the edges is maintained
  - Adding endcaps on the sides



# Stitched sensors prototypes

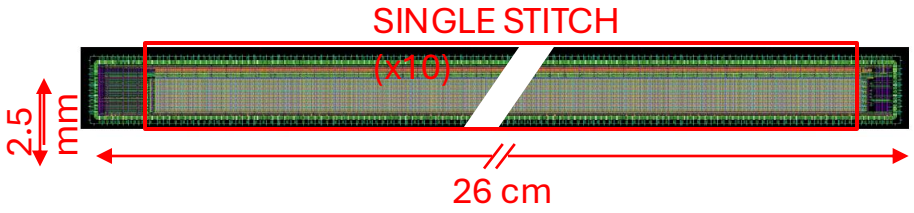
## MOSS: (MONOLITHIC STITCHED SENSOR)


- **14 mm x 259 mm**
- Two pixel pitches: 18um and 22.5um
- Modification of well established, priority encoder readout scheme (digital)
- Independent powering of half stitched units
- Conservative layout

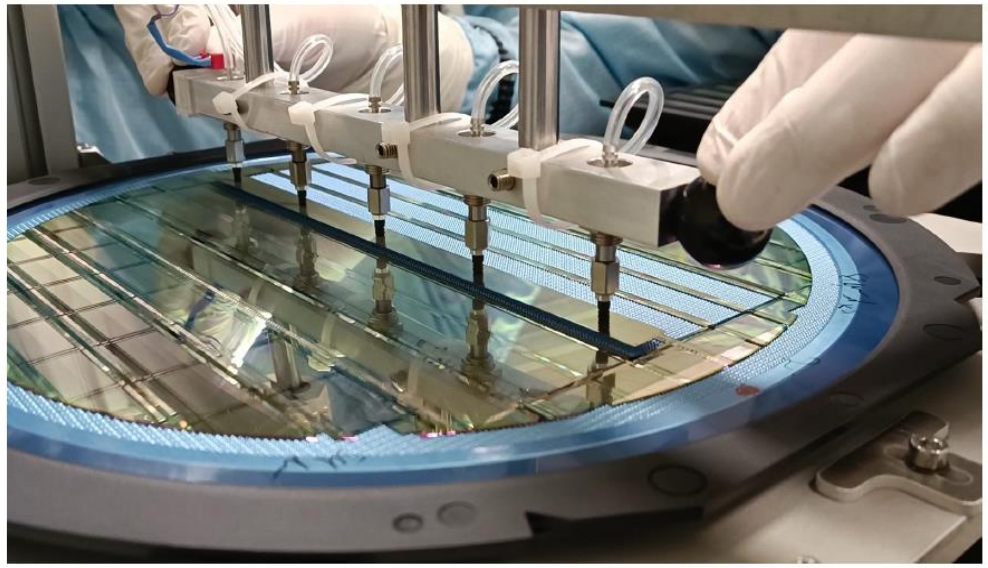


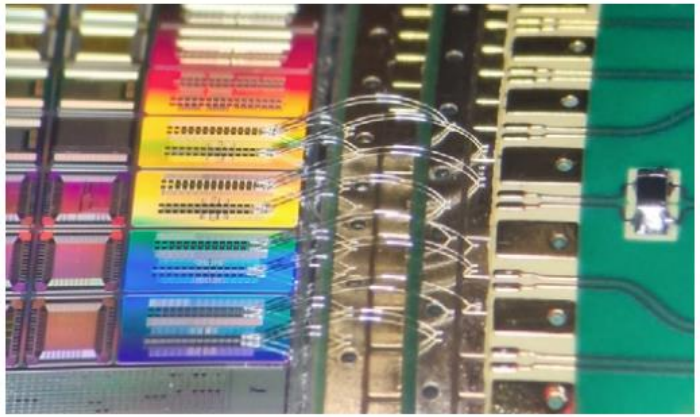

## MOST: (MONOLITHIC STITCHED SENSOR WITH TIMING)

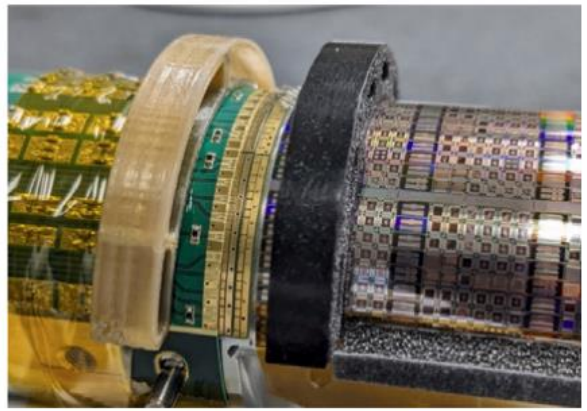

- **2.5 mm x 259 mm**
- Pixel pitch: 18um
- Asynchronous hit-driven readout (ToA + ToT information)
- 4 common power domains
- High granularity local power gating to mitigate defects
- High local density preserved

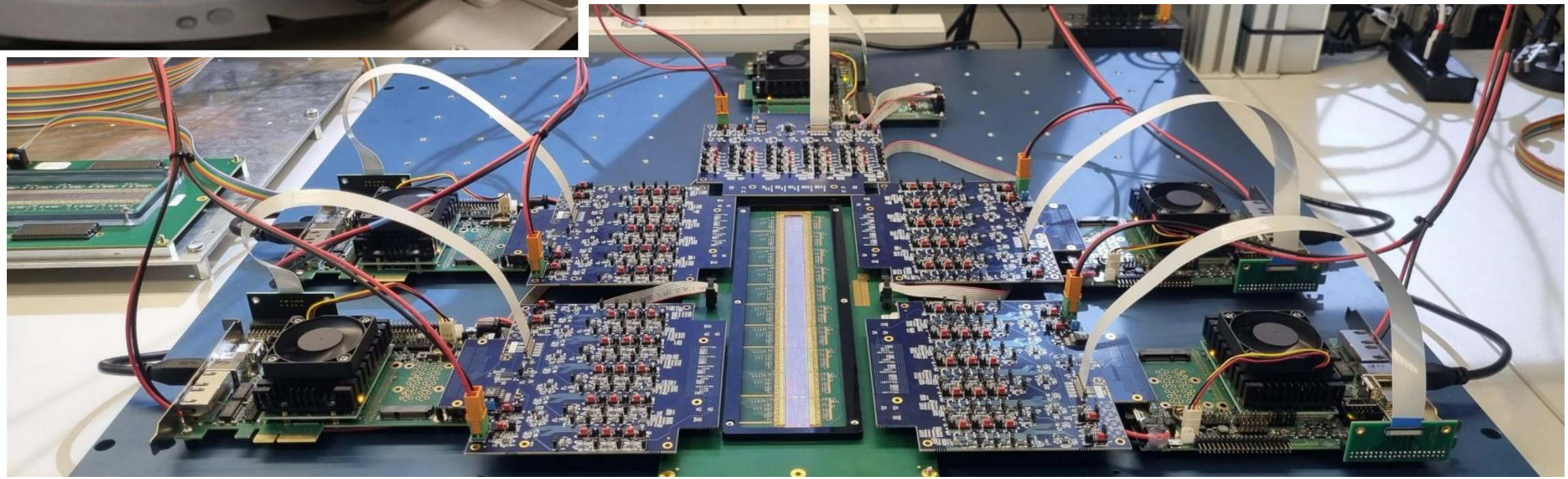


# Measurement setups







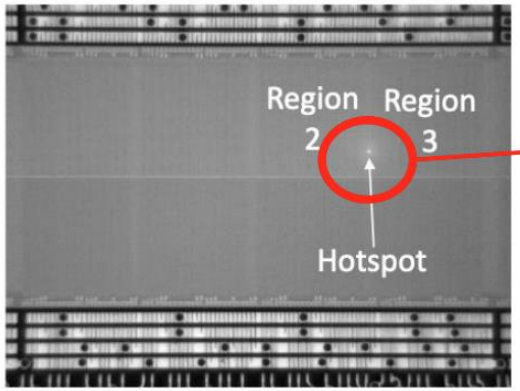


# MOSS Yield

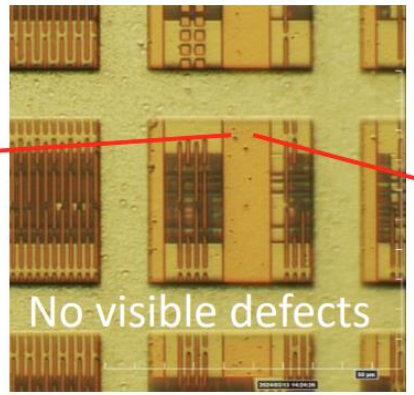
- **Considerable fraction of the MOSS test units failing during power-up**
  - Shorts between power nets
  - Significant wafer to wafer variations

- **Understood thanks to indepth investigation**
  - Vertical shorts between two metal layers
  - Followed-up with foundry
  - Expected to disapear with the next submission

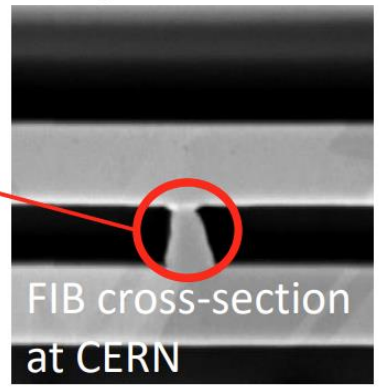
Thermal Imaging reveals shorts



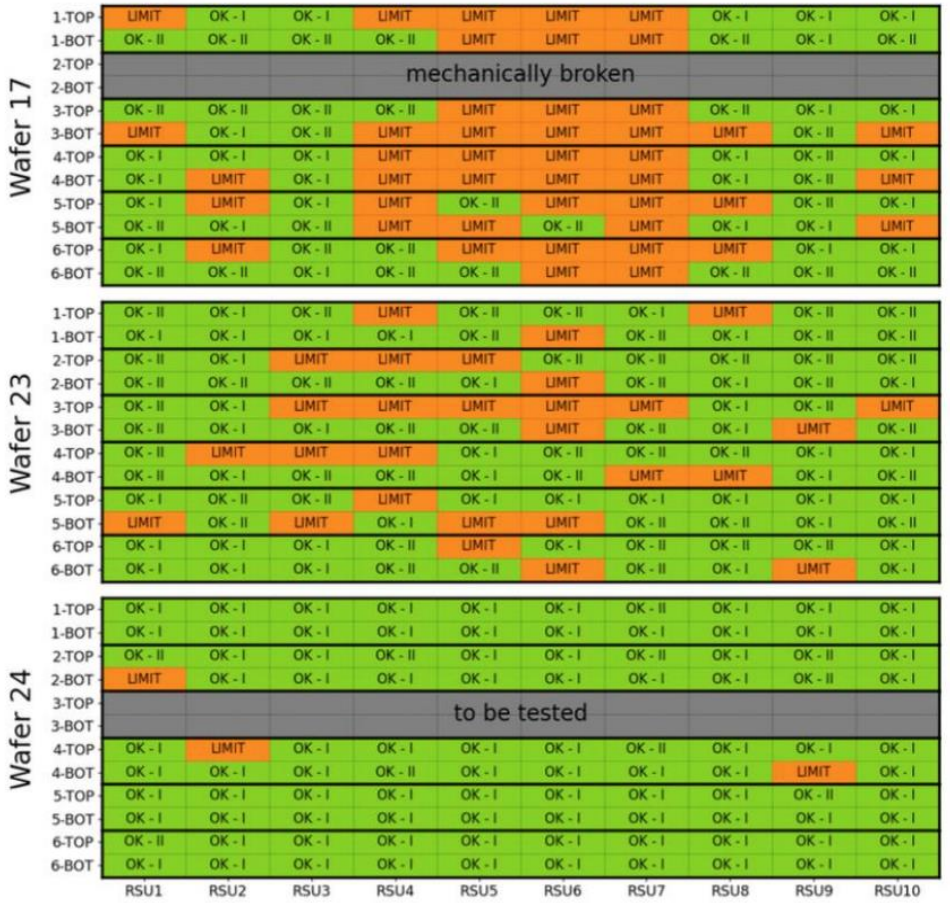

Optical Microscope




SEM image of metal-to-metal short

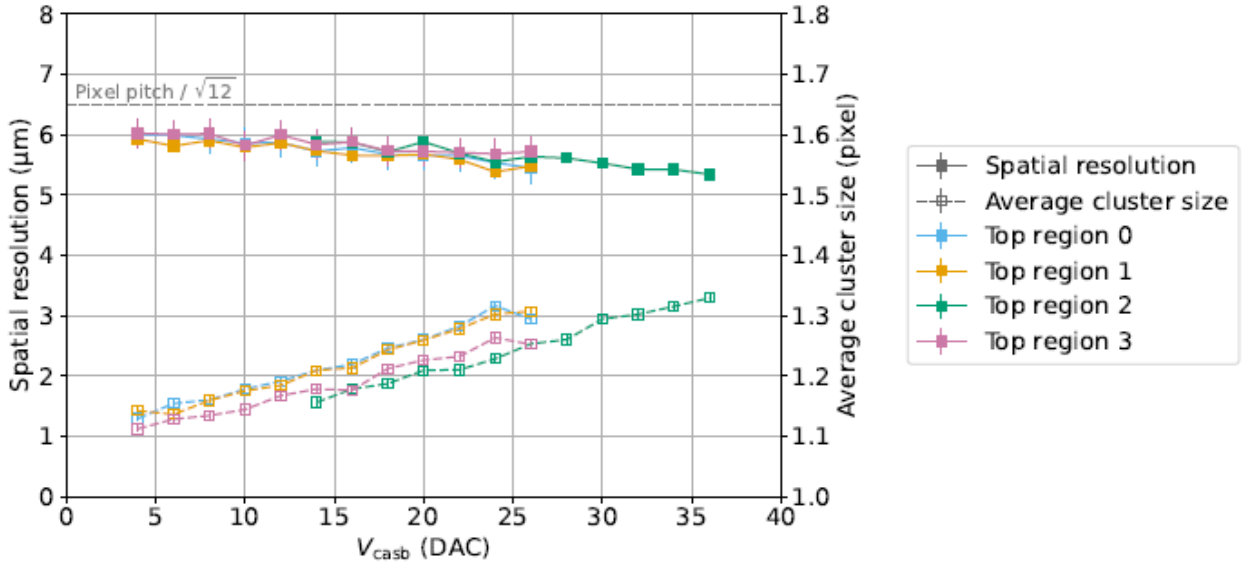


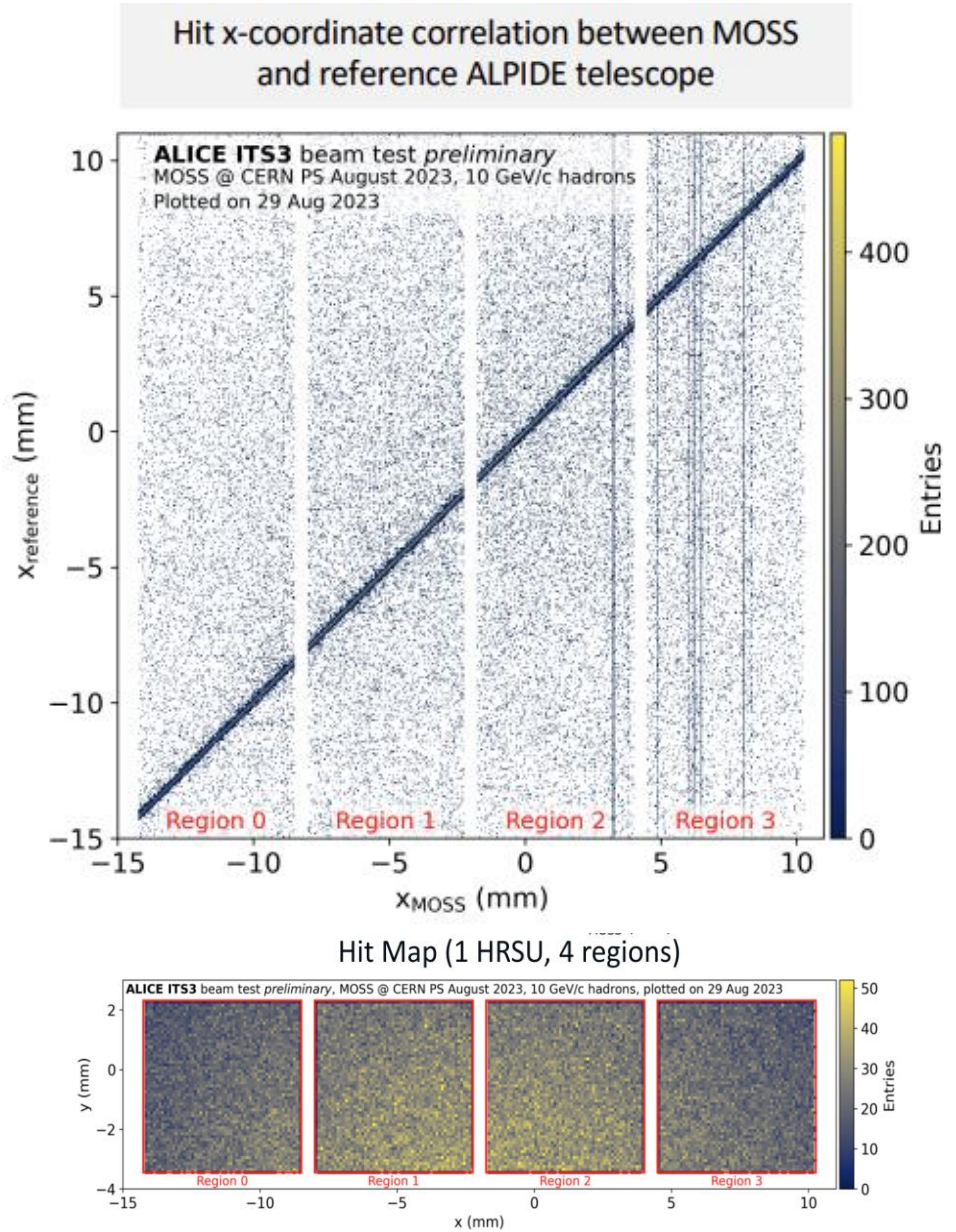

CERN-LHCC-2024-003 / ALICE-TDR-021
Powering tests from chips of the first three wafers tested.
The chips were thinned, diced, glued and bonded before testing



# MOSS test beam results

- **MOSS measurement activities on-going on multiple fronts**
  - Full/Single-Stitch chips
  - Test-beams
    (efficiency, FHT, resolution)
  - Irradiation camaigns
  - SEU / SEL crossection measurements

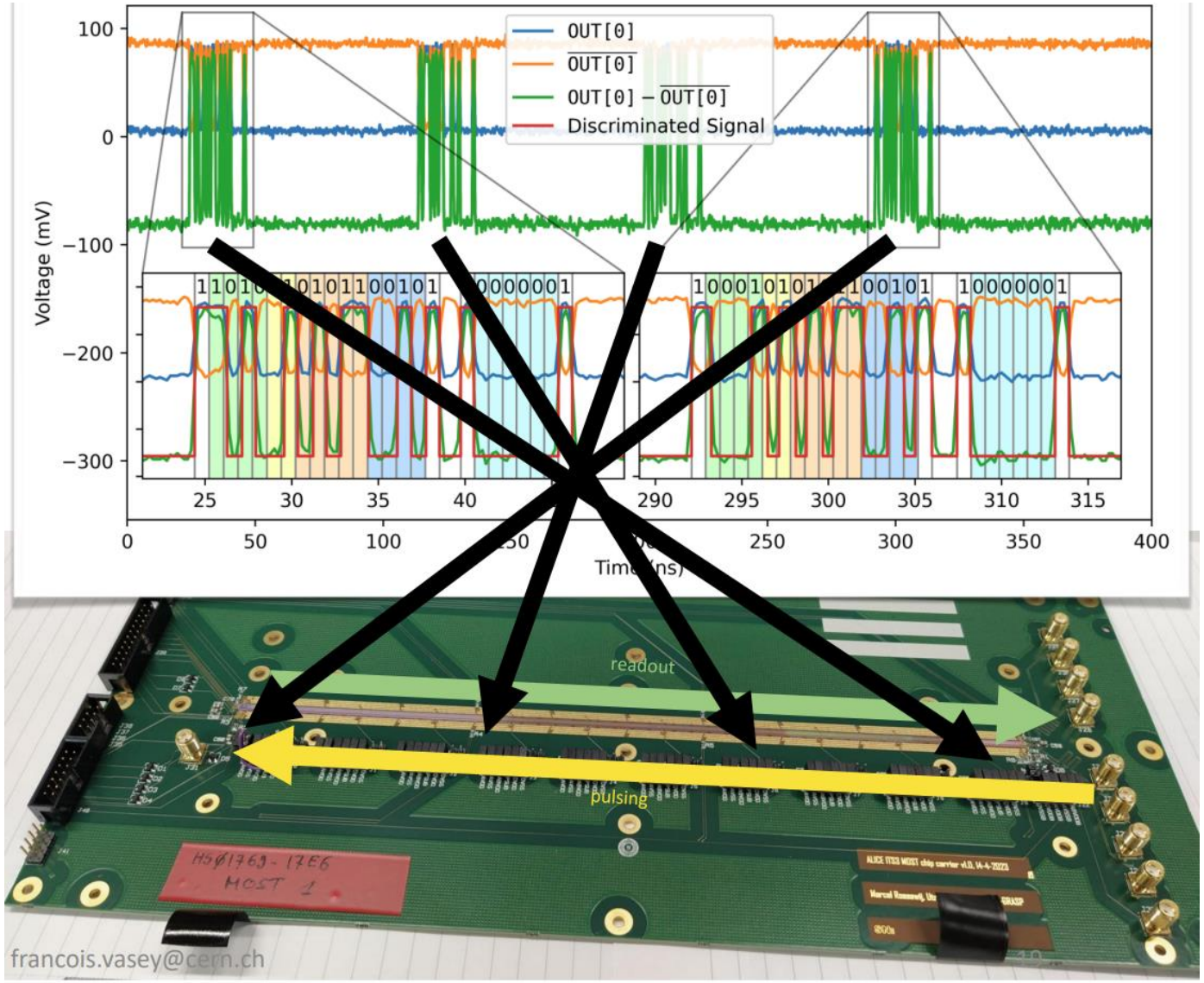



*„EP R&D WP1.2 Monolithic CMOS Sensors" by F. Vasey*

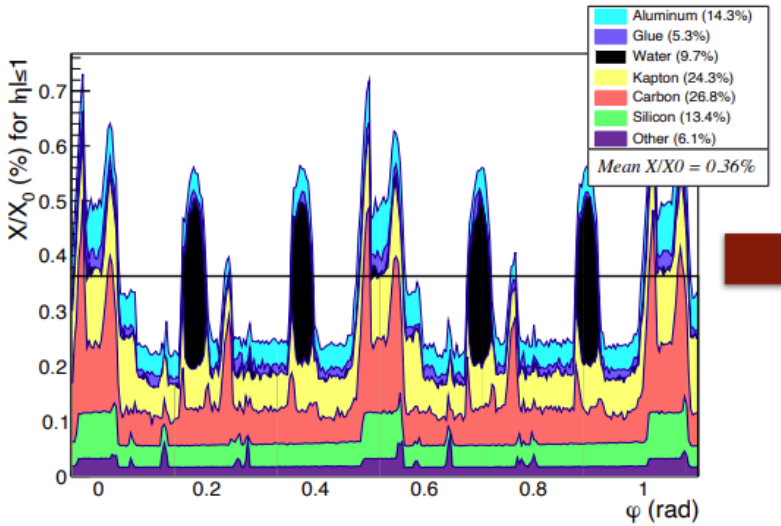
# MOST results

- **Chip fully functional**
- **Prove of concept for the asynchronous, hit-driven readout**
- **No issues across stitching boundaries**
  - 256 readout lines fully working across full length of the chip
  - About 300ns round-trip propagation delay
- **Recently tested with the beam**
  - data analysis on-going

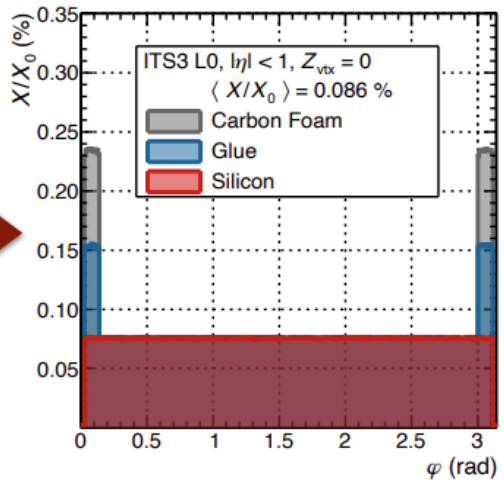


# Third submission (ER2)

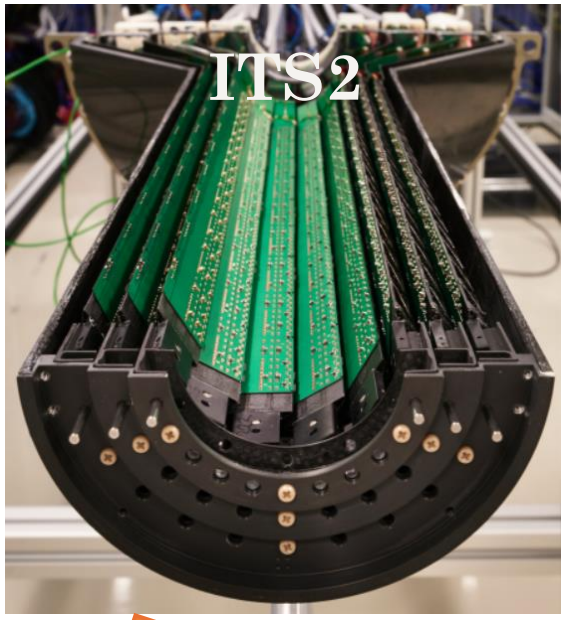
# Motivation: ALICE ITS3




ITS2 Layer 0

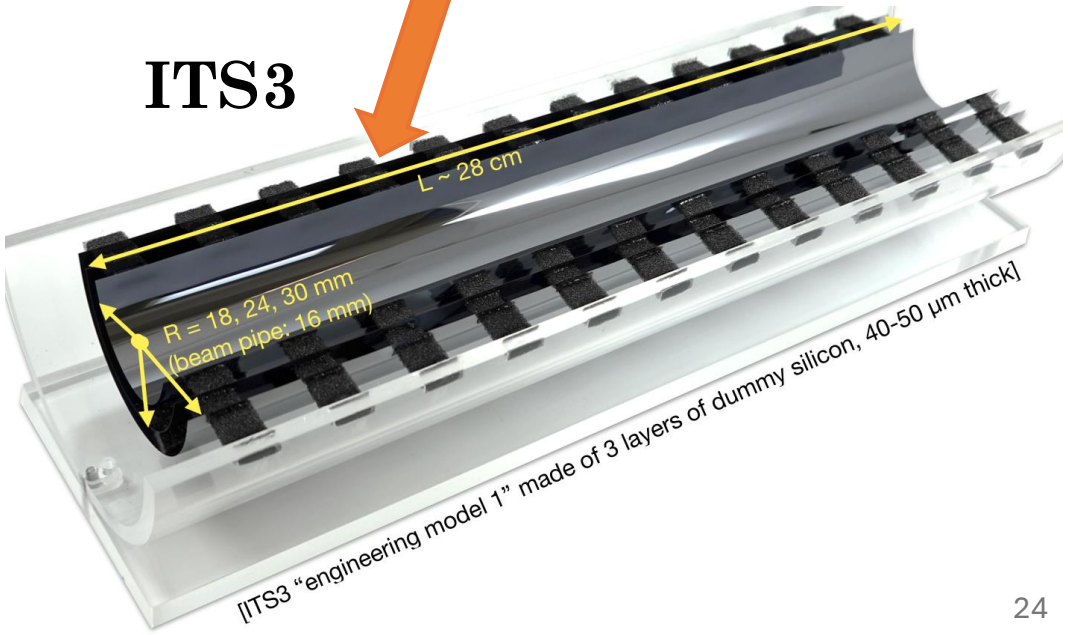



ITS3 Layer 0




- ALICE Inner Tracker System Udgrade:
  - replacement of a standard stave based modules with truly cylindrical full silicon layers
    --> minimal mechanical support thanks to the stiffens of bent silicon
  - 5x lower material budget
  - closer to the interaction point

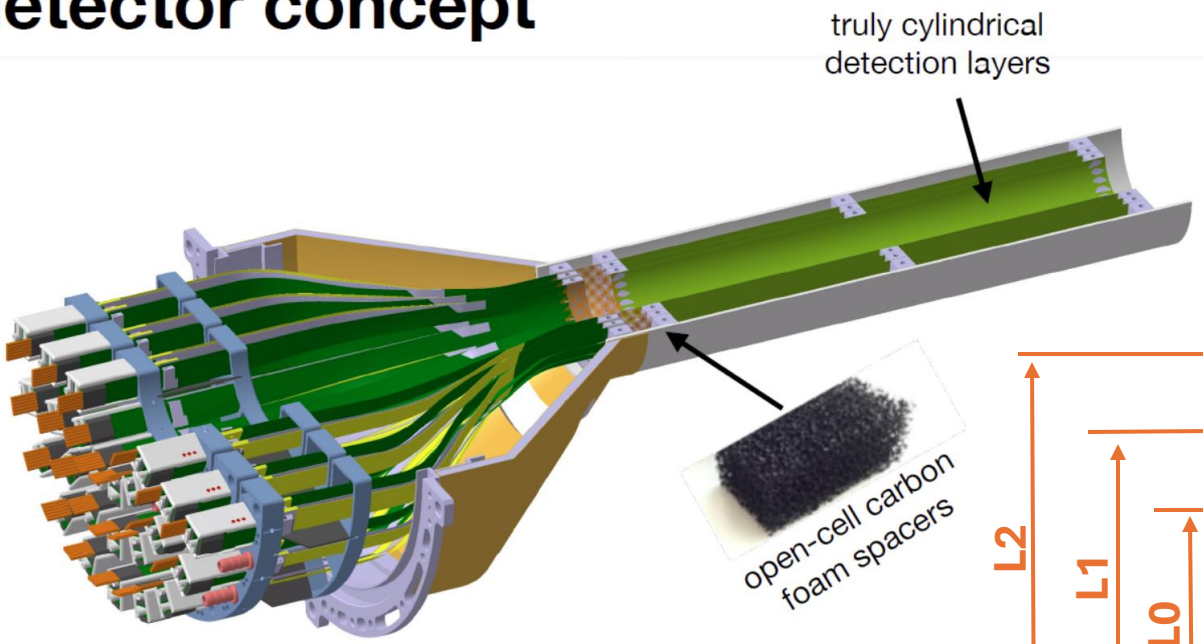
ITS3

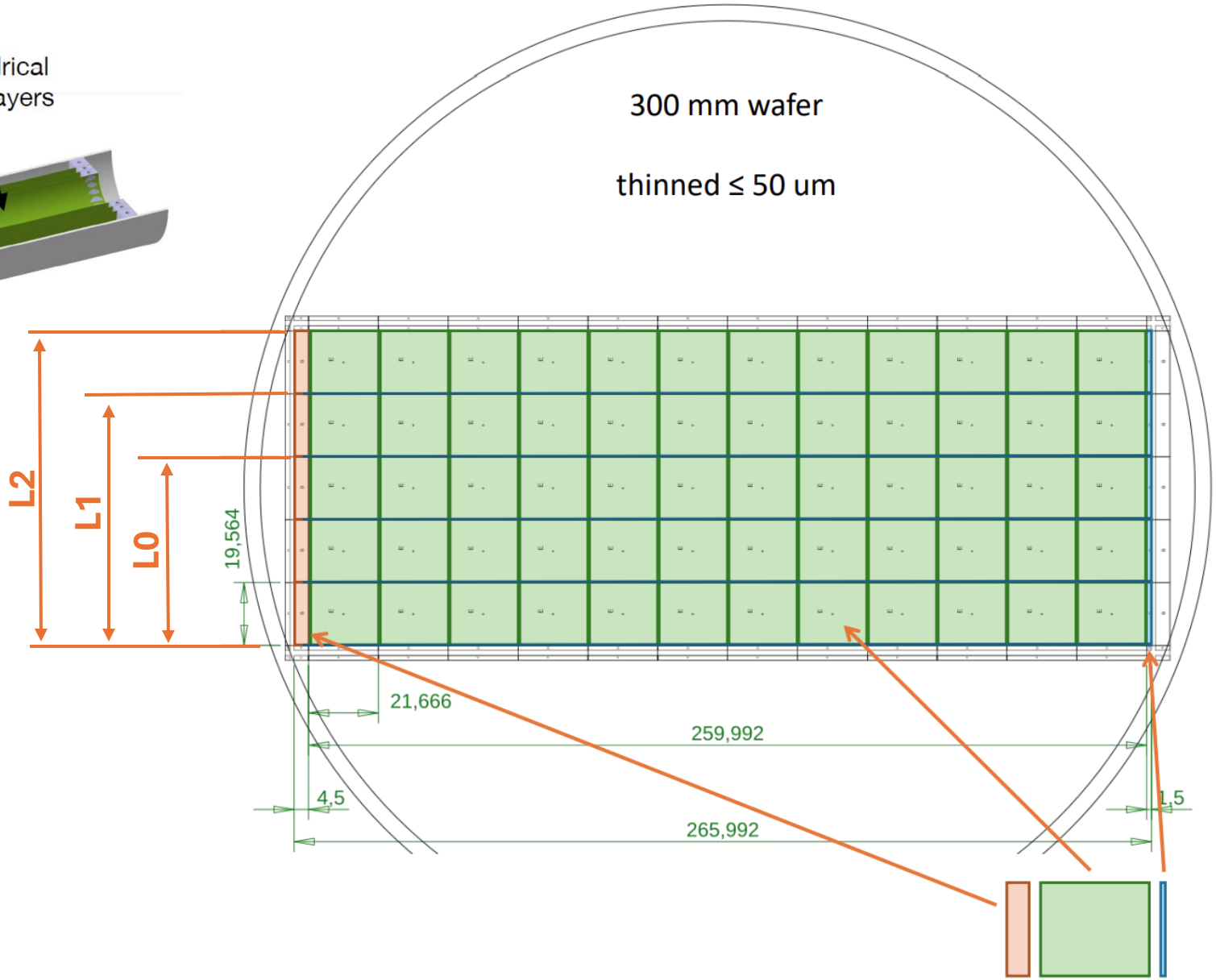



*„MAPS sensor developments in ALICE" by F. Reidt*

# Motivation: ALICE ITS3

## detector concept

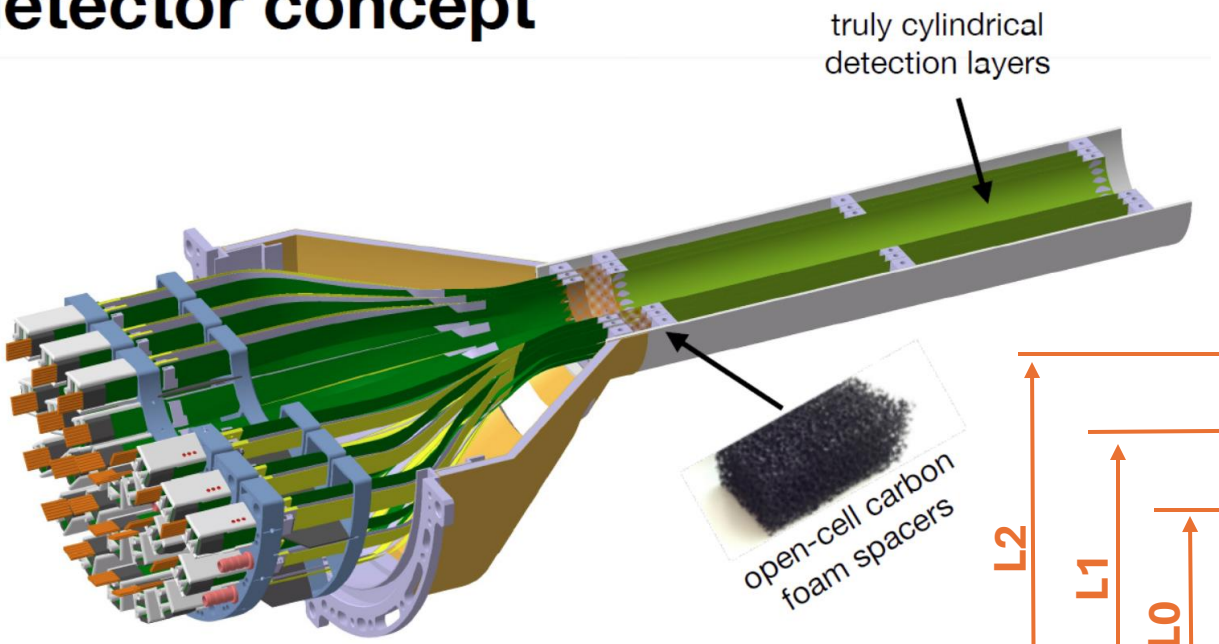


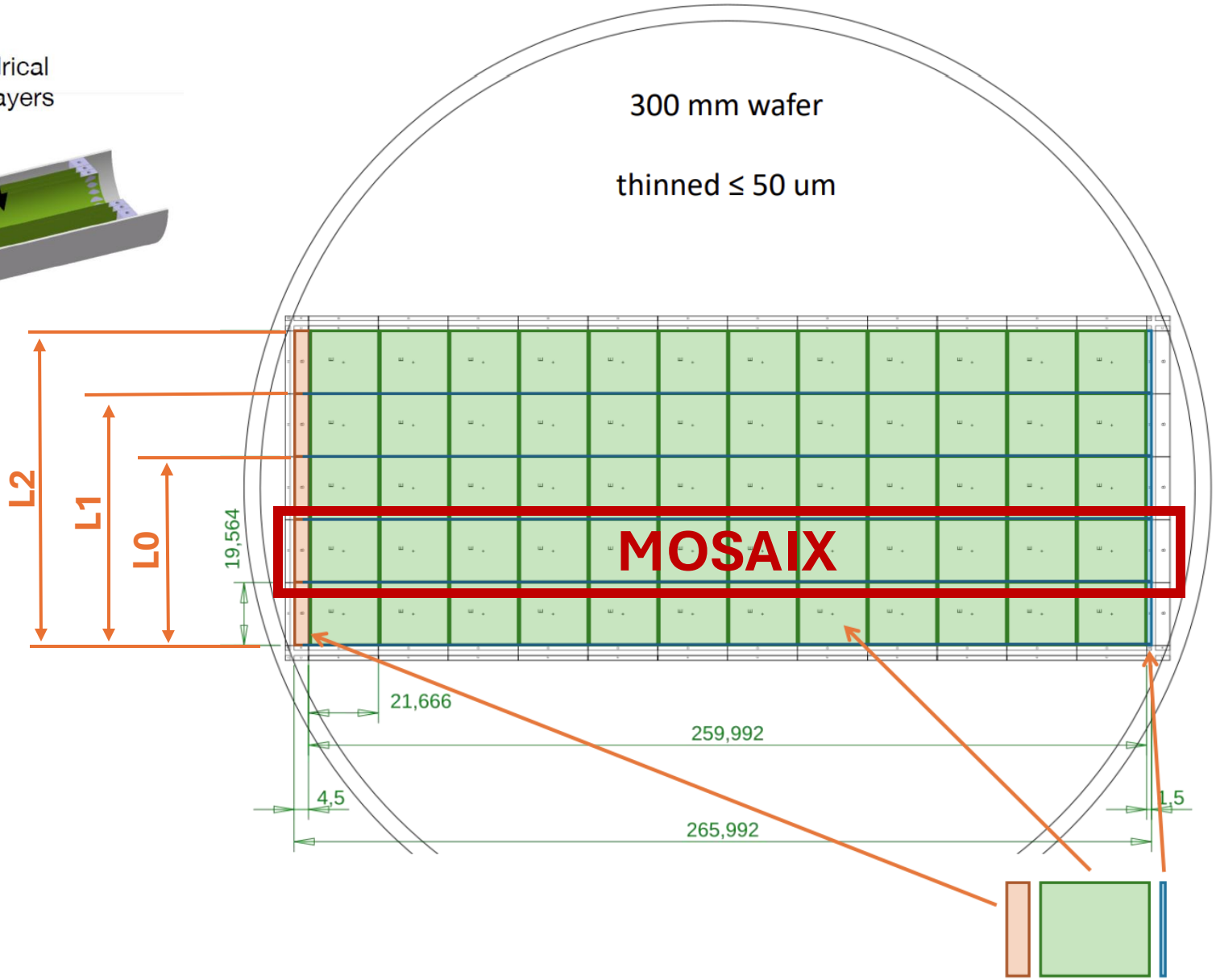




- Detector requirements:
  - 50 um thick **wafer-scale monolithic** detector
  - extremely **low power** (below 40 mW/cm²)
  - **powered only from the endcaps**
  - **bare silicon:**
    - no off-chip power reinforcement
    - no off-chip data links

# Motivation: ALICE ITS3

## detector concept




➢ Detector requirements:

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  - extremely **low power** (below 40 mW/cm$^2$)
  - **powered only from the endcaps**
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  - no off-chip power reinforcement
  - no off-chip data links

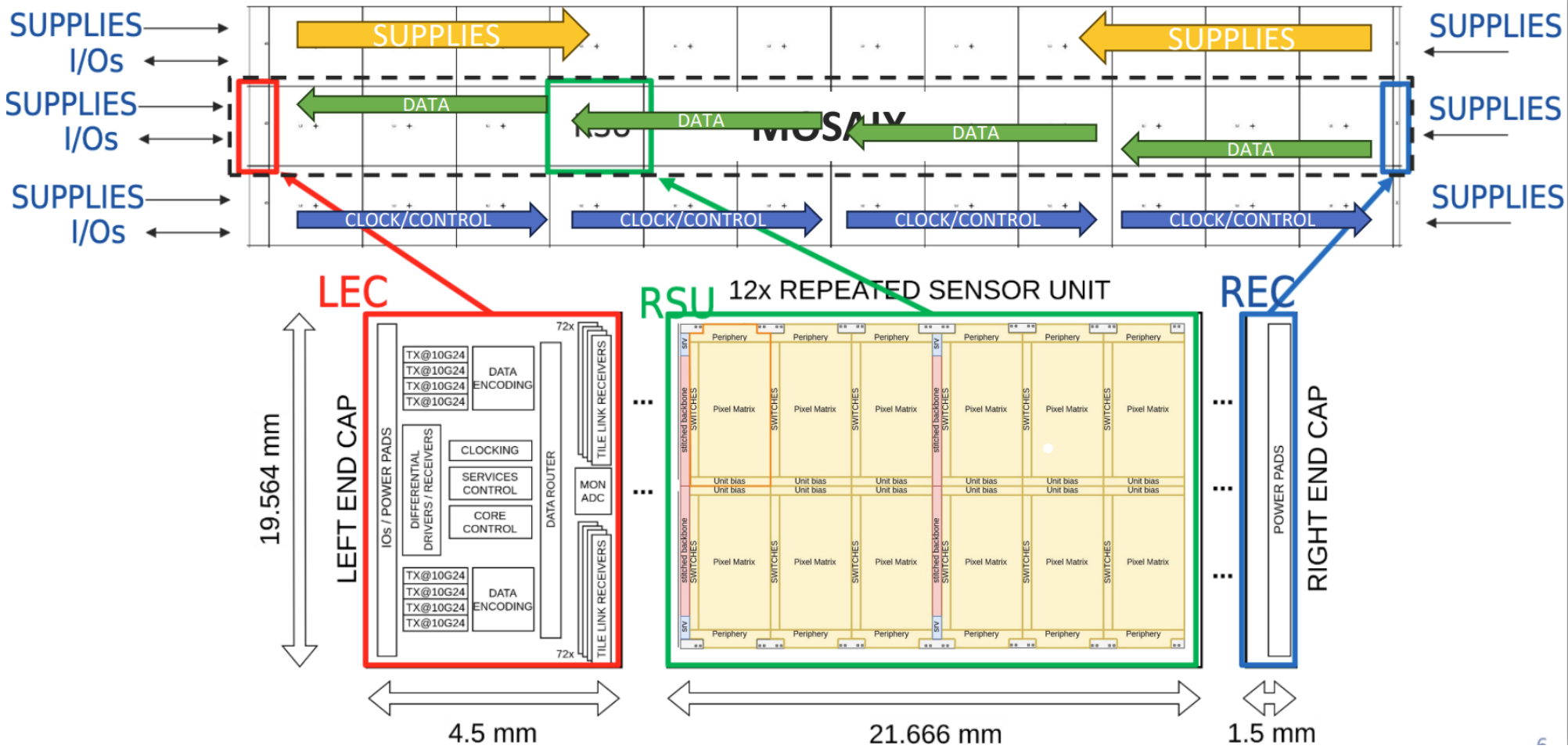
# MOSAIX detector

- 1D stitching
  - 19 mm x 266 mm
  - Pixel size: 18um x 22.8 um
  - ~10 Mpixels
- Detection efficiency > 99%
- FHR < 0.1 pixel$^{-1}$ s$^{-1}$
- < 40mW/cm$^2$

- Rad-hard
  - $10^{13}$ NIEL (1MeV neq cm$^{-2}$)
  - 10 kGray TID
  - Triple modular redundancy

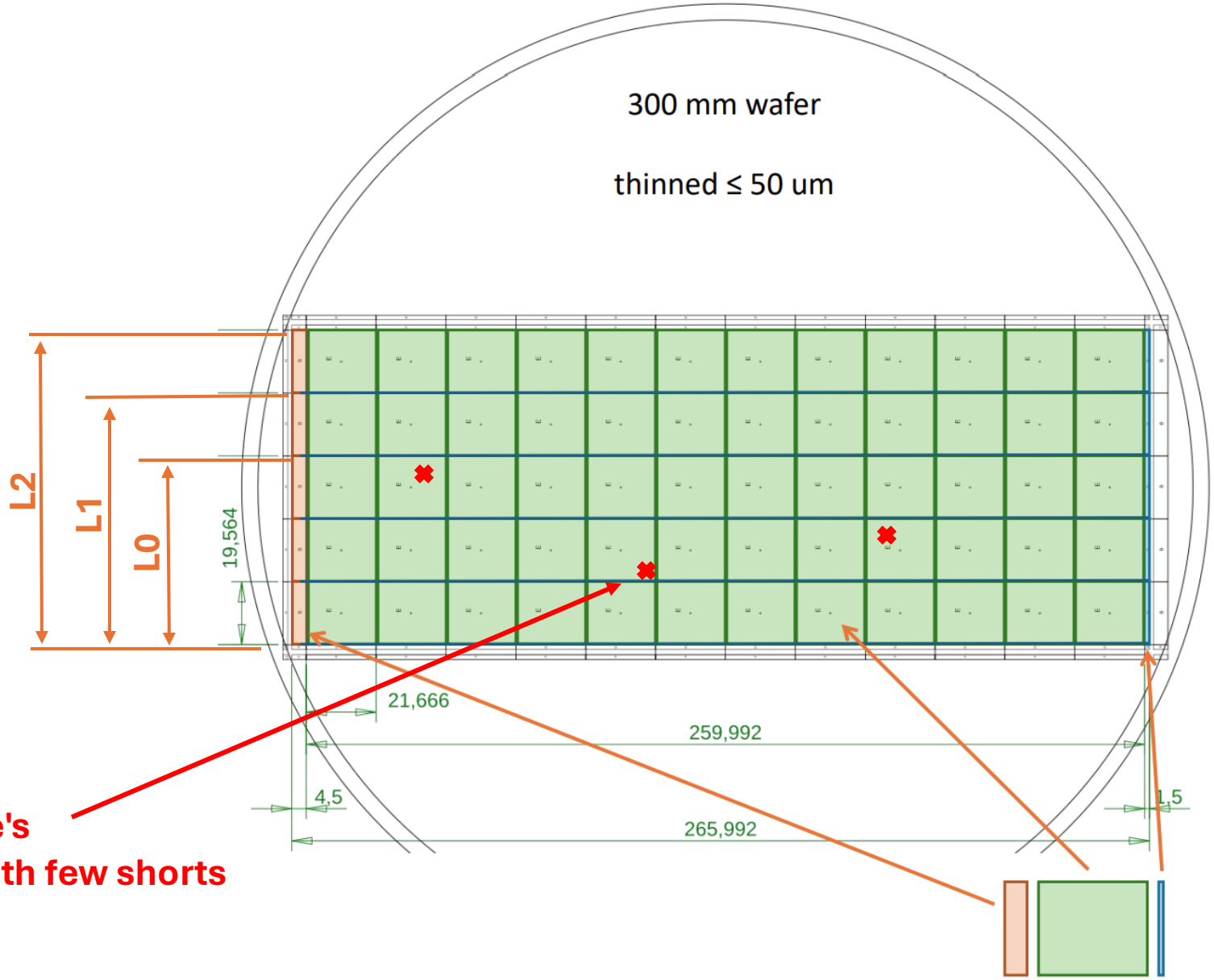
- 2 us integration time
- 4.4 MHz/cm$^2$ particle rate

- **Stave on chip**



# Yield

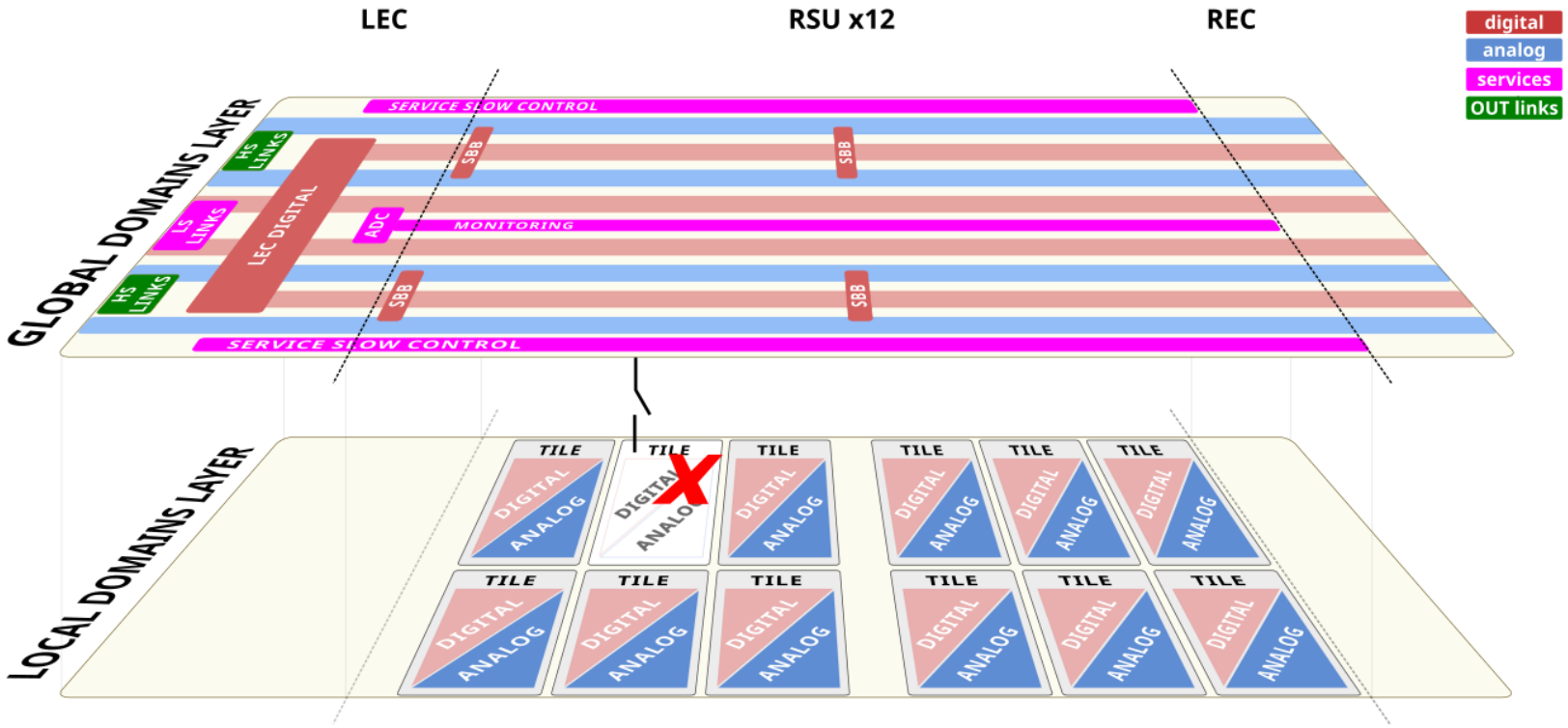
- Alice ITS3 layer: **26 cm x 6-10 cm devices**
- **Yield needs careful assessment!**
- Operation with few defects must be possible
- Shorts probability to be minimized




**Without countermeasure's**
**--> yield gets very low with few shorts**

# Yield: Power planning – power segmentation

- Two powering layers
  - GLOBAL
    - **very robust**
    - supplies only configuration circuitry
  - LOCAL
    - powers most of the chip
    - **segmented** into 144 independent tiles
    - allows **defects isolation**



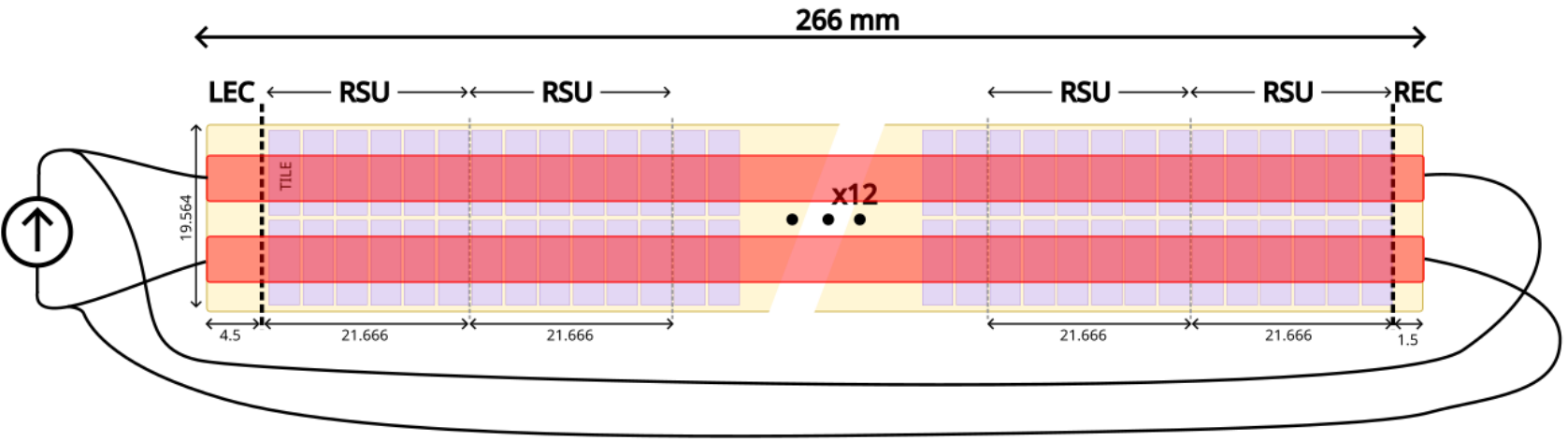

- Safe power-up procedure:
  - Separate services power domain
  - TIle's power for configuration before others supplies are ON

**Defective tile adds 0.7% of dead area, but chip maintains functional!**

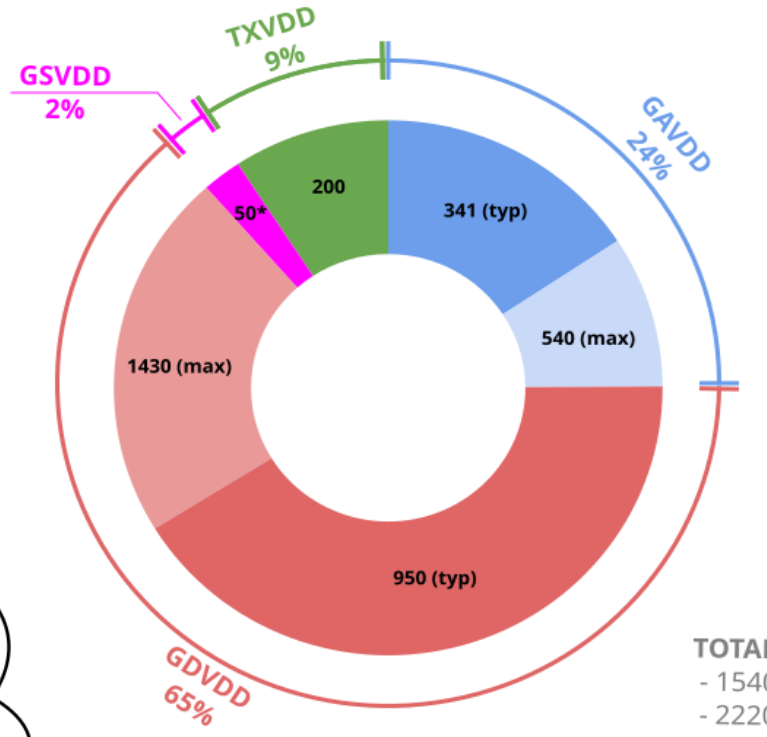
*„Power distribution over the wafer-scale monolithic pixel detector - MOSAIX for ALICE ITS3" by S. Bugiel*

# MOSAIX powering

- **>2 A** via short edge – only 28 supply pads (A+D) on LEC
- **Redistributed on-chip** over the **26 cm**
  - **IR drops** --> challenging despite **<40 mW/cm²**



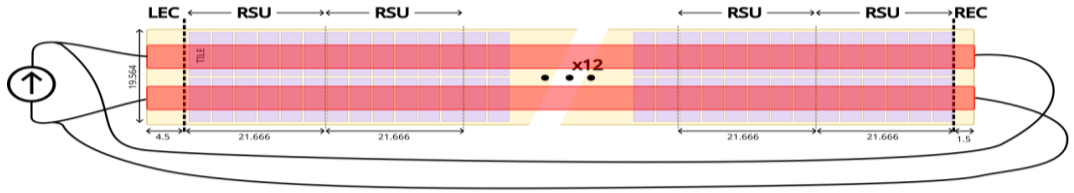

**MOSAIX consumption breakdown**



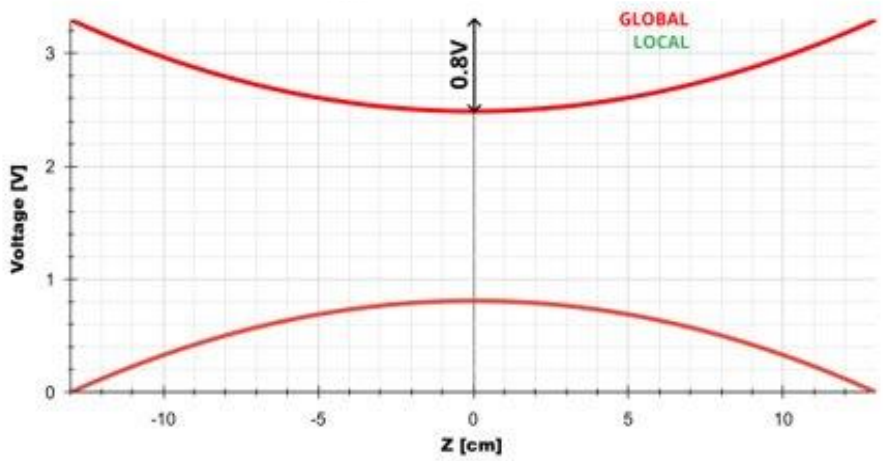

**TOTAL:**
- 1540 mA (typ)
- 2220 mA (max)

**LEC** – Left End-Cap
**RSU** – Repeated Sensor Unit
**REC** – Right End-Cap

# Tiles powering schemes



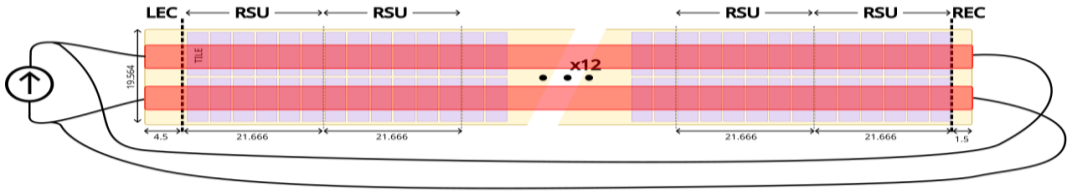

## Initial worst case IR drops estimates




➢ **How to derive local power from the global?**

- Serial powering:
  - \+ reduces IR drops
  - ✗ not an option --> common PSUB

# Tiles powering schemes

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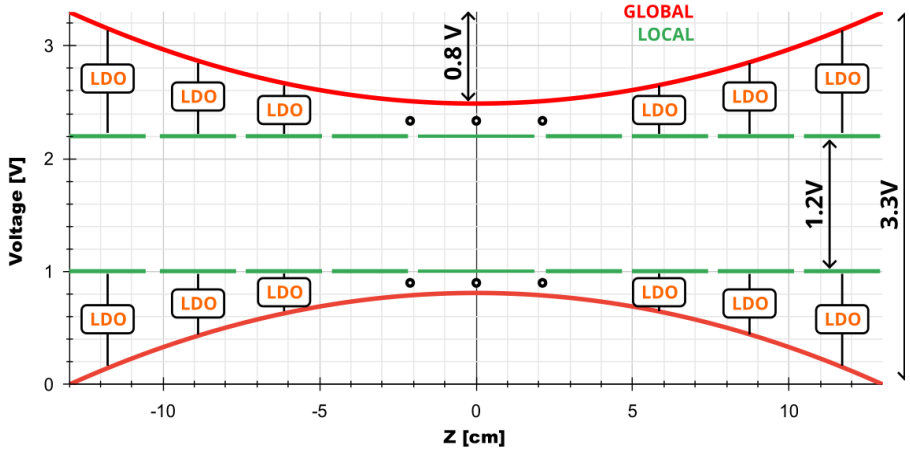
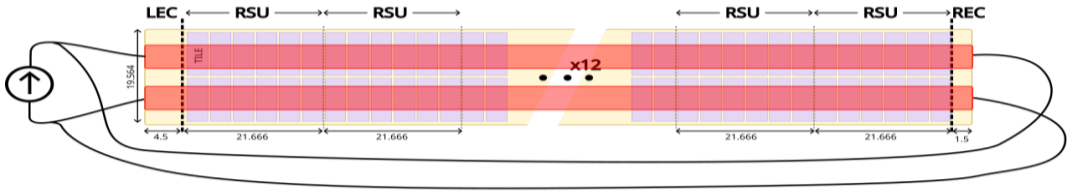



➢ **How to derive local power from the global?**

- Serial powering:
  - \+ reduces IR drops
  - ✗ not an option --> common PSUB
- Per-tile Low-Dropout regulators (LDO):
  - \+ control
  - \+ current stability (shunt LDO)
  - \- needs 3.3 V supply --> power consumption
  - \- dual-rail regulation
  - \- complexity --> dead area
    - ➢ The only choice with up to 800 mV IR drops (per rail!)

# Tiles powering schemes

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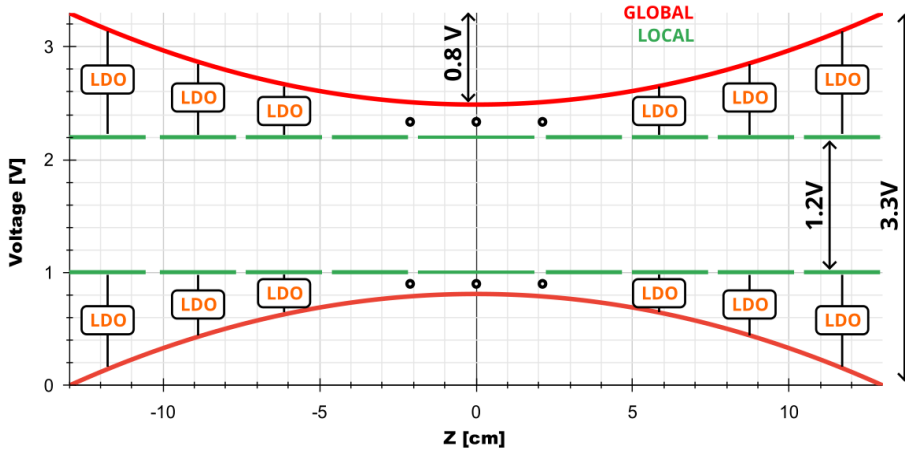
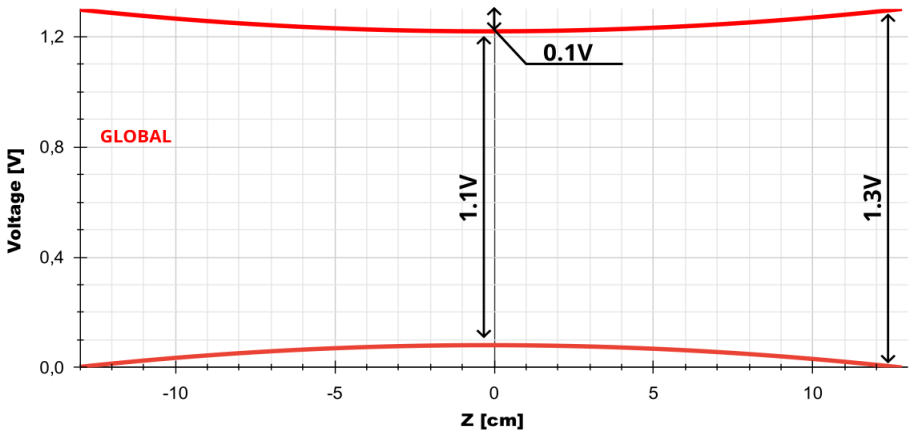


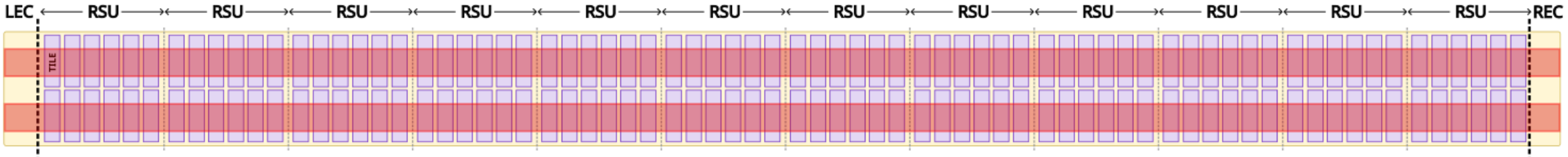

## Worst case IR drops in new metal stack




➢ **How to derive local power from the global?**

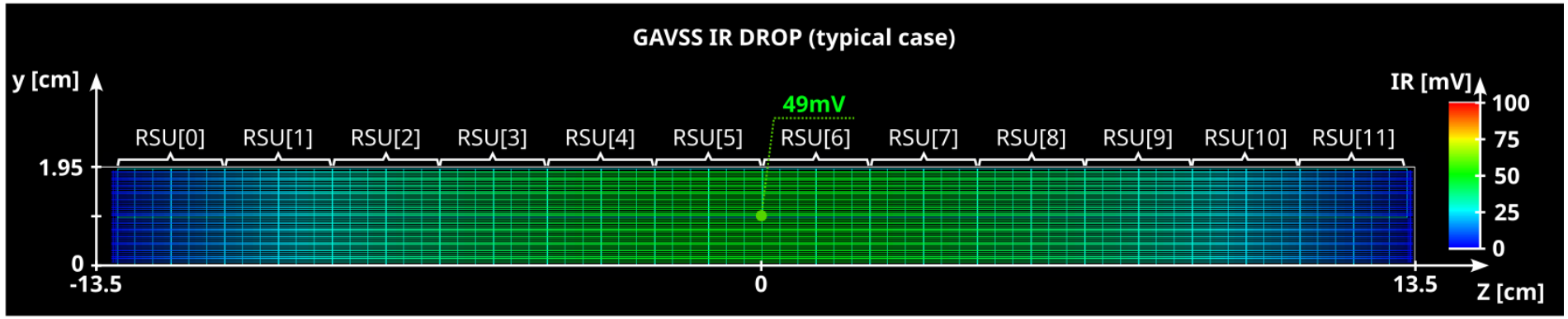
- Serial powering:
  - \+ reduces IR drops
  - ✗ not an option --> common PSUB
- Per-tile Low-Dropout regulators (LDO):
  - \+ control
  - \+ current stability (shunt LDO)
  - \- needs 3.3 V supply --> power consumption
  - \- dual-rail regulation
  - \- complexity --> dead area
    - ➢ The only choice with up to 800 mV IR drops (per rail!)
- Power switches:
  - \+ simplicity --> least area
  - \+ power-efficient
  - \- no control
  - \- tiles operate at different supplies
    **--> [1.2V +/- 10%] operation margins**

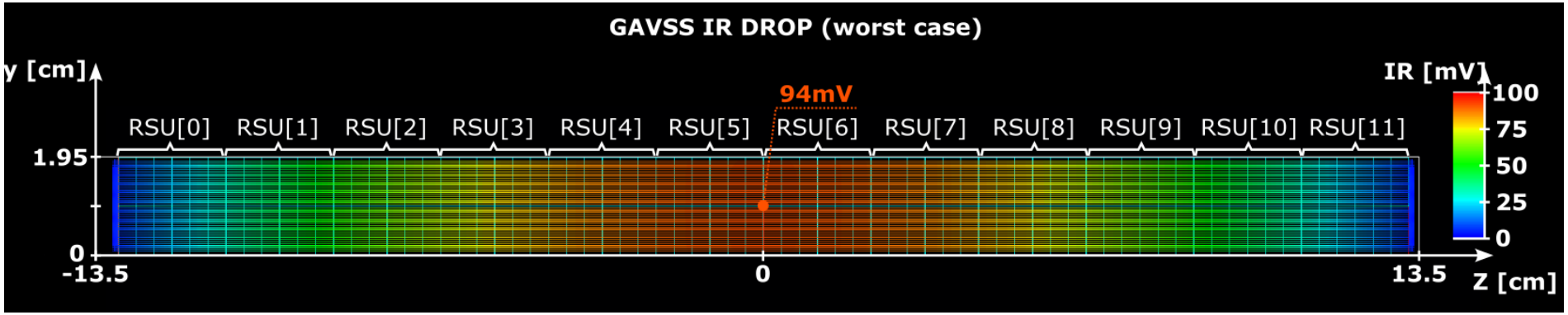
# Global power grid simulation



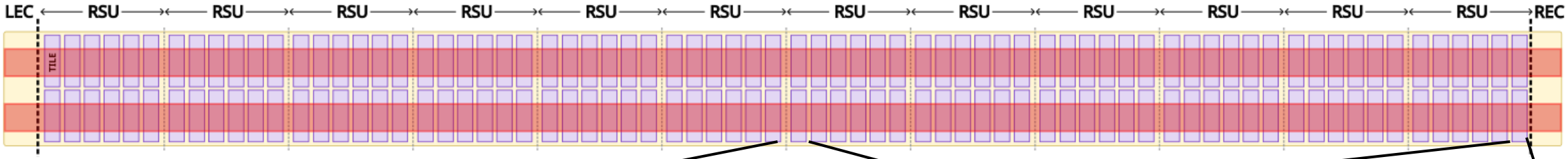

## Results

- **Simulation results matching preliminary predictions**
  --> within specs
- **Analog domain**
  - typical: **50mV** max IR drop
  - worst: **90mV**
    (high consumption, worst RC)
- **Digital domain**
  - typical: **50mV** max IR drop
  - worst: **80mV**



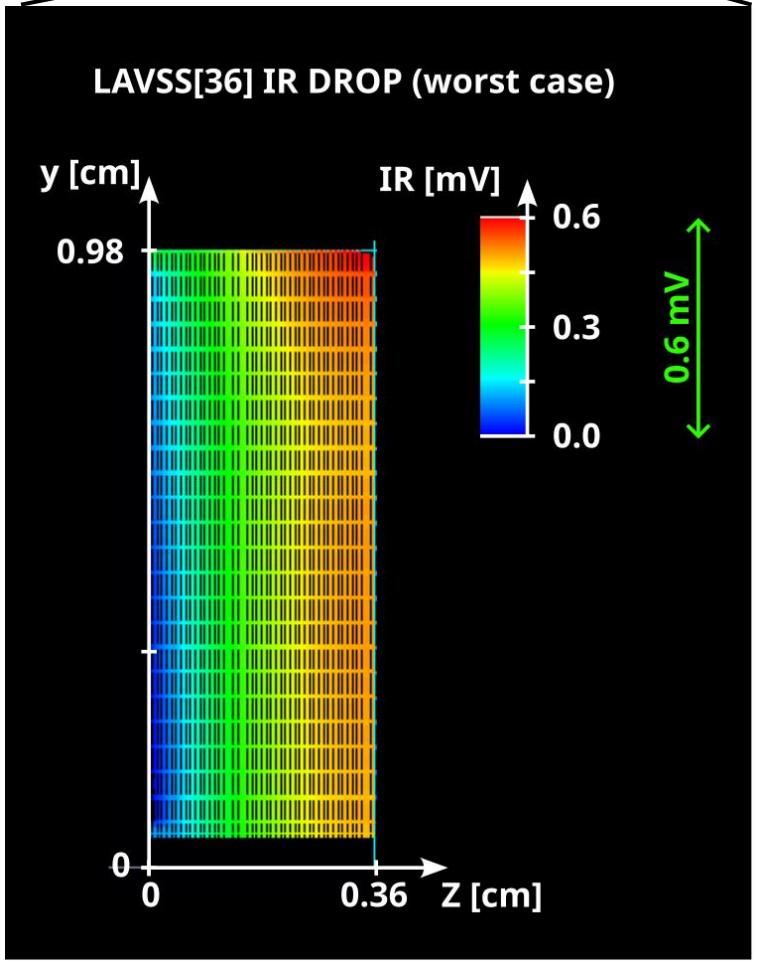
# Local power grid simulation

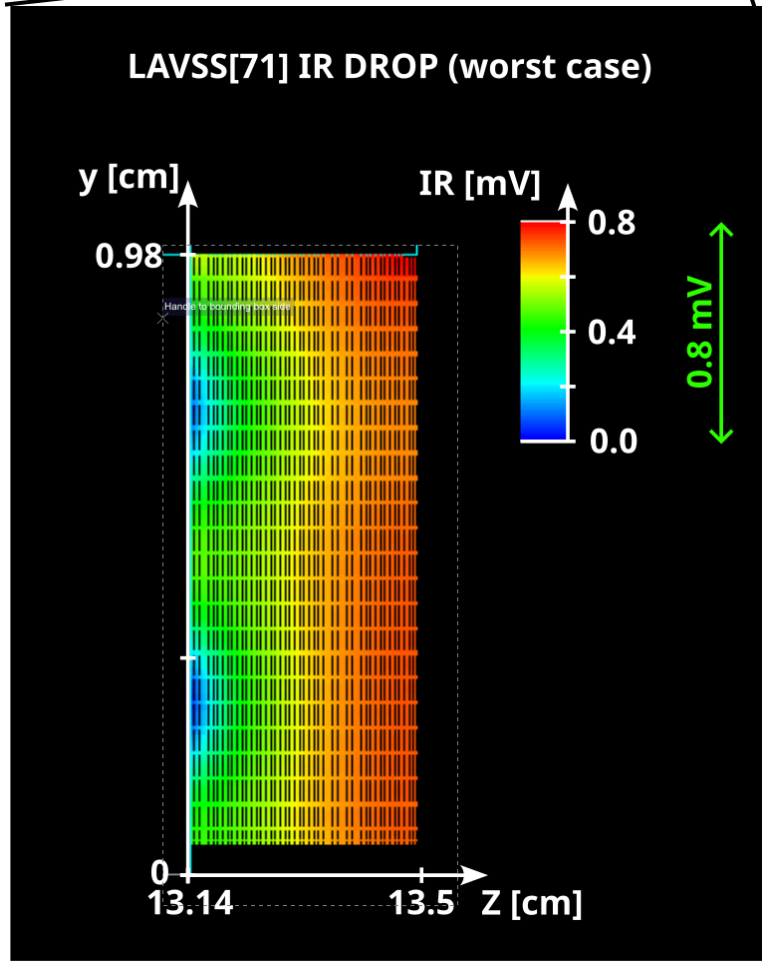



## Results

- **Analog domain**
  - excellent uniformity ( < 1 mV spreads)
  - minor impact of global grid (fan-in into pads)

- **Digital domain**
  - good uniformity ( < 1 - 4 mV spreads)
  - some impact of global grid visible (pads locations)




GAVSS pads

# Summary

- **MLR1 test structures qualified the TPSCo 65nm technology for the HEP applications**
  - DPTS: 99% detection efficiency at $10^{15}$ NIEL, 27 *C
  - transistors radiation hardness comparable to the other 65nm nodes
  - <100 ns timing resolution
  - MIP MPV ~600 e-

- **First stitched chip prototypes (MOSS, MOST) fabricated and being tested**
  - both functional
  - validated the feasibility of wafer-scale detector
  - yield require careful assessment

- **MOSAIX now in an advanced design stage**
  - full-scale, fully-functional ALICE ITS3 prototype
  - stave on chip
  - power segmentation introduced to cope with yield
  - power consumption limited by the power distribution not by cooling

# Thank you!

# Backup

# Off-chip power delivery

- Padring:
  - up to 20 mV drop over standard power IO`s
    --> redesigned to increase conductivity towards the core
    --> 4x improvement

- Off-chip powering:
  - up to 20 mV drop on wire bonds
    --> customizes bond pads
    --> 2x improvement
  - 15mV/rail cabling to C side
  - Settling accuracy: ~15 mV

- With all the improvements we are just within specs!