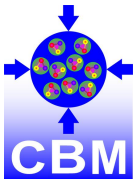

COMPRESSED BARYONIC MATTER EXPERIMENT

CBM-TN-20nnn
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The Front-end Electronic for CBM-ToF

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Abstract

The scope of this Technical Note is the description of the complete front-end electronic (FEE) chain for the CBM TOF Readout System. It is the base for the front-end electronic PRR.

The TN includes the description of the pre-amplifier and discriminator FEE with the custom made PADI-XI ASIC, the time to digital converter board with the custom made GET4 2.0 ASIC (GSI event driven TDC with 4 channel) and the GBTx based readout board. Further more the obtained results from various test systems and the QA procedure will be discussed.

Contents

1 Introduction

This Technical Note describes the front-end electronic (FEE) to be used in the CBM Time of Flight system (TOF). It will be the basis for the TOF FEE PRR.

Relevant topics that should be addressed:

- Type of used FEE
- Functionality and performance of the FEE
- Achieved results with the FEE

The CBM TOF system [1] consists of the TOF wall delivering the stop time of the through-going charged particles. The start time is delivered by a diamond start counter belonging to the BMON subsystem (BMON electronics is part of a different PRR). The TOF wall relies on Multi-gap Resistive Plate Chambers (MRPCs) with different granularity's depending on their position in the wall. All MRPC types have 32 readout strips which are read out on both ends. The TOF wall is subdivided into an inner and an outer wall. They face a different mechanical design. The outer wall consists of 218 modules housing 5 MRPC with 64 channels each. The inner wall comprises 12 modules with 316 MRPCs in total. Further details can be seen in [1]. In total the CBM TOF Wall will have $\approx 90,000$ readout channels.
Due to the different design configurations of the inner and outer wall enforced by the much higher channel density for the inner wall it was natural to develop two types of FEE configurations called inner wall FEE and outer wall FEE (see section 3 and 4). The backbone for both FEE versions are the pre-amplifier and discriminator ASIC named PADI XI [2] in conjunction with the time to digital converter (TDC) ASIC called GET4 2.0 [3, 4] (see TN "The Front-end ASICs for CBM-ToF"). All FEE components were developed in the the Experiment Electronic department at GSI.

2 The CBM TOF Readout Concept

A sketch of the CBM TOF readout is presented in Fig. 1. All electronic components located in the cave are part of this PRR, the part depicted to the right of the dashed line in Fig. 1 is covered in the Online-system TDR.

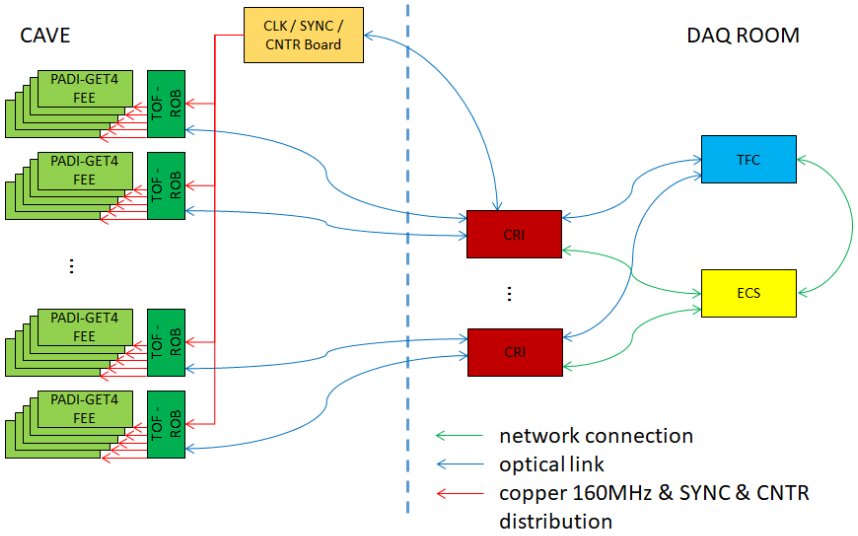

Figure 1: Simplified sketch of the CBM TOF readout system

The CBM experiment aims for a free-running DAQ system. The readout concept is adopted to the need to read out both sides of MRPC units comprising 32 readout strips. The raw MRPC signals are amplified and discriminated by the PADI ASIC which generates LVDS signals where the raw time over threshold information is reflected in the LVDS signal width. The LVDS signals are sent to the TDCs (GET4 ASIC) where they are digitized in 32 bit words. The GET4 ASIC digitize all incoming pulses. The data of several TDCs are collected by the GBTx ASIC [5] and further transmitted via optical fibers to the **C**ommon **R**eadout **I**nterface board (CRI). The synchronicity of the entire CBM DAQ system is guaranteed by the TFC system, which provides the clock and the time information to the CRIs. One dedicated optical link is used to transmit the clock and timing information from the DAQ room down to the CBM Cave. A dedicated board recovers the clock signal and transmits it to a copper based clock distribution tree before it terminates on the TDCs. A highly stable clock is required to guarantee a faultless communication between the GET4 ASIC, running on the clock tree, and the GBTx ASIC, which receives the clock from the connected CRI.
Since each and every incoming signal will be digitized by the TDC it is of upmost importance to have a adequate impedance matching between detector and FEE in order to suppress any reflections. In CBM TOF the imput impedance of the pre-amplifier is adjustable to cope with the impedance if 50Ω differential for the outer wall MRPCs and 100Ω differential for the inner wall detectors.
The main driving requirement is a system time resolution better than 80 ps for the full surface of the CBM TOF Wall.

3 The Inner Wall FEE

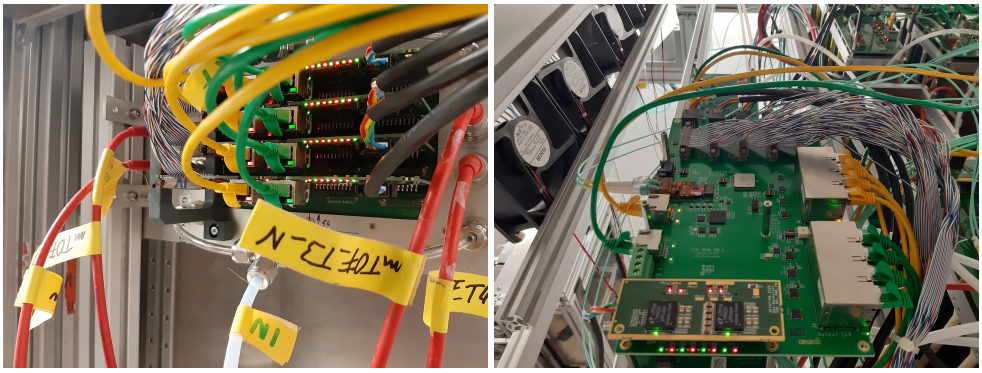

Figure 2: Inner Wall FEE Prototypes used in mCBM

Due to the high channel density the raw MRPC signals are transmitted via twisted pair cables inside the module box to the back side of the module where a PCB with proper connectors serves as a signal feed-through. On the outer side of the PCB connectors allow a direct connection of the signals to the inner wall PADI-GET4 FEE PCB (cf. left side of Fig 2). The 32 bit long data words generated by the PADI-GET4 FEE in LVDS standard are transmitted via twisted pair cable of upmost 2 m length to the inner wall readout board (TOF-iROB). The TOF-iROB, housing a GBTx concentrator ASIC, aggregates the data from five PADI-GET4 FEE boards (40 e-links in total). Furthermore the TOF-iROB provides the necessary low voltage power-lines and the clock and control signals for each of the connected PADI-GET4 FEE.

3.1 Inner Wall PADI-GET4 FEE

Figure 3 depicts the current prototype for the inner wall. Here both ASICs, PADI XI and GET4-2.0, are equipped on the same PCB. The male pin header connects the PADI-GET4 FEE to the feed through PCB of the MRPC box. On the opposing side the following connections are visible starting from left to right: power (+3,5 V, +2,7 V, +2 V and GND), clock and control signals (2 × RJ45 connectors) and

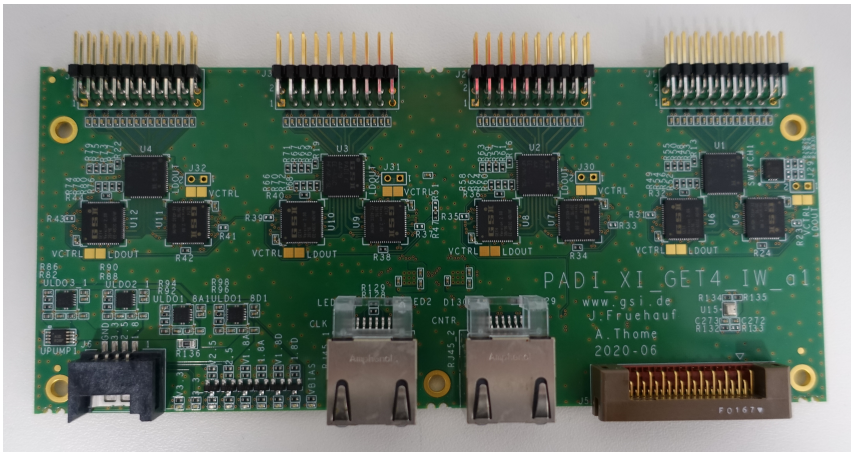

Figure 3: Picture of the inner wall front end electronic

the connector for the data cable (KEL40). For monitoring, several LEDs indicate the power status. This board will be produced and equipped in China at Central China Normal University (CCNU).

3.2 Inner Wall Readout PCB (TOF-iROB)

The TOF-iROB has two applications. The major use case is to collect the data from up to 5 inner wall PADI-GET4 FEE PCBs. However, the TOF-iROB can and will be used to generate a 160 MHz clock signal (needed for the GET4 TDC) and a periodically distributed signal (called SYNC signal, necessary for synchronisation of all GET4 ASICs and to the other subsystems) out of the received and decoded information from the TFC System. Both use cases are discussed in more detail in the following subsections. The TOF-iROB boards will be produced in Germany.

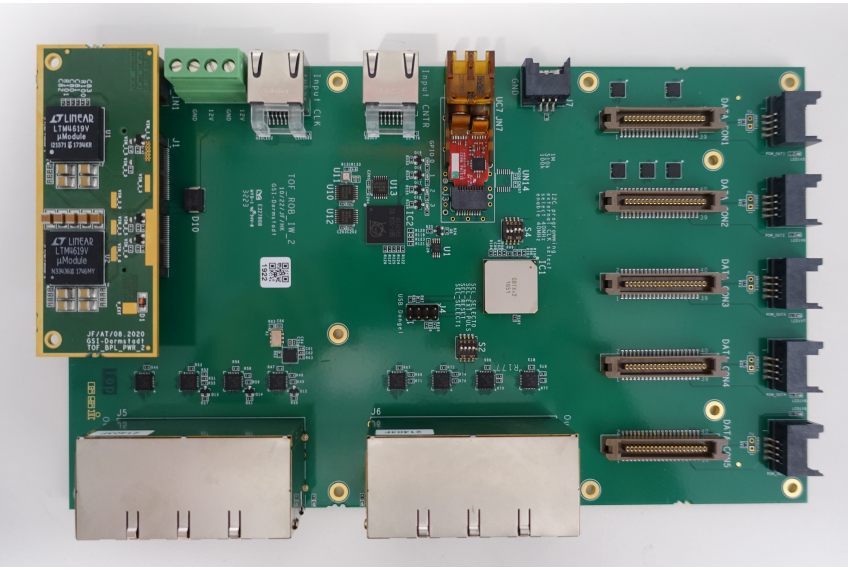

Figure 4: Picture of the inner wall readout baord (TOF-iROB)

3.2.1 TOF-iROB as readout board

The TOF-iROB hosts the GBTx concentrator ASIC and a radiation hard optical transceiver (VTRx) to interconnect the PADI-GET4 FEE with the readout electronic in the DAQ room. The board is supplied by an external +12 V source and generates on an addon PCB (see Fig. 4 left side) the needed low voltages (+1,6V, +2 V, +2.7 V, +3.5 V) for the board itself and for the connected PADI-GET4 FEE boards. Each

PCB has two RJ45 input connectors (Fig. 4 top side). One for the 160 MHz clock and SYNC signal and one for the so called control link where an external pulser signal can be selected and send towards the FEE. Each of the signal paths from the RJ45 connector is multiplied and distributed further towards the FEE that connect to the RJ45 jacks on the lower edge of the Fig. 4.

3.2.2 TOF-iROB as clock master

The TOF-iROB can be configured to provide the 160MHz clock for the GET4-TDCs and to transmit the SYNC signal via a deterministic e-link from the GBTx. Since the GBTx ASIC recovers 160 MHz clock from the optical link, it is phase locked to the CBM clock which is distributed by the TFC system. From here a cooper tree, based on CAT6 cables, will serve the full CBM TOF Wall with these signals. Dedicated fan-out boards as shown in Figure 5 are used for serving all endpoints. It is essential to distribute the clock from a single clock source in a star like fashion towards all TDCs in order to keep the required precision between them. We aim for a clock distribution system with a jitter better than 10 ps inside the cave. Furthermore, it is possible to send a pulse signal, the required control signals and a reset signal via additional e-links.

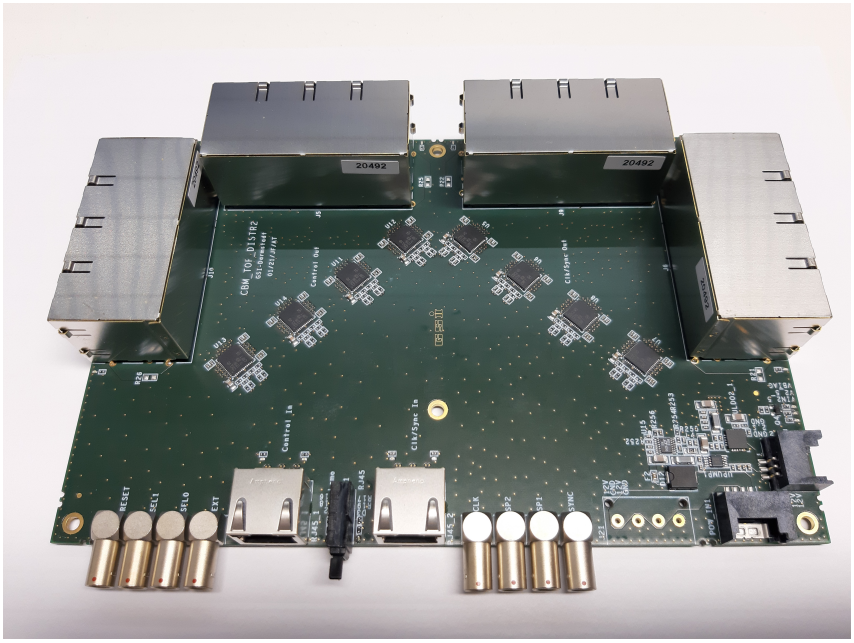

Figure 5: Picture of the clock distribution pcb

On the clock distribution board (Fig. 5) all 4 differential pairs of the two RJ45 Inputs are copied 16 times.

4 The Outer Wall FEE

For the modules located in the outer part of the TOF wall the PADI-FEE PCB will be connected directly to the MRPC inside the gas tight box. The discriminated signals from PADI, the digital LVDS output signals, are transmitted via twisted pair cables to one side wall of the module box. Here two feed through PCBs (FT-OW), having connectors on both sides, serve as an interface to the GET4 TDC. Outside the detector housing, 5 TDC-PCBs are directly attached to each FT-OW. A crate-like frame with proper guidance keeps the PCBs in position and gives them mechanical stability. The same group of 5 TDC-PCBs is connected on the opposite side of the feed trough directly to the readout PCB (TOF-oROB) which houses the GBTx ASIC. Figure 6 shows the arrangement of the various PCBs. The TOF-oROB is interconnected via optical transceiver with the CRI. The needed supply voltages (+1,6V, +2 V, +2.7

V, +3.5 V) are generated at an addon card sitting on the TOF-oROB and routed through each PCB up to their destination.

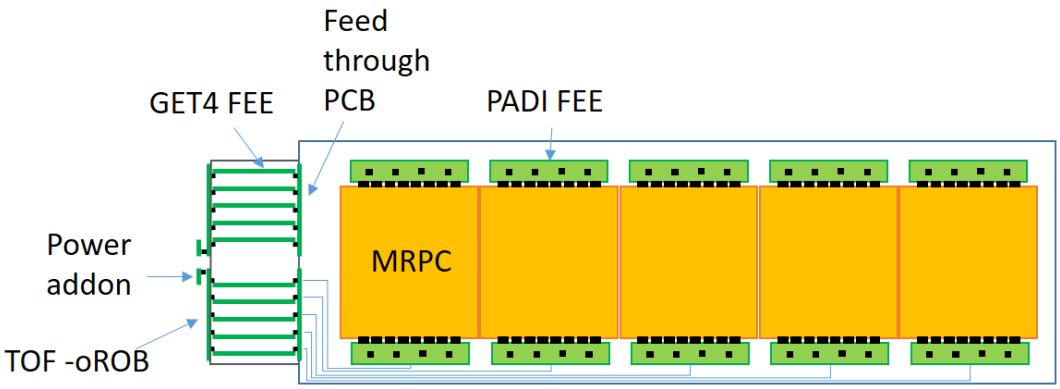

Figure 6: Sketch of the outer wall module visualizing all used PCBs

4.1 Outer Wall PADI FEE

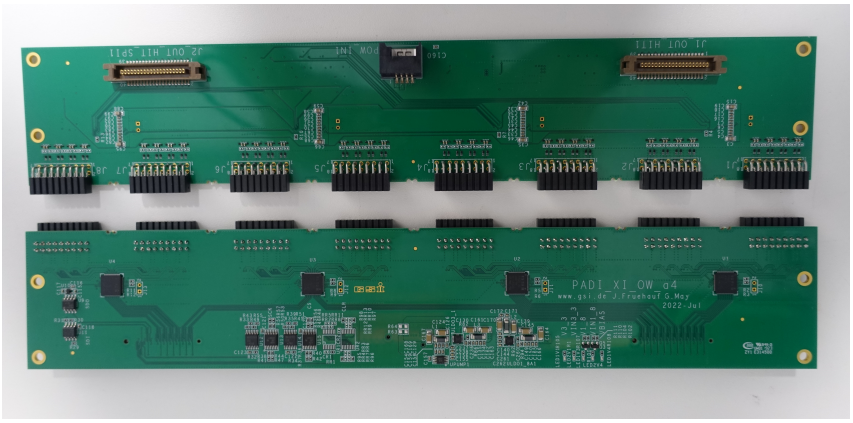

Figure 7: PADI FEE top and bottom view

The outer wall PADI FEE has female connectors for direct connection to the Detector. According to the 32 readout strips the FEE has 32 channels distributed to 4 PADI XI ASICs. The discriminated signals are transmitted via twisted pair cables towards the Feed Through PCB. For threshold setting purpose the PADI has a SPI slave implemented. The SPI data is chained over the 4 PADI ASICs while the other SPI signals are distributed in a star arrangement. The PCB has two power inputs to optimize the voltage drop for the two needed low voltage regulators (LDO). Each input stage of the PADI is protected with two ESD protection diodes with an additional resistor in series in between, to prevent a damage on the ASIC in case of over-current from the detector. The schematics of this protection schema is illustrated in figure 8.

4.2 Feed Trough PCB

The Feed Through PCB (Figure 9) has two tasks. The first task is to interconnect all PADI signals and service lines with the TDC. The second task is to keep the gas box gas tight. The PCB has on the side facing the box interior cable connectors for LV cable and data cable in order to serve five PADI FEEs. On the outer side 5 connectors for direct connection of the GET4 FEE are placed. In order to guaranty the gas tightness all holes are plugged or blind holes. A ring shape metal surface acts as a counterpart for the O-ring.

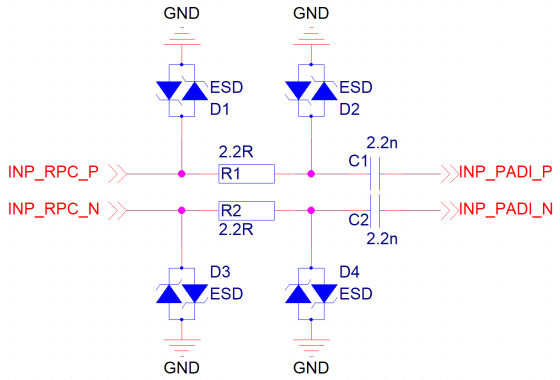

Figure 8: PADI input protection

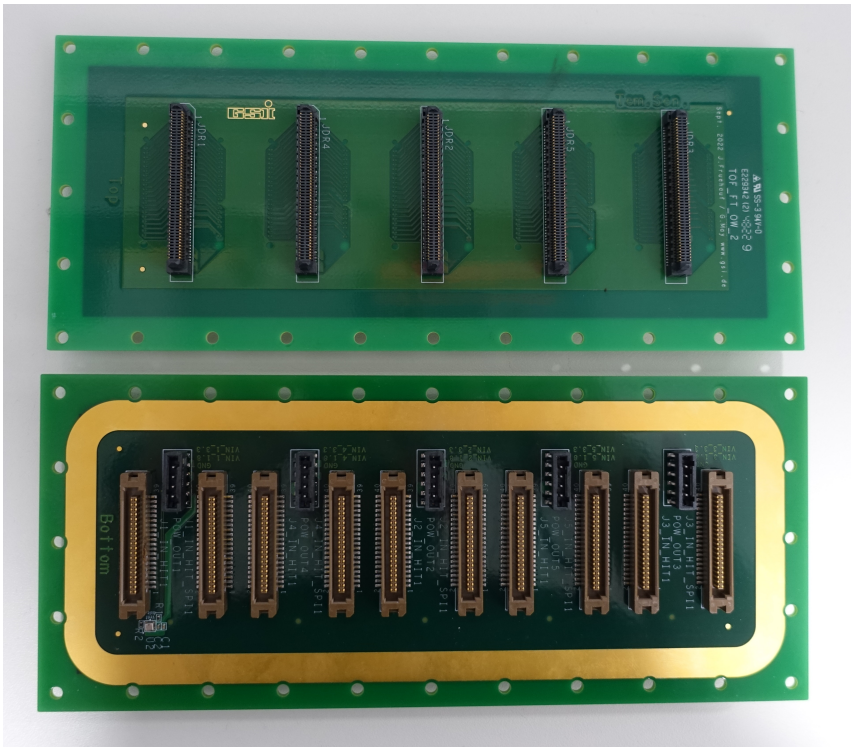

Figure 9: Feed Through PCB. Top: side facing the outer side of the gas box. Bottom: side facing the inner side of the gas box.

4.3 Outer Wall GET4 FEE

The GET4 FEE is designed to allow a direct connection on one side to the feed through pcb and on it's other side to the readout pcb. It hosts 8 GET4 2.0 ASICs in order to readout 32 PADI channels. One of the GET4 ASICs acts in addition as SPI Master for the connected PADI FEE. On board low drop low voltage regulators generate a clean power for the ASICs and for the clock and sync distribution system. Via an externally controlled switch one of the 32 inputs is connected to an external signal source. This allows to inject an external pulser signal besides the MRPC signals. With injecting this external signal the synchronicity and time jitter of the FEE over the full TOF wall can be measured.
In the latest version, the connector type on both sides of the board is changed to a variant with a lager pin pitch since connectivity issues in the previous version were observed.

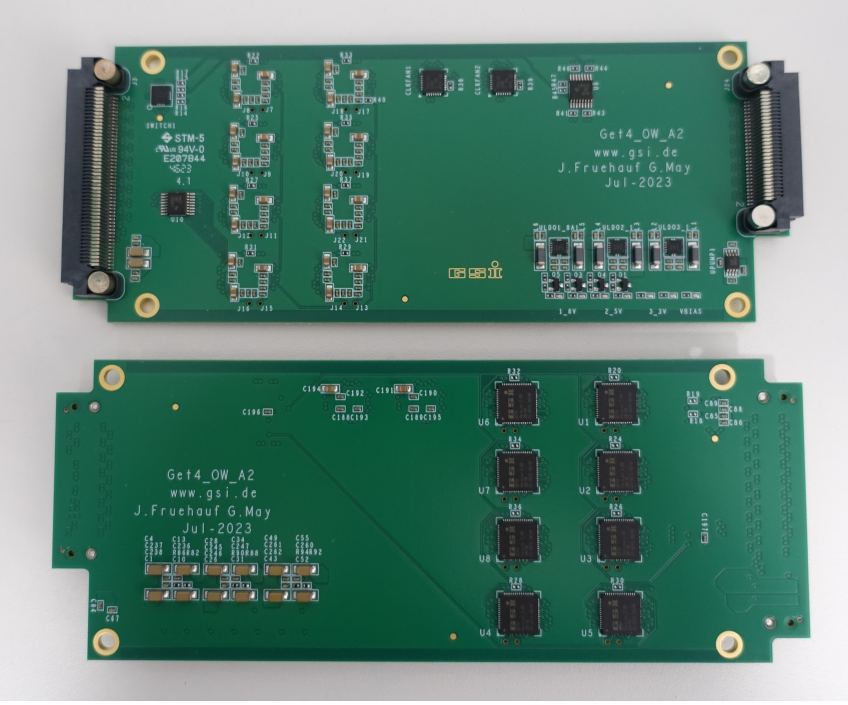

Figure 10: GET4 FEE top and bottom view

4.4 Outer Wall Readout PCB (TOF-oROB)

The outer wall readout PCB (TOF-oROB) is in it's functionality similar to the TOF-iROB. In contrast to the inner wall design the ToF-oROB-PCB features on one side the counterpart connectors of the GET4 FEE. Via this connection not only the LVDS lines for the GET4-TDCs but also all needed lv-power lines for the TDC- and PADI-boards are routed. 5 TDC-PCBs can be read out with one TOF-oROB, filling up all 40 links of the GBTx. TOF-iROB and TOF-oROB share the same power addon PCB design (compare Fig. 4 with Fig. 11). Each outer wall module is read out by two TOF-oROBs.
Due to not enough available VTRx modules the final version of the TOF-oROB will be equipped with SFP+ optical transceivers for the connection to the CRI instead. The radiation level on the outer wall modules dropped to moderate value and we do not see a substantial risks in using non radiation hard SFP+ at this location.
A further component where the quantity is not enough to equip all PCBs is the slow control ASIC SCA. The SCA ASIC reads and provides the information of the on board voltages and the environmental parameters (temperature, pressure and humidity) from BOSCH sensors which are installed on the inside of the feed-through PCB and on the TOF-oROB PCB itself. In addition, the SCA steers a dip switch where can be selected to use the foreseen external clock (as described above) or a locally generated TDC clock by the GBTx. In general the external clock is supposed to have a lower jitter over the full TOF wall compared to the locally generated clock (called internal clock) and is therefore the preferred and selected solution. However, to have the possibility to switch to the internal clock allows for more flexibility and redundancy and comes almost for free. Since the SCA offers enough resources to serve two TOF-oROBs only one TOF-oROB PCB per module will carry the SCA, acting as master. The slave oROB is interconnected via cable to the master.

4.5 Rate capability

The rate capability of the GET4 ASIC depends on the adjusted readout speed.

For the TOF system the 80 MBit readout is sufficient. With this readout speed it is possible to use all 40 connections on the GBTx ASIC. Furthermore it fits to the maximum simulated chip level hit rate of $\approx$

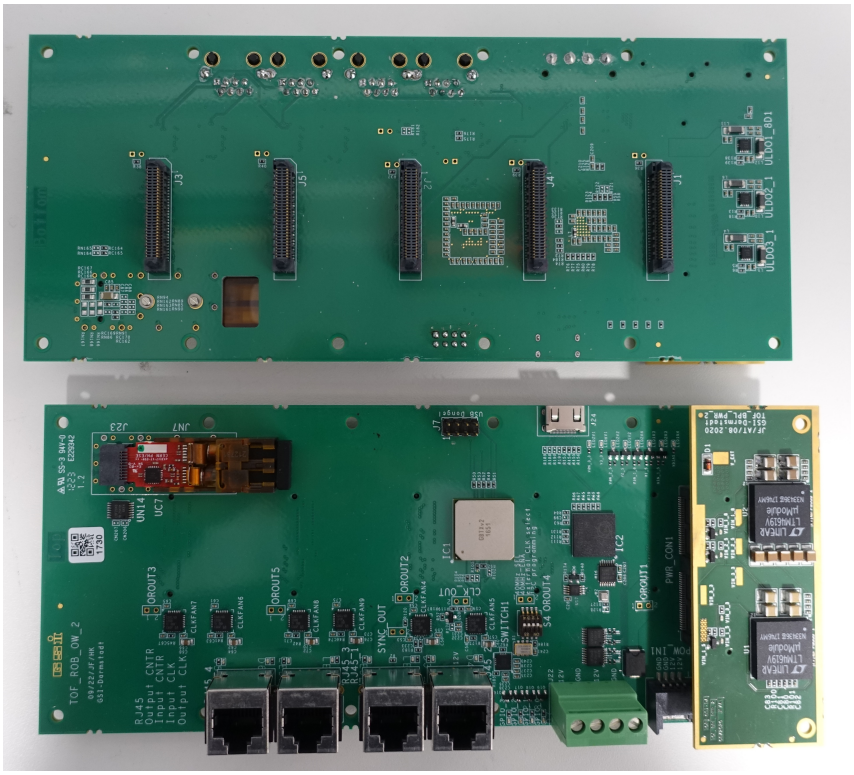

Figure 11: TOF-oROB top and bottom view

Configuration	Readout speed	Hit rate capability
100	40 MBits/s	0.9 MHits/s
101	80 MBits/s	1.8 MHits/s
110	160 MBits/s	3.6 MHits/s
111	320 MBits/s	7.2 MHits/s
double link	640MBits/s	13.2 MHits/s

Table 1: Hit rate capability in conjunction of adjusted readout speed.

1.3 MHz and still provides about 30 % safety margin.

5 Experience

The PADI-GET4 readout-chain is used and has been tested at various places with different MRPC types and different conditions.
1) A read out test stand installed at the electronic department at GSI operated with pulser in order to test basic functionalities and perform quality assurance of the newly produced FEE boards.
2) A permanent cosmic test stand for MRPCs operated at the ”Physikalisches Institute Heidelberg” comprising several test modules. Here it is possible to inspect the MRPC performance as well as the performance of the FEE with real detector signals at low rates.
3) A permanent installation of several full size TOF modules at mCBM in the scope of the FAIR Phase 0 Program at GSI in order to test counter and readout under realistic CBM conditions.
4) a fourth opportunity to gain experience with the readout ASICs is a long term operation of the endcap TOF detector (eTOF) installed at the STAR experiment at Brookhaven National Laboratory (BNL) as well within the FAIR Phase 0 Program. eTOF comprises 36 CBM TOF modules (108 MRPC counters) arranged in wheel-like structure which is mounted on the east side end-cap of the magnet at STAR.

5.1 Laboratory Test Stand

A permanent pulser test stand is available at the laboratory of the EE department at GSI. Here it is possible to inspect the response of the PADI ASIC exposed to pulses which can be variate in amplitude, shape and frequency. The output signals of PADI can be investigated via oscilloscope or with injecting the output signal into the GET4 TDC with the full data chain behind. With the GO4 analysis framework the time spectra between different channels the time over threshold spectra of all channels can be inspected. This test stand will be used for quality assurance of newly produced PCBs. Experience from FEE production for the STAR experiment showed very promising results regarding yield of the FEE PCBs, which is listed in table 2.

PCB	number of produced PCB	yield
PADI FEE	300	99 %
GET4 FEE	300	97 %
Feed Through PCB	100	100 %
TOF-oROB	100	98 %
Power Add-on	100	100 %

Table 2: Yield of FEE PCBs produced for the STAR Experiment

5.2 Cosmic Stand

The Test setup of the cosmic stand is visualized in Figure 12. It shows 6 MRPCs, grouped in 3 modules, horizontally staggered measuring cosmic tracks in order to determine counter properties as efficiency and time resolution. Figure 13 shows the result of the efficiency measured with this ToF-readout chain for

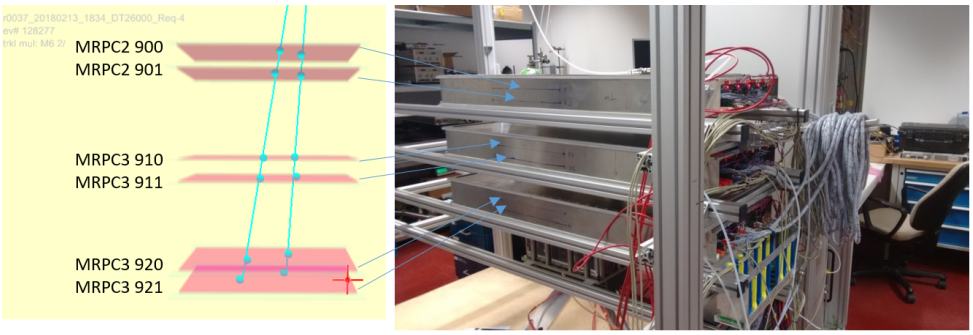

Figure 12: Cosmic test setup. Left: event display showing two multiplicity 6 cosmic tracks in one event. Right: Photograph of the test stand.

the MRPC3 prototype. It reaches about 98 % efficiency while maintaining and a counter time resolution less than 50 ps.

Similar results were obtained for the inner wall counter MRPC1a.

5.3 FAIR Phase 0 Program: mTOF@mCBM

The mTOF setup at the mCBM is arranged in a double and triple stack configuration as shown in Figure 14. The analysis of the counter properties is based on a track analysis as well, this time, however, the particle tracks are generated in a nucleus-nucleus collision.

The mTOF Setup comprises 5 real size modules with 1600 readout channels in total. Sandwiched between the double stack modules test boxes with various counter types were installed, which scales up the number of readout channels to about 2000. The double stack modules act as a reference for the test boxes and allows to investigate the efficiency of the various DUT counters. All beam tests where performed

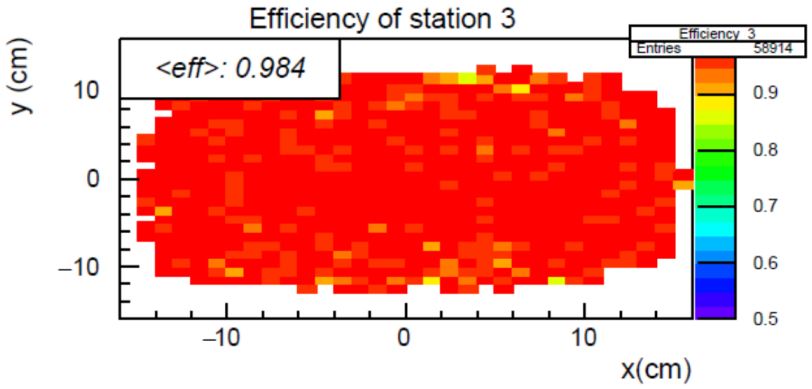

Figure 13: Cosmic stand efficiency

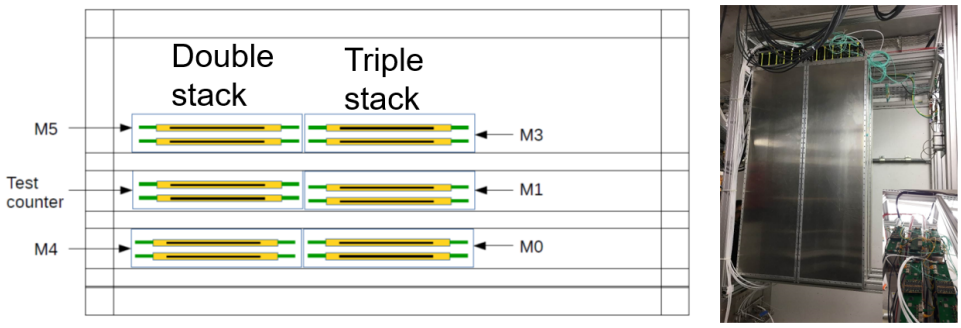

Figure 14: mTOF test setup at mCBM. Left: Sketch of the mTOF setup. Right: Photograph of the mTOF setup.

with counters equipped with PADI X and later on with PADI XI together with the GET4 2.0 TDC. Here we highlight a result obtained with the MRPC2 prototype operated with PADI XI. Fig. 15 shows on the left the efficiency as function of the counter active area. The integral denotes to 97 % efficiency. The time difference between measured time and estimated time calculated from the fitted tracks is depicted on the right of Fig 15. The Gaussian fit applied to the distribution shows a system time resolution of 70 ps. From this value a counter time resolution of less than 50 ps can be deduced including the electronic precision.

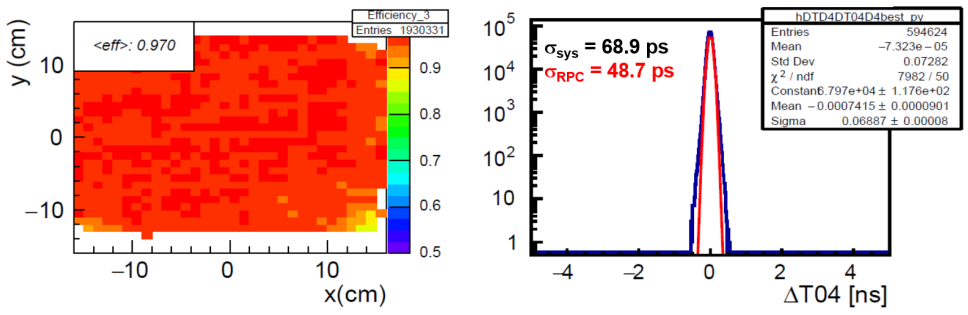

Figure 15: Cosmic teststand

The electronic contribution to the measured resolution is in the order of 30 ps since the single channel electronic resolution is on mean σ_{Fee} = 20 ps and the MRPC signals are readout on both strip ends. Therefore an intrinsic counter time resolution in the order of 40 ps can be declared. This is in the same order as the time resolution of the electronic chain itself.

5.4 FAIR Phase 0 Program: eTOF@STAR

The eTOF detector installed at the STAR experiment at BNL started its operation in 2018 within the scope of the FAIR Phase 0 Program. It compromises 6912 electronic readout channels equipped with PADI-X and GET4 2.0. A picture of the eTOF detector is depicted on the left side of figure 16. The

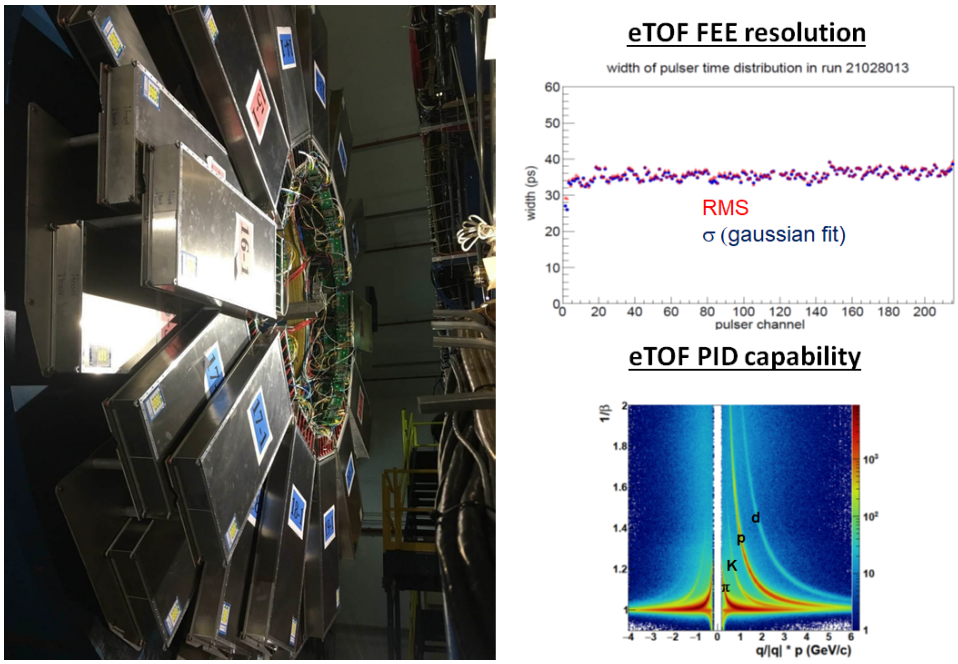

Figure 16: eTof Detector @ STAR Experiment and it's performance

achieved results in terms of test pulser resolution between the FEE cards and the PID capability on the right side demonstrate reliable functionality of the PADI-GET4 solution. This gives confidence for the employment in CBM TOF.

6 Quality Assurance

Table 3 summarises the production location, the total needed amount and current prices for the various boards.

PCB	Location	Produced in	Total amount*	Estimated price**
PADI-GET4 FEE	inner wall	China	700	150 €
TOF-iROB	inner wall	Germany	150	300 €
PADI FEE	outer wall	China	2500	100 €
GET4 FEE	outer wall	China	2500	90 €
Feed Through PCB	outer wall	China	500	160 €
TOF-oROB	outer wall	Germany	500	200 €
Power Add-on	both	China	650	120 €

Table 3: Production location, the total needed amount and estimated price of the different FEE PCB types. * The total amount includes 15 % overhead. ** the price is estimated based on former productions plus an 20 % increase.

The boards which are produced and equipped in China undergo a first optical inspection at CCNU in China. However, the main QA tests are performed at the EE at GSI. The first test is the a power consumption test. When the board shows no noticeable problems the board will be installed in the test setup. At GSI a dedicated test stand was installed and is currently in use to test boards from the pre-productions.

The QA test readout chain is very similar to the final CBM TOF read out chain (cf. Fig. 17). The test is carried out with a pulser signal which is distributed to all input channels. Positive and negative input can be tested individually. The generated data are analyzed via the FAIR ROOT software. Here the time over threshold distribution and the time resolution of each channel are measured and inspected. A general time resolution below 40 ps RMS, including the contributions of the pulser, the clock distribution, the PADI and the GET4 FEE, is considered as accepted. Within the test phase, only one board type will be tested, while the other boards (which passed already the QA) within the chain will stay the same. The test setup allows to test up to 5 boards simultaneously. QA plots (see Fig. 18) will be stored in a database. A second, more general QA test will be performed after installation in modules where the entire module will be tested in a cosmic test stand (subject of module PRR). An exception is the QA of the TOF-iROB and TOF-oROB. They will first be checked regarding power consumption before installing them on the final module. During Module QA all functions (including the slow control part) of the boards will be tested. In case of malfunction of individual boards they can be easily exchanged and inspected in more detail in the EE lab. The feed through PCBs undergo only an optical inspection justified on an excellent experience of the last 150 boards.

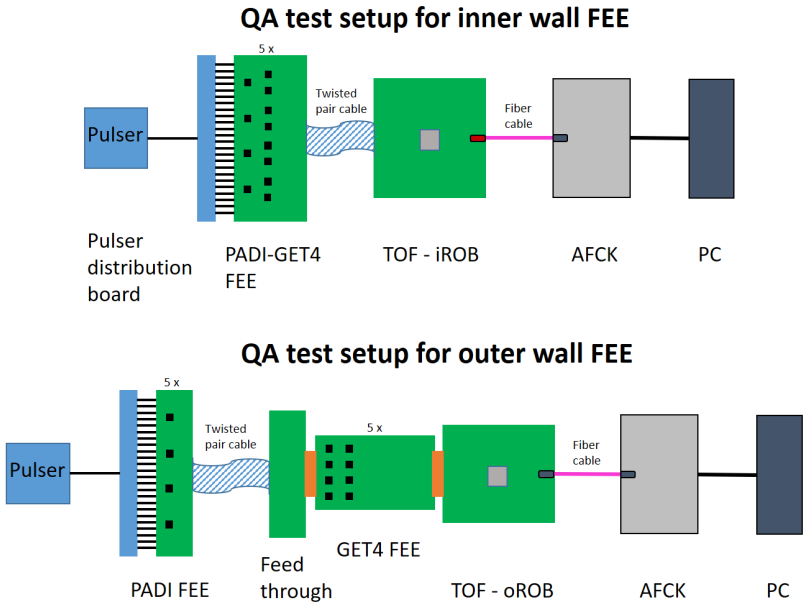

Figure 17: QA test setups: upper - inner wall, lower - outer wall

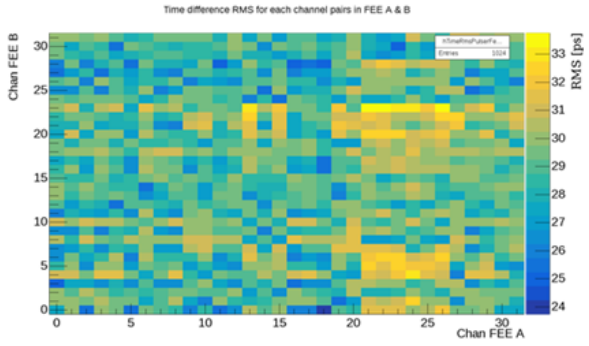

Figure 18: Time resolution plot: RMS of the time difference between all channels of two different PADI boards.

7 Summary

A set of two FEEs for the inner and the outer wall of the CBM TOF System are developed and tested. The obtained results have demonstrated that all required specifications of the CBM TOF System are fulfilled in a satisfactory manner. The reliability has been proven in various test systems. Small modifications have been implemented in the latest FEE versions for better protection and handling of the FEE. We are confident that no further development step is necessary.

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8 Appendix: