Workshop on Silicon Multiplier and Associated Electronics

Activities and results from IFIN-HH

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February 16, SMI Viena

Timing with SIPMs in TOF systems

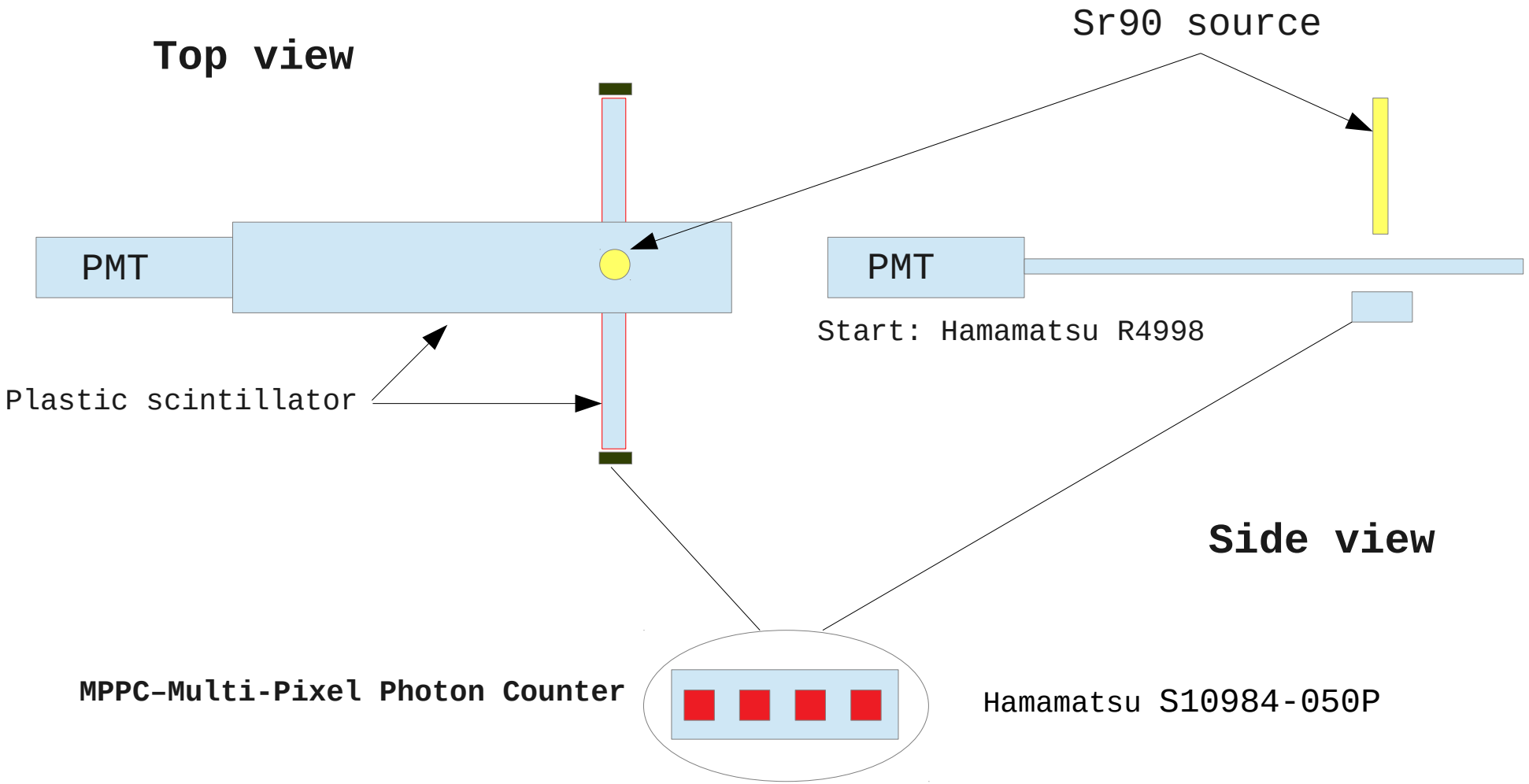
FPGA & TDC system

Digitizer system

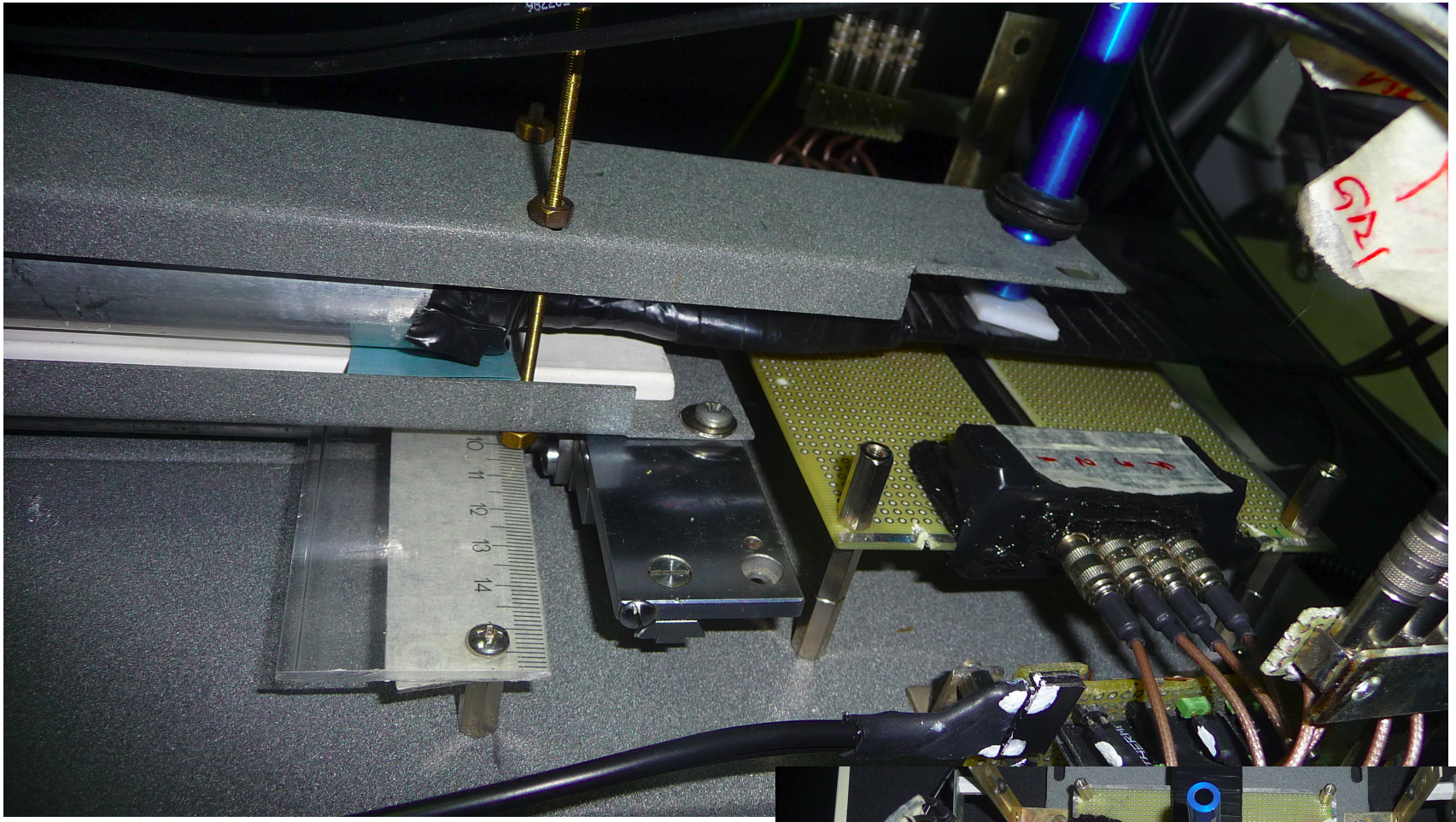
Both systems are suitable for studying low thresholds

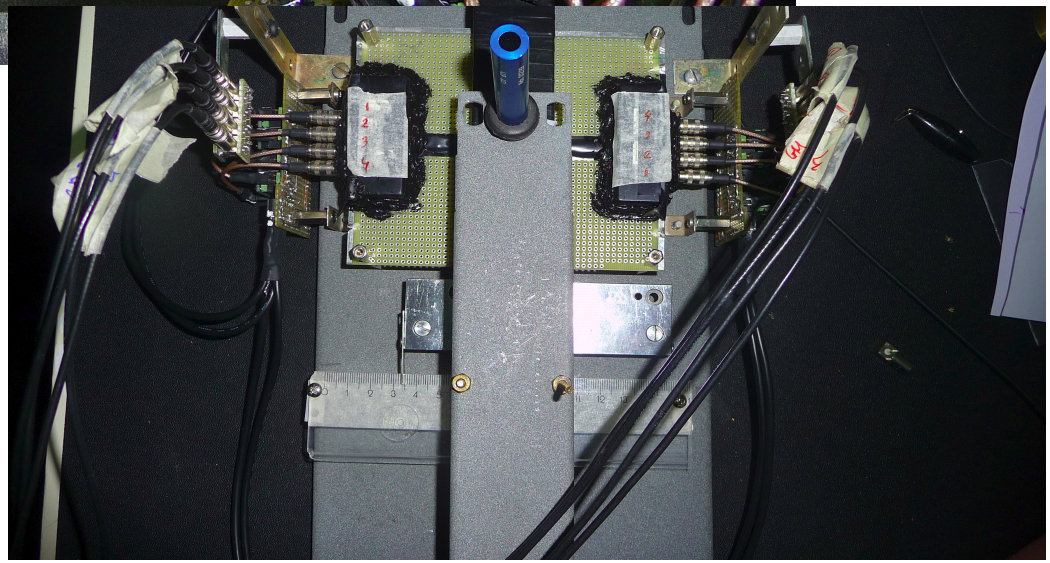
Experimental setup

- New logics for time discrimination
- Low thresholds



Side view



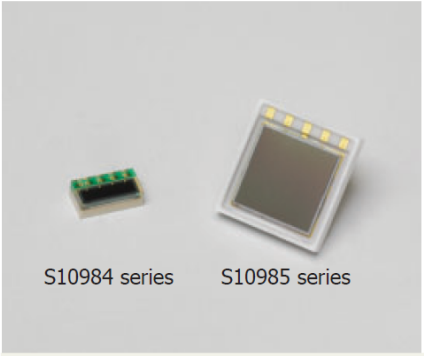


Top view

HAMAMATSU

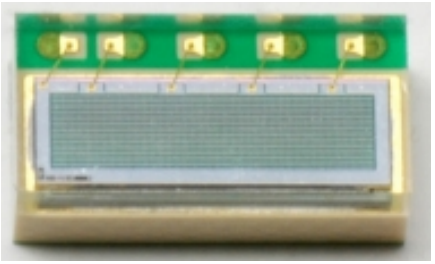
MPPC® (multi-pixel photon counter)

S10984/S10985 series

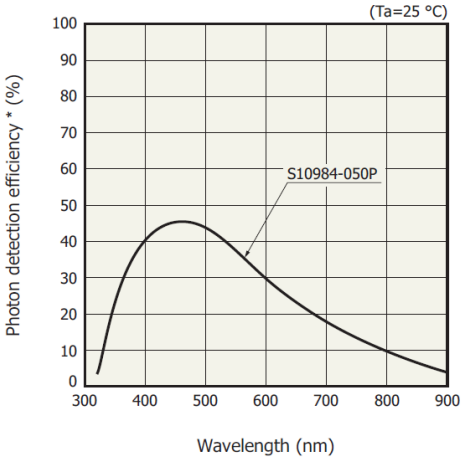


New type of Si photon-counting device, Array type (1 × 4 ch, 2 × 2 ch)

S10984-050P



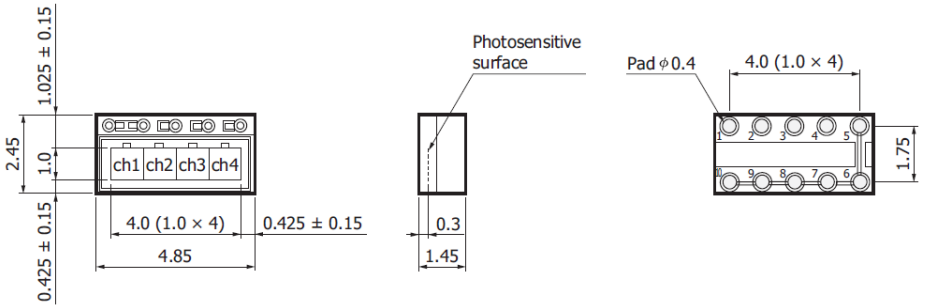
Photon detection efficiency (PDE) vs. wavelength (typical example)



* Photon detection efficiency includes effects of crosstalk and afterpulses.

Dimensional outlines (unit: mm)

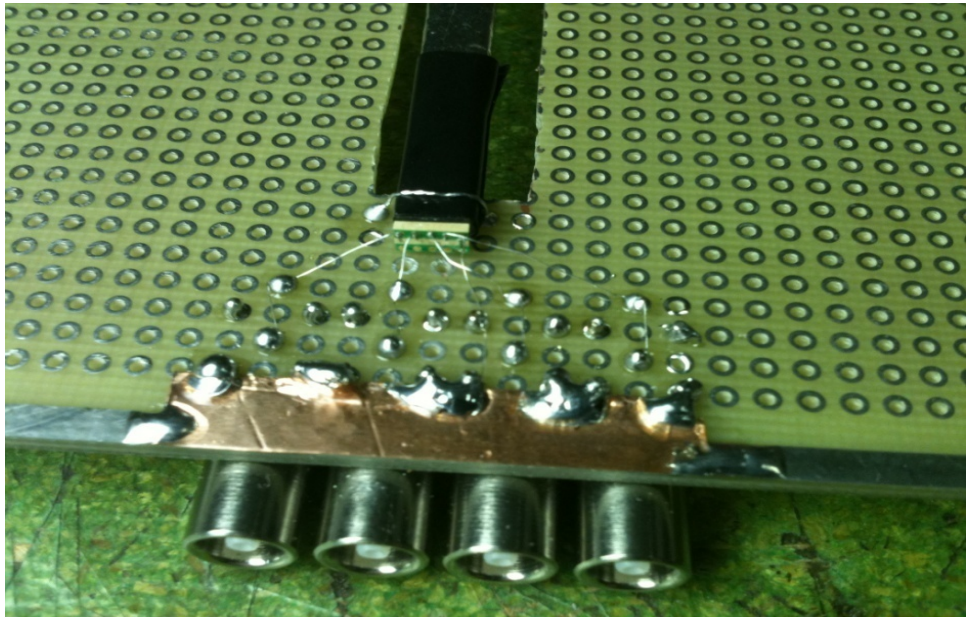
S10984 series



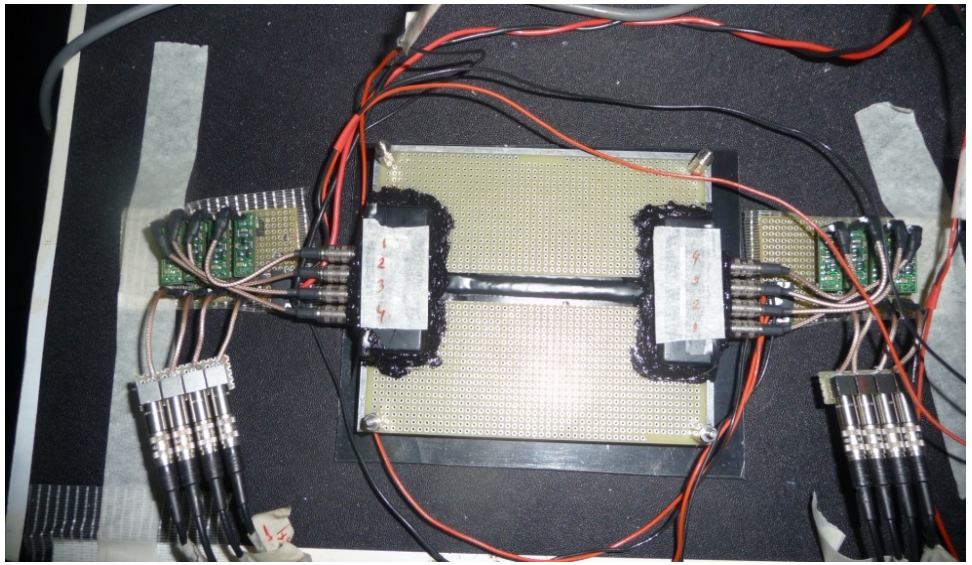
Pad No.	Connection
1	Anode ch4
2	Anode ch3
3	Anode ch2
4	Anode ch1
5	Cathode (common)
6	Cathode (common)
7	Cathode (common)
8	Cathode (common)
9	Cathode (common)
10	Cathode (common)

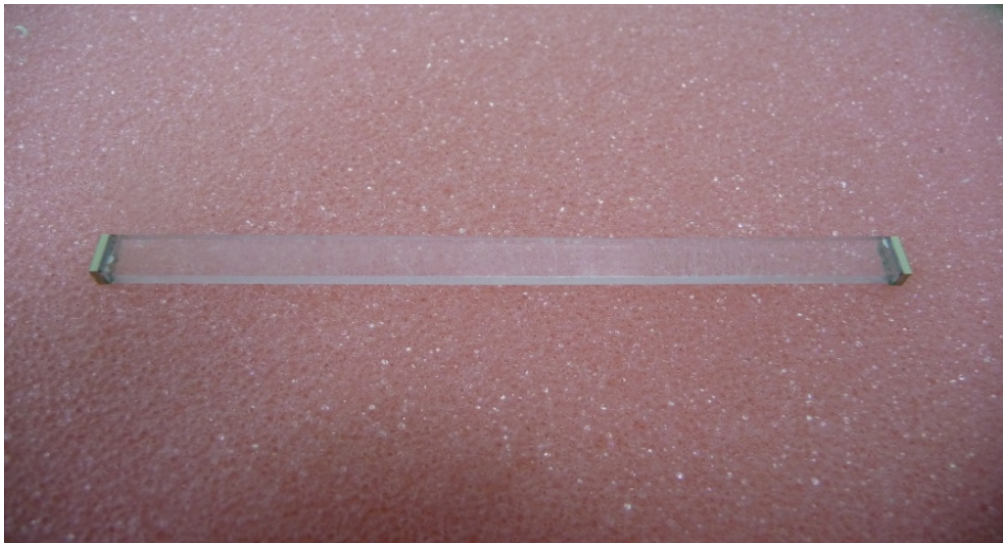
Package	Glass epoxy
Number of channels	4 (1×4) ch
Effective photosensitive area	1 x 4 mm
Number of pixels /ch	400
Pixel size	50 x 50 um
Fill factor	61.5 %
Spectral response range	320 to 900 nm
Peak sensitivity wavelength (typ.)	440 nm
Operating voltage range (typ.)	70±10 V
Dark count/ch (typ.)	400 kcps
Terminal capacitance/ch (typ.)	35 pF
Gain (typ.)	7.5×105
Measurement condition	Ta=25 °C

IFIN-HH SiPM R&D

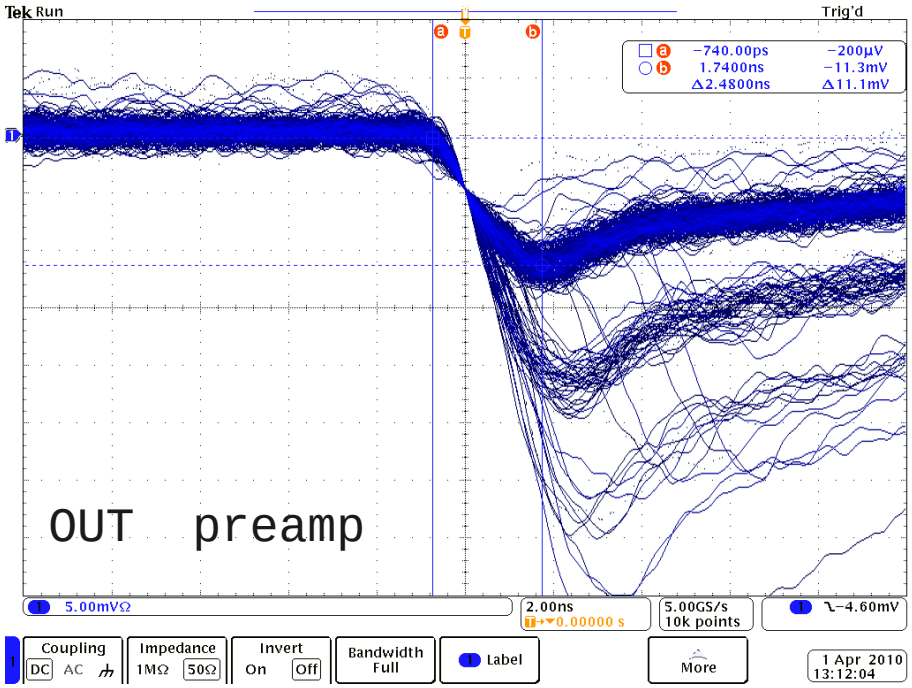


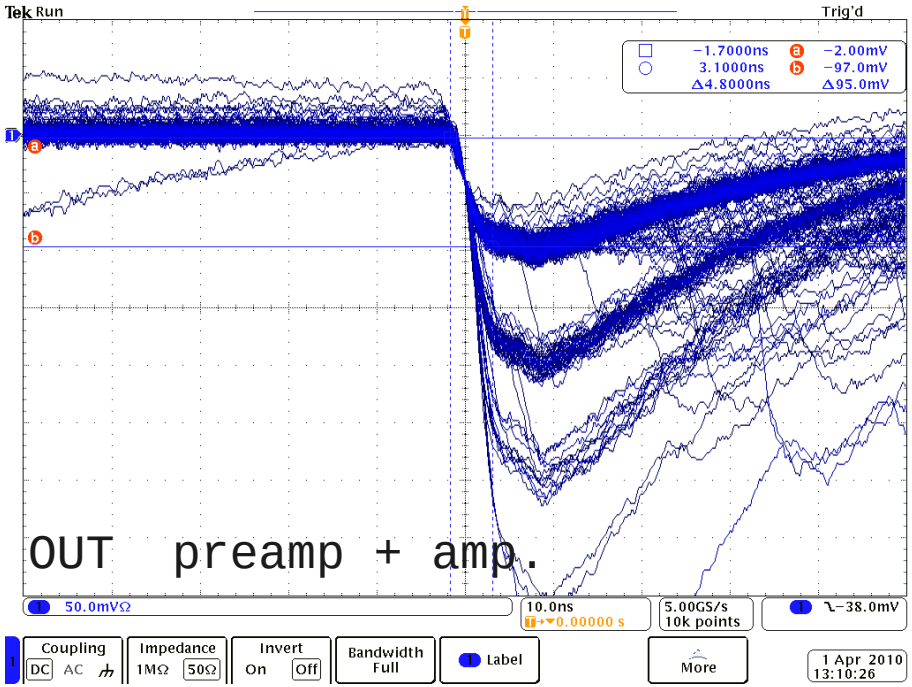
- plastic scintillator (BC420)
- 100mm x 5mm x 1.5 mm (L x l x h) ;
- 2 x S10984-050P, 4 channels 1mm^2;
- optical cement BC600;





IFIN-HH SiPM R&D

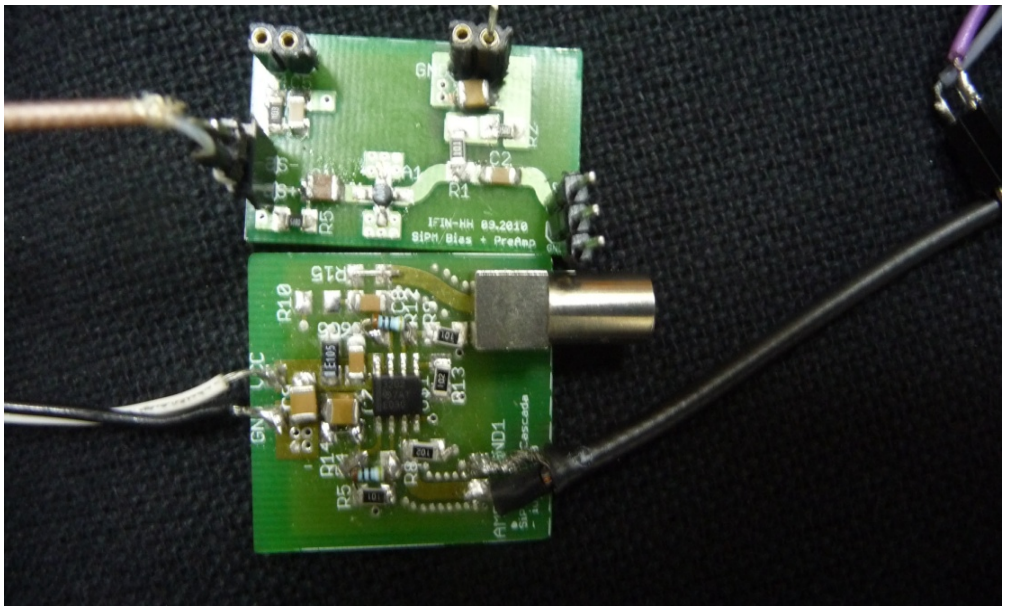




HAMAMATSU S10362-11-100C

2.4×10^6 @ 69.9 V
480 K @ 0.5 Thr

Preamplifier:
- comercial monolithic amplifier;
- typical gain 32.5 db @ 100 MHZ;
- maximum current 65 mA ;
- power 500mW



User customizable FPGA Unit

LVDS/ECL/PECL inputs (differential)

64 inputs, expandable to 162 (with 32 outputs)

32 outputs, expandable to 130 (with 64 inputs)

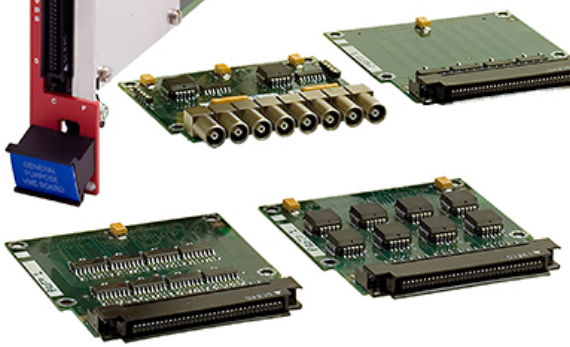
405 MHz maximum frequency supported by clock tree for registered logic

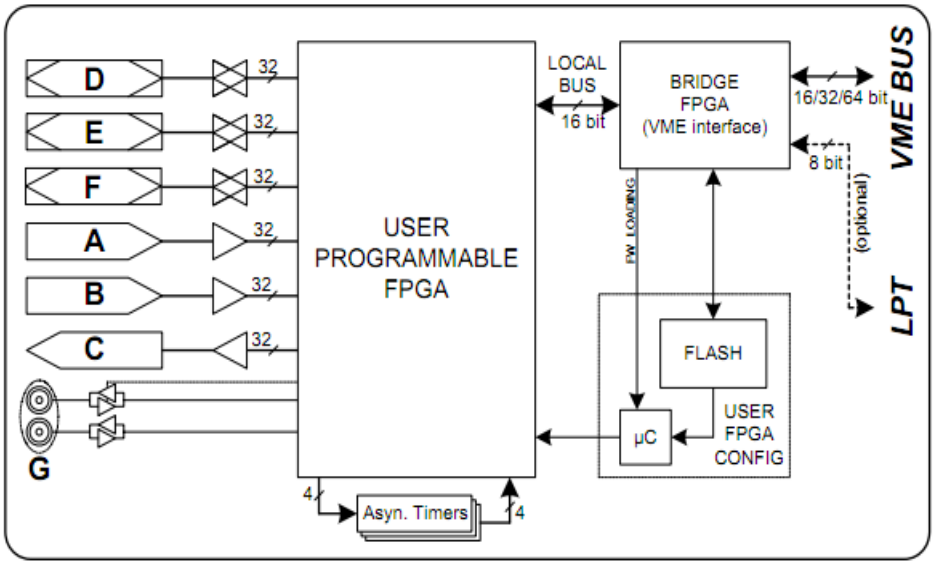
I/O delay smaller than 15 ns (in Buffer Mode)

Programmable 3-color LED

Libraries (C and LabView) and Software tools for Windows and Linux

V1495





user firmware Quartus 2 (Altera);

16 channel Multihit TDC

V1290

5 ps LSB
21 bit resolution
52 µs full scale range
NIM Input Signals
5 ns Double Hit Resolution
Leading and Trailing Edge detection
Trigger Matching and Continuous Storage
- acquisition modes

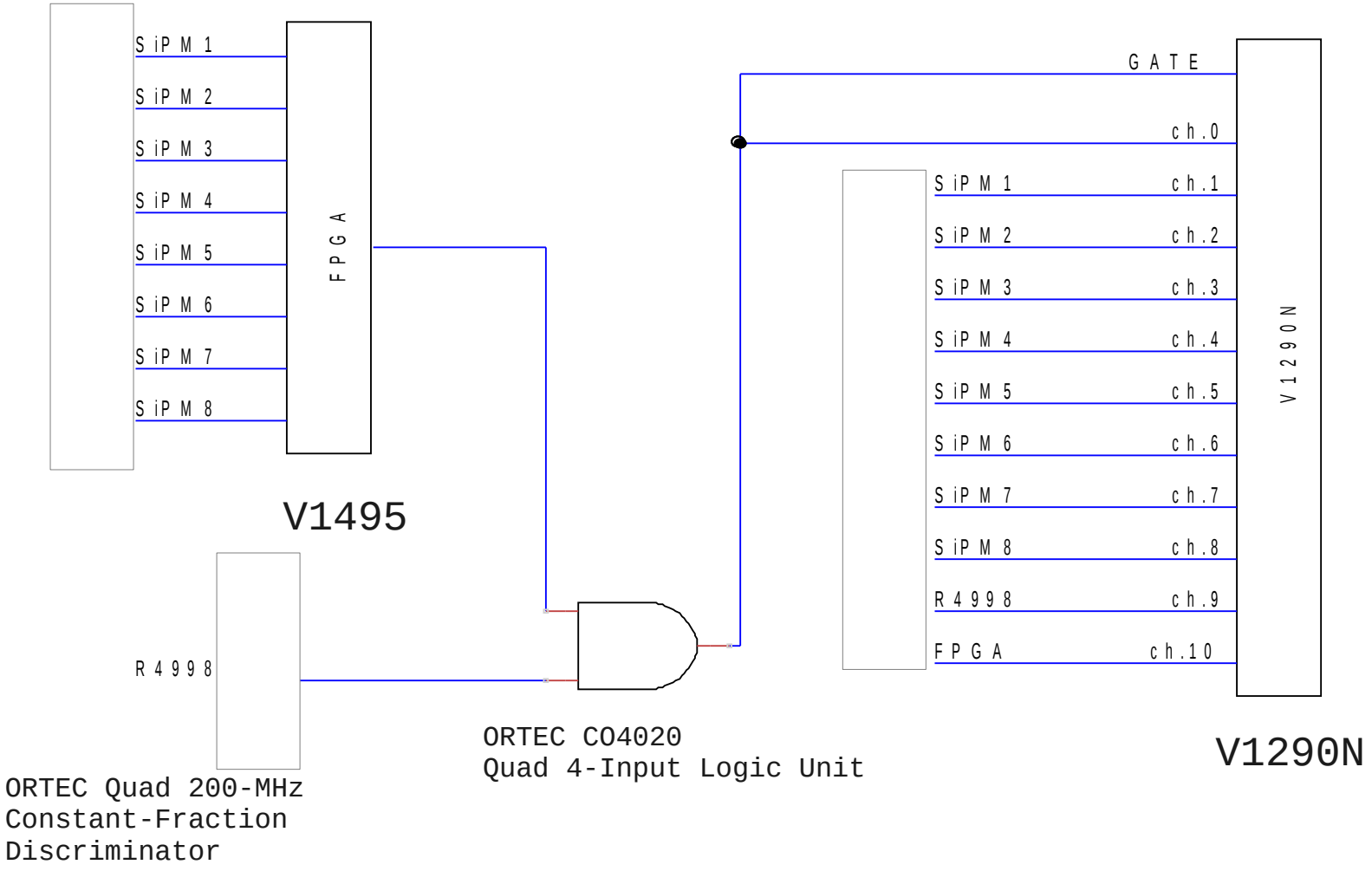
32 k x 32 bit output buffer
MBLT, CBLT and 2eSST data transfer

DAQ devices

CAEN
Company Network

DAQ logic

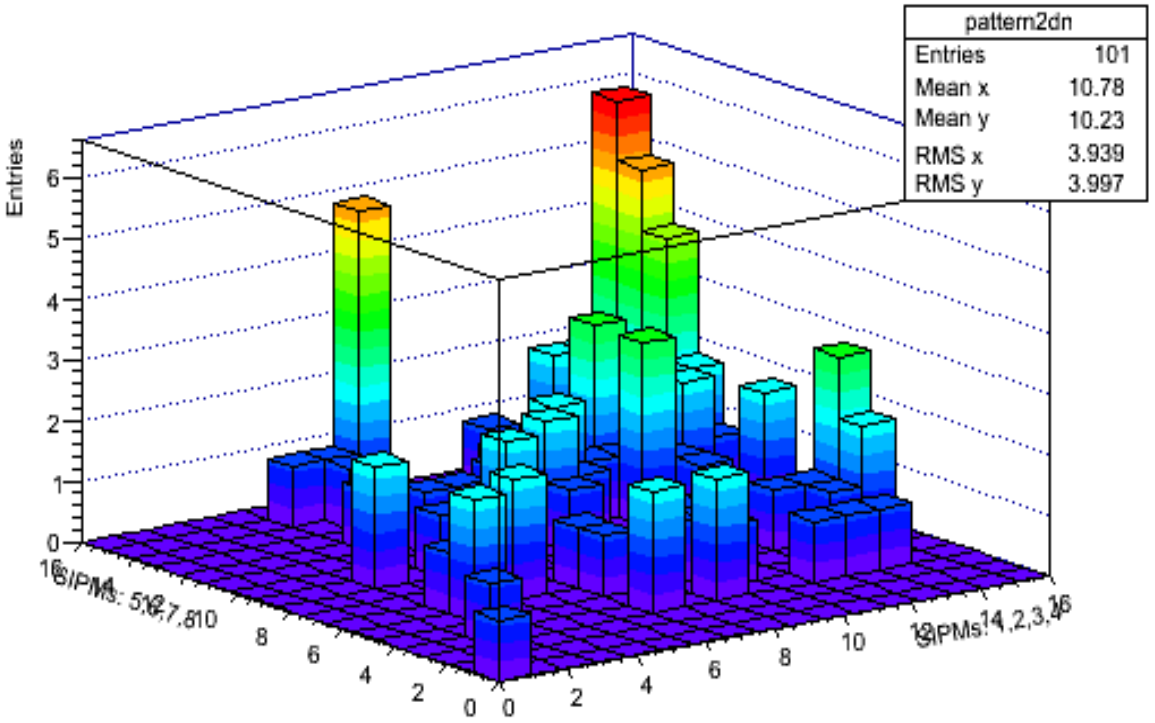
Canberra 454 200 MHz Quad
Constant Fraction
Discriminator

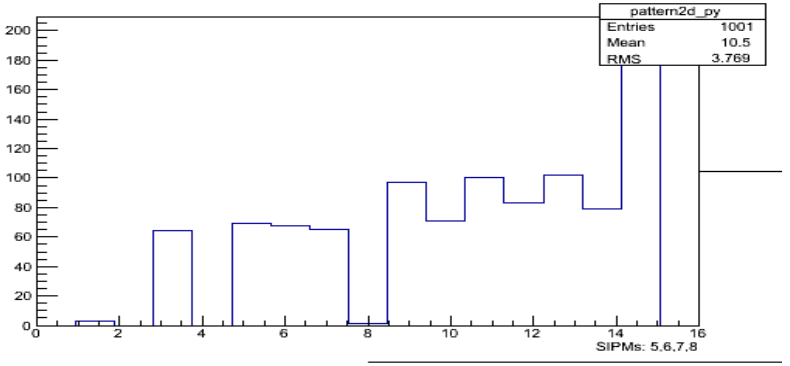


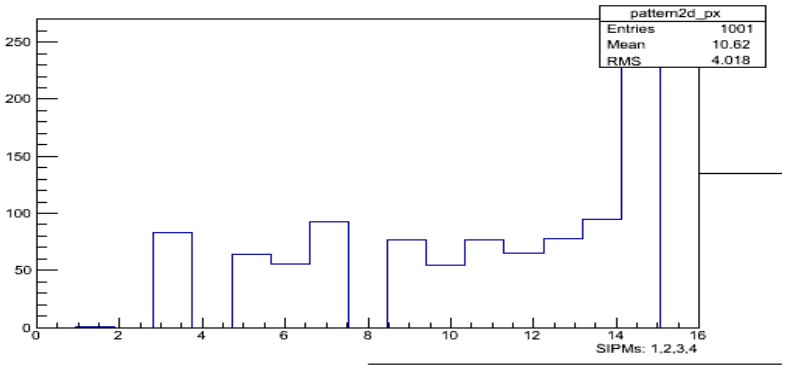
DAQ software: LabView & C+;
FPGA: VHDL

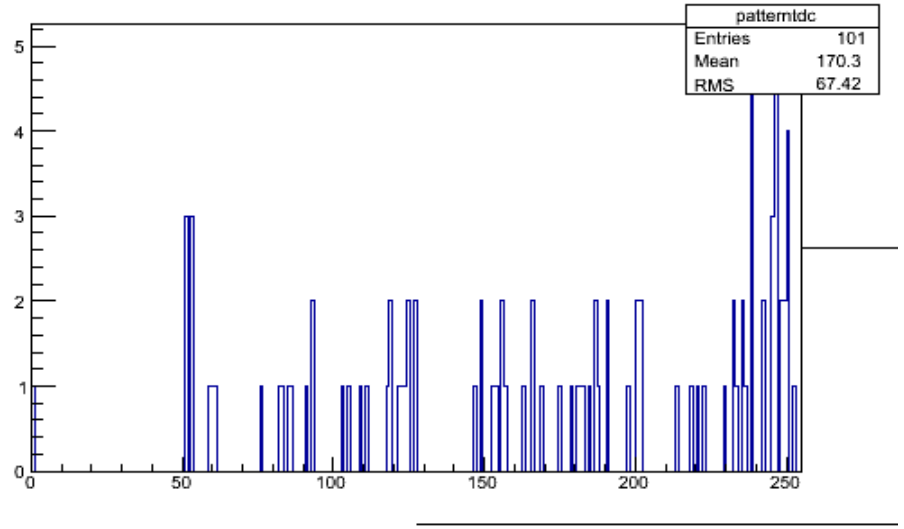
FPGA hits

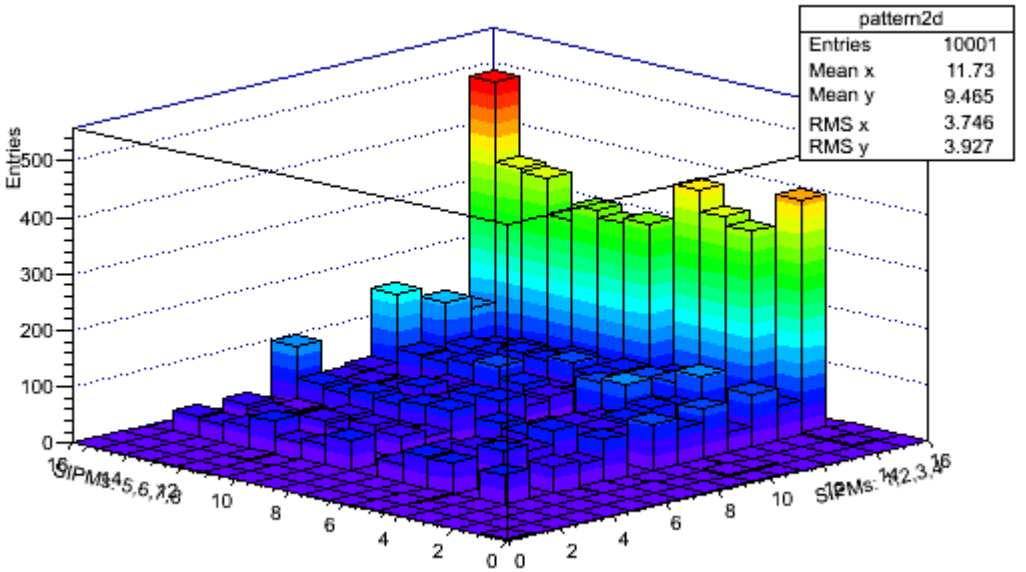
Combinations of coincidences

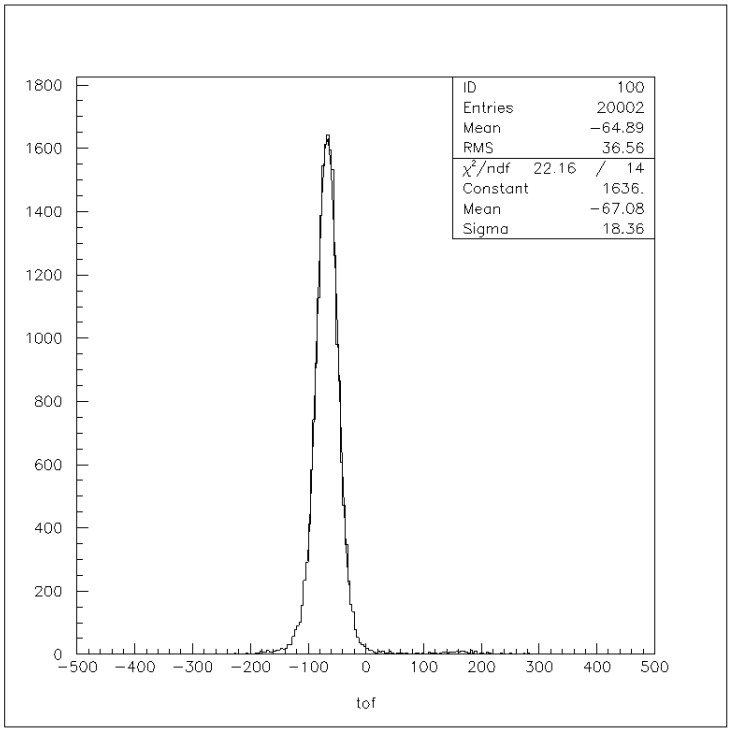




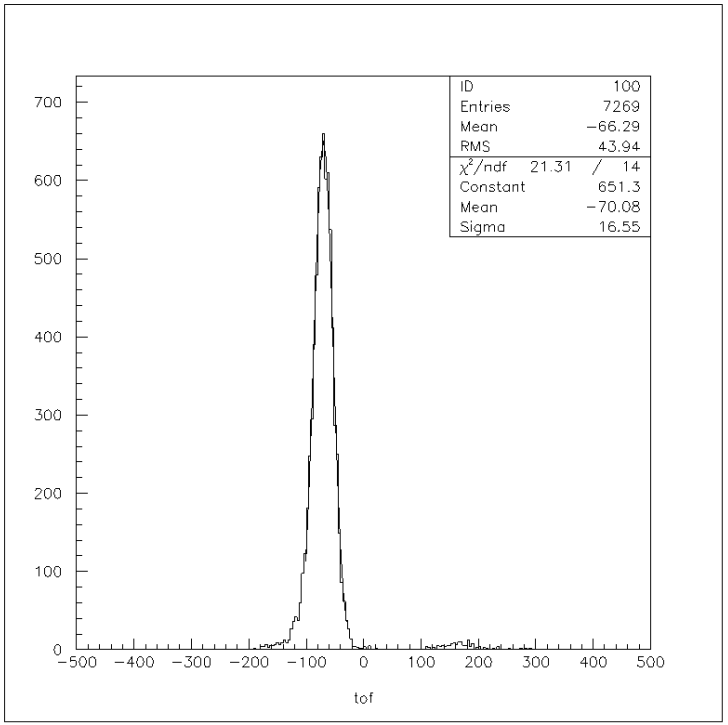




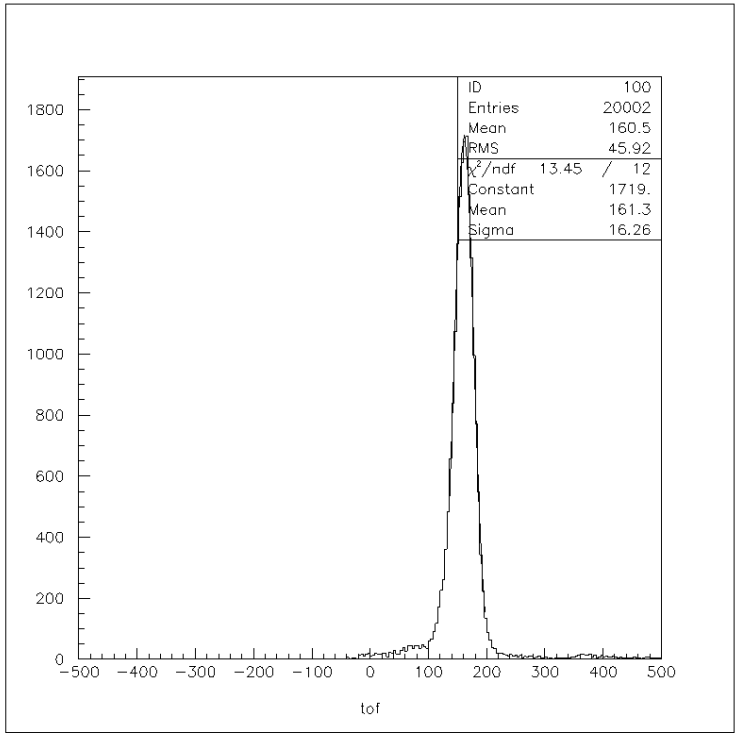




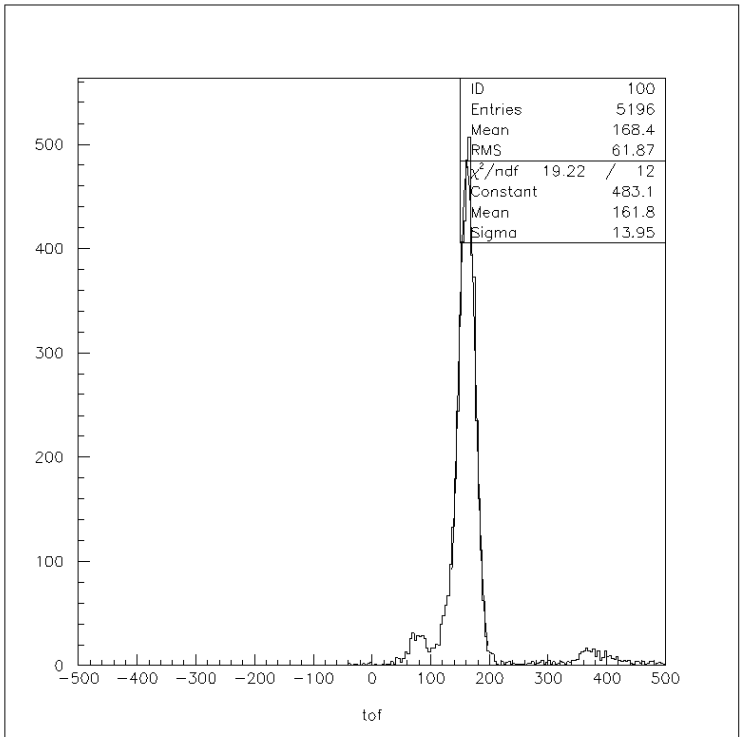
Best **FWHM**
Canbera
no pattern



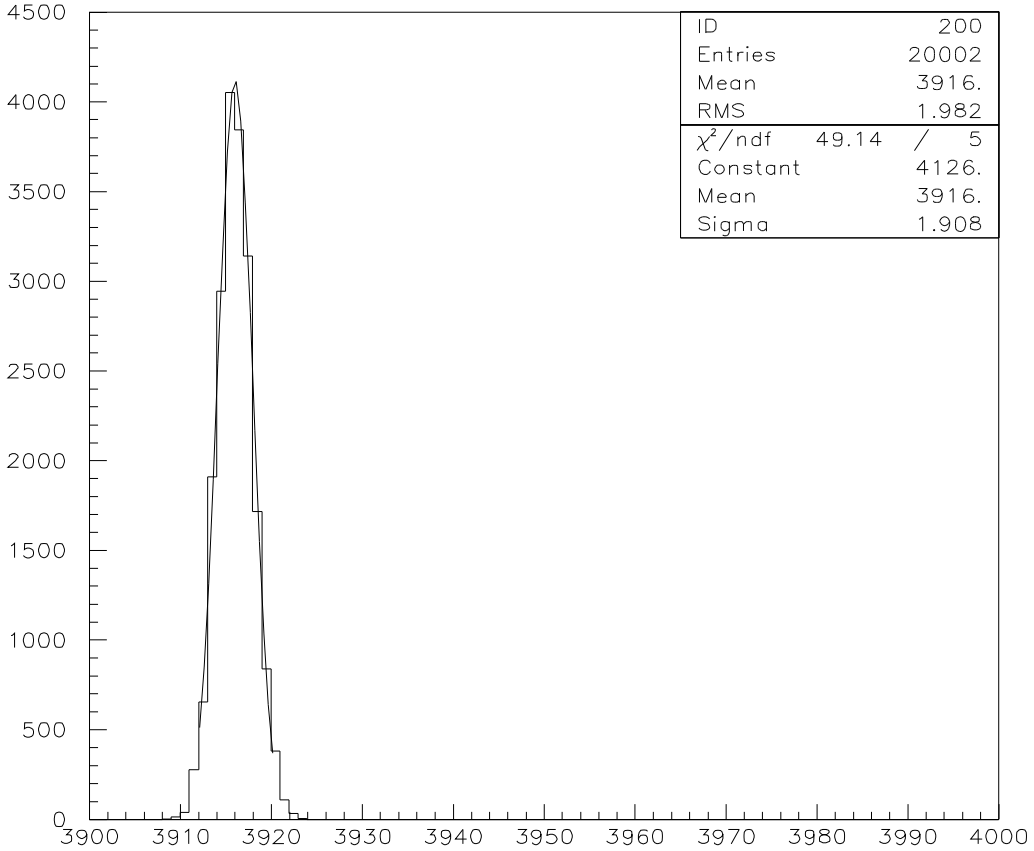
Best **FWHM**
IFIN
no pattern



Best **FWHM**
Canbera
pattern



Best **FWHM**
IFIN
pattern

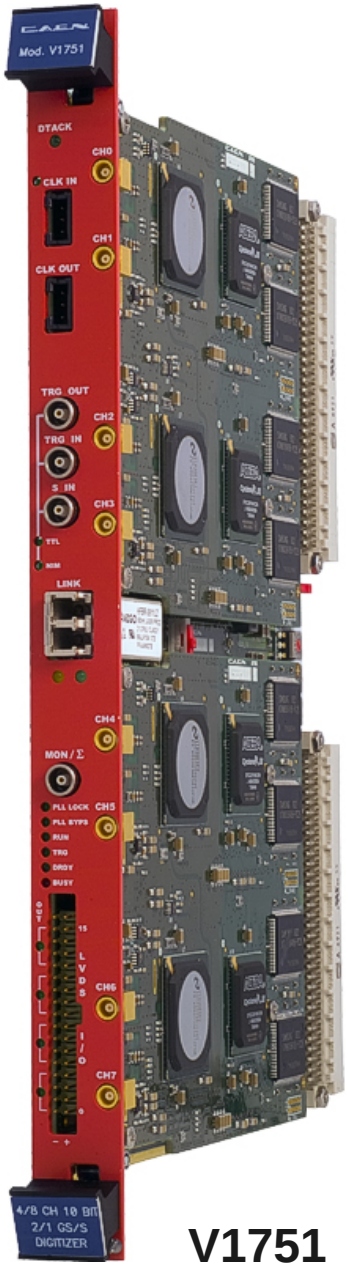


TDC START (trigger –PMT) 23 ps/ch

for the start signal the resolution was under 100ps FWHM

Best values obtained @IFIN-HH are:

Preamplifier	Threshold CFD	FWHM	FWHM corrected
Photonique	9.5 pe-	990 ps	894 ps
IFIN-HH	9.5 pe-	870 ps	754 ps



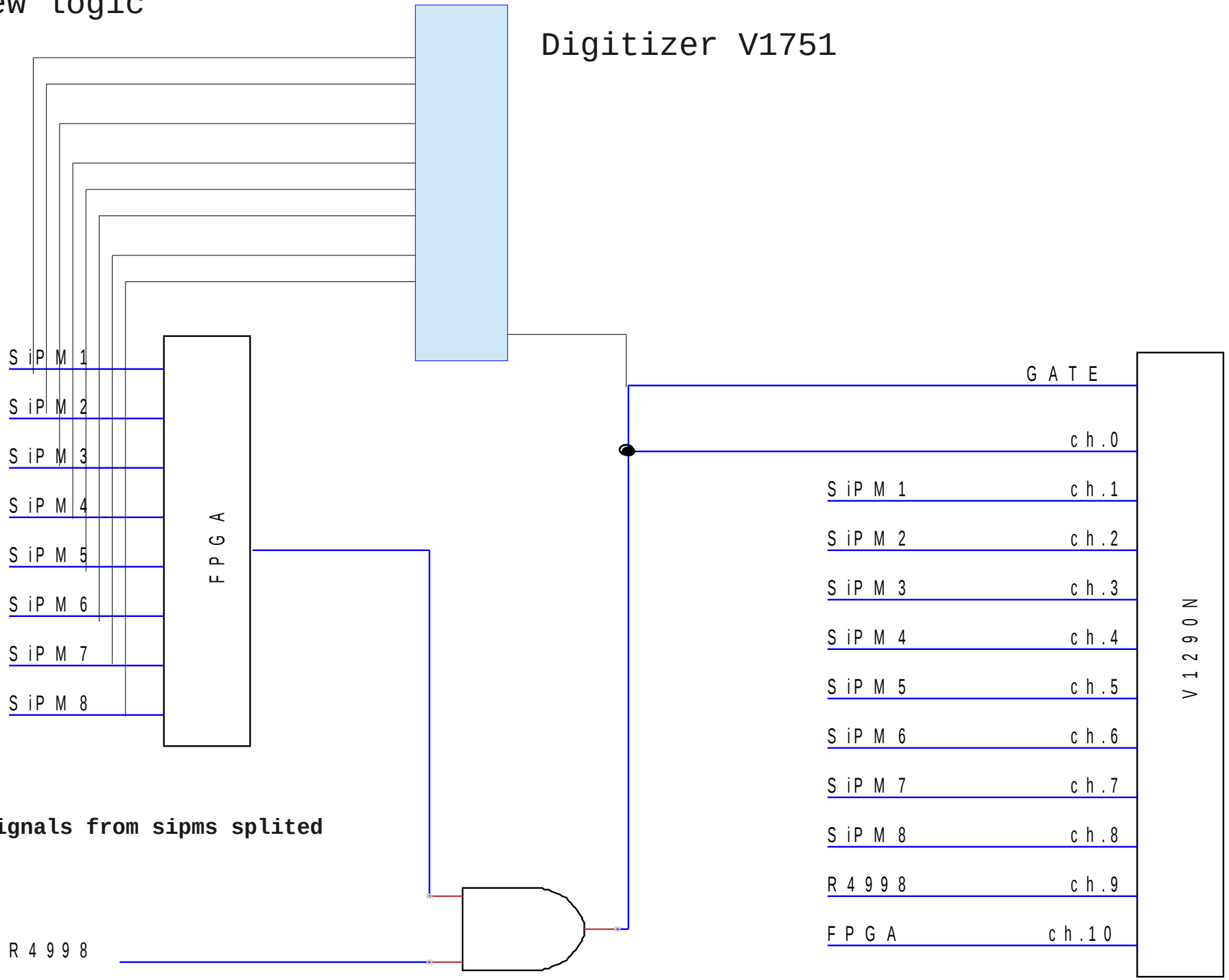
V1751

TOF using digitizers

good solutions for the multichannel systems

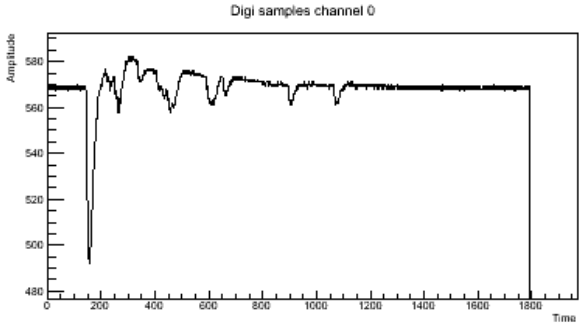
10 bit 2 GS/s (interleaved) - 1 GS/s ADC
4/8 channel
FPGA for real time Digital Pulse Processing:
1 Vpp input dynamics single ended or differential
16-bit programmable DC offset adjustment: ±0.5 V
Trigger Time stamps
Memory buffer: up to 14.5 MSample/ch

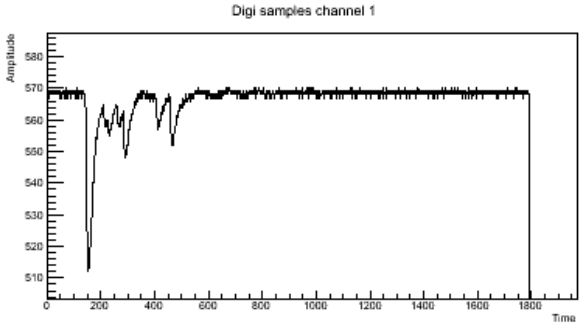
New logic

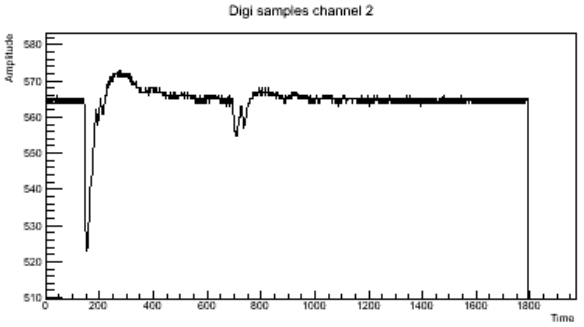


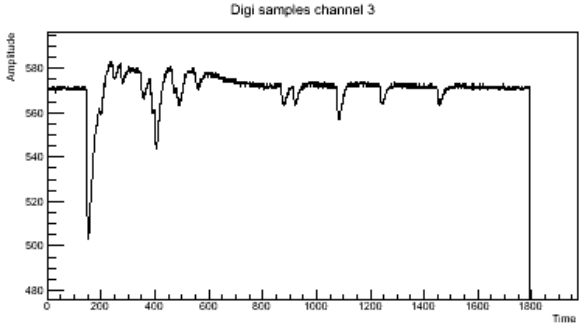
Signals from sipms splited

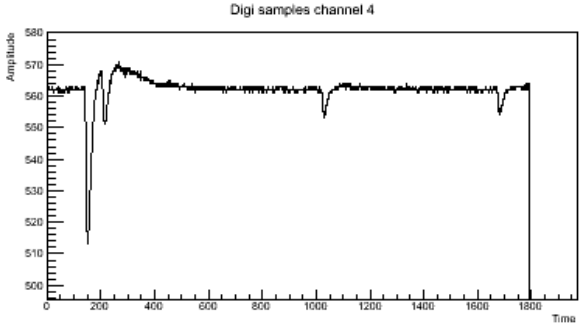
CAEN V1751 1G 8ch digitizer

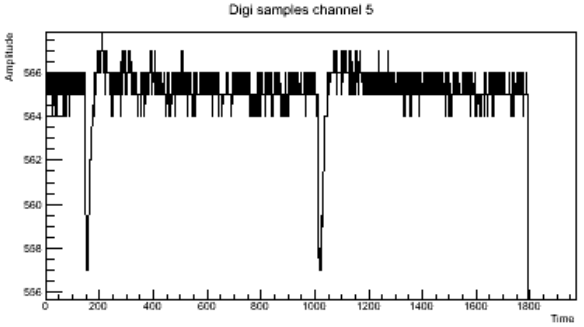


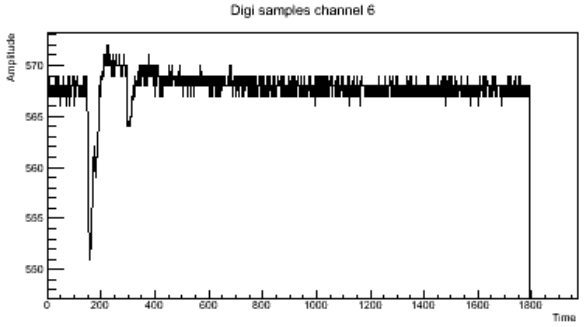


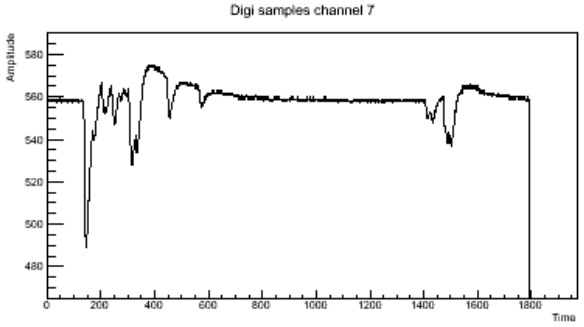


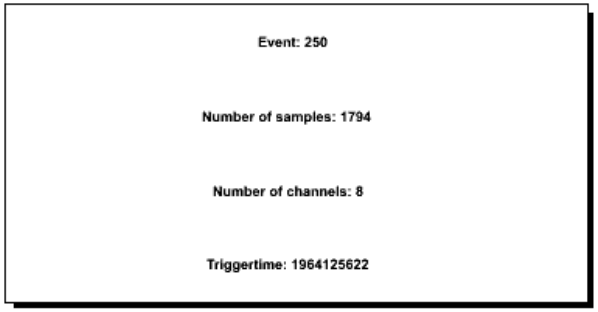






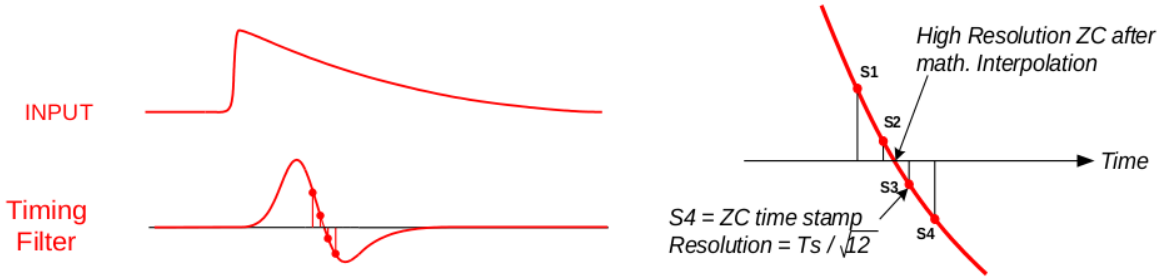






Need a software algorithms to get timing information from waveform data

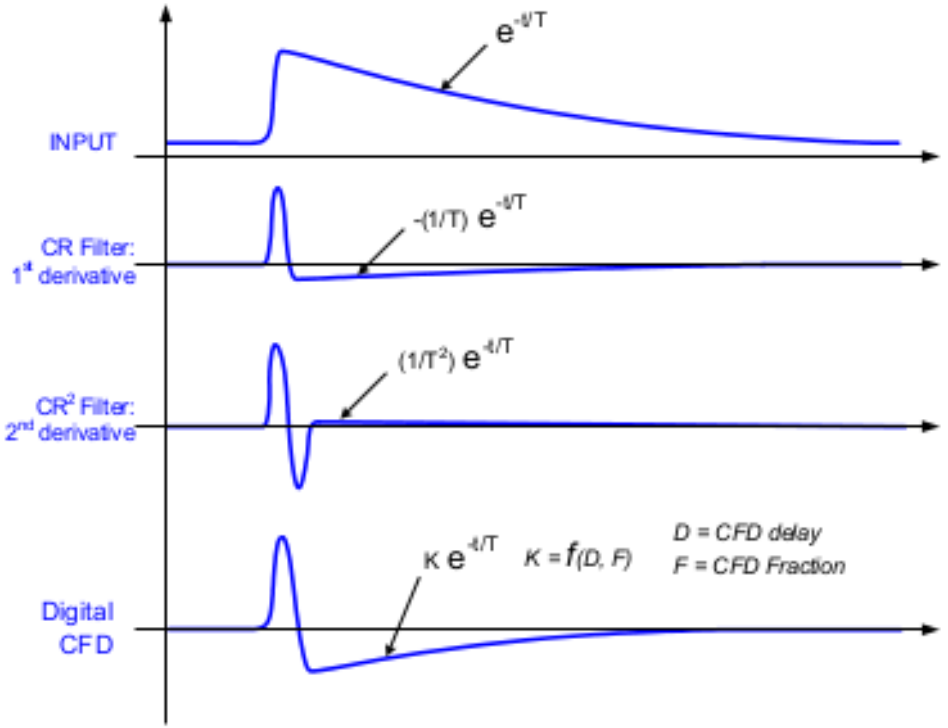
Software algorithms for timing with digitizers



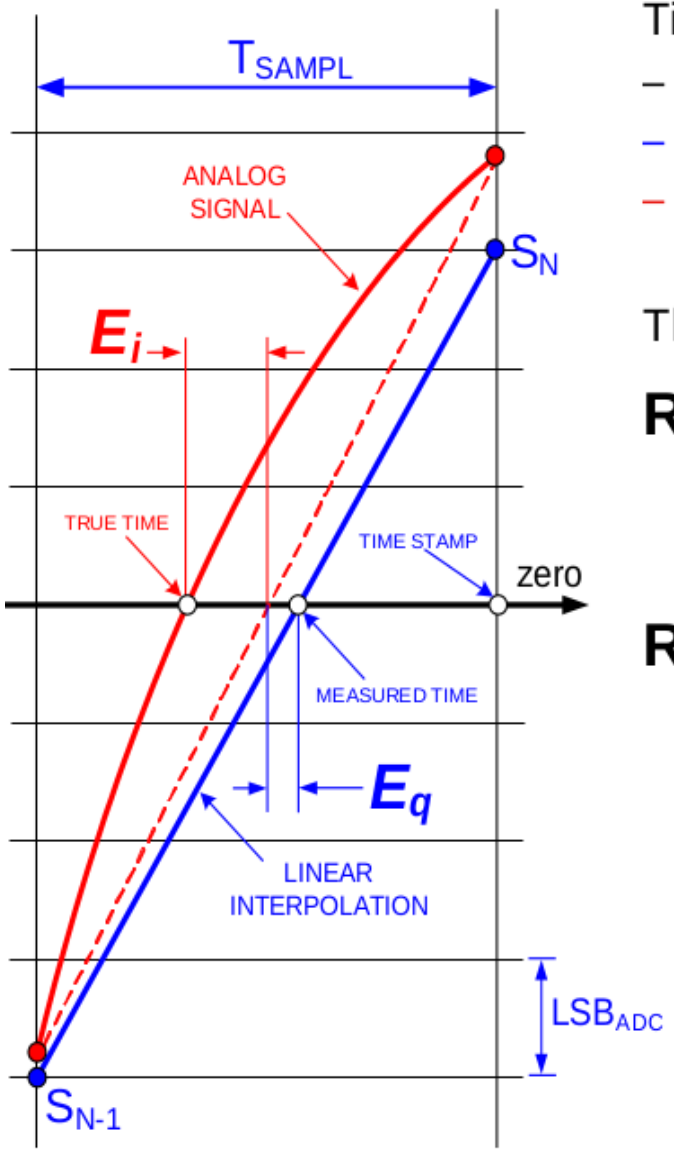
Graphics taken from Digital Pulse Processing for Physics Applications Triumf – December 7th, 2011 Carlo Tintori

many types of timing and triggering filter

transform the pulses into bipolar signals whose zero crossing
(pulse amplitude independent) can be used for the determination of the Time Stamp



Graphics taken from WP2081 Digital Pulse Processing in Nuclear Physics



Timing resolution affected by three types of noise:

- *Electronic noise in the analog signal (here ignored)*
- *Quantization error **Eq***
- *Interpolation error **Ei***

There are 2 different cases:

Rise Time > 5*Ts

linear interpolation is good: ***Ei*** << ***Eq***
The resolution is proportional to **δV/δT** and to the number of bits of the ADC.

Rise Time < 5*Ts

approximation to a straight line is too rough:
Ei is the dominant error (***Eq*** is negligible). Such a geometric error varies with the position of the signal respect to the sampling clock giving non gaussian spectra and other non-physical effects. The resolution becomes inversely proportional to the rise time.

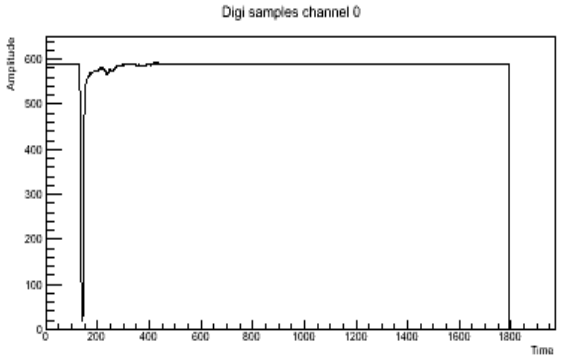
Optimum Rise Time = 5*Ts
for any type of digitizer!

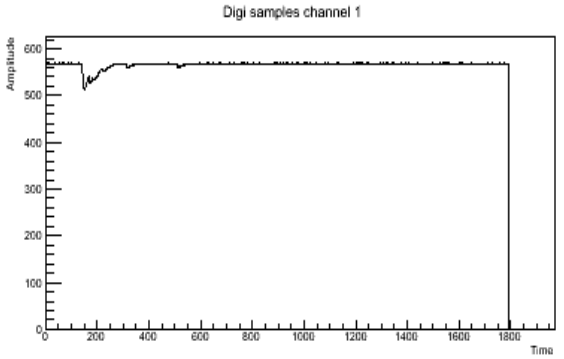
Graphics taken from Digital Pulse Processing for Physics Applications Triumf – December 7th, 2011 Carlo Tintori

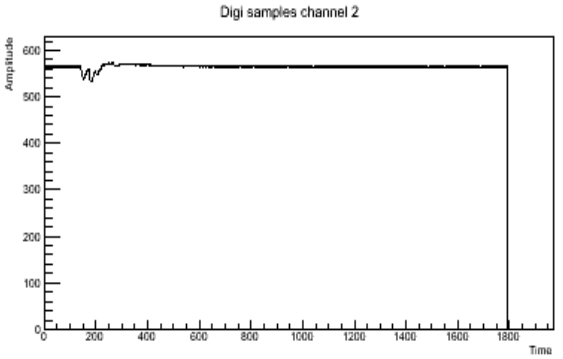
8ns trigger sample uncertainty

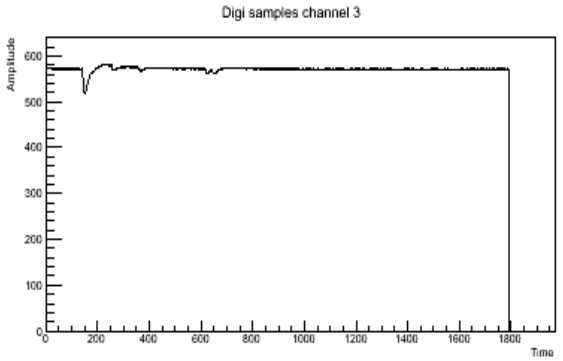
CAEN Technical Information Manual
Revision n. 12 3.2.3. Trigger Clock

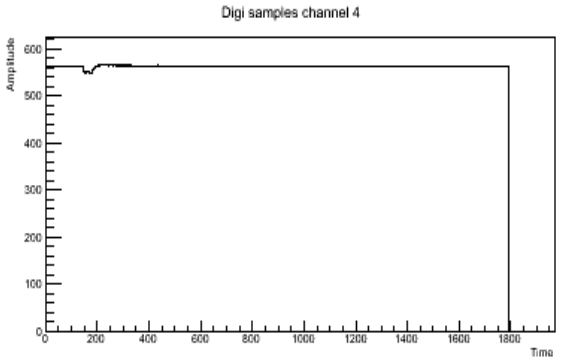
1ch should be used for the trigger signal

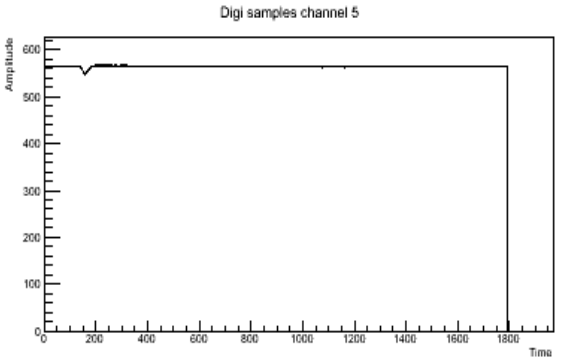


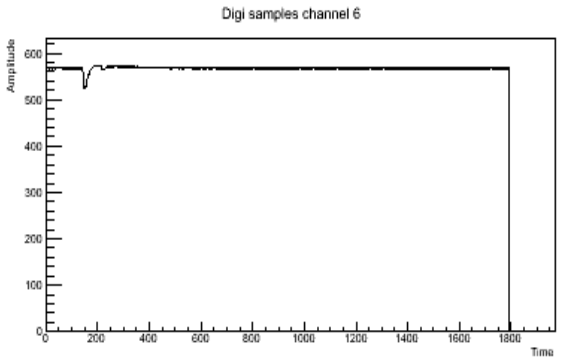


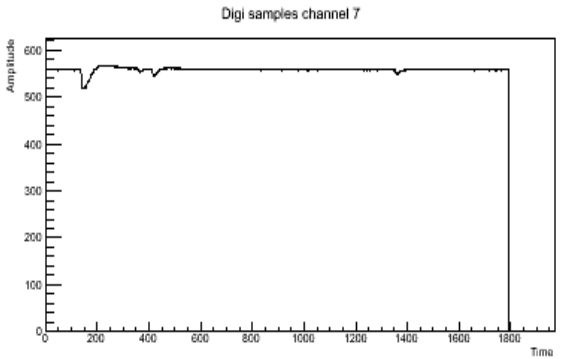


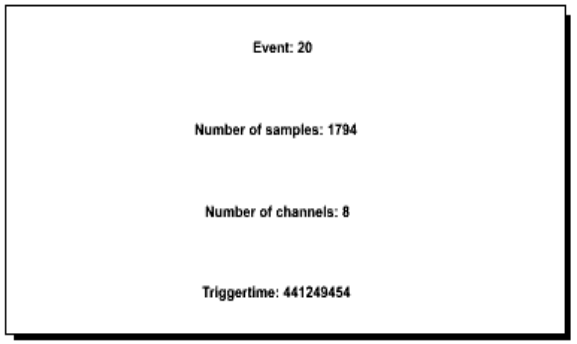


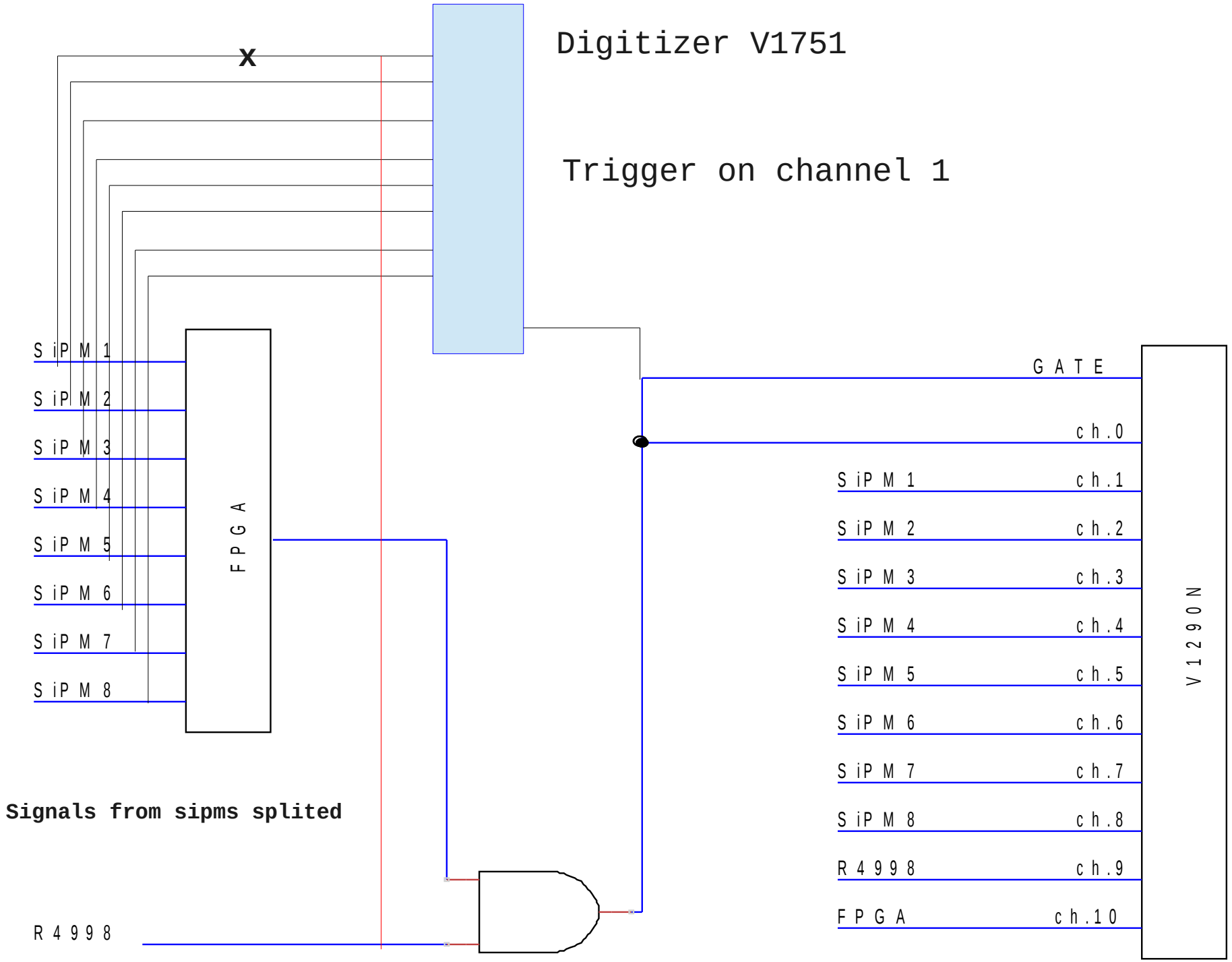






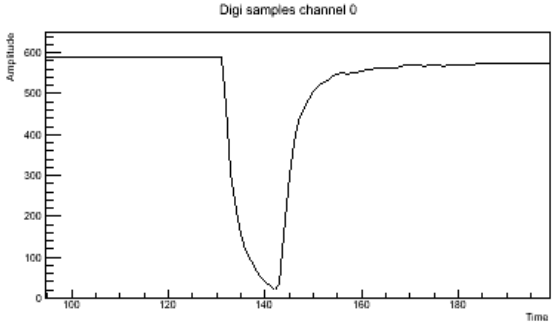


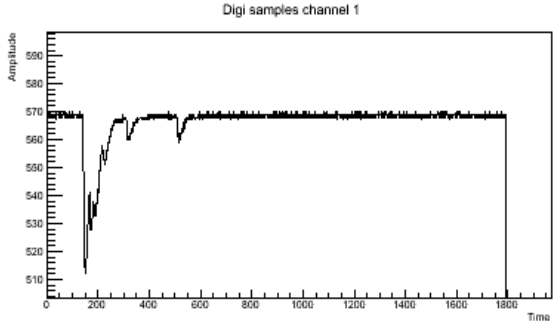


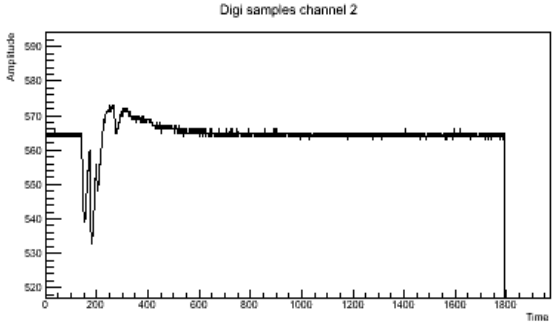


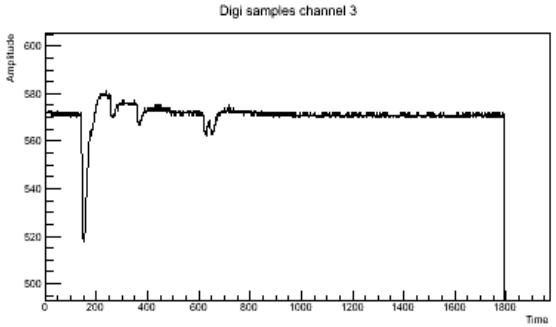
Signals from sipms splited

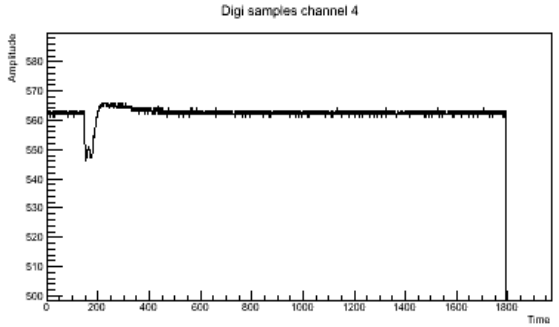
Rise Time of the PMT is too small – the shape has to be a bit modified

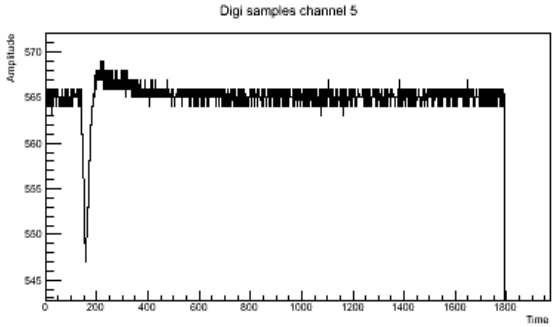


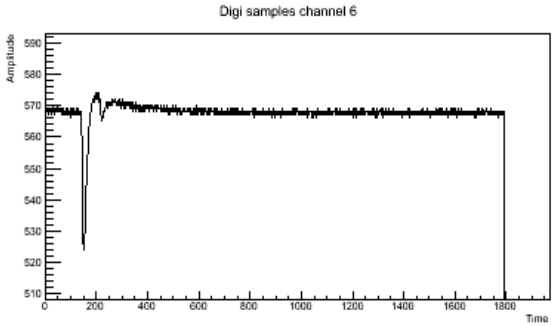


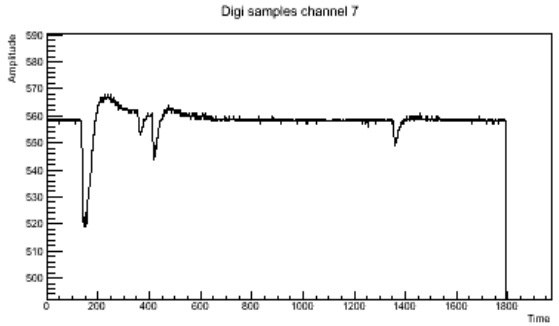


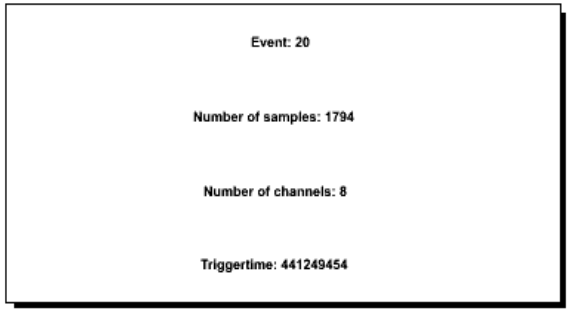


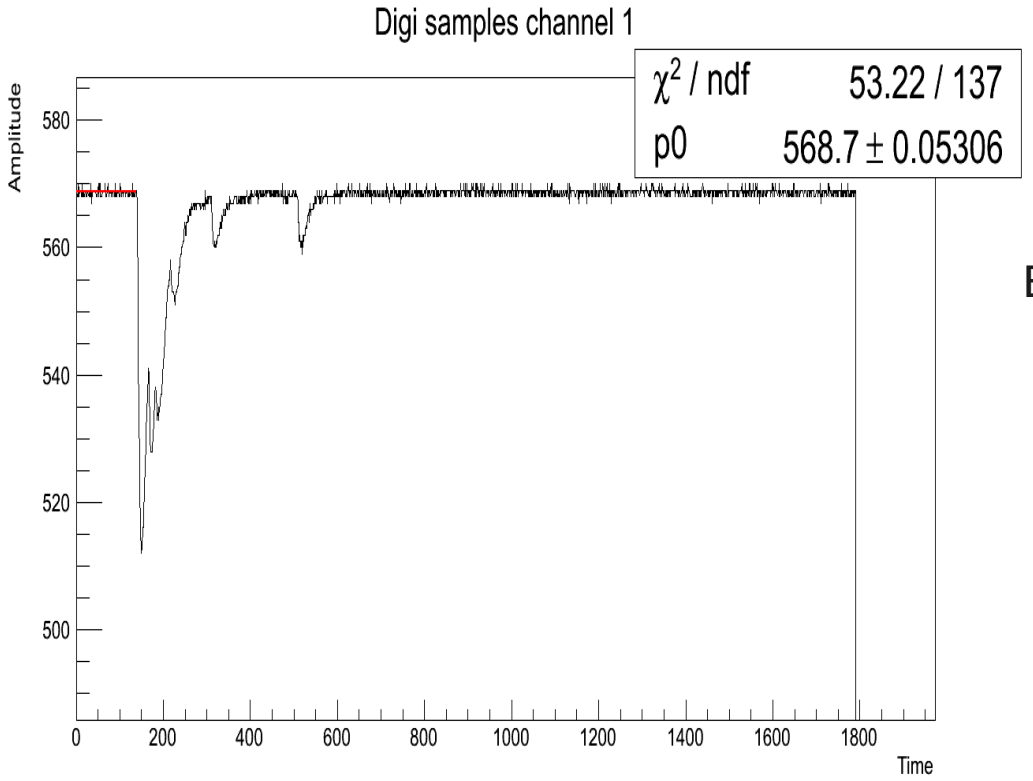




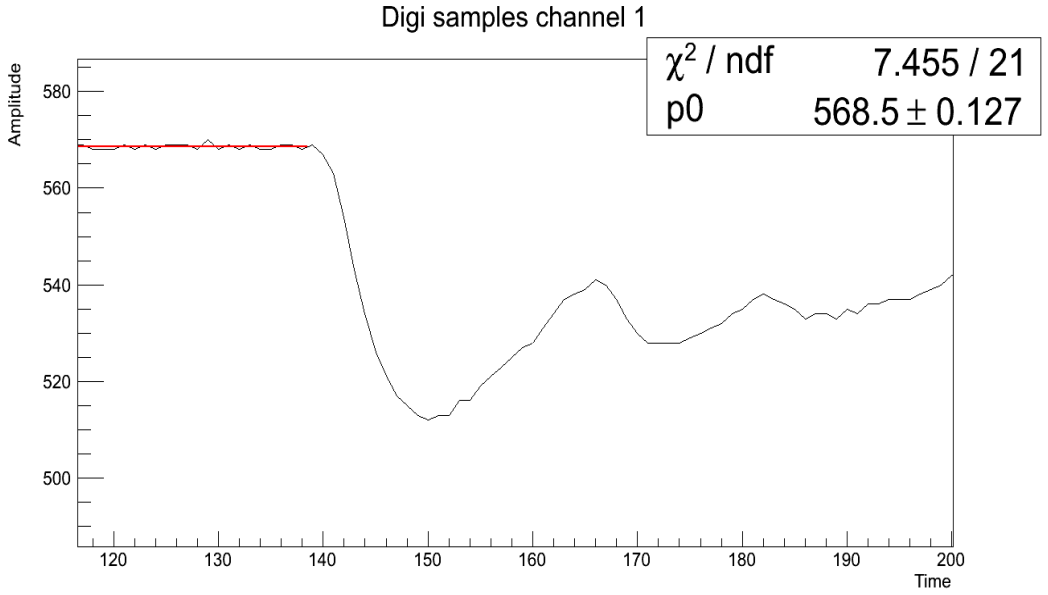








Baseline determination



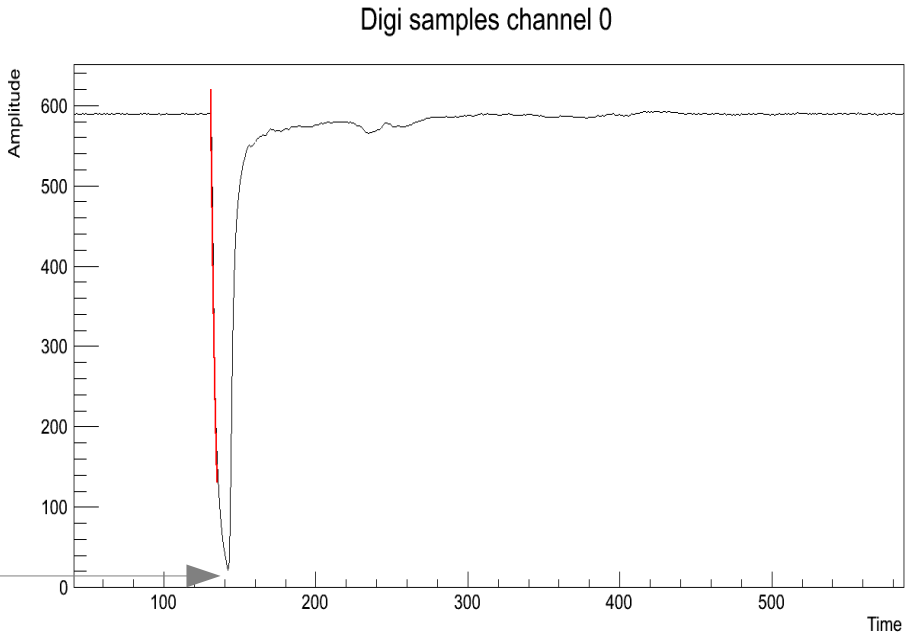
First 100 samples are “clean”

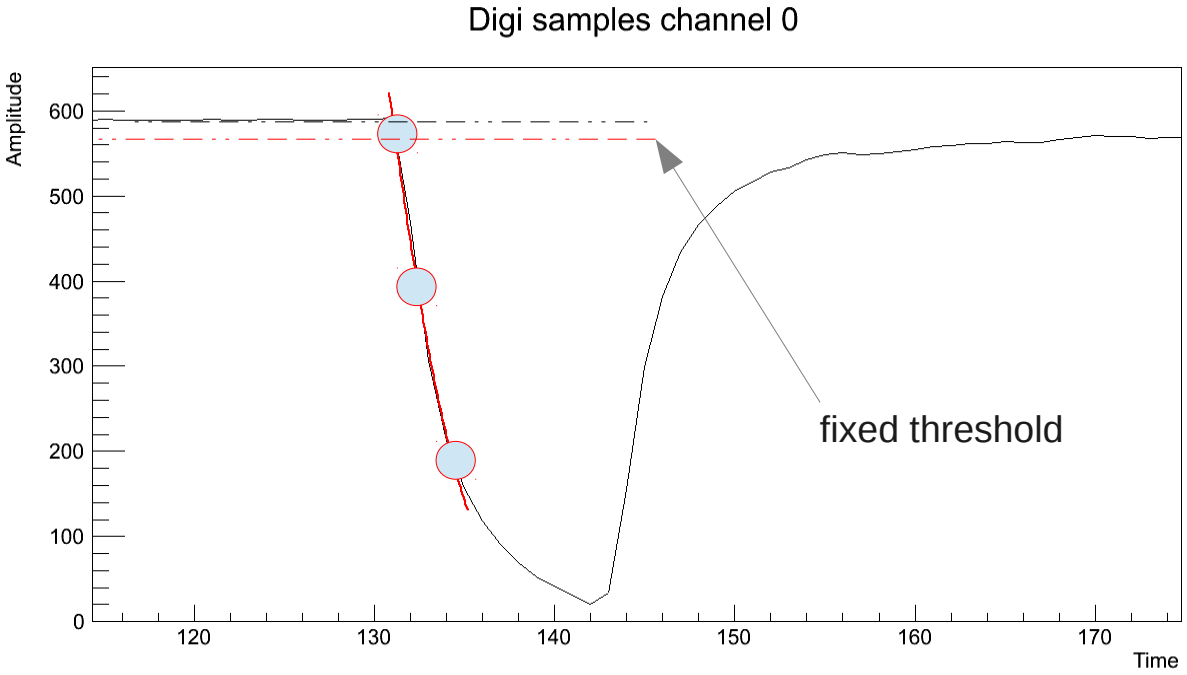
Trigger channel

For each channel - peak identifier

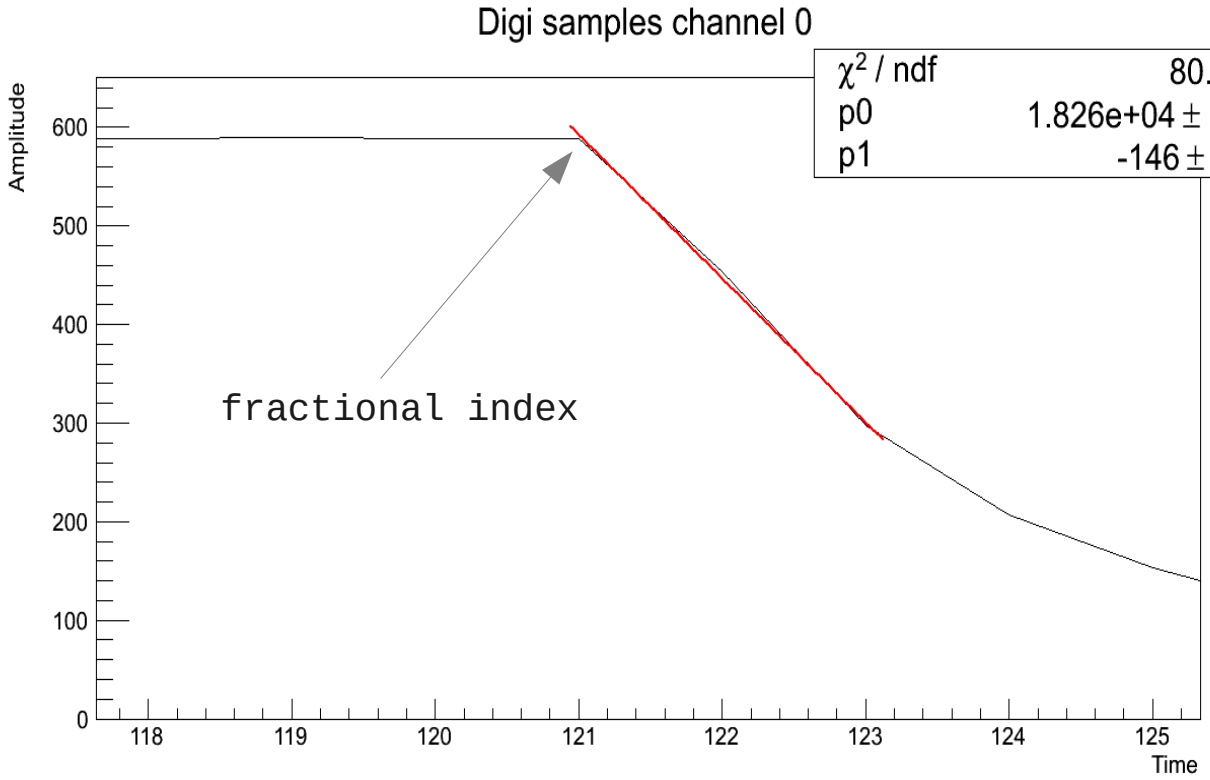
Still very small rise time

Baseline-Min ~amplitude

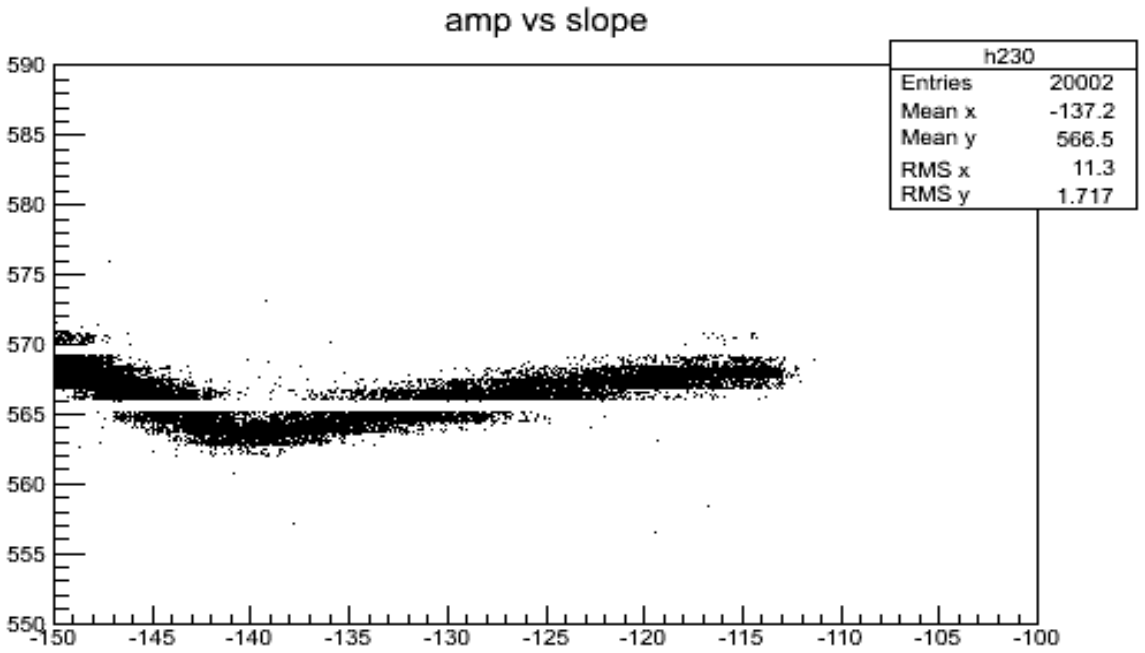




First three points over the threshold are used for the fit



trigger reference

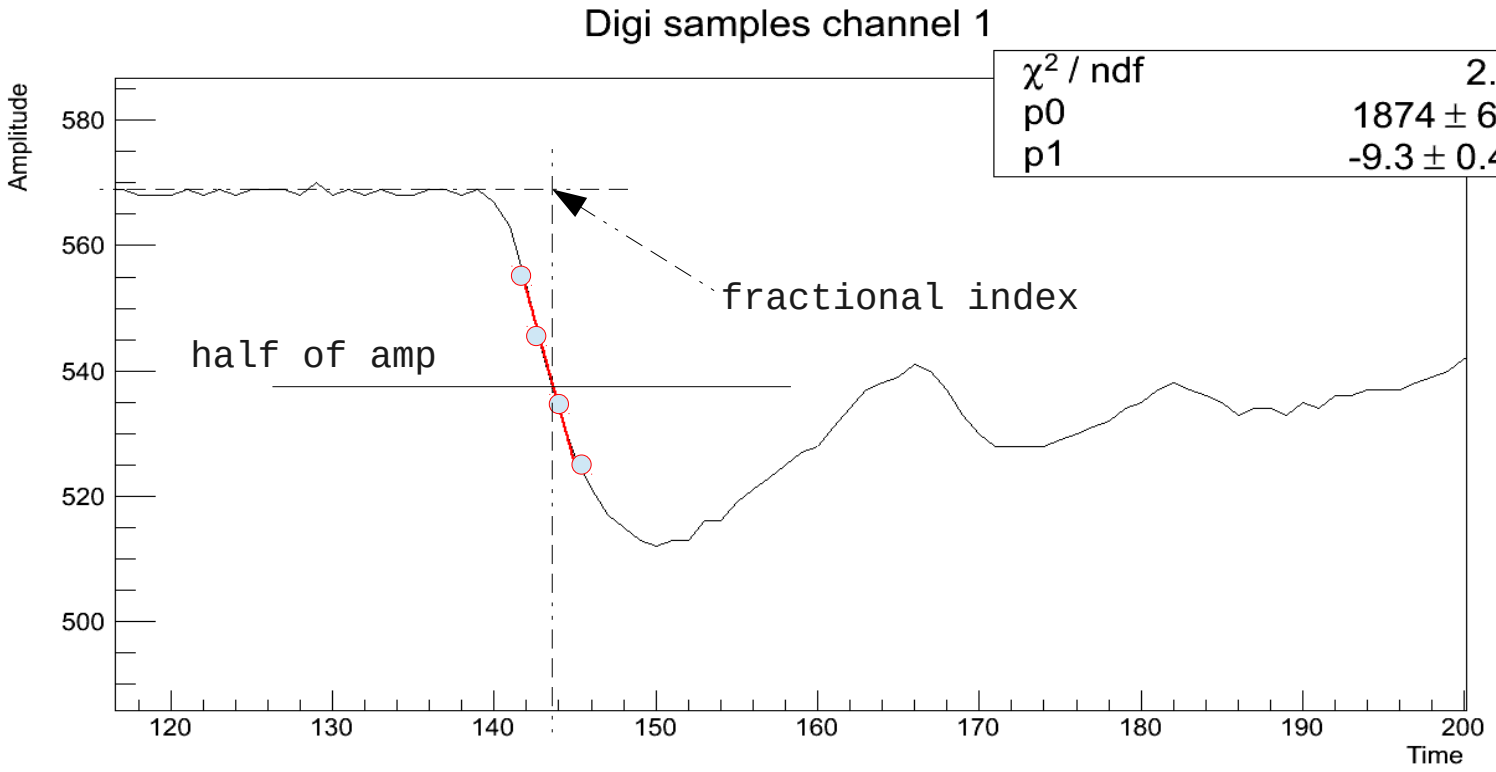


Improvement of the fits:

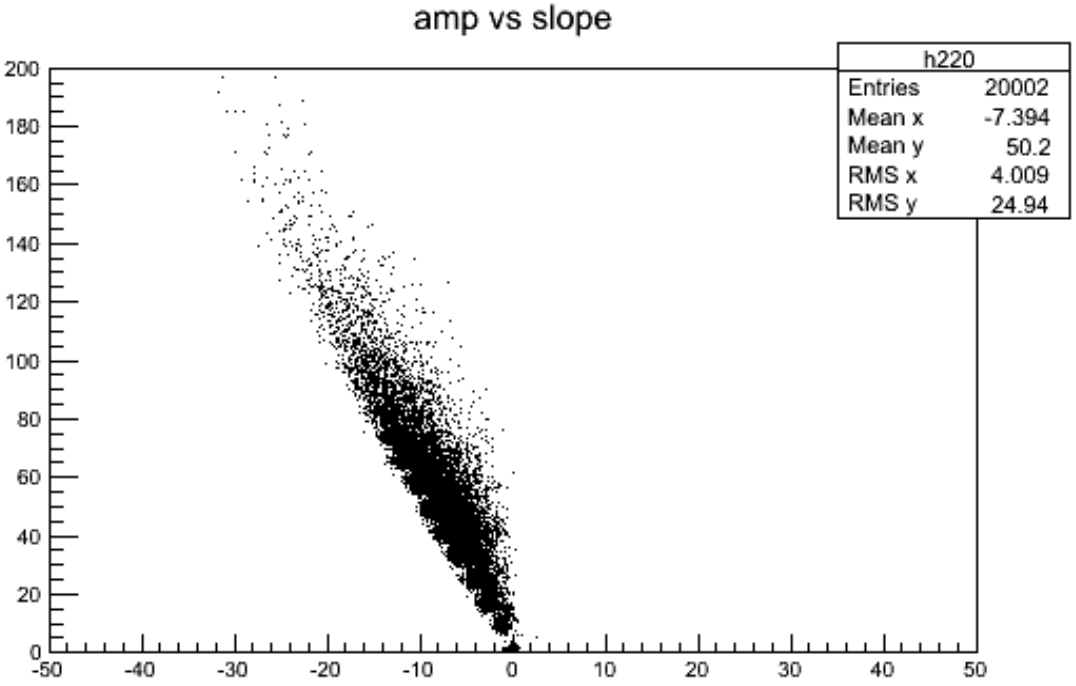
faster digitizer

rise time over 5ns

better fit function or
better shape signal



Four points for fit



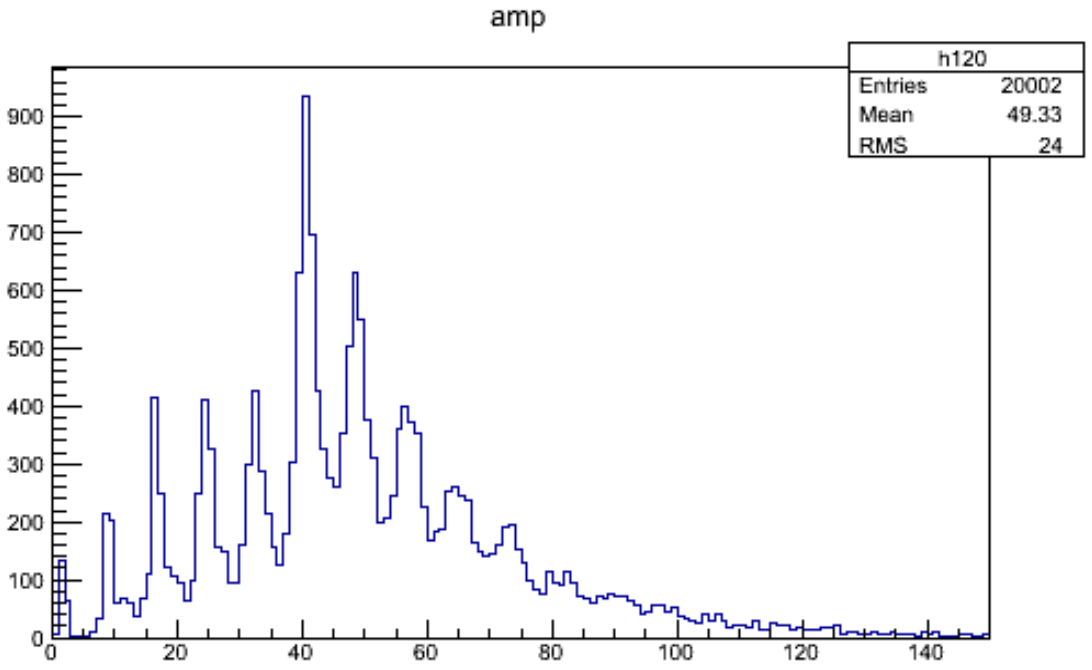
errors are caused by the small amplitudes

Improvement of the fits:

Variable no of points for small amplitudes

Faster digitizer

Use of the proper fit function

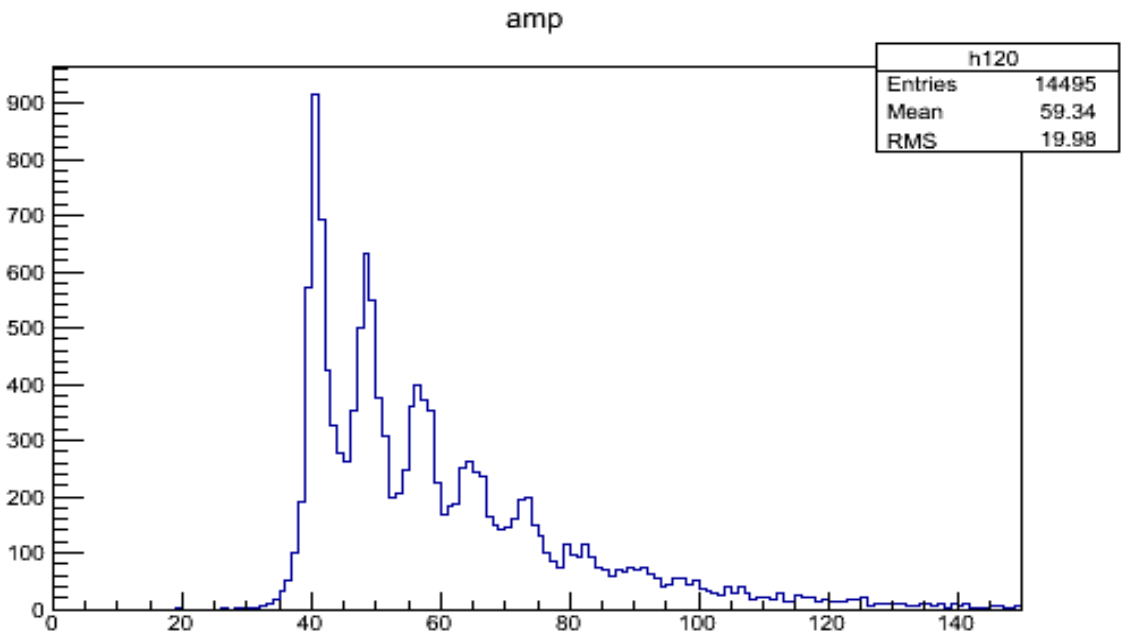


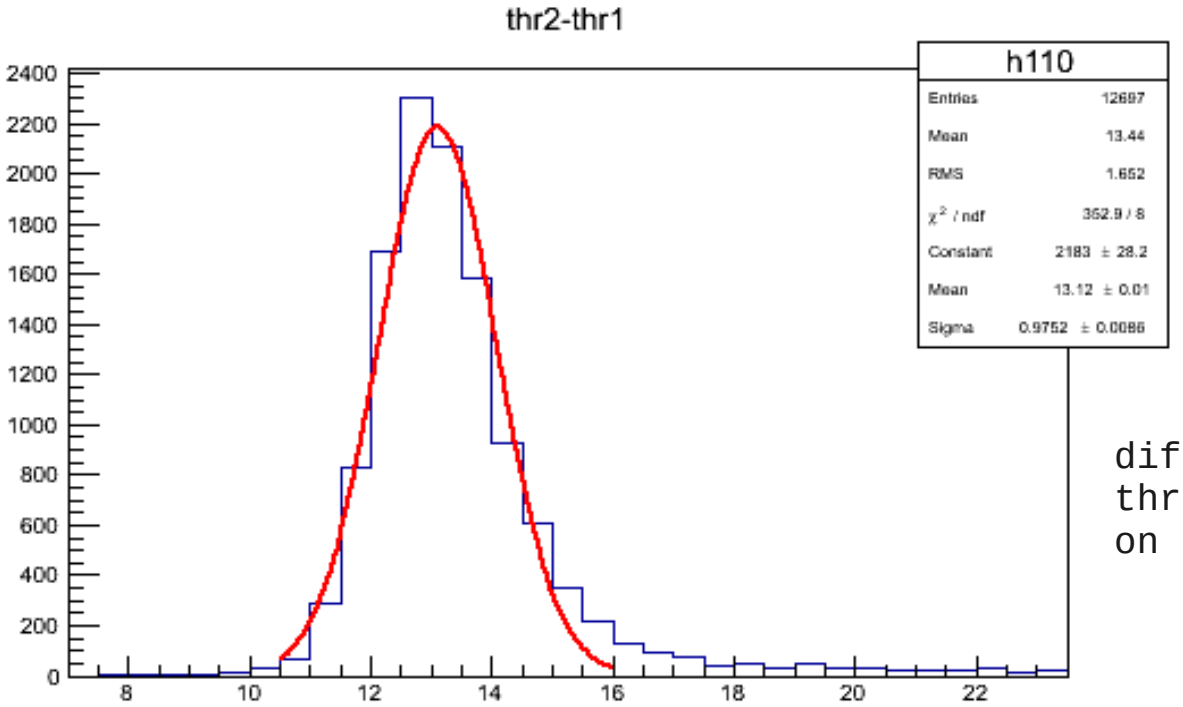
amplitude spectra

Tdc cut

Crosstalk at the digitizer level

Events are not seen on
the oscilloscope





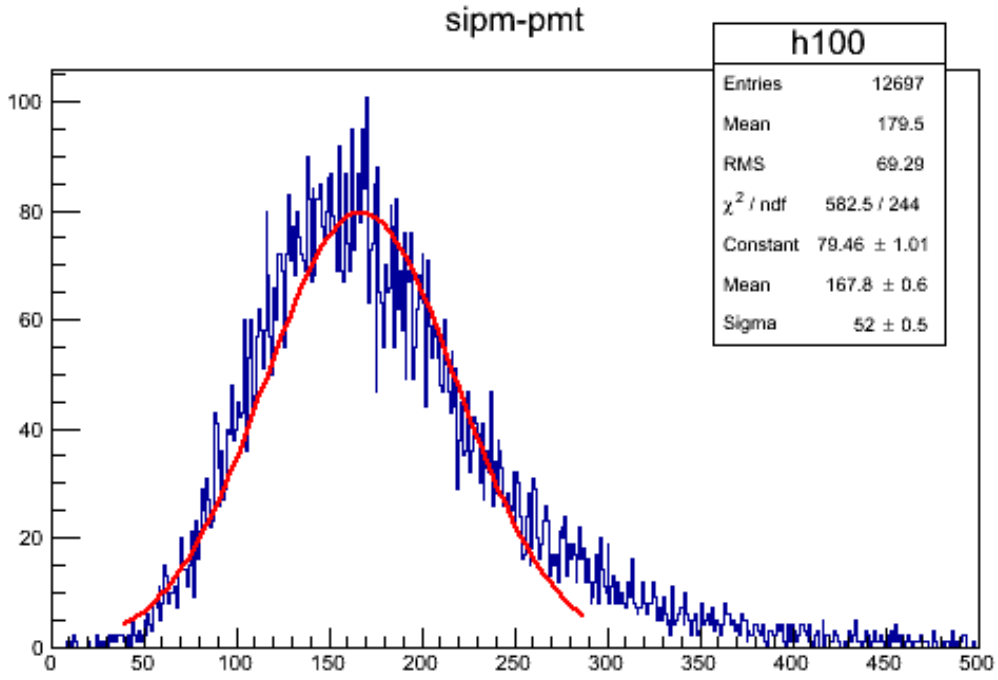
time spectra

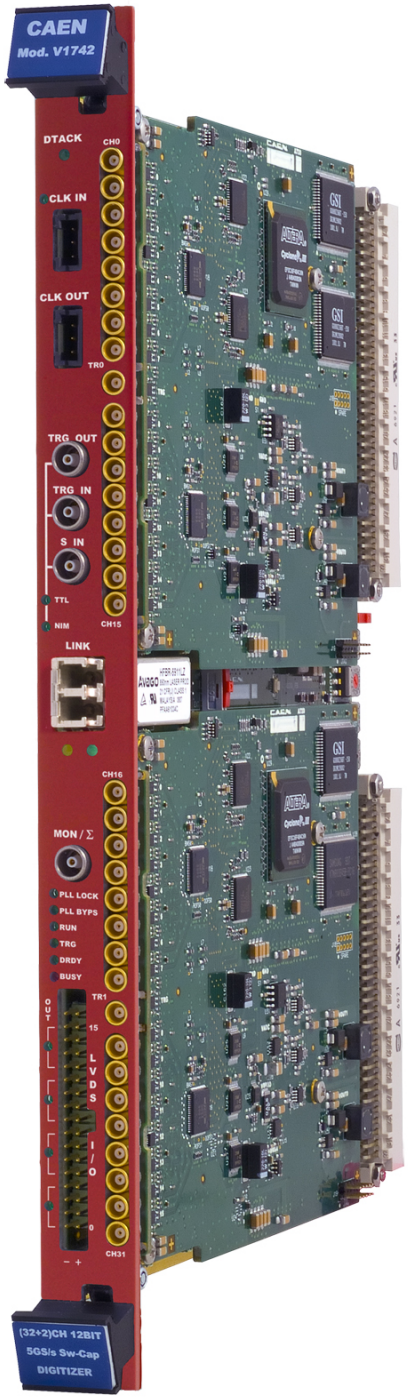
FWHM 2303 @1ns/ch

difference between half amplitude threshold on SiPM and fixed threshold on PMT

Bad resolution, but checking the tdcs:

FWHM 2810.6 @23ps/ch





Next steps: 1. a faster digitizer already in our lab!!!!

32+2 channel

12 bit; Selectable 5, 2.5, 1 GS/s Switched Capacitor ADC

1 Vpp input dynamics, single ended, 50 Ohm, MCX coaxial connectors

Based on DRS4 chip (Paul Scherrer Institute design)

1024 storage cells per channel (200 ns recorded time per event @ 5GSample/s)

Trigger Time stamps

Memory buffer: 128 events/ch (optional: 1024 events/ch)

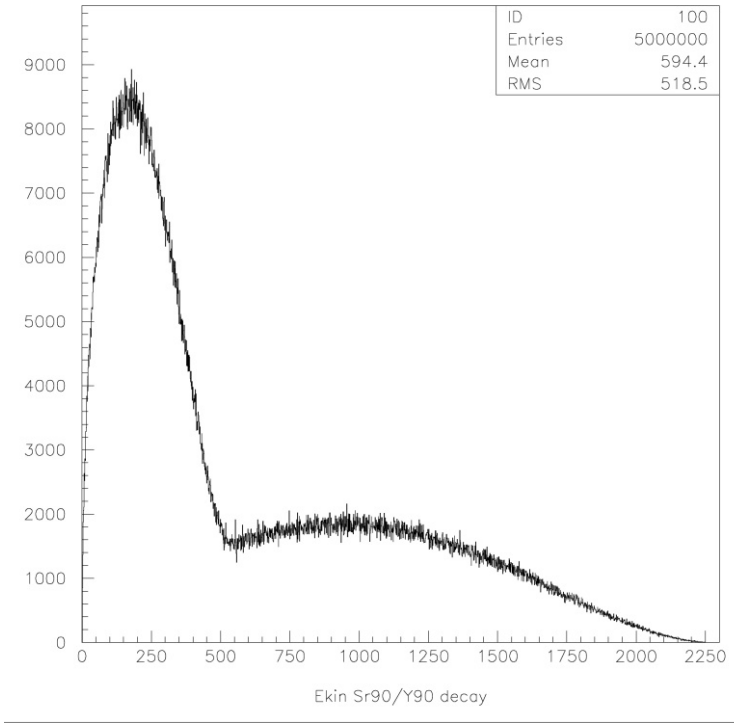
Dead Time: 110µs Analog inputs only, 181µs Analog inputs

The data throughput can be extremely high: it may be no possible to transfer raw data to computers!!!

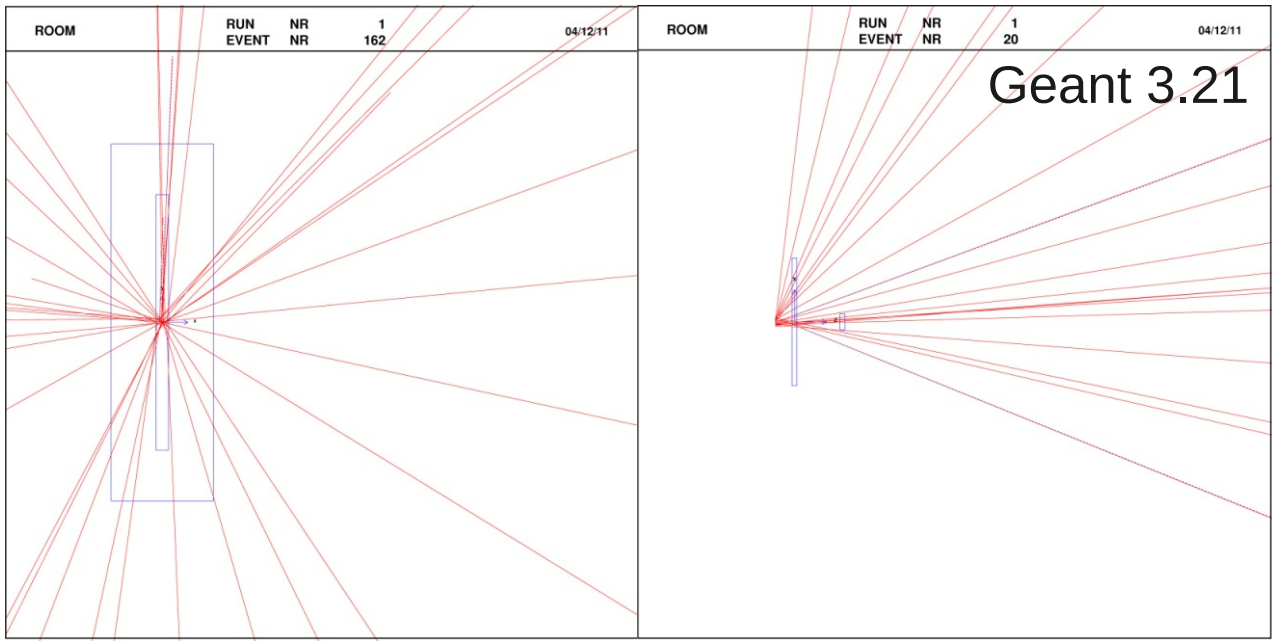
2. On-line Digital Pulse Processing

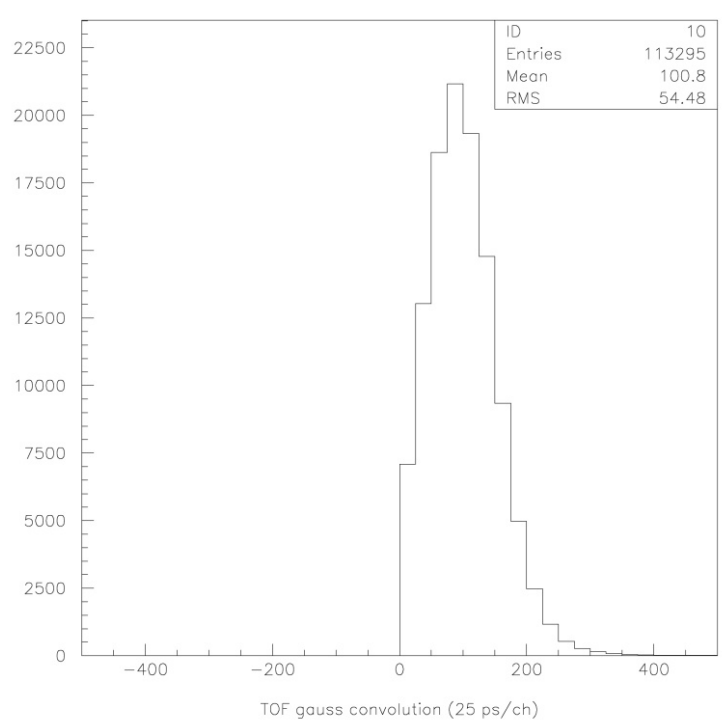
Digitizer FPGA programming

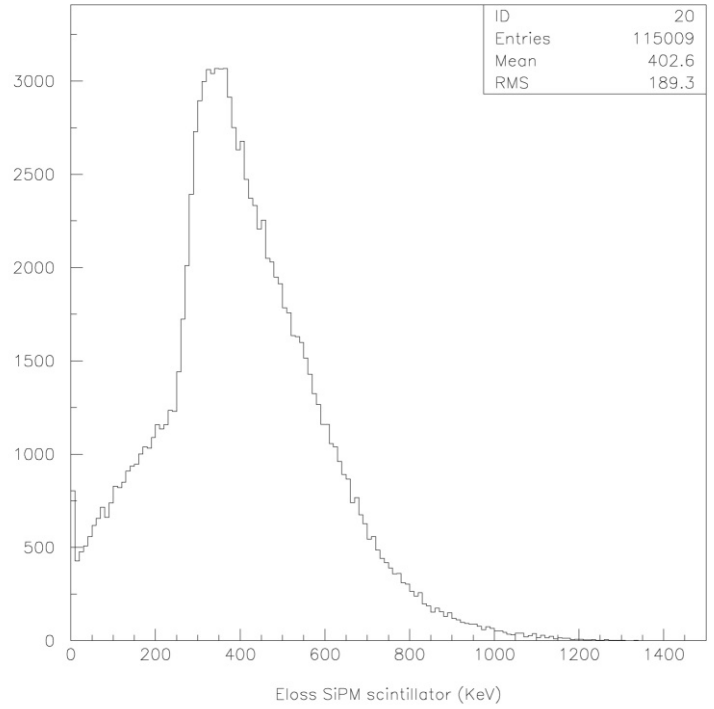
Thank you!



- Sr90 (T1/2=29 years, Q=0.546 MeV)
- Y90 (T1/2=64 hs, Q=2.28 MeV)







Monte Carlo:- 125-150 ps F.W.H.M.
4000 photons !!!