The Upgrade II of the LHCb RICH system

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On behalf of the LHCb RICH Collaboration

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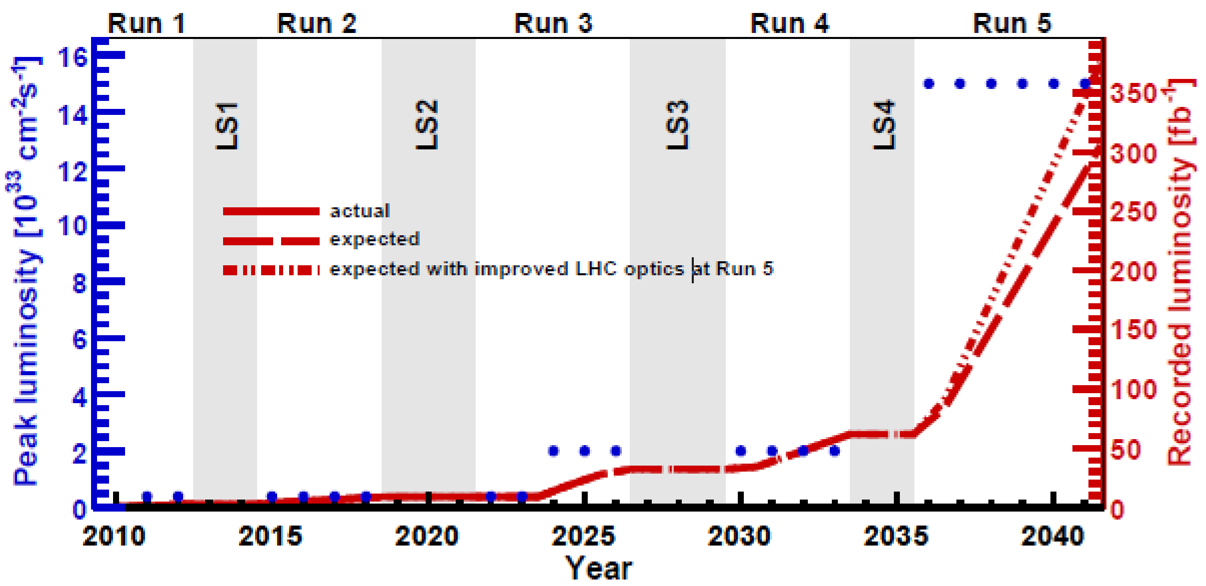
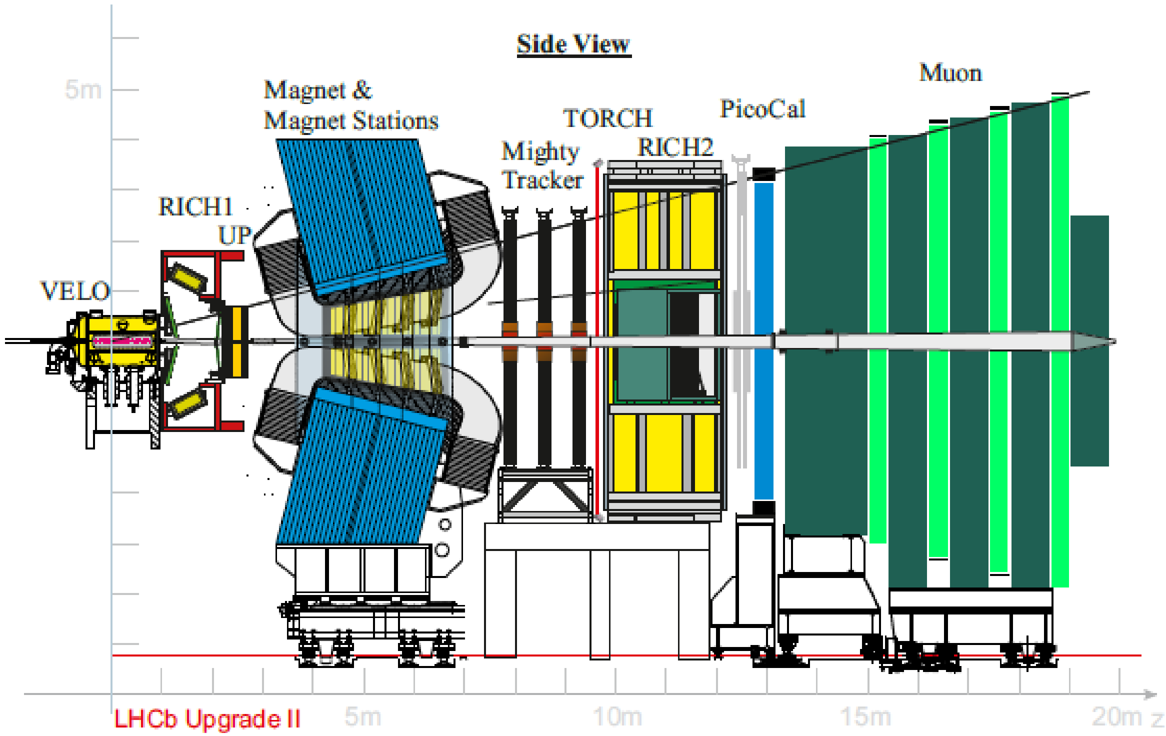
LHCb Upgrade 2

- **LHCb experiment [2010-2018]**
  - collected 9 fb^{-1} in LHC Runs 1 and 2
- **LHCb Upgrade I [2022 -]**
  - Collected ≈ 16 fb^{-1} so far
  - Aims at 50 fb^{-1} by the end of Run 4
- **LHCb Upgrade 2 [2036 -]**
  - 5x - 7.5x increase in peak luminosity
  - Aims to collect 300 fb^{-1}
  - Expression of Interest CERN-LHCC-2017-003
  - Physics case CERN-LHCC-2018-027
  - Framework TDR CERN-LHCC-2021-012
  - Scoping document CERN-LHCC-2024-010



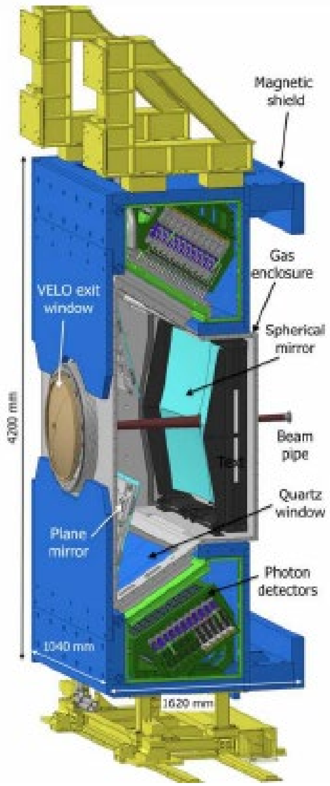


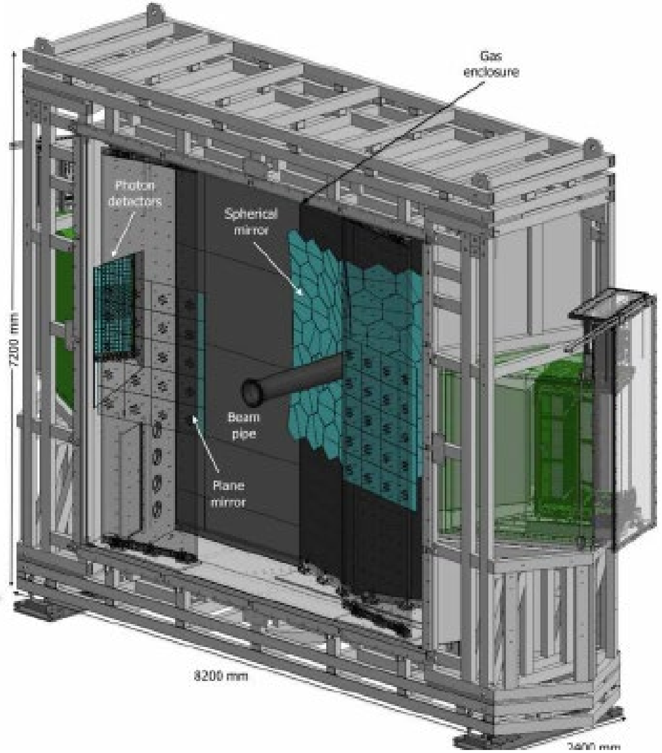
The RICH System

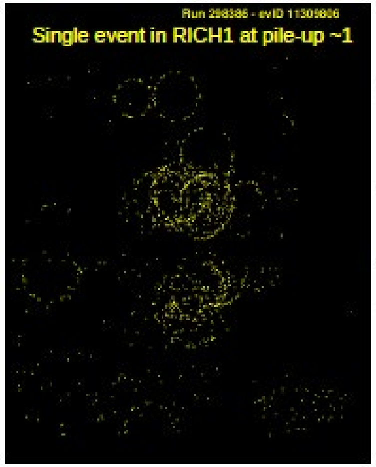
- **RICH 1**
  - 2 GeV/c - 40 GeV/c (C_4F_{10})
  - Upstram, covers 25 - 300 mrad
- **RICH 2**
  - 15 GeV/c - 100 GeV/c (CF_4)
  - Dowstream, covers 15 - 120 mrad
- System installed and operated in Run 1 & 2
- Upgraded during LS2 and operating since 2022

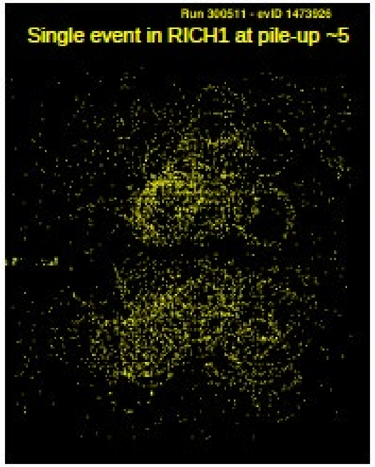
See talk by G. Cavallero:
The LHCb RICH detectors: operations and performance

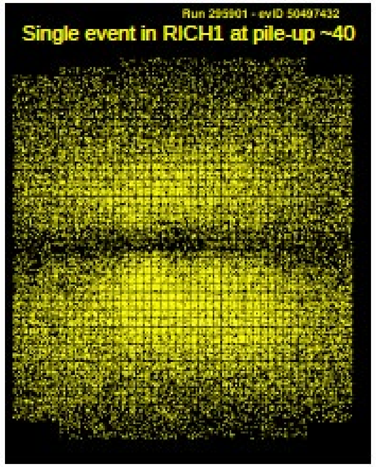
- **Goal for Upgrade 2**:
  Maintain the same (or better) PID performance of Run 3 with a 5x - 7.5x higher luminosity
  - Much harsher conditions (pile-up, radiation, …)
  - Tightly constrained detector envelope





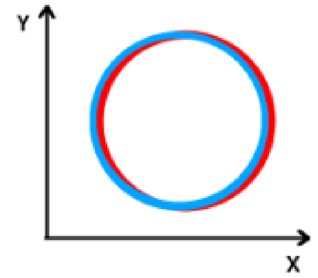


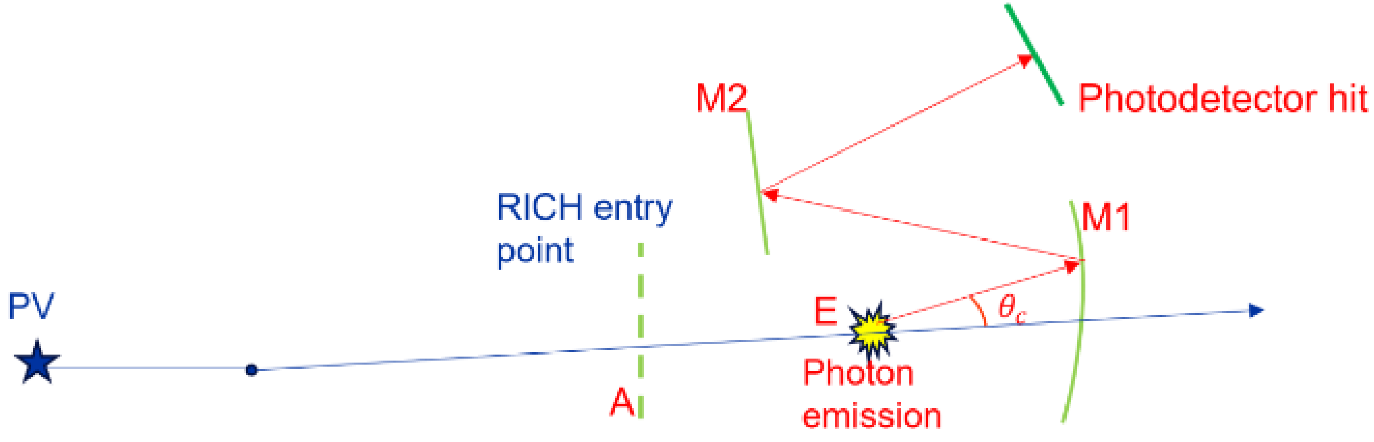


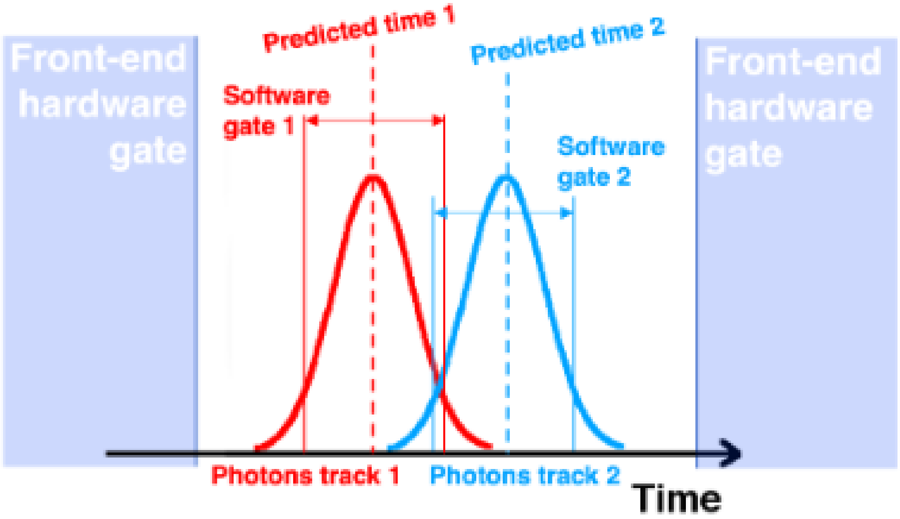


Timing in the LHCb RICH (1)

- The time of arrival of Cherenkov photons from a given track can be predicted to ≈**10 ps**
  - The emission of Cherenkov photons is prompt
  - Different photon paths inside the radiator cancel out
- A hardware gate (**a few ns**) can be used to reject background (6.25 ns already implemented in Run 3)
- Fine timing (≈**100 ps**) can help to separate Cherenkov rings



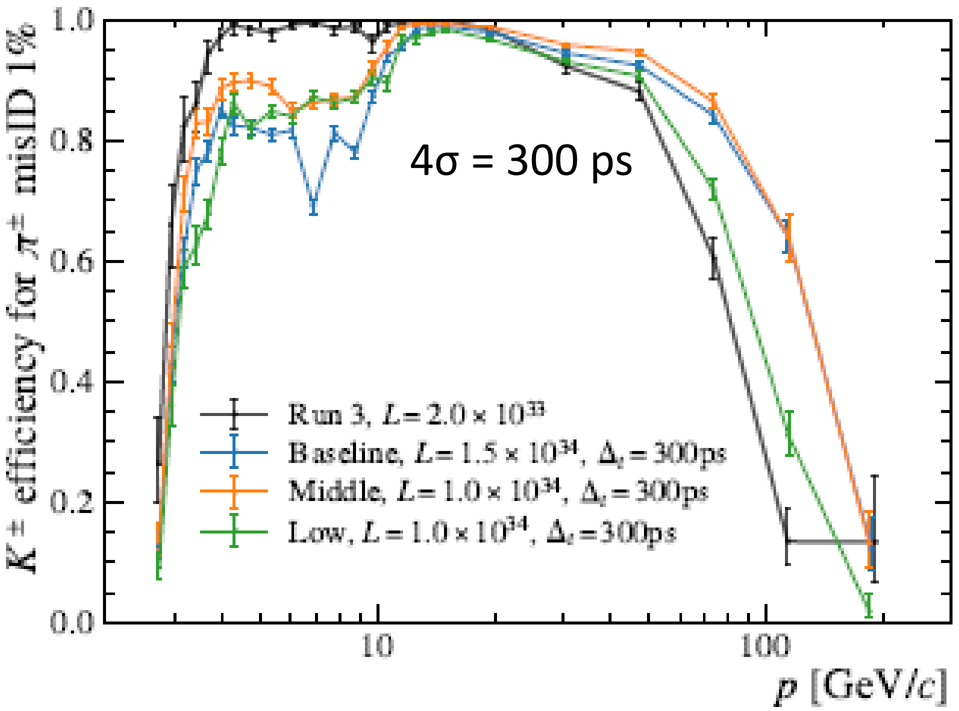


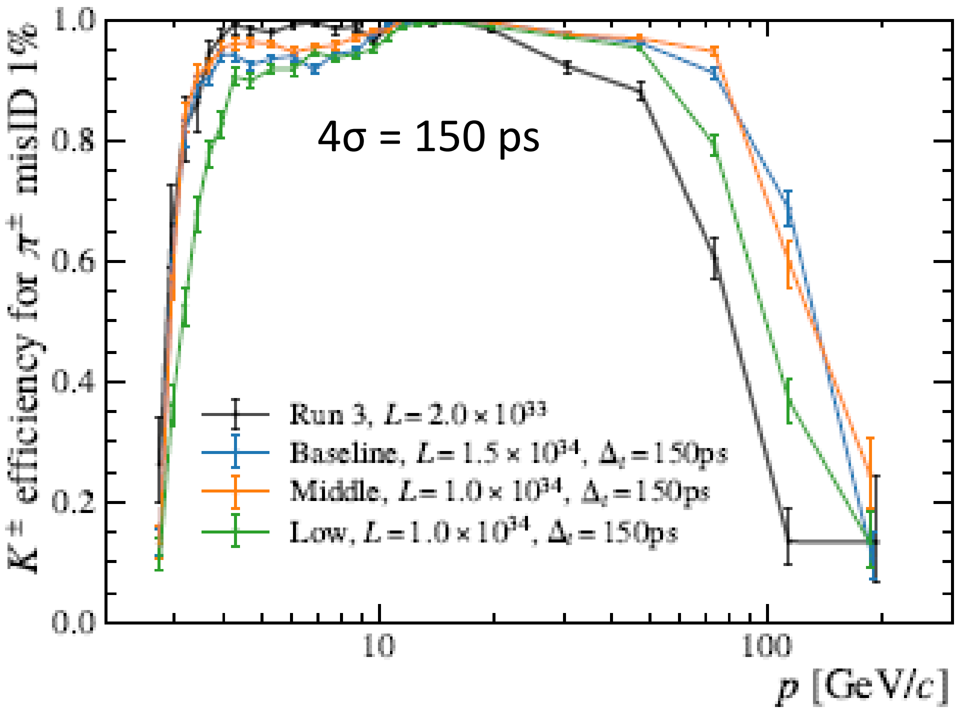


See talk by A. Upadhyay:
Primary vertex time reconstruction using the LHCb RICH detectors

Timing in the LHCb RICH (2)

- Introducing timing in the LHCb RICH detector is a powerful tool to recover PID performance at high pile-up
  - Black curve: Current PID performance (Run 3, simulated)
  - Coloured curves: x5 – x7.5 luminosity (Upgrade 2 scenarios)
  - Better time resolution translates directly to better PID





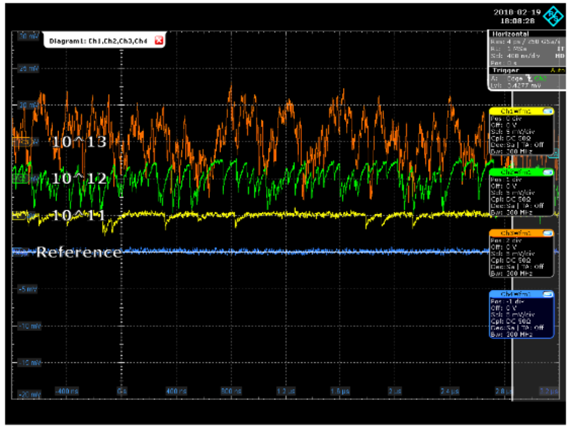
Photon Detectors

- **Multi-anode PMTs** are used in the present (Upgrade I) RICH system
  - Pixels of ≈ 3x3 mm^2, timing not great (≈ 150 ps RMS)
  - Peak occupancy is already ≈30% in the central region of RICH1 (≈10^6 photons/s/mm^2)
  - Without a significant increase in the focal length, pixels of 3x3 mm^2 are too large
  - May still be used in Upgrade 2 in low occupancy regions, as a backup solution

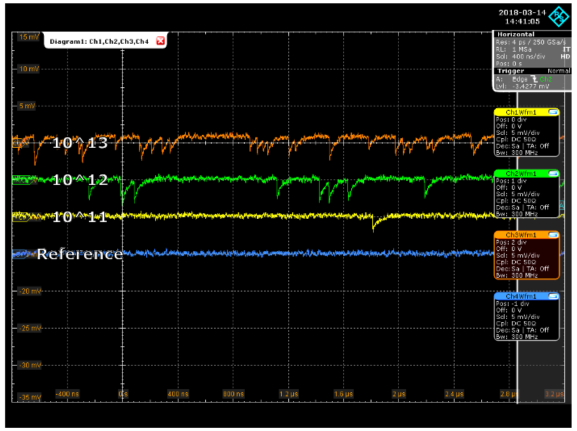
- **SiPMs** are the most promising candidates
  - Small pixels, good timing, high QE
  - **Fluence of a few 10^{13} n/cm^2** before shielding, no safety factor
    - Require shielding and annealing
    - Need cooling to very low temperature (likely down to LN2)
    - Might require replacing during the run

- **MCP-PMTs**
  - Ideal for time resolution, pixels size, radiation tolerance
  - Typically **saturate** at ≈100 kHz/mm^2, 1-2 orders of magnitude below the expected photon rate in high occupancy regions of RICH1 in Upgrade 2

Hamamatsu s13360-1350cs
(state of the art)
https://doi.org/10.1016/j.nima.2019.01.013



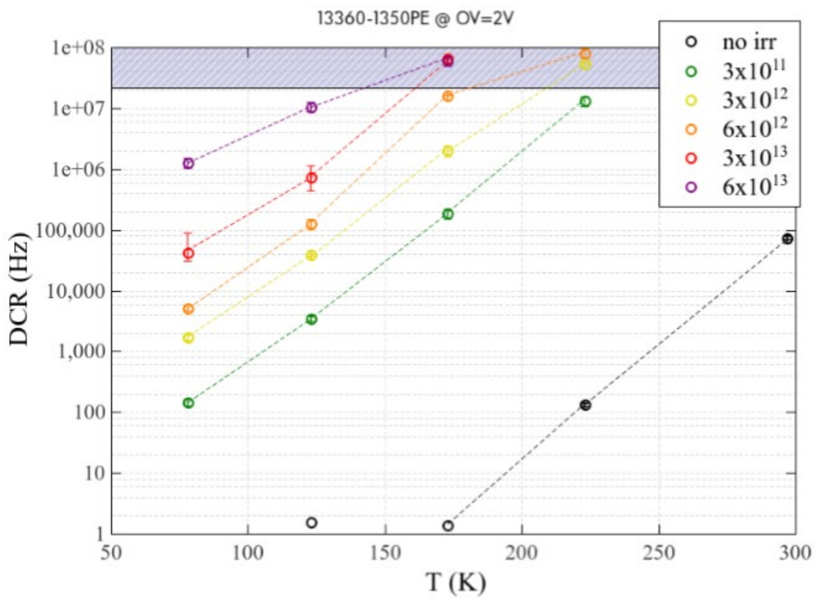
-30°C before annealing



-30°C after annealing
(weeks at 175°C)
DCR still too high

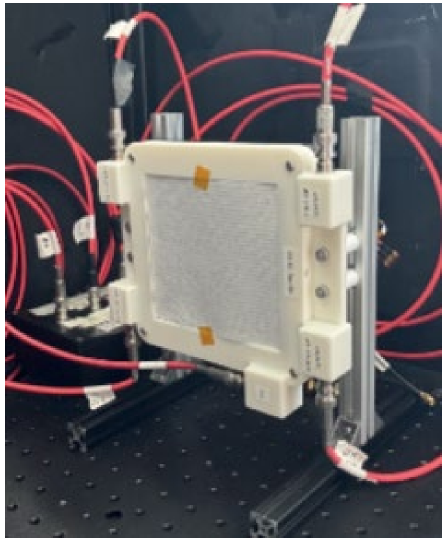
Photon Detector R&D

- SiPMs R&D:
  - Commercial SiPMs at a few 10^{13} n/cm^2 are severely damaged
  - Dark count rate ≈ 1 MHz/mm^2 already at 77 K and reduced overvoltage (2V)
  - Annealing not yet considered
  - Gain and time resolution are not significantly affected by neutron fluence
  - R&D ongoing with Hamamatsu and FBK to develop custom devices with better radiation tolerance



See poster by M. Guarise:
Characterization of SiPMs for the LHCb RICH Detectors Upgrade-II

- MCP R&D:
  - High Rate Picosecond Photodetector (HRPPD) from Incom shows promising increase of rate capability compared other MCP-PMTs

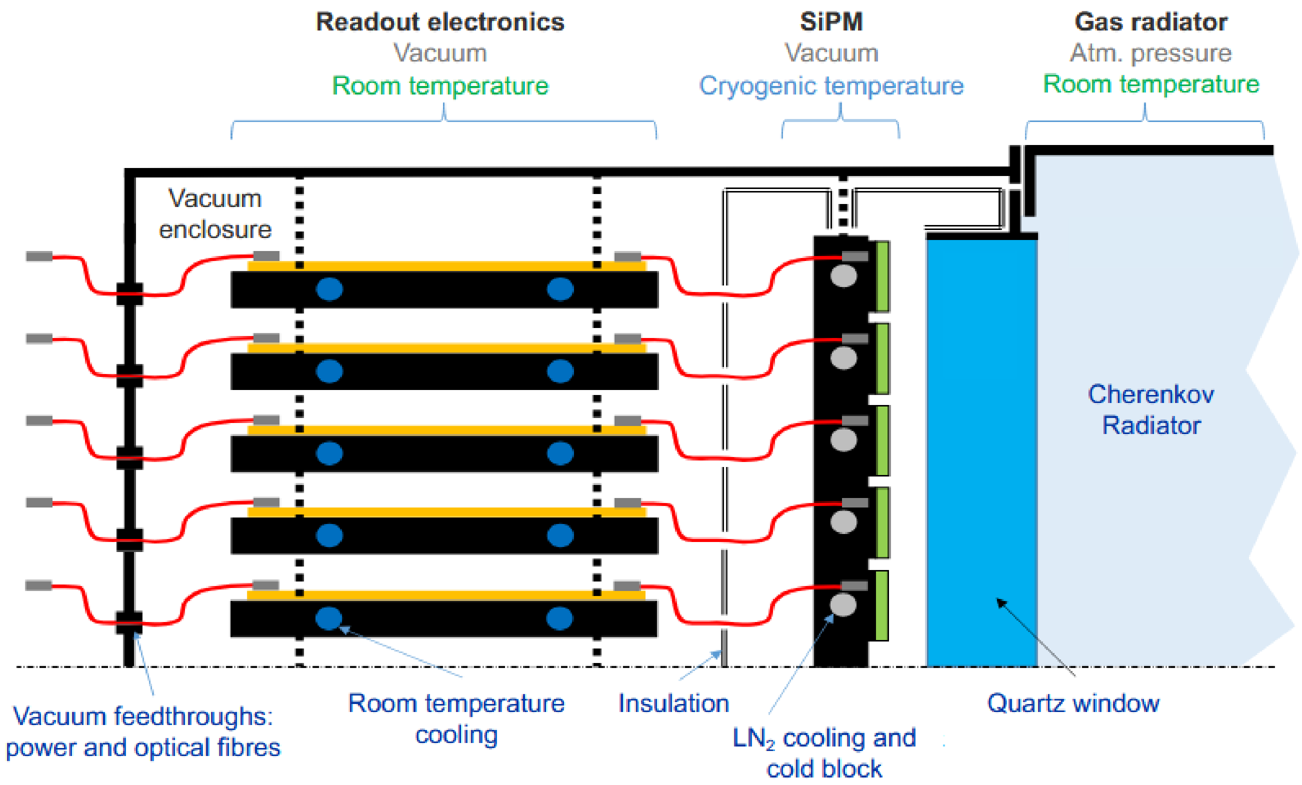


See poster by D. Foulds-Holt:
Large Area Picosecond Photodetector for the Upgrade II of the LHCb RICH

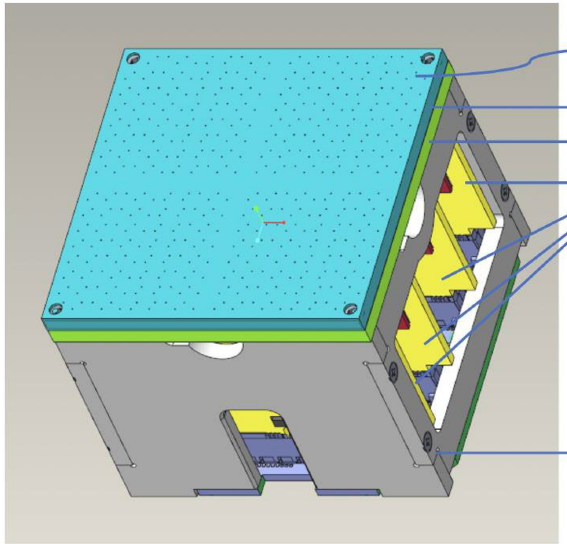
Photon Detector Cooling

- Cryostat concept:
  - Thick (≈50 mm) transparent window between the photodetector plane and the gas enclosure
  - SiPMs at LN2 temperature
  - SiPMs and front-end electronics in vacuum, connected by a flex PCB
  - Extremely challenging

See poster by L. Malentacca:
A cryogenic RICH detector demonstrator for SiPM operation with integrated flex-PCB electronics



- Possible alternative:
  - Locally cool the SiPMs to -60°C or -80°C
  - SiPM mounted on a ceramic PCB with carved cooling pipes
  - Viable if R&D on SiPMs results in improved radiation tolerance, and/or if SiPMs can be replaced periodically

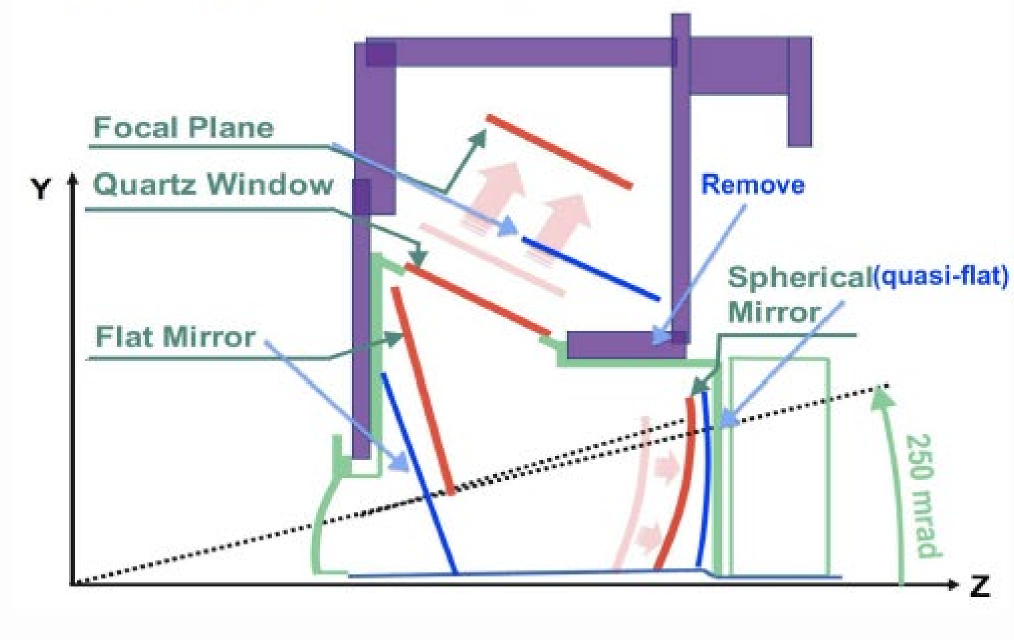


RICH Optics (1)

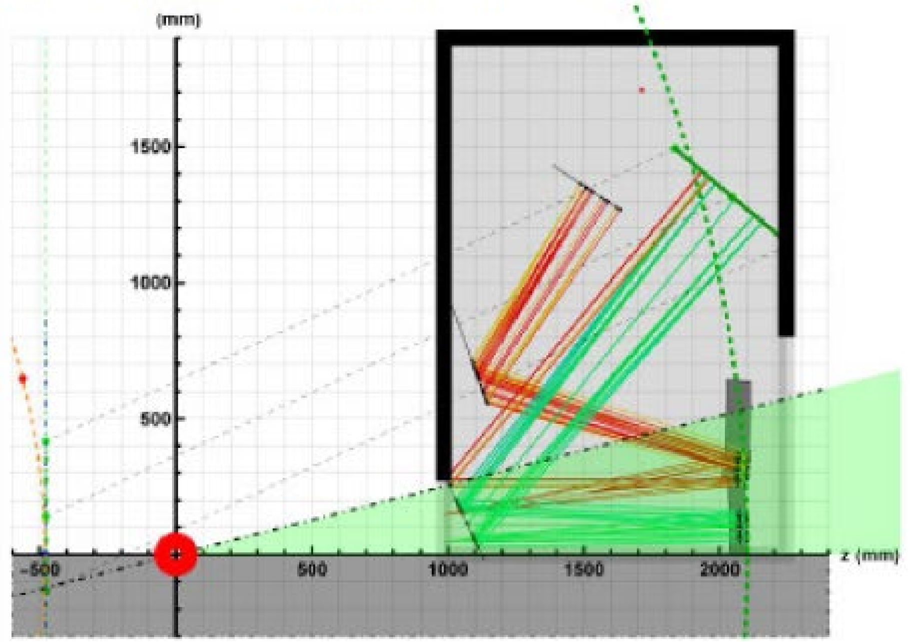
- **Move flat mirrors in the acceptance**, to reduce aberration and improve emission point error
- **Increase the radius of curvature** of spherical mirrors, to reduce occupancy and improve pixel error
  - Upper limit due to contraints on the overall detector envelope

- Two layouts under study, single and split optics

FTDR design for RICH1



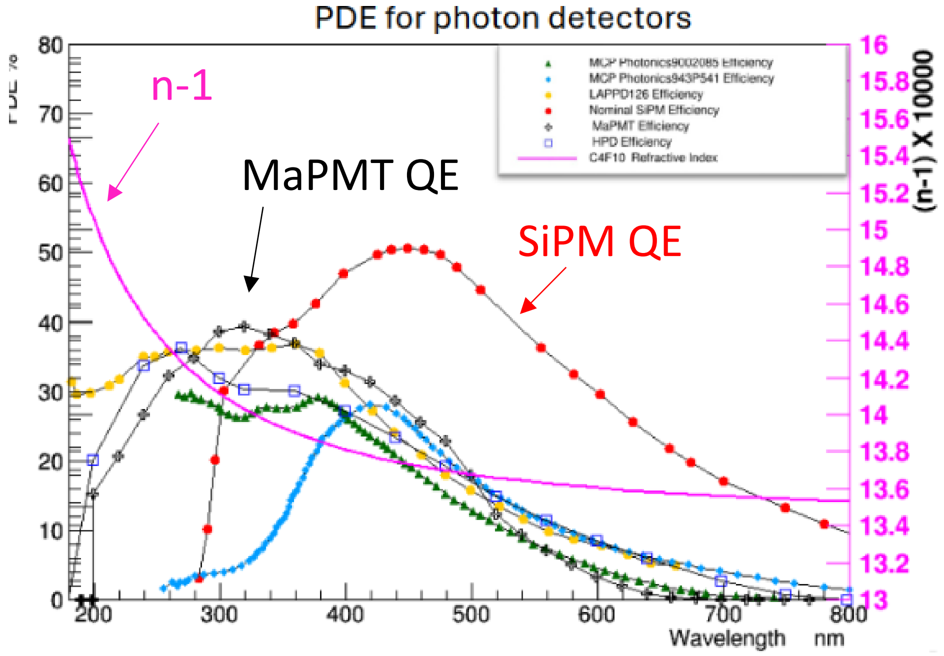
Split optics design for RICH1



RICH Optics (2)

- Both options improve the Cherenkov angle resolution by a factor ≈2 compared to current (Run 3)
- SiPMs as photon detectors also help (smaller pixels, higher QE at longer wavelength)
- Studies still ongoing

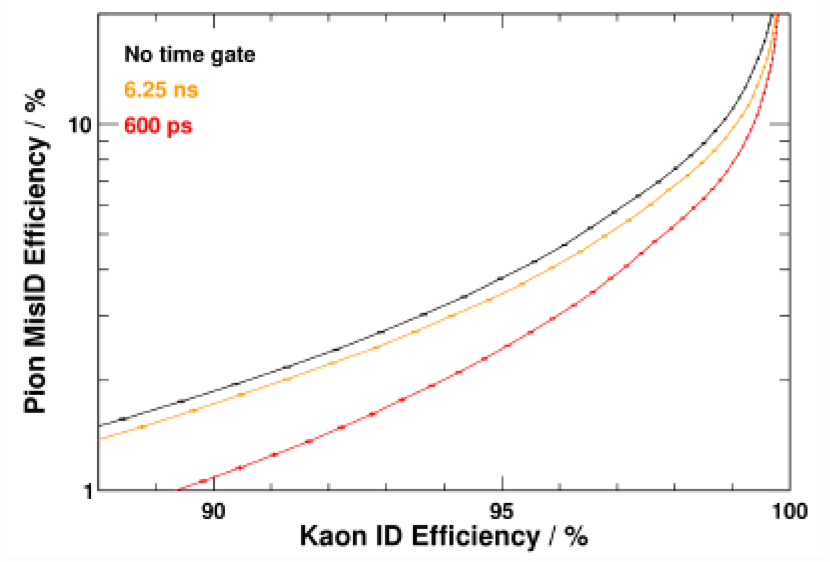
	Total [mrad]	Chr. [mrad]	Emis.Pt [mrad]	Pixel [mrad]	Yield
Split-Optics/MaPMT	0.71	0.59	0.15	0.38	50
Split-Optics/SiPM-Hamamatsu	0.37	0.30	0.12	0.14	56
Split-Optics/SiPM-FBK	0.38	0.33	0.12	0.13	57
Run3/MaPMT	0.83	0.58	0.37	0.46	59
Run3/SiPM-Hamamatsu	0.59	0.34	0.45	0.18	68
FTDR/MaPMT	0.75	0.58	0.16	0.44	48
FTDR/SiPM-Hamamatsu	0.42	0.31	0.13	0.17	53

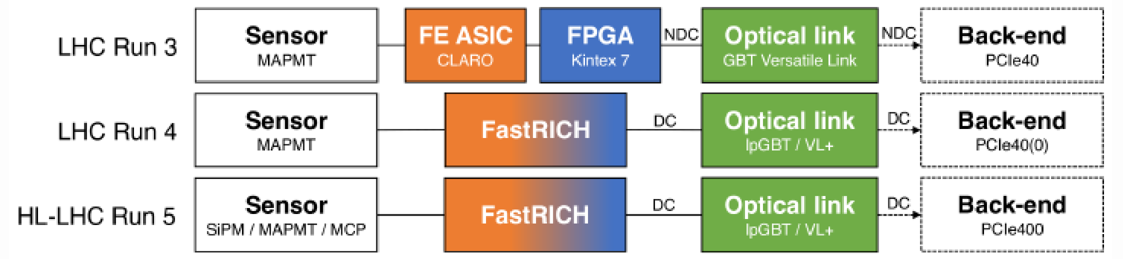


See poster by E. Spadaro Norella:
Optimized optical design of the LHCb RICH detectors for Upgrade-II

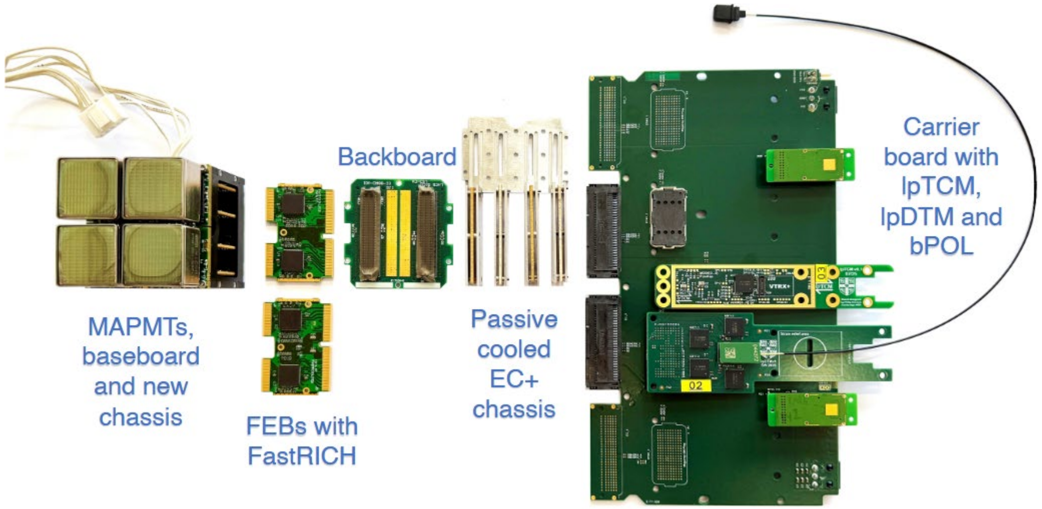
LS3 Enhancements

- Introduce time stamp of Cherenkov photons already in Run 4
- Keep MaPMTs, replace the front-end electronics
  - FastRICH ASIC with 25 ps TDC bins, potentially ready for Upgrade 2
  - Prototypes received in May 2025: under test
  - Timing in Run 4 will be limited by photon detectors to ≈150 ps RMS
  - Expected improvement in PID performance already in Run 4
- PID Enhancement TDR [CERN-LHCC-2023-005]





	Sensor [σ]	ASIC time walk	FE time gate	TDC time bin
LHC Run 3	150 ps	< 4 ns	6.25 ns	None
LHC Run 4	150 ps	CFD correction	2 ns	25 ps
HL-LHC Run 5	~ 50 ps	CFD correction	2 ns	25 ps

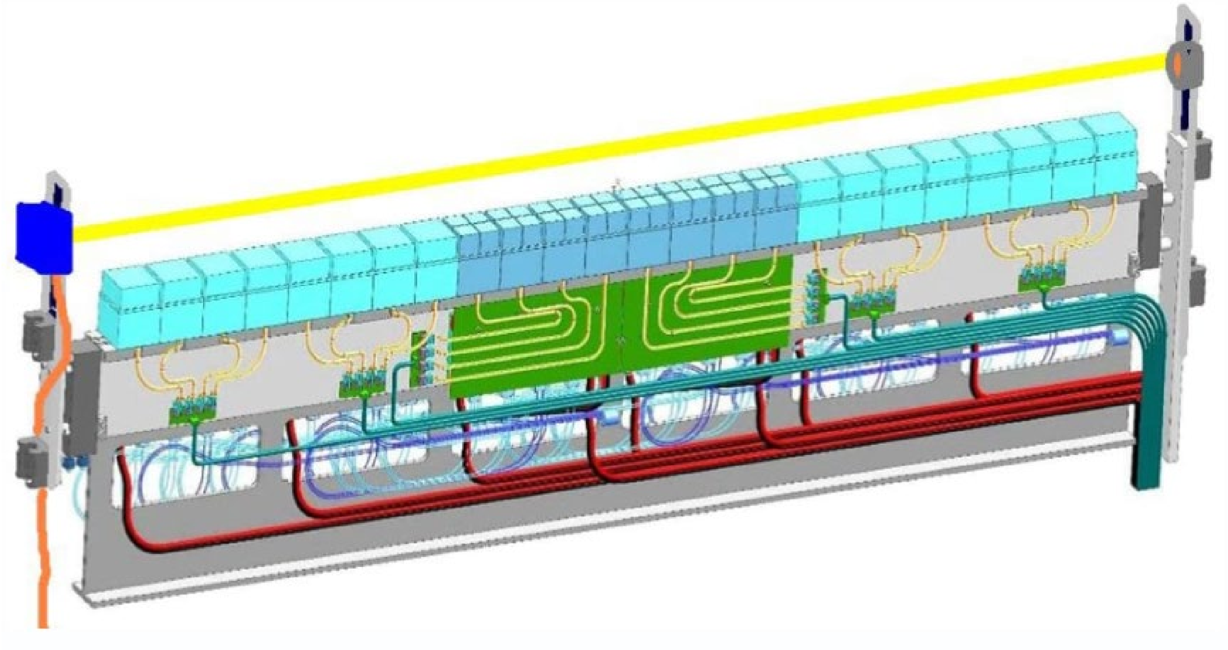


See poster by V. Placinta:
The LS3 Enhancement of the RICH detectors

See poster by F. Keizer:
The FastRICH ASIC for next-generation RICH detectors

Calibration and alignment

- A calibration, alignment and monitoring system («CalAliMon») based on Rayleigh scattering
  - Pulsed laser beam parallel to the photon detector plane
  - Scattered photons result in uniform illumination with good time resolution
  - Plans to deploy it during LS3 and keep it for Upgrade 2



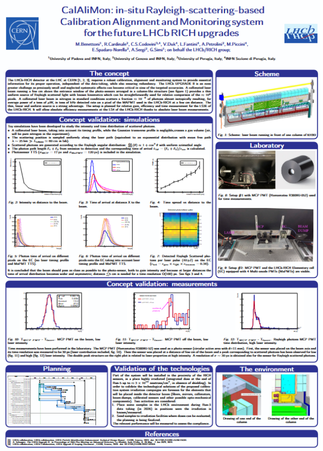
See poster by R. Cardinale:
CalAliMon: In-Situ Rayleigh-Scattering based Calibration Alignmnent and Monitoring system for the future LHCb RICH upgrades

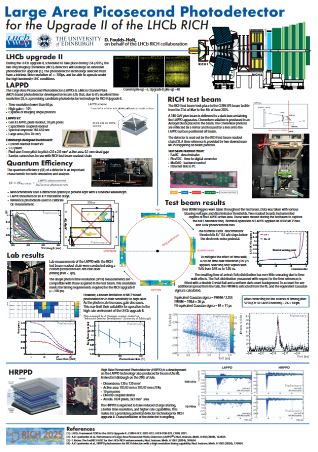
Conclusions

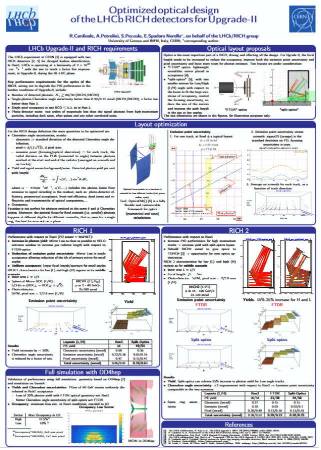
- The LHCb Upgrade 2 poses unprecedented challenges for a RICH detector
- Strong synergy with DRD4 in all areas, but shorter time scale

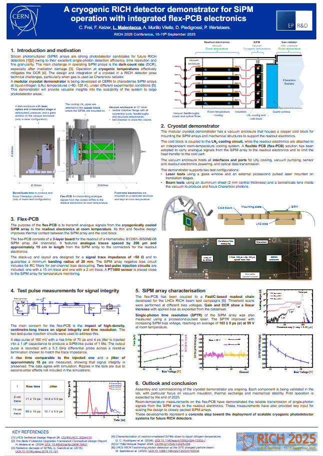
- R&D ongoing on all fronts:
  - Photon detectors
  - Cooling
  - Optics
  - Mechanics
  - Fast electronics
  - Calibration and Alignment

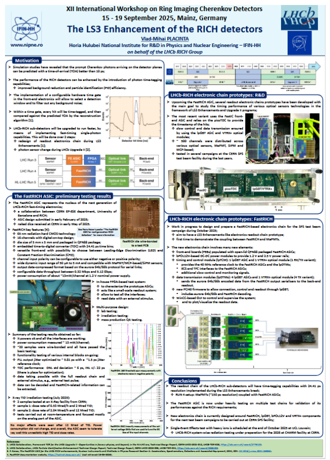
- **Thank you!**
- These is still time to go into details with our poster presenters…
- …and plenty of work for anybody willing to join!

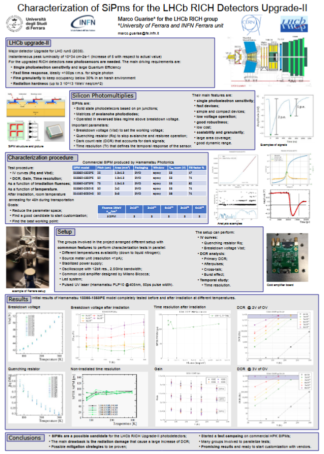


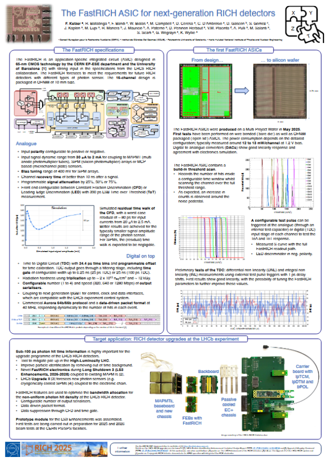










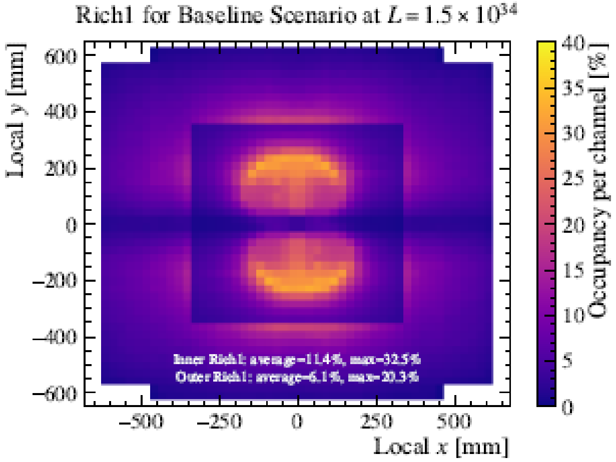


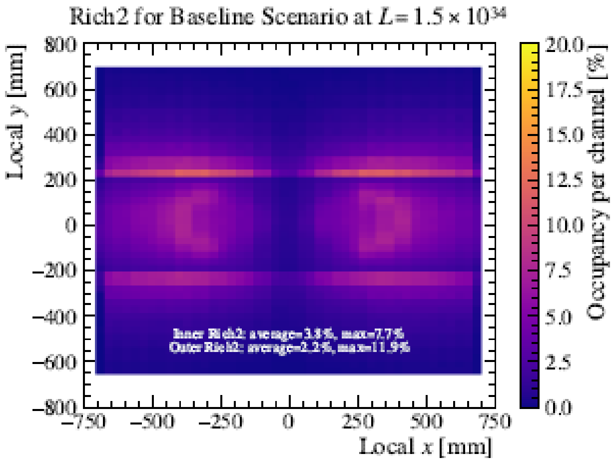
Spare slides

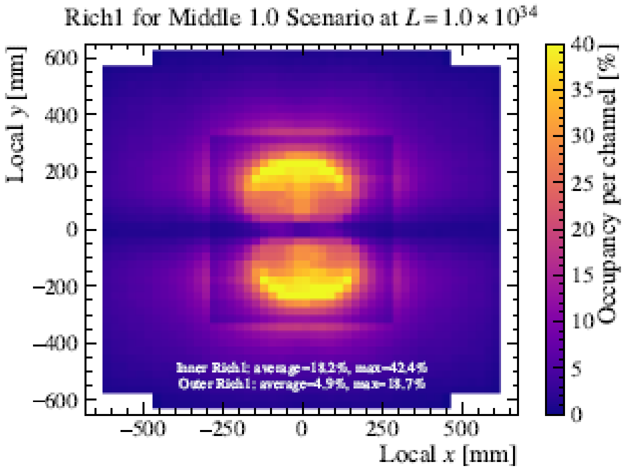
Scoping scenarios

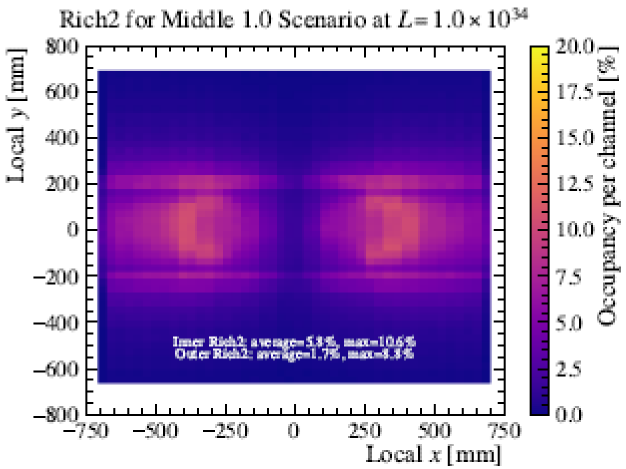
Baseline	**Middle**	**Low**
$1.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$	$1.0 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$	$1.0 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$
	RICH1/2	
inner:outer $\frac{1}{3}$:$\frac{2}{3}$	inner:outer $\frac{1}{4}$:$\frac{3}{4}$	inner:outer $\frac{1}{4}$:$\frac{3}{4}$
inner 1.4 mm SiPM	inner 2.0 mm SiPM	inner 2.0 mm SiPM
outer 2.8 mm SiPM	outer 2.8 mm SiPM	outer 2.8 mm MaPMT
new optics	new optics	new optics (RICH1 only)
750,000 channels	469,000 channels	445,000 channels

Scenario	High occupancy area	Pixel size in high occupancy area	Pixel size in low occupancy area	Readout channels	New optical layout
Baseline	1/3	$1.4 \times 1.4\,\mathrm{mm}^2$	$2.8 \times 2.8\,\mathrm{mm}^2$	750,000	RICH1, RICH2
Middle	1/4	$2.0 \times 2.0\,\mathrm{mm}^2$	$2.8 \times 2.8\,\mathrm{mm}^2$	469,000	RICH1, RICH2
Low	1/4	$2.0 \times 2.0\,\mathrm{mm}^2$	$2.8 \times 2.8\,\mathrm{mm}^2$	445,000	RICH1



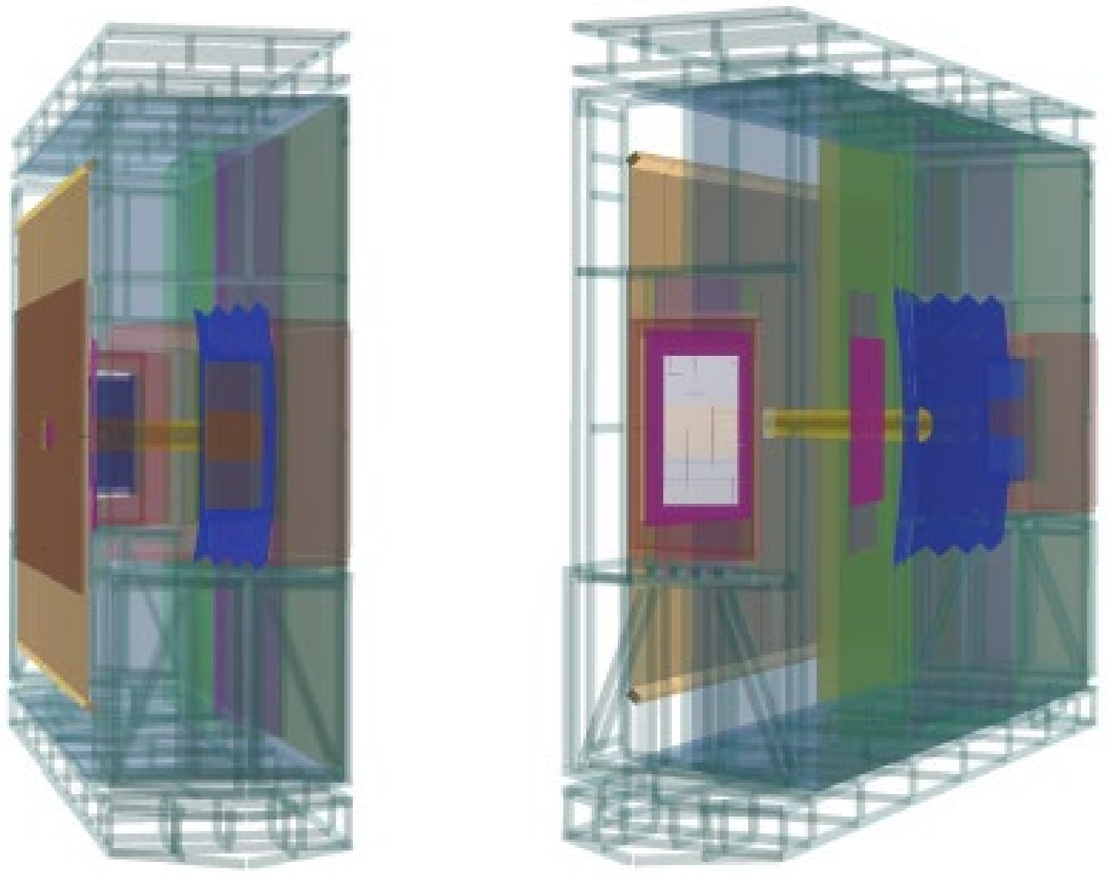






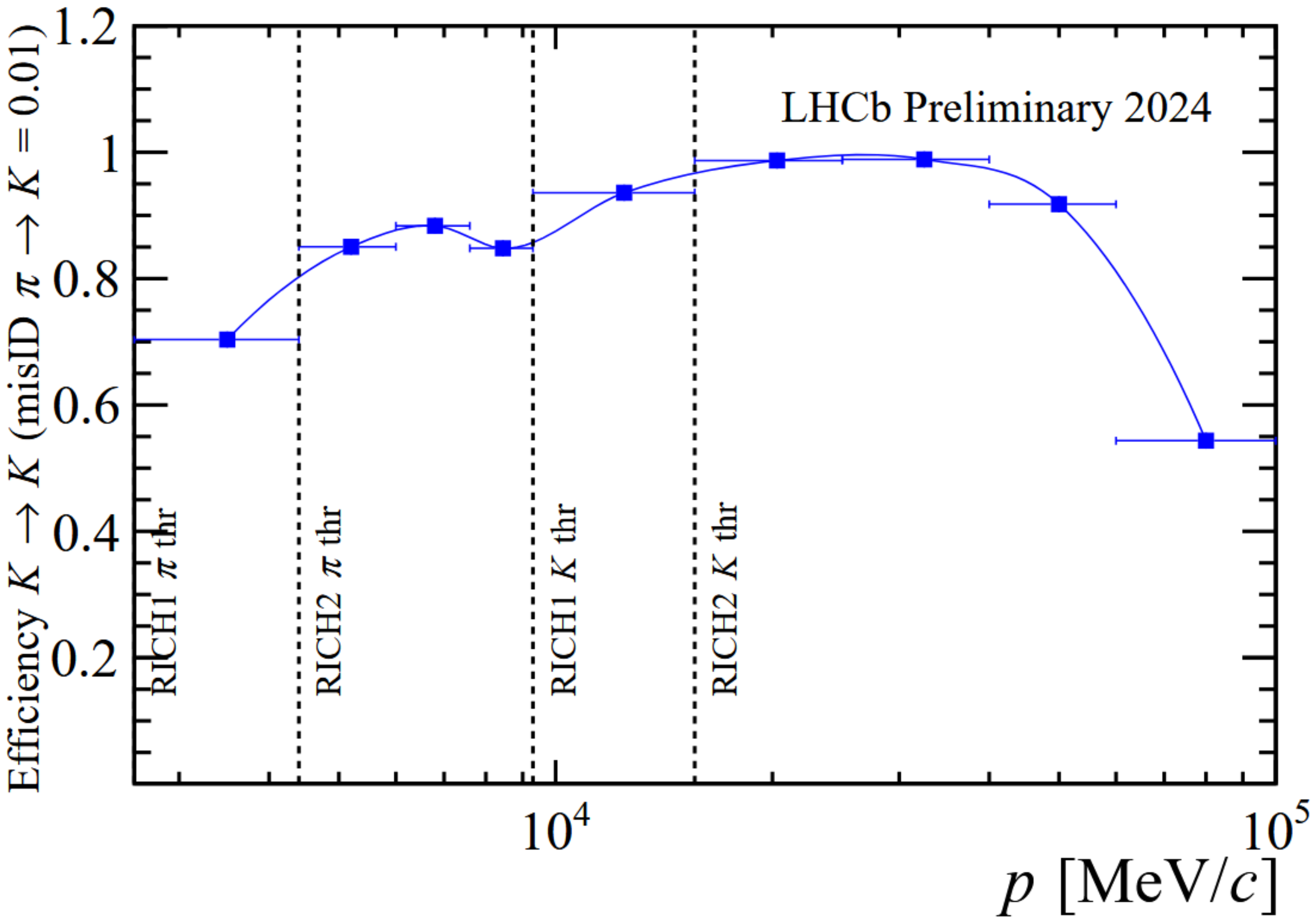
RICH+TORCH

- TORCH could improve the overall LHCb PID by complementing the RICH at low momenta
- TORCH integration forces reworking the RICH2 vessel
- Combined performance studies are ongoing



TORCH inside RICH2

Run 3 performance



FastRICH

Parameter	Specification
Technology	65 nm CMOS
Die dimensions / # of pads	$5 \times 5\,\text{mm}^2$ / $\mathcal{O}(100)^2$
Package / sensor coupling	QFN88
Radiation hardness	Yes (TID > 100 Mrad and triplication)
# of channels	16
Channel type	Linear (i.e. not pixelated)
Channel connection	Single-ended
Polarity	Configurable positive or negative
Input signal attenuation	Configurable per channel: 0, 25%, 50%, 75%
TDC time bin	25 ps
Electronics time jitter	~ 40 ps RMS for 50 μA pulses. ~ 30 ps RMS for pulses above 100 μA.
Residual time walk	< 200 ps pk-to-pk (after CFD, over 50 μA to 5 mA range)
CFD recovery time	15 ns
Time gate	2 ns nominal, configurable width and offset to the 40 MHz clock
Power consumption analog	Target < 4.5 mW * per channel
Power consumption digital	~ 2 mW per channel
Energy resolution	Non linear (not required when CFD is implemented).
Dynamic range	5 μA to 5 mA **
Maximum front-end rate	Ability to detect signals spaced by 25 ns
Testing and calibration	Internal test charge generation controlled by digital signal
Slow control interface	I2C with multiple chips on the same I2C bus
VCO oscillation freq.	1.28 GHz
# of VCO stages	16
ToA Bits/event	fToA @800ps: 2 (Assumes a 2 ns gate) ufToA @25ps: 5
Output	Digital differential, lpGBT compatible
Output links freq.	160, 320, 640, 1280 MHz
# of output links	Programmable at chip level from 1 to 4