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The FastRICH ASIC for next-generation RICH detectors

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A novel ASIC, called the FastRICH, is designed and produced for the front-end electronics of single-photon detectors in future RICH detectors. Owing to the prompt Cherenkov radiation and precise optical arrangement of RICH detectors, the Cherenkov photon time-of-arrival can be used to improve the particle identification performance. The 24.4 ps detector hit timestamps provided by the FastRICH will equip the detector for such fast-timing reconstruction techniques. The addition of time information, especially when combined with the increased particle multiplicity in High-Luminosity LHC experiments, requires advanced data-compression techniques to limit the front-end bandwidth requirements. Dedicated design features therefore include constant-fraction discrimination, an on-chip time gate to remove out-of-time background and an optimised data-driven output format. In order to deal with the typically non-uniform hit rates in different regions of the RICH detectors, the 16-channel FastRICH has a configurable output data rate between 320 Mb/s and 5.12 Gb/s. The ASIC has a wide input signal dynamic range allowing it to be flexibly coupled to different types of fast single-photon sensors including silicon photomultiplier arrays and vacuum-based sensors. A strong design effort was made to minimise the power consumption (simulated to be less than 16 mW/channel at 1.2 V) for integration into compact future detectors with high channel densities. The FastRICH is produced in 65 nm CMOS technology with triplication of sensitive logic for tolerance against single-event effects due to radiation in high-energy physics applications. The FastRICH is developed in the context of the LHCb experiment and compliant with the 40 MHz event rate and experiment timing and control system. The ASIC can be coupled directly to the next-generation CERN front-end optical link chipset for data transfer. The FastRICH ASICs were produced in May 2025. A detailed measurement campaign is launched to validate the design at the single-chip level as well as a full module for beam tests at the CERN PS/SPS facilities. In this contribution, the key features and the first test results of the FastRICH ASIC are reported.

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