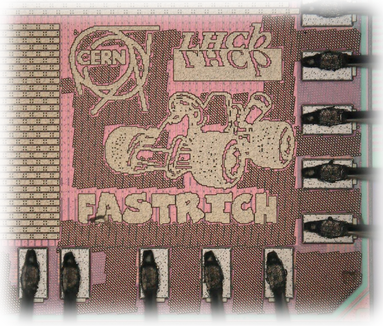

The FastRICH ASIC for next-generation RICH detectors

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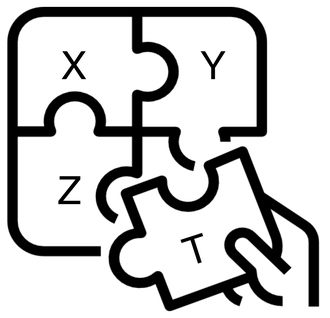
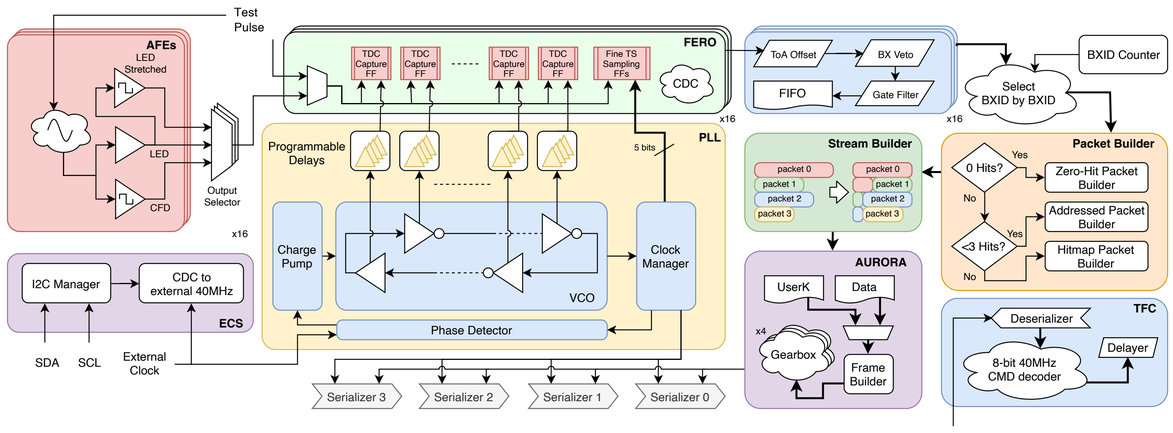


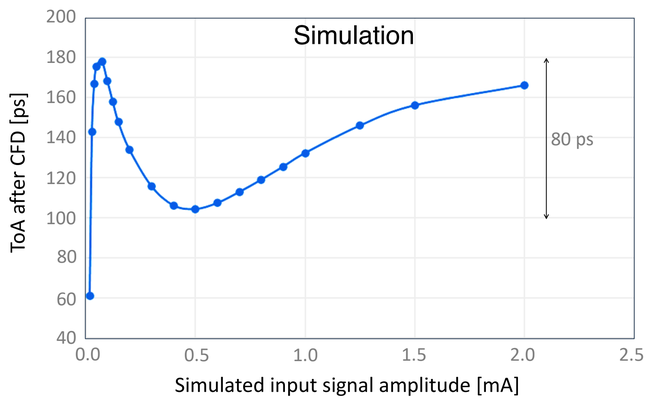
The FastRICH specifications

The FastRICH is an application-specific integrated circuit (ASIC) designed in **65-nm CMOS technology by the CERN EP-ESE department and the University of Barcelona [1]** with strong input in the specifications from the LHCb RICH collaboration. The FastRICH foresees to meet the requirements for future RICH detectors with different types of photon sensor. The **16-channel** design is packaged in QFN88 of 10 mm size.



Analogue

- Input **polarity** configurable to positive or negative.
- Input signal dynamic range from **30 µA to 2 mA** for coupling to MAPMT (multi-anode photomultiplier tubes), SiPM (silicon photomultiplier) arrays or MCP-based (microchannel plate) sensors.
- **Bias tuning** range of 400 mV for SiPM arrays.
- Channel **recovery time** of better than 10 ns after a signal.
- Programmable **signal attenuation** by 25%, 50% or 75%.
- Front-end configurable between Constant-Fraction Discrimination (**CFD**) or Leading-Edge Discrimination (**LED**) with 390 ps LSB Time-over-Threshold (**ToT**) measurement.



Simulated **residual time walk of the CFD**, with a worst-case residual of ~ 80 ps for input currents from 20 µA to 2.5 mA. Better results are achieved for the typically smaller signal amplitude range of the photon sensor. For SiPMs, the (residual) time walk is expected to be negligible.

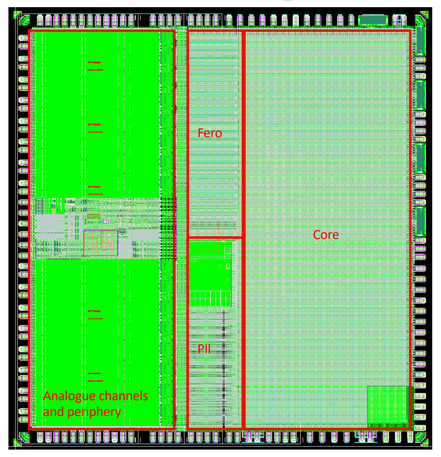
Digital on top

- Time-to-Digital Circuit (**TDC**) with **24.4 ps time bins** and **programmable offset** for time calibration. TDC output goes through a filtering stage, including **time gate** of configurable width up to 6.25 ns (25 ps TDC) or 25 ns (100 ps TDC).
- Radiation hardness using **triplication** up to ~ 2 x 10^{13} n_{eq}/cm^2 and ~ 12 kGy.
- **Configurable** number (1 to 4) and speed (320, 640 or 1280 Mbps) of **output serialisers**.
- Coupling to next-generation lpGBT for control, clock and data interfaces, which are compatible with the LHCb experiment control system.
- Commercial **Aurora 64b/66b protocol** and a **data-driven packet format** at 40 MHz, responding dynamically to the number of hits in each event.

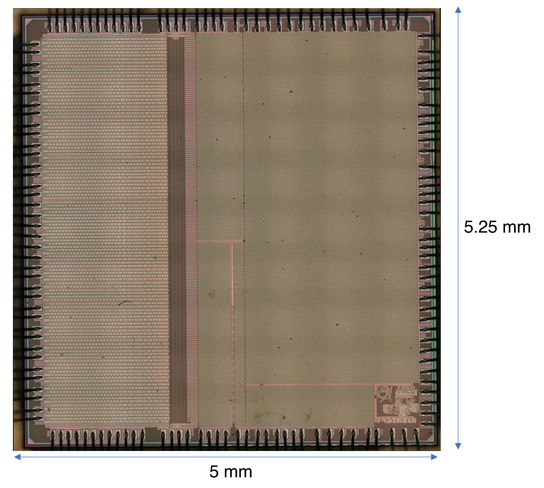
Example of a few different FastRICH data packets depending on the number of hits in the event [1].

The first FastRICH ASICs

From design…



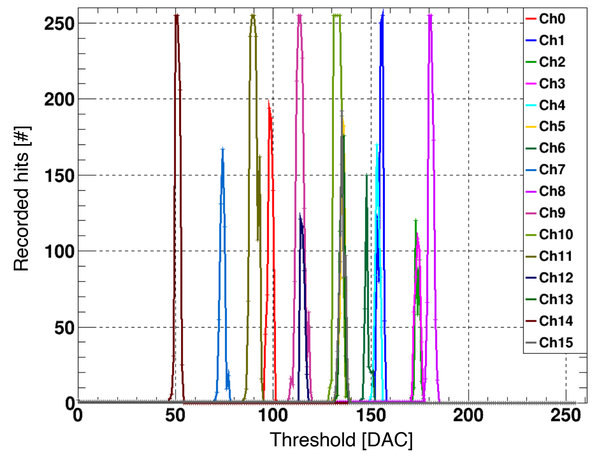
… to silicon wafer

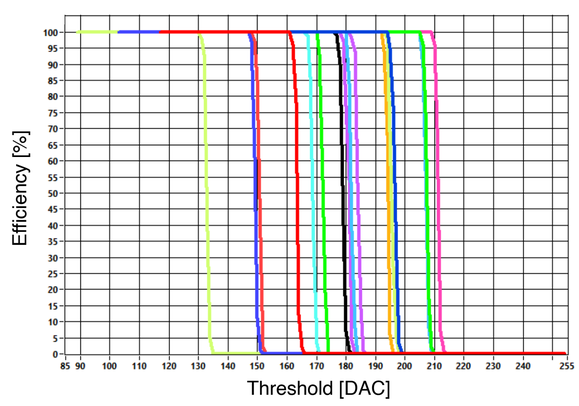


The FastRICH ASICs were **produced** on a Multi-Project Wafer in **May 2025**. **First tests** have been performed on wire-bonded ('bare-die') as well as QFN88 packaged ('open-lid') ASICs. The power consumption depends on the detailed configuration; typically measured around **12 to 13 mW/channel** at 1.2 V bias. Digital-to-analogue converters (**DACs**) show good linearity response and agreement with electronics simulation.

The FastRICH ASIC contains a **build-in threshold scan**.

- Records the number of hits inside a configurable time window whilst scanning the channel over the full threshold range.
- As expected, an increase in counts is observed around the noise pedestal.

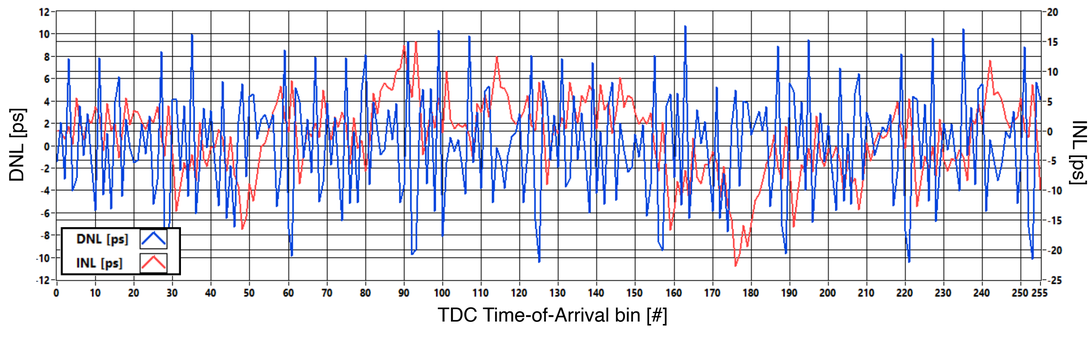




A configurable test pulse can be triggered at the analogue (through an internal test capacitor) or digital (TDC) input stage of each channel to test the ToA and ToT response.

- Measured S-curve with the full FastRICH readout path.
- LED discriminator in neg. polarity.

Preliminary **tests of the TDC**: differential non-linearity (DNL) and integral non-linearity (INL) measurements using external test pulse triggers with 1 ps delay shifts. First results show good linearity, with the possibility of tuning the FastRICH parameters to further improve these values.



Target application: RICH detector upgrades at the LHCb experiment

Sub-100 ps photon hit time information is highly important for the upgrade programme of the LHCb RICH detectors.

- Tool to mitigate pile-up in the **High-Luminosity LHC**.
- Improve particle identification by removing out-of-time background.
- Novel **FastRICH electronics** during **Long Shutdown 3 (LS3 Enhancements, 2026-2028)** coupled to existing MAPMTs [2].
- LHCb **Upgrade II** [3] foresees new photon sensors (e.g. cryogenically cooled SiPMs [4]) coupled to the electronic chain.

FastRICH features are used to optimise the **bandwidth allocation** for the **non-uniform photon hit density** at the LHCb RICH detector.

- Configurable number of output serialisers.
- Data-driven packet format.
- Data suppression through CFD and time gate.

Prototype module for the LS3 Enhancements was assembled. First tests are being carried out in preparation for 2025 and 2026 beam tests at the CERN PS/SPS facilities.

Image courtesy of the LHCb RICH Collaboration

Further information

The FastRICH ASIC documentation is available at [1] https://fastrich.docs.cern.ch .
Details on the LHCb RICH upgrades can be found in [2] *LHCb Particle Identification Enhancement Technical Design Report* (2023) 10.17181/CERN.LAZM.F5OH and [3] *Upgrade II Scoping Document* (2025) 10.17181/CERN.2RXP.HDK0 . At this conference, see other contributions: [2] poster on *The LS3 Enhancement of the RICH detectors*, [3] talk on *The Upgrade II of the LHCb RICH system* and [4] poster on *A cryogenic RICH detector demonstrator for SiPM operation with integrated flex-PCB electronics.*