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Online AI-based distributed data reduction for the dual-radiator RICH detector in the ePIC experiment

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The ePIC experiment at EIC integrates a dual-radiator RICH (dRICH) detector for particle identification in the forward region. The detector will use silicon photomul tipliers (SiPMs) to detect Cherenkov radiation with single-photon sensitivity over a surface of ~3 m2. The ~320k detector channels will be readout by 4,992 Front End Boards (FEBs); each of the 1,248 Readout Boards (RDOs) will collect data from four FEBs and forward them via a VRTX+ optical link to a Data Aggregation and Manipulation Board (DAM) supporting up to 48 ports. DAMs will be implemented by FPGA-based FELIX-155 cards designed for the ATLAS experiment. They will collect and merge data from 42 RDOs, forwading them through 100 GbE channels to the ePIC data buffering system (Echelon 0). To mitigate the potential risk of an excessive dRICH output bandwidth demand due to the increasing SiPM Dark Current Rate(DCR), expected to reach a maximum of 300 KHz during the experiment lifetime, we designed a real-time data reduction system that will reduce the detector output bandwidth by an order of magnitude at least. This will be accomplished by implementing a distributed data-flow processing scheme on the DAMs and on an additional Felix-155 card that will act as a Trigger Processor (TP), selecting and discarding online the DCR noise only events. Current design is characterized by a distributed Multi-Layer Perceptron Neural Network performing the Noise-Only event discrimination, with 30 separate sub-network replicas deployed on each DAM which processes its event fragment to extract a set of features that are passed to the TP using a direct low-latency communication channel. The TP implements a different sub-network that, having in input the full set of features extracted by each DAM, performs the classification task and generates the corresponding trigger signal to keep or discard the event, respectively, in the case of a physics (including background) signal plus DCR noise and DCR noise only. The main EIC clock will be at 100 MHz, corresponding to ~10 ns election-ion bunch crossing: this will be the main challenge in the implementation of the system. We will outline our approach to this issue, covering both the FPGA computing pipelines and communication, along with the current implementation status.

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