XII International Workshop on Ring Imaging Cherenkov Detectors
15 - 19 September 2025, Mainz, Germany

The LS3 Enhancement of the RICH detectors

Vlad-Mihai PLACINTA

Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering – IFIN-HH

on behalf of the LHCb RICH Group

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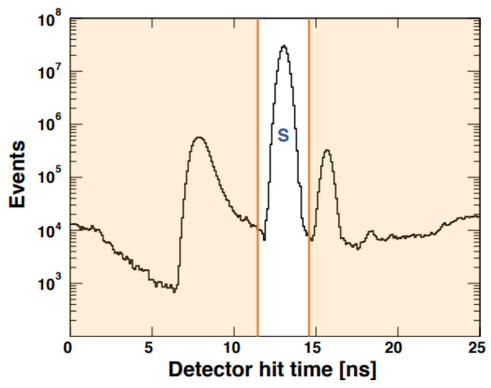
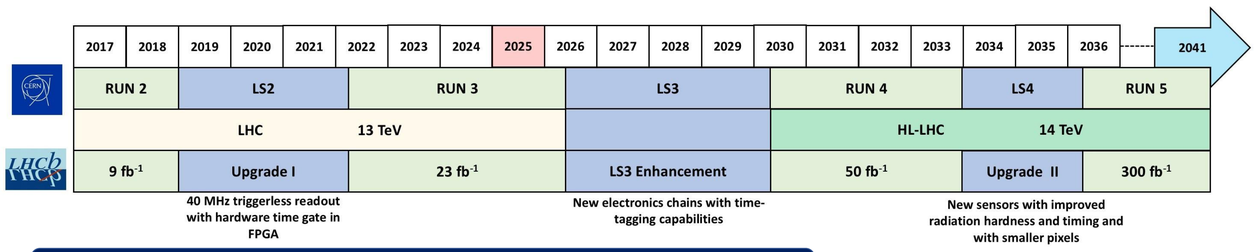
Motivation

- Simulation studies have revealed that the prompt Cherenkov photons arriving on the detector planes can be predicted with a time-of-arrival (TOA) better than 10 ps;
- The performance of the RICH detectors can be enhanced by the introduction of photon time-tagging capabilities;
  - ❖ improved background reduction and particle identification (PID) efficiency.
- The implementation of a configurable hardware time gate in the front-end electronics will allow to select a detection window and to filter out any background noise;
- Within a time gate, every hit will be time-tagged, and then compared against the predicted TOA by the reconstruction algorithm [1];
- LHCb-RICH sub-detectors will be upgraded to run faster, by means of implementing fast-timing single-photon capabilities. This will be done over 2 steps:
  - ❖ redesign of readout electronics chain during LS3 Enhancements [1];
  - ❖ photon sensor change during LHCb Upgrade II [2].

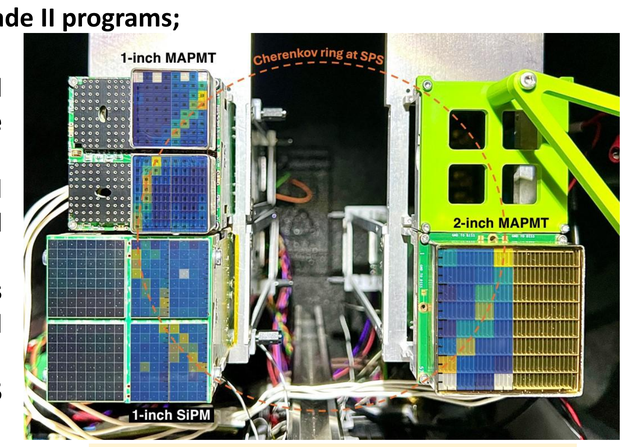


	Sensor		FPGA		Optical link		Back-end
LHC Run 3	MAPMT	FE ASIC CLARO	Kintex 7	NDC	GBT Versatile Link	NDC	PCIe40
LHC Run 4	MAPMT	FastRICH		DC	lpGBT / VL+	DC	PCIe40(0)
HL-LHC Run 5	SiPM / MAPMT / MCP	FastRICH		DC	lpGBT / VL+	DC	PCIe400

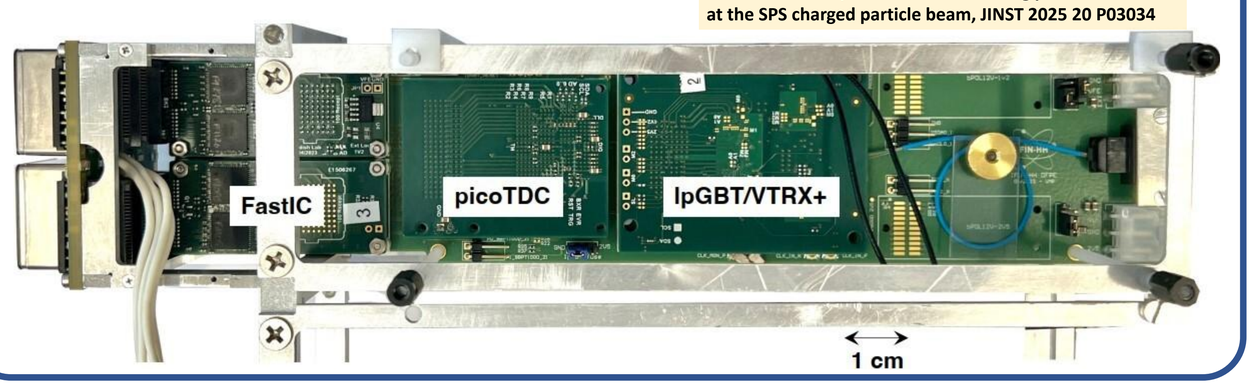


LHCb-RICH electronic chain prototypes: R&D

- Before the submission of the FastRICH ASIC, several readout electronic chains prototypes have been developed with the main goal to study the timing performance of various optical sensors technologies in the framework of LS3 Enhancements and Upgrade II programs;
- The most recent variant uses the FastIC front-end ASIC and relies on the picoTDC to provide the timestamp of the hits;
  - ❖ slow control and data transmission ensured by using the lpGBT ASIC and VTRX+ optical modules;
  - ❖ ~ 500 channels were distributed across various optical sensors, MaPMT, SIPM and MCP-based;
  - ❖ tested in several campaigns at the CERN SPS test beam facility during the last years.



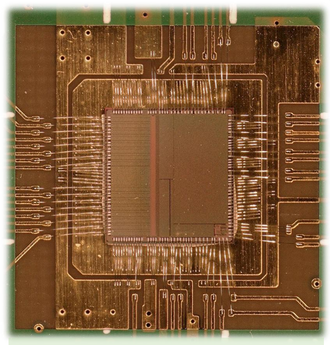
M. Bartolini *et al*, LHCb RICH Fast-timing photon detection at the SPS charged particle beam, JINST 2025 20 P03034



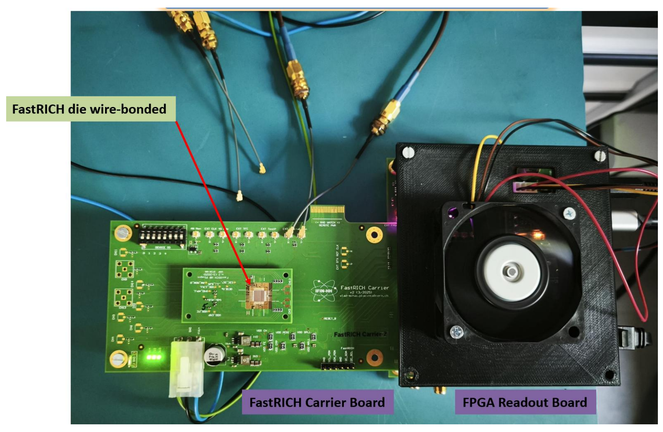
The FastRICH ASIC: preliminary testing results

- The FastRICH ASIC represents the nucleus of the next generation of LHCb-RICH fast-timing electronics;
  - ❖ a collaboration between CERN EP-ESE department, University of Barcelona and RICH;
  - ❖ ASIC design submitted in early February of 2025;
  - ❖ naked dice received at CERN in early May of 2025.
- FastRICH key features [4]:
  - ❖ 65 nm radiation-hard CMOS technology;
  - ❖ 16-channels with digital-on-top design;
  - ❖ die size of 5 mm x 5 mm and packaged in QFN88 package;
  - ❖ embedded time-to-digital converter (TDC) with 24.41 ps time bins;
  - ❖ versatile front-end with possibility to choose between Leading-Edge Discrimination (LED) and Constant Fraction Discrimination (CFD);
  - ❖ channel input polarity can be configurable to use either negative or positive polarity;
  - ❖ wide dynamic input range of 50 µA to 5 mA and compatible with MaPMT/MCP-based/SiPM sensors;
  - ❖ output data-compressed format based on the aurora 64b/66b protocol for serial links;
  - ❖ configurable data throughput between 0.32 Mbps and 5.12 Gbps;
  - ❖ power consumption of about ~13mW/channel at 1.2 V nominal power supply.

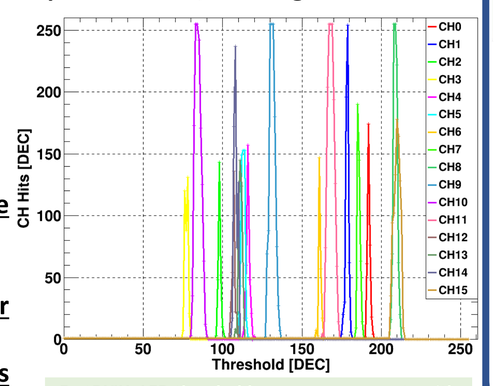
See Floris Keizer's poster "The FastRICH ASIC for next-generation RICH detectors"



FastRICH die wire-bonded to a test PCB



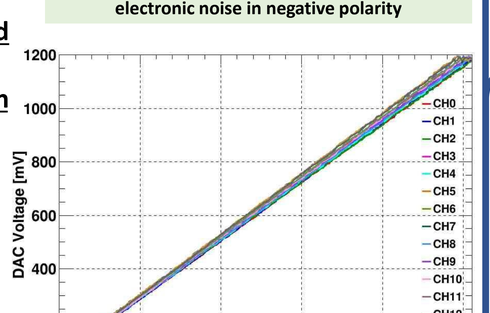
- In-house FPGA-based test system:
  - ❖ to characterize the prototype ASICs;
  - ❖ acts like a small-scale readout system;
  - ❖ allow to test all the interfaces;
  - ❖ read data with an external stimulus.
- Multi-purpose design:
  - ❖ lab testing;
  - ❖ irradiation testing;
  - ❖ mass production QA testing.



FastRICH: LED threshold scan measurements with electronic noise in negative polarity

- Summary of the testing results obtained so far:
  - ❖ power on test and control of all interfaces;
  - ❖ power consumption measured ~ 13 mW/channel;
  - ❖ ~20 samples were wire-bonded and all have passed the basic testing;
  - ❖ functionality testing of various internal blocks on-going;
  - ❖ PLL output jitter optimized to ~ 5.81 ps with a ~1.5 ps jitter reference clock;
  - ❖ TDC performance: DNL std deviation ~ 6 ps, INL +/- 22 ps (there is place for optimization);
  - ❖ data taking possible with the full readout chain and external stimulus, e.g., external test pulse;
  - ❖ data can be decoded and FastRICH-related information can be extracted.
- X-ray TID irradiation testing (July 2025):
  - ❖ 2 samples tested at an X-Ray facility from CERN;
  - ❖ sample 1: dose rate of 0.53 Mrad/h and 2 Mrad TID;
  - ❖ sample 2: dose rate of 2.04 Mrad/h and 12 Mrad TID;
  - ❖ tests carried out at room-temperature and focused mostly on the analog part of the ASIC.

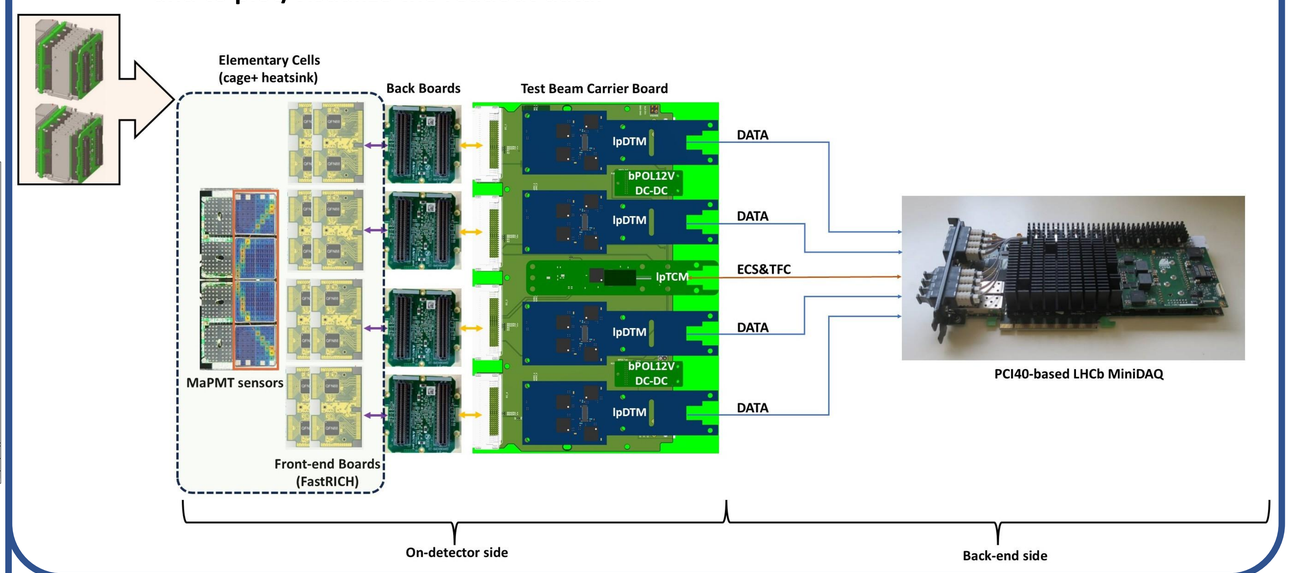
No major effects were seen after 12 Mrad of TID. Power consumption did not change, and overall, the ASIC seem to tolerate vey well this unrealistic high TID and dose rates.



FastRICH: DAC linearity measurements of the rail-to-rail voltage DACs that are used to tune the DC bias of the input channels

LHCb-RICH electronic chain prototypes: FastRICH

- Work in progress to design and prepare a FastRICH-based electronics chain for the SPS test beam campaign during October 2025;
  - ❖ aim to have a LS3 Enhancements-like electronics readout chain prototype;
  - ❖ first time to demonstrate the coupling between FastRICH and MaPMTs.
- The new electronics chain involves many new elements:
  - ❖ front-end boards (FEBs) populated with open-lid QFN88 packaged FastRICH ASICs;
  - ❖ bPOL12V-based DC-DC power modules to provide 1.2 V and 2.5 V power rails;
  - ❖ timing and control module (lpTCM): 1 lpGBT ASIC and 1 VTRX+ optical module (1 RX/TX variant);
    - ▪ provides the 40 MHz reference clock to the FastRICH ASICs and the lpDTMs;
    - ▪ ECS and TFC interfaces to the FastRICH ASICs;
    - ▪ additional slow control and monitoring signals.
  - ❖ data transmission modules (lpDTMs): 4 lpGBT ASICs and 1 VTRX+ optical module (4 TX variant);
    - ▪ sends the aurora 64b/66b encoded data from the FastRICH output serialisers to the back-end readout.
  - ❖ new PCI40 firmware to allow connection, control and readout through lpGBT;
    - ▪ includes aurora 64b/66b and FastRICH decoding.
  - ❖ WinCC-based GUI to control and supervise the system;
    - ▪ and to plot/visualize the readout data.



Conclusions

- The readout chain of the LHCb-RICH sub-detectors will have time-tagging capabilities with 24.41 ps resolution implemented during the LS3 Enhancements break;
  - ❖ RUN 4 setup: MaPMTs (~150 ps resolution) coupled with FastRICH ASICs;
- The FastRICH ASIC is now under full validation on multiple test chains for validation of its performances against the RICH requirements;
- New electronics chain is currently designed around FastRICH, lpGBT, bPOL12V and VRTX+ components for the next test beam campaigns to be carried out at CERN SPS facility, starting with October 2025;
- Single-Event Effects test with heavy ions is scheduled at the end of October 2025 at UCL Louvain;
  - ❖ LHCb-RICH system-wise radiation testing under preparation for the 2026 at CHARM facility at CERN.

References:

1. LHCb Collaboration, *Framework TDR for the LHCb Upgrade II - Opportunities in flavour physics, and beyond, in the HL-LHC era*, Technical Design Report, CERN-LHCC-2021-012, LHCB-TDR-023, https://cds.cern.ch/record/2776420.
2. LHCb Collaboration, *LHCb Particle Identification Enhancement Technical Design Report*, Technical Design Report, CERN-LHCC-2023-005, LHCB-TDR-024, https://cds.cern.ch/record/2866493.
3. F. Keizer, *The FastRICH ASIC for the LHCb RICH enhancements*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2024, DOI: 10.1016/j.nima.2024.169664.
4. *FastRICH documentation website*, https://fastrich.docs.cern.ch/ (last retrieved 10-09-2025).