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High-Precision Timing Characterization of MCP-PMT Using Front-End ASIC and TDC ASIC

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Introduction

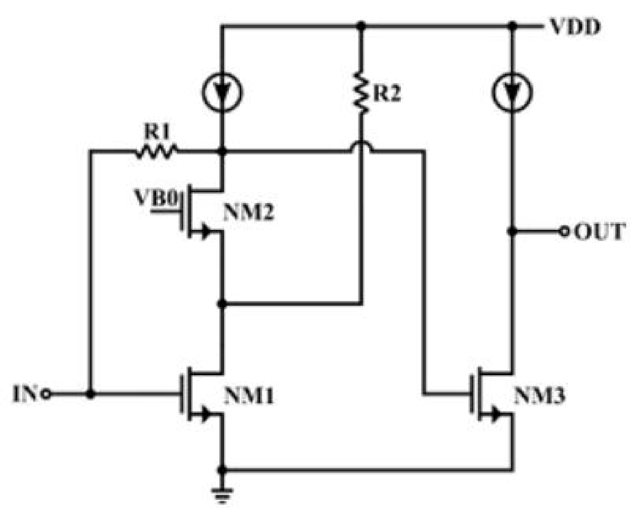
Micro-Channel Plate Photomultiplier Tubes (MCP-PMTs), with their high time resolution (single-photon Transit Time Spread, TTS < 30 ps) and low-noise characteristics, are critical detectors for particle identification, time-of-flight (TOF) measurements, and Cherenkov imaging in high-energy physics experiments.

The FPMROC is designed in a 55 nm CMOS process and incorporates a full readout chain, including a low-noise preamplifier, discriminator, time-to-digital converter (TDC) for time of arrival (TOA) and time-over-threshold (TOT) measurements, as well as fast data serialization and data driver for output. The TOT is used for time-walk correction of the TOA measurement. In addition, a charge injection circuit is implemented to allow for testing and calibration. Additional peripheral circuits include DACs for calibration and threshold, a PLL and a SPI.

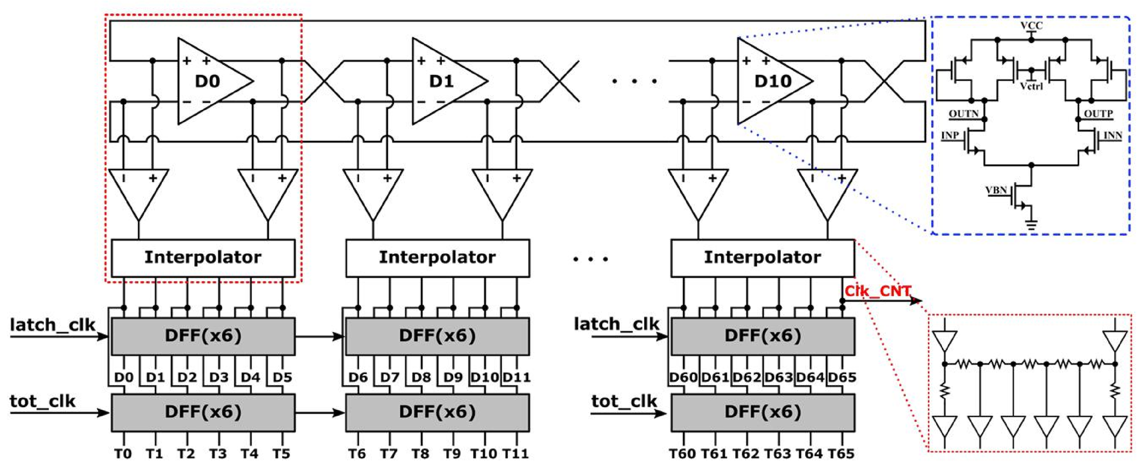
The proposed transimpedance amplifier employs a two-stage amplification architecture, where the first-stage amplifier demonstrates significantly high gain. This design strategy reduces subsequent amplification stage requirements, thereby optimizing system complexity while maintaining high stability and enhanced noise immunity. The architecture of the TDC is based on a ring oscillator interpolation method.

1. Design and Performance of FPMROC

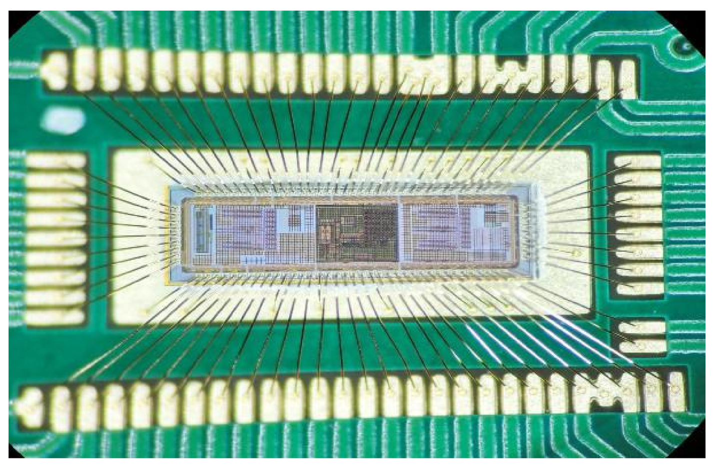
- Through innovative implementation of high-gain pre-amplification and dynamically controlled feedback mechanisms, the TIA achieves optimal balance between broad bandwidth (>1 GHz) and ultra-low noise performance (<500 µV RMS), making it particularly suitable for high-sensitivity photodetection systems.
- The TDC block utilizes 11 voltage-controlled differential delay cells, which construct a ring oscillator using an interpolator approach.
- The time jitter of the CML-level output from the analog front-end is below 8 ps, while the bin size of the TDC reaches 13 ps.



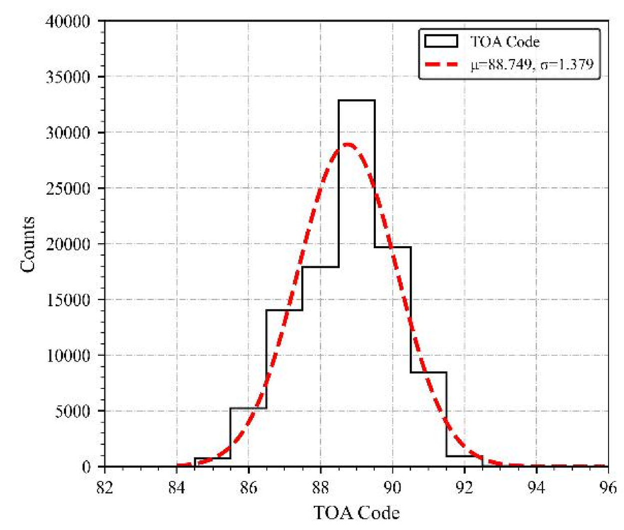
Schematic of the trans-impedance amplifier.



The architecture of the TDC delay line.



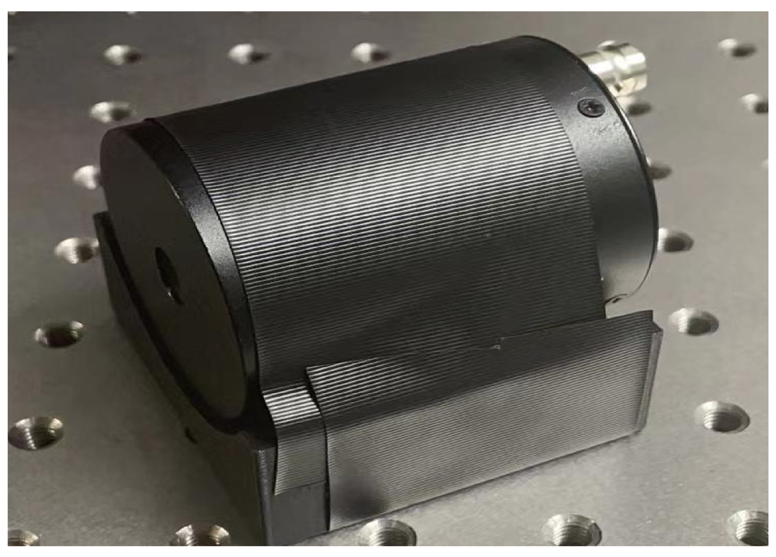
FPMROC1 Chip



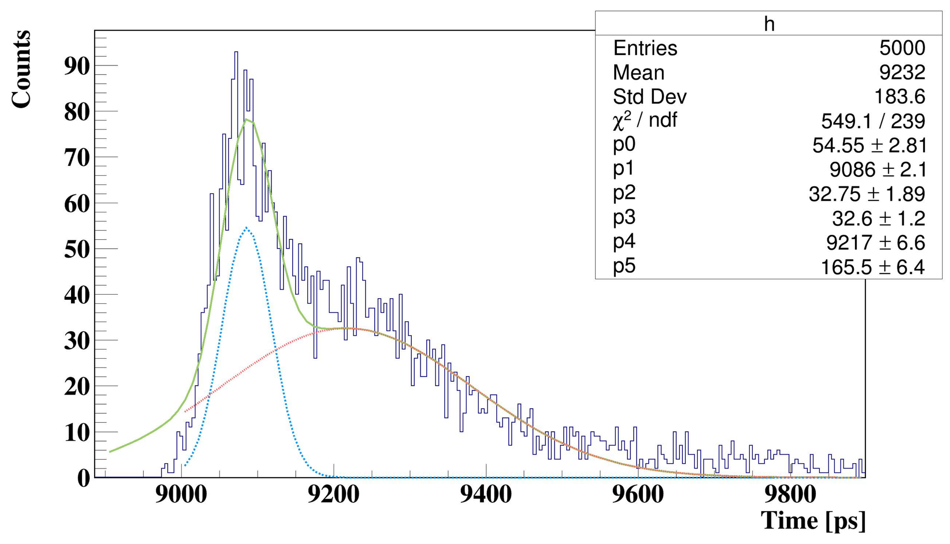
TDC measurement precision

2. Performance of FPMT

- The structure of the single anode FPMT was optimized to achieve a TTS about 30 ps when it detects single-photon.
- Using the existing two-layer MCP structured FPMT with a gain of approximately 4E6, the signal peak amplitude measures around 30 mV.
- The signal's rise time is less than 300 ps, and its pulse width is less than 500 ps.



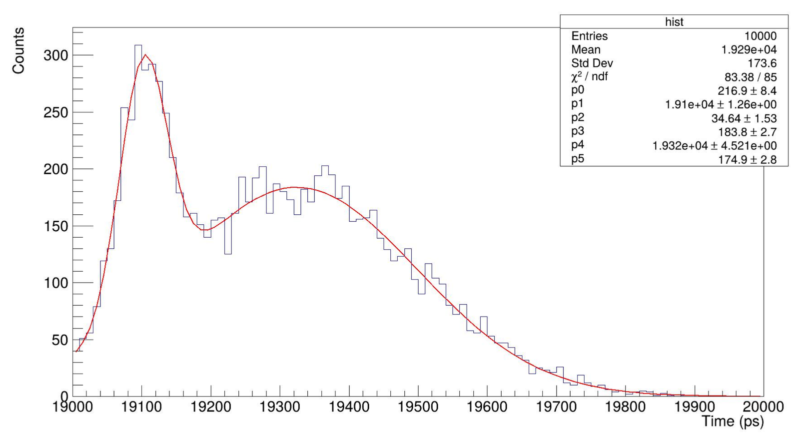
Single Anode FPMT



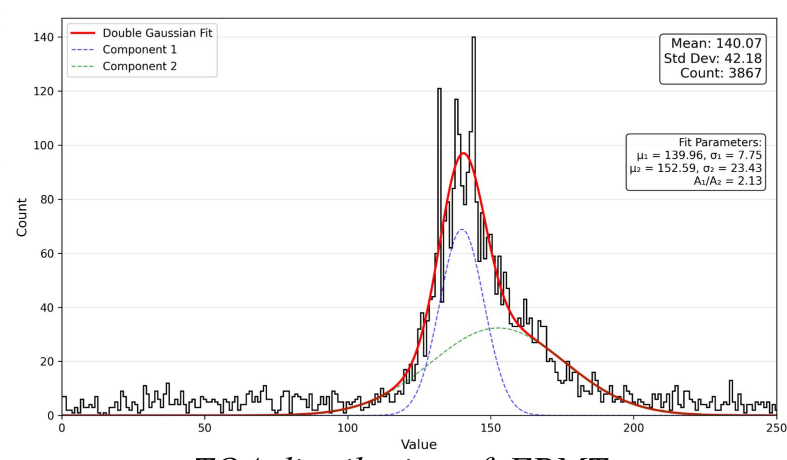
TTS of FPMT

3. Preliminary results of the timing system

- During preliminary testing, the input signal for the FPMT's time measurement was delivered via a nearly 1-meter-long coaxial cable.
- The reference clock of TDC is provided by the clock board. Simultaneously, the clock board supplies a synchronized single-ended signal to trigger the picosecond laser. The FPGA handles data acquisition.
- During preliminary system integration tests, the FPMT's TTS was found to be less than 100 ps.



FEE measurement with FPMT



TOA distribution of FPMT

4. Conclusions

- We have develop a prototype timing system for MCP-PMT.
- The resolution of the timing system is approximately 13 ps, and it can process signals from the MCP-PMT at the single-photon level.
- Prior to integration, testing measured a TTS of less than 100 ps for the FPMT, validating the feasibility of the system setup. The next step involves integrating the detector with the ASIC to achieve optimal time-resolution.

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