Front-end electronics for RICH detectors

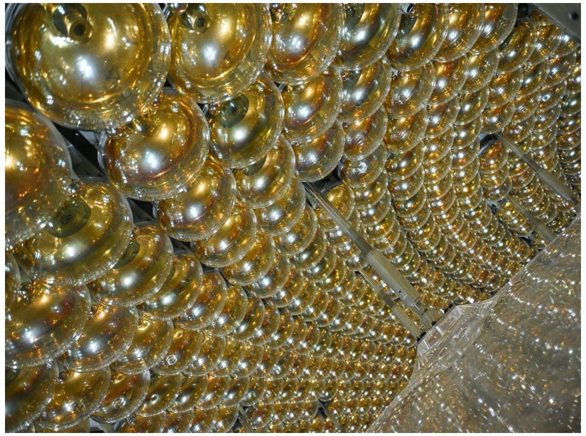
general requirements, design criteria and examples of current projects

Floris Keizer (CERN)

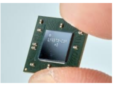
XII international workshop on RICH detectors,

19 September 2025

Which ~~electronics~~ experimental conditions?



JUNO expt.



Lab study with one sensor

- Not many constraints on space, power, cost and complexity of readout.
- Measure **full waveform** information.
- Few channels and large readout.

HEP experiment

- Stringent requirements on detector integration, scalabililty, power, radiation hardness, etc.
- Must carefully select **which information to keep**.
- 10^5 channels and small readout.

There are many different **readout systems**, all optimised for their **applications**, taking many **design aspects** into consideration. I will be giving my view on only a subset of these developments.

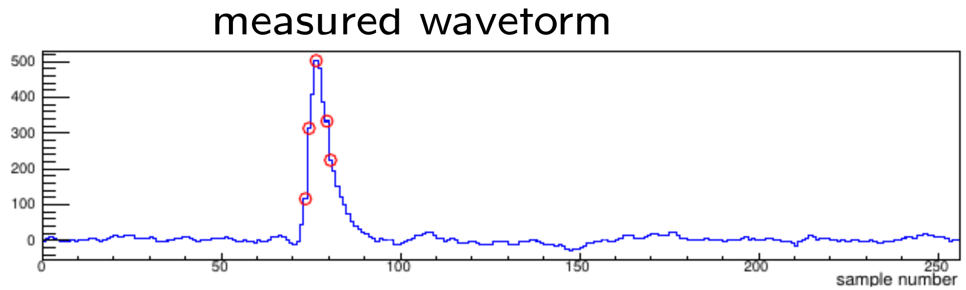
FPGAs for digital processing

FPGAs (field-programmable gate arrays) have **reconfigurable** logic (firmware).

- Attractive technology for **digital** processing.
- Often **combined with analogue front-end ASIC** tailored to sensor/application.

Belle II TOP: IRSX (TOPSoC) ASIC + FPGA.

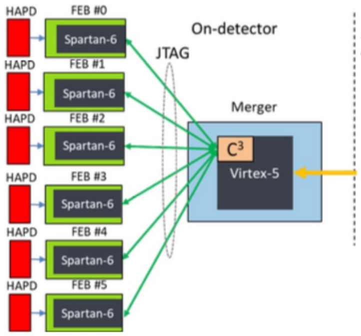
- **Waveform sampling** 2.7 Gs/sec.
- Designed for 30 kHz trigger rate.

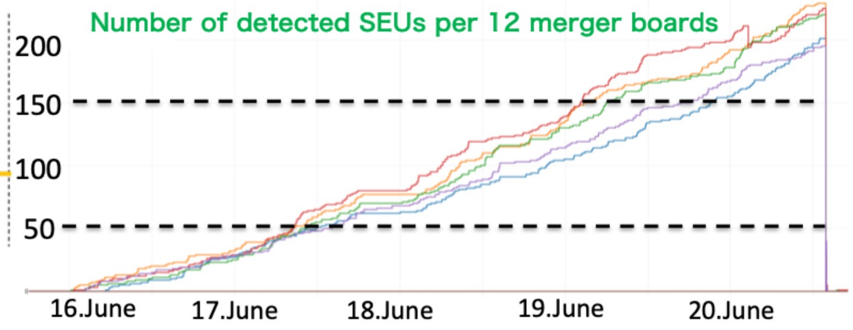


Talk M. Staric

Belle II ARICH: SA03 ASIC + FPGA.

- **Single-Event Upsets** (SEU) in FPGA, **scrubbing techniques** to recover.
- Order 10^{11} MeV n_{eq}/cm^2 per year.





https://www.sciencedirect.com/science/article/abs/pii/S0168900223006253

FPGAs for digital processing

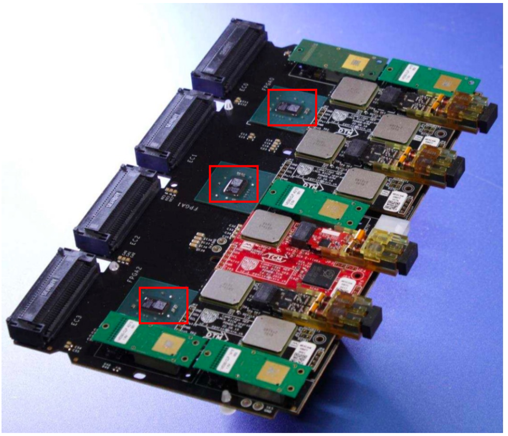
Talk G. Cavallero

LHCb RICH: CLARO ASIC + FPGA.

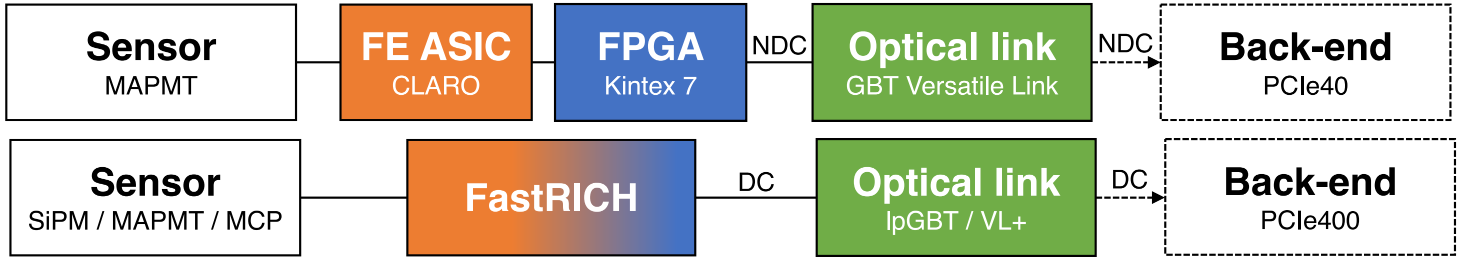
- 40 MHz data “pass through” and 10^{11} - 10^{12} MeV n_{eq}/cm^2 per year.
- By design, use **only few % of logic** resources to limit SEU.

Towards the future: general shift from **FPGA to ASIC**.

- Increased luminosity (HL-LHC).
- Especially using smaller technology nodes (e.g. 65 nm CMOS) and protecting sensitive logic against SEU (triplication and/or parity bits).



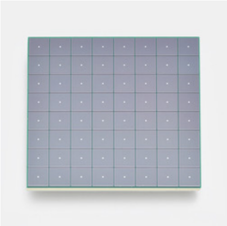
Flexible Kintex7 FPGA-based digital Board interfacing with LHCb backend boards using the GigaBit Transceiver protocol



Poster V.Placinta

- **Best solution for moderate** requirements.
- **Low** radiation.
- **Commercial** off the shelf components.

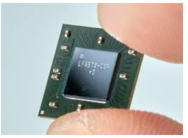
Sensor



Analogue FE amplifier & discriminator

Digital FPGA

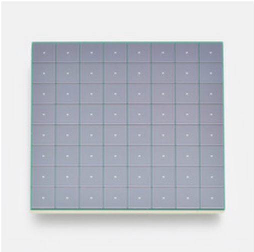
Optical control



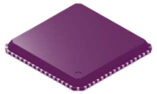
SFP+ commercial link

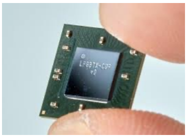
- **Necessary for stringent** requirements.
- **High** radiation.
- **ASIC / specific** component developments.

Sensor

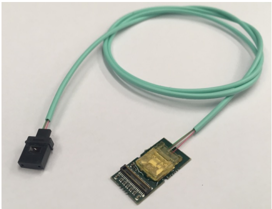


Analogue & digital ASIC





lpGBT and VTRX+ optical link chipset



Today's focus

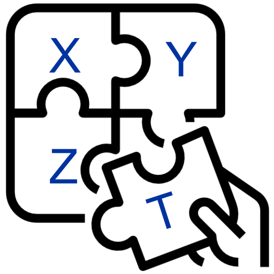
Some ASIC examples at RICH2025

	FastRICH	ALCORv3	FPMROC	Petsys-TOFPET2	Preamp + NINO + HPTDC
@ Conference	Poster F. Keizer	Poster R. Preghenella	Poster S. Qian	//	//
Main application	LHCb RICH	ePIC RICH	ToF-PET	Commercial / Belle-II DIRC	NA62
Technology	65 nm	110 nm	55 nm	110 nm	250 nm
Target sensor	MAPMT, SiPM, MCP	SiPM	MCP	MCP	PMT
Channel	16	64	8	64	8
Amplifier	Current buffer	Current buffer	TIA and amplifier	Charge sensitive	Custom charge amplifier
TDC bin	25 or 100 ps	25 or 50 ps	13 ps	30 ps	100 ps
Input bandwidth	30 uA – 2 mA	Tuned to SiPM	10^5 gain MCP (2 – 200 mV)	Up to 1500 pC	100 fC – 2 pC, differential
Mode	CFD and ToT	ToT	ToT	ToT and energy	ToT
Power [mW/ch]	~ 12	~ 12	~ 40 (sim)	~ 8	O(100)
Bits per hit	~ 10 bit, dynamic	32 bit	64 bit	64 bit	64 bit
Encoding	64b66b	8b10b	64b66b	8b10b	//
Event rate [MHz/ch]	40 (25 ns periods)	2.5 – 5 (10 ns periods)	< 40	0.5	~ 1
Serialiser max. rate [Gbps]	5.12 (configurable 1 to 4 links)	1.28 (4x 320 Mbps)	10.24 (64 bit parallel at 160 MHz)	3.2 (configurable 1 to 4 links)	(Parallel bus)
Target radiation	~ 2 x 10^{13} n_{eq}/cm^2 (LHCb)	~ 2 krad (ePIC)	Not specified	Not specified	//

Front-end electronics

- **Time resolution (MCP)**
- High-rate operation (SiPM)
- Readout density and integration
- Data throughput and optical links
- Considerations on ASICs

Time resolution



RICH detectors are highly suited to use detector hit time information:

- **Prompt Cherenkov + focusing optics = predictable hit time of arrival**.
- Often new requirement: increased luminosity (reduce **pile-up**) environments or out-of-time SiPM DCR (improve **signal to noise**).

Couple sensors with good time resolution to **TDC (Time-to-Digital) circuit**.

- TDC circuits come with:
  - increased **power** consumption (PLL, high frequency clocks and buffers),
  - higher **data** throughput,
  - more demanding **calibration**.

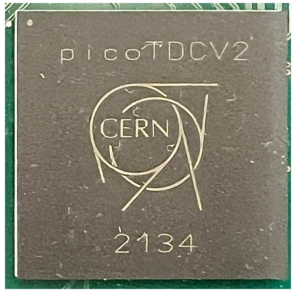
Picosecond Time-to-Digital Circuit (TDC)

TDC-in-FPGA

- E.g. CLAS12 and GlueX, DiRICH for CMB/HADES.
- Digital input (can be analog).
- Typically loose time requirements: > few-100 ps.
- Faster TDCs possible (e.g. DiRICH 20 ps), but relies on manual placement of logic slices, careful calibrations and specific to FPGA version.

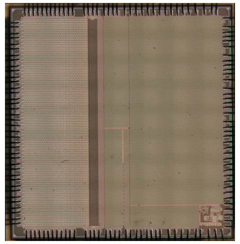
Dedicated TDC ASIC

- E.g. picoTDC, HPTDC.
- Digital input.
- Typically fast: picoTDC down to 3 ps bins.
- Trade-off between generic and application specific: power, data rate, radiation hardness etc.



Integrated TDC

- E.g. FastIC+, FastRICH, ALCOR, FPMROC.
- Analogue sensor input.
- Fully application specific, meets sub-100 ps requirement at low power for single-photon sensors.
- Increases ASIC complexity: digital-on-top design and verification required.



Electronics time gating

Select the TDC window where event data is expected.
“Picture” instead of “video”.

Reduction in data size:

- Exclude out-of-time background:
  fewer hits to transmit.
- Reduce TDC range to encode in data-packer:
  fewer bits to transmit.

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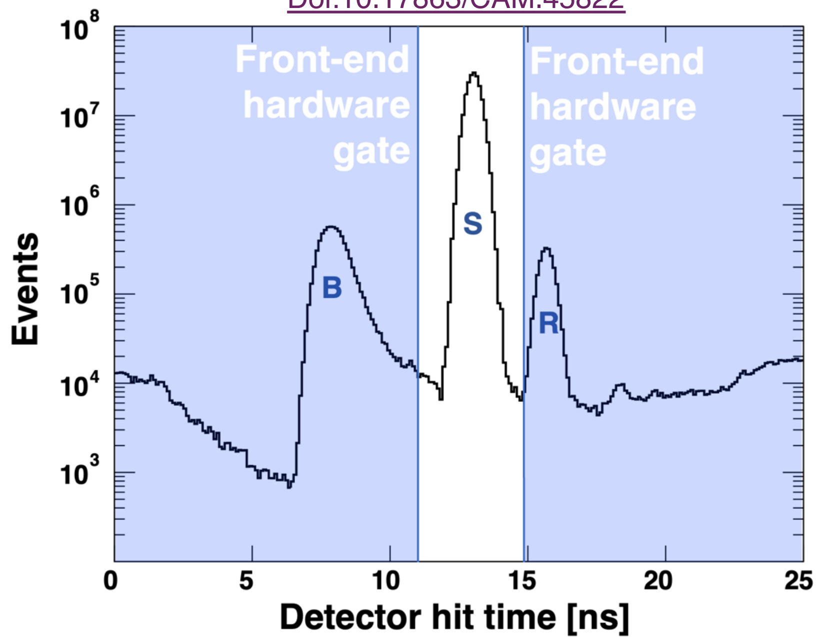
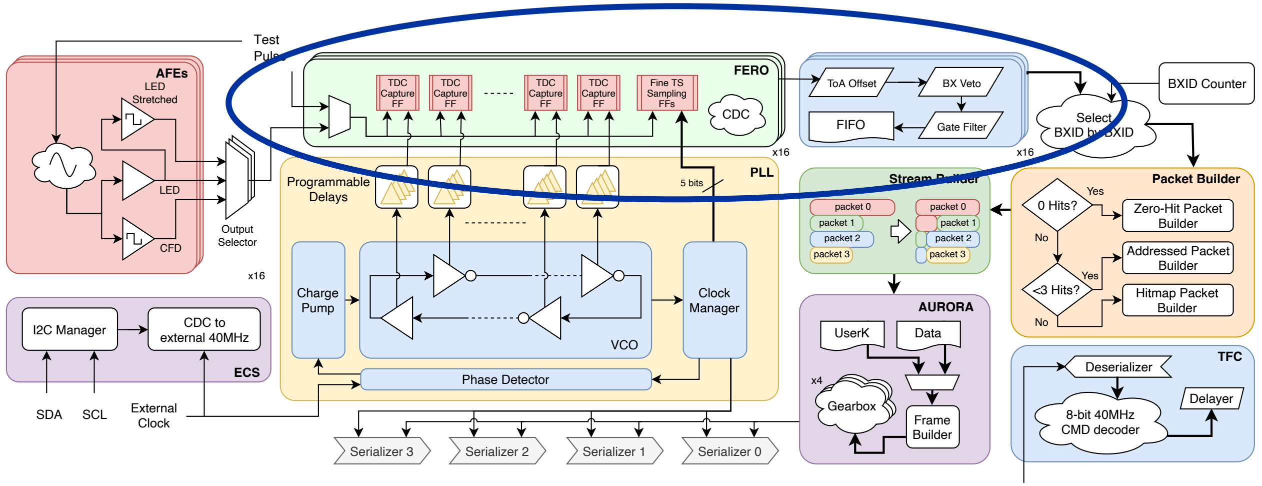
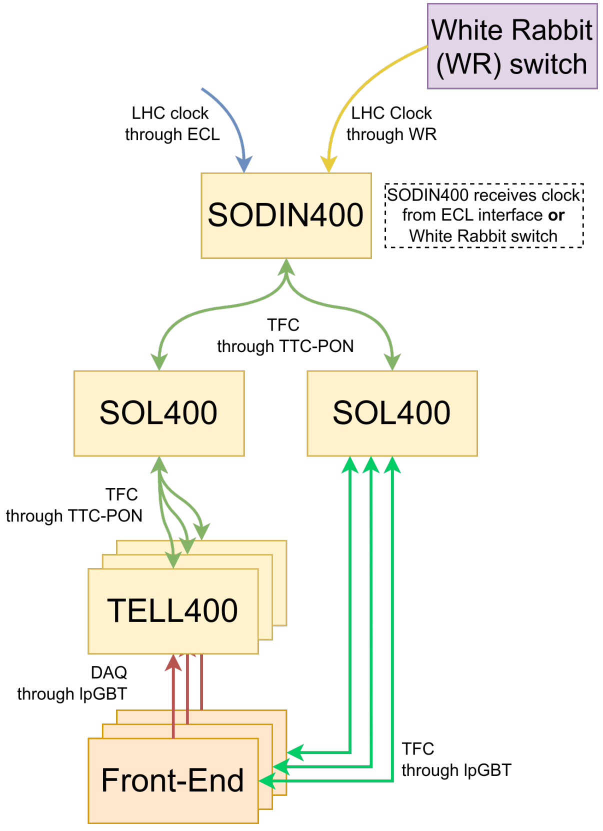




Time gate implemented during processing of TDC data inside the ASIC.

Timestamps within the gate are used for PID enhancements. Talk A. Upadhyay.

High precision clock distribution



https://cds.cern.ch/record/2886764/files/LHCB-TDR-025.pdf

For good time resolution you need an even better reference clock.

White rabbit project to provide **LHC clock** through Ethernet-based network connecting thousands of nodes.

- Random **jitter** as well as the **deterministic phase** are defined by the detector requirements - targeting O(10) ps.

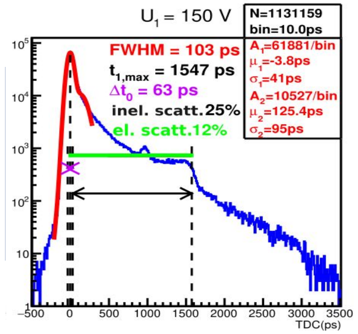
Many fibre links with TFC (Timing & Fast Control) to FE electronics.

- Minor **variations in length** affect **clock phase** at each Front-End board. How to calibrate?
- **Test pulses** not helpful: usually generated from **same clock** + paths in ASIC **not calibrated** to picosecond.
- Strategy: modules from same TFC link calibrated in time in the lab, afterwards **in-situ pulsed picosecond laser and beam data**.

Poster on Rayleigh-scattering-based calibration optics.

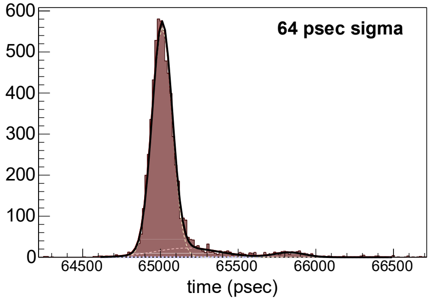
MCP-based detector readout – few examples

Excellent **time resolution is key** – typically **rate is not** a strong requirement due to intrinsic MCP limit.

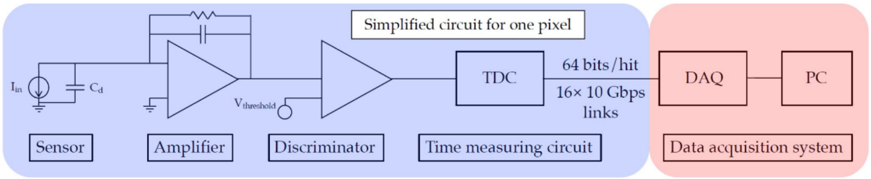


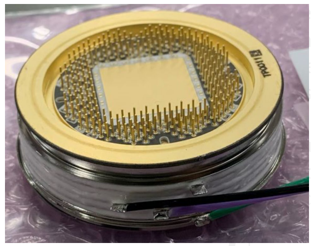
Tests of LAPPD with **PETsys TOFPET2** ASIC and **FastIC** ASIC (family of FastRICH). Talk R. Dolenec.

Also studies in LHCb with prototype **FastIC+picoTDC**.
Poster V. Placinta, Poster D. Foulds-Holt.



ANNIE **PSEC4** fast sampling (10Gs/sec) of LAPPD output. Talk M. Wetstein.

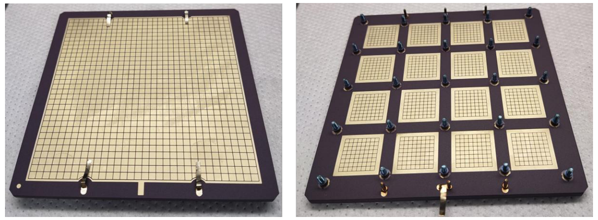




4DPHOTON with **TimePix4 ASIC**. Talk E. Franzoso.
Measured 65 ps RMS for single photons.

Anode plate vacuum side

Anode plate air side



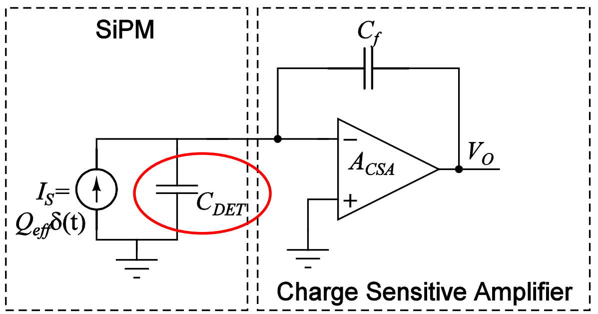
FCFD ASIC for **ePIC pfRICH**. Talk B. Page.

Front-end electronics

- Time resolution (MCP)
- **High-rate operation (SiPM)**
- Readout density and integration
- Data throughput and optical links
- Considerations on ASICs

Coupling: SiPM input signal amplifier

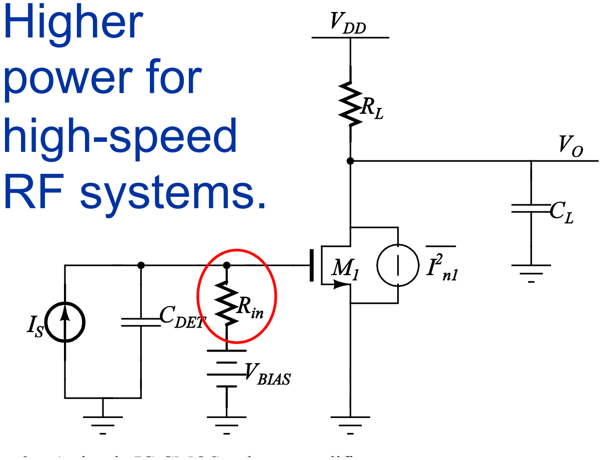
F. Ciciriello et al.



Low noise, for short and fast signals at low C_{DET}.

Charge-sensitive preamplifier: not suitable for SiPM ($C_{DET} >> C_{feedback}$ and bandwidth is strongly affected).

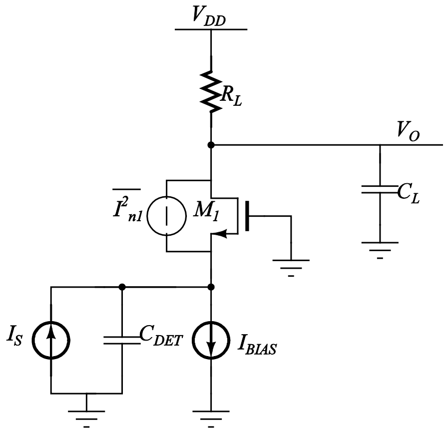
Higher power for high-speed RF systems.



Voltage preamplifier: input resistance R_{in} **large for fast signal**, $\tau_{in} = C_{DET}\, R_{in}$, but R_{in} is also in series with quench resistor $\tau_{recovery} = \tau_{quench} + R_{in}(C_{grid} + N_{SPAD} \cdot C_d)$.
i.e. results in long tails and **signal pile-up at higher rate**.

Current buffer: small input resistance and fast discharge. Relatively good power consumption.

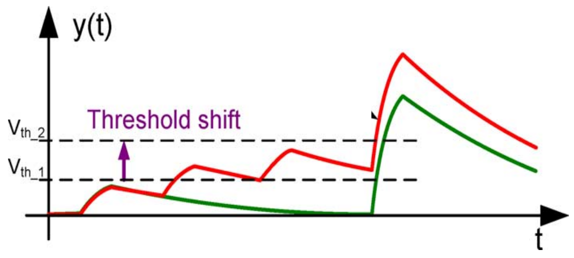
- Preferred coupling of readout ASIC to SiPM.



High-rate applications, medium power & wider input bandwidth.

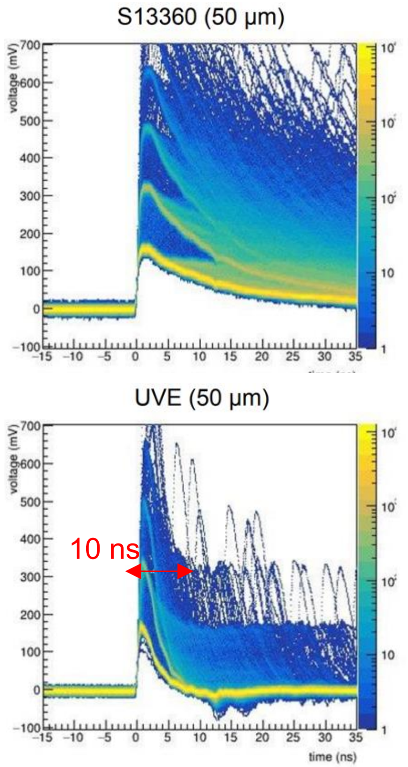
SiPM operation at high rate

MCP-based photon sensors have relatively low rate capabilities. (Talk A. Kiselev)
MAPMT (multi-anode PMTs) can operate up to about 10 MHz photon hit rate. (Talk G. Cavallero)



SiPM SPADs have a relatively slow recovery time constant.

- Potential **pile-up** of signal **at high rates**, resulting in shift of baseline and effective Leading-Edge Threshold.



Talk M. Contalbrigo

Some techniques **in ASIC to compensate** this effect in the output.

- Typically to be **tuned** to the specific signal (i.e. SiPM type and operating conditions).
- **Masks** the analogue pile-up but **doesn't remove it**. R&D required for **SiPM with fast recovery times** and tuning of quench resistor.

SiPM operation at high rate

High-pass filter between the SiPM and the ASIC input.

- Discrete components (outside / inside ASIC).

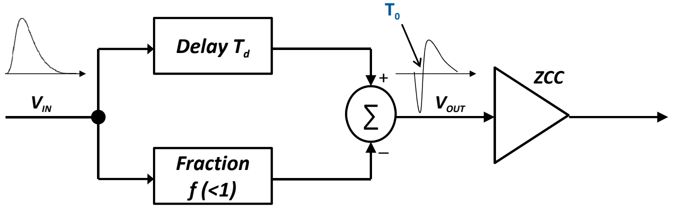
Pole-zero cancellation.

- Separate shaping stage in the readout to compensate the baseline (i.e. low frequency component).
- E.g. TF01A64 ASIC Belle-II ARICH. Poster S. Kurokawa.

Delayed leading-edge discrimination (DLED).

- Invert and delay pulse from pre-amp.
- E.g. CMS Barrel MIP Timing Detector (TOFHIR2 ASIC).
- Significant reduction in signal amplitude.

(Can CFD already partially improve pile-up effect? Similar to DLED, except only a *fraction* is inverted.)



Pole-zero cancellation A. Gola

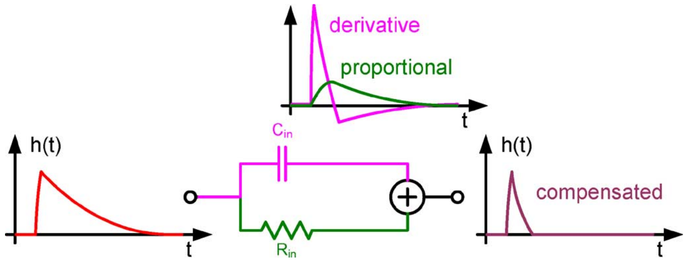


Fig. 6. Time-domain explanation of the PZ compensation.

DLED implementation TOFHIR2

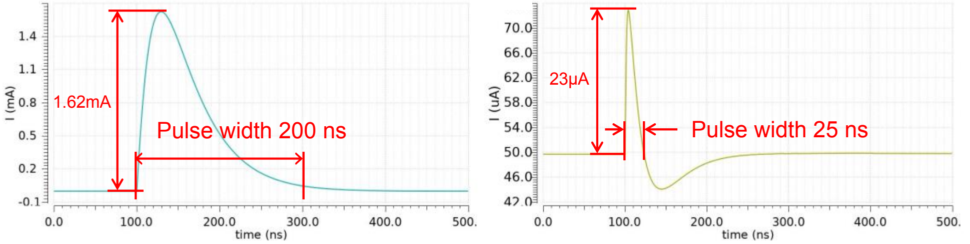


Figure 5. DLED input (left) and output (right) waveform. The example is for EoO conditions.

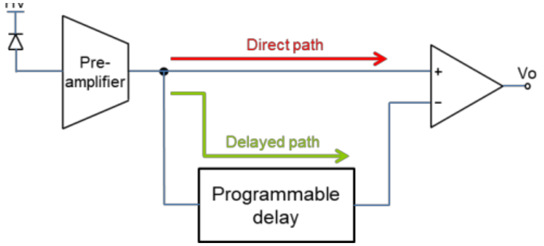


Figure 3. DLED block diagram.

Front-end electronics

- Time resolution (MCP)
- High-rate operation (SiPM)
- **Readout density and integration**
- Data throughput and optical links
- Considerations on ASICs

Spatial resolution

Detector occupancy (max av. hits per channel per event):

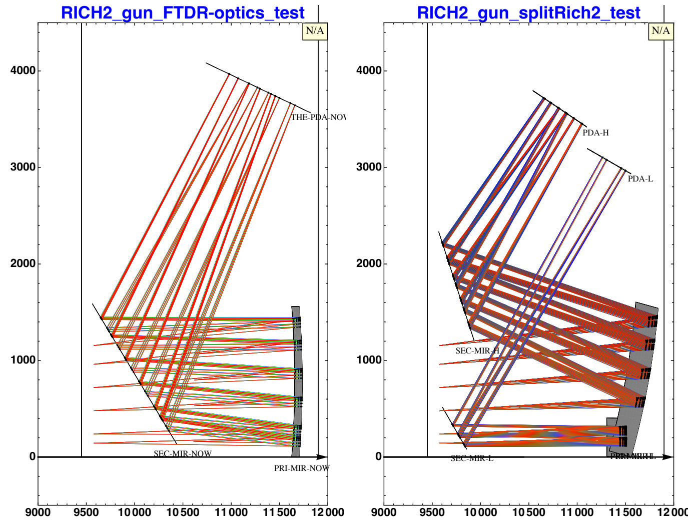
- Depends also on **optical** design.
- Need to stay in **single photon regime** for counting and timestamping.
- **Sensor** may have limited hit rate per channel (**saturation/damage**).

Cherenkov angle resolution:

- **Pixel vs chromatic and optical errors** in the system.
- Example $(\sigma_\theta \cdot f) \lesssim \sqrt{A_{ch}}$ for mirror focal point f and channel area A_{ch}.

Sensor capacitance (in case of SiPM).

- Increases with number of SPADs i.e. channel area per readout channel.



(Poster E.Spadaro Norella)

These requirements tend to push to smaller channel sizes and **denser electronic readout**.

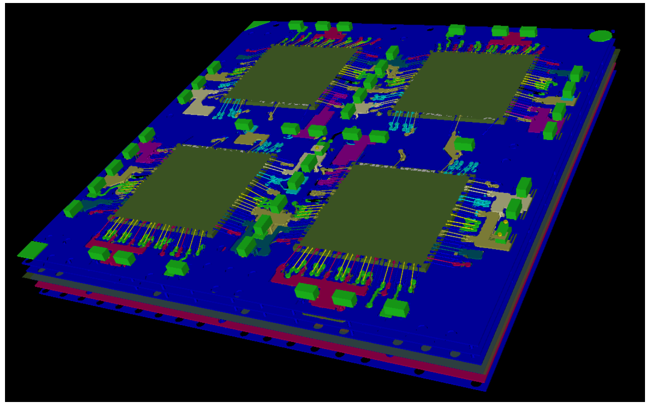
Spatial resolution: number of channels in ASIC

Why **fewer channels** per chip:

- **ASIC design**: less concerns about on-chip power-drops, clock skew, routing constraints and signal propagation delays, complication of digital packet managers, etc.
- **PCB routing** and shorter **input signal traces** (less parasitic inductance).

Why **more channels** per chip:

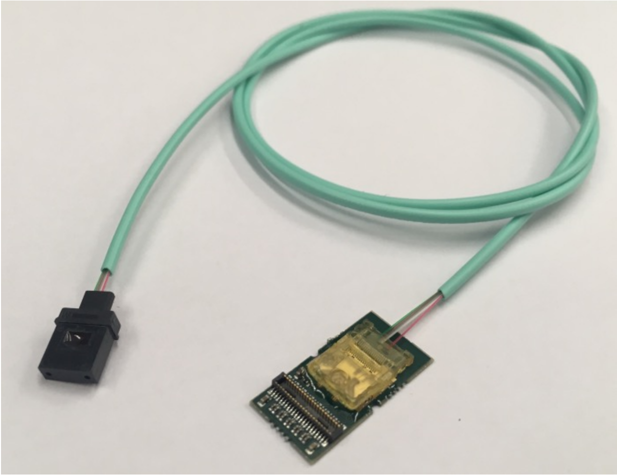
- Smaller **overheads due to packaging** of the silicon die: less space on the board.
- **Fewer control and clock signals** to distribute on board (“less daisy-chain”).
- Some **optimisations** e.g. in number of serialisers for chips with low data rates.



System-in-Package for FastIC+ 32ch (FastRICH 64ch).
Talk R. Pestotnik.

ASIC footprint / inputs is not necessarily the limiting space constraint in a detector system: there are other considerations such as ***power consumption*** *and* ***data throughput.***

bPOL12V plugin ~25 mm

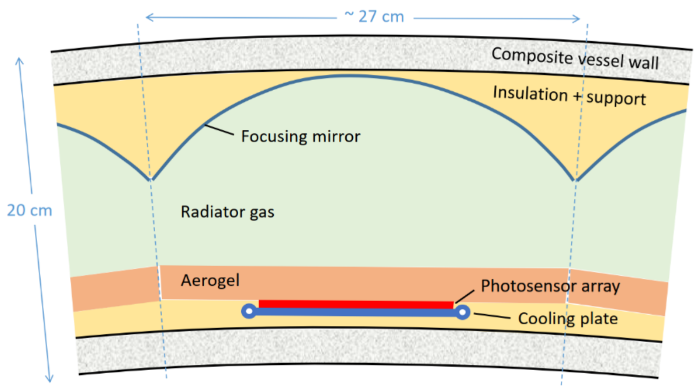


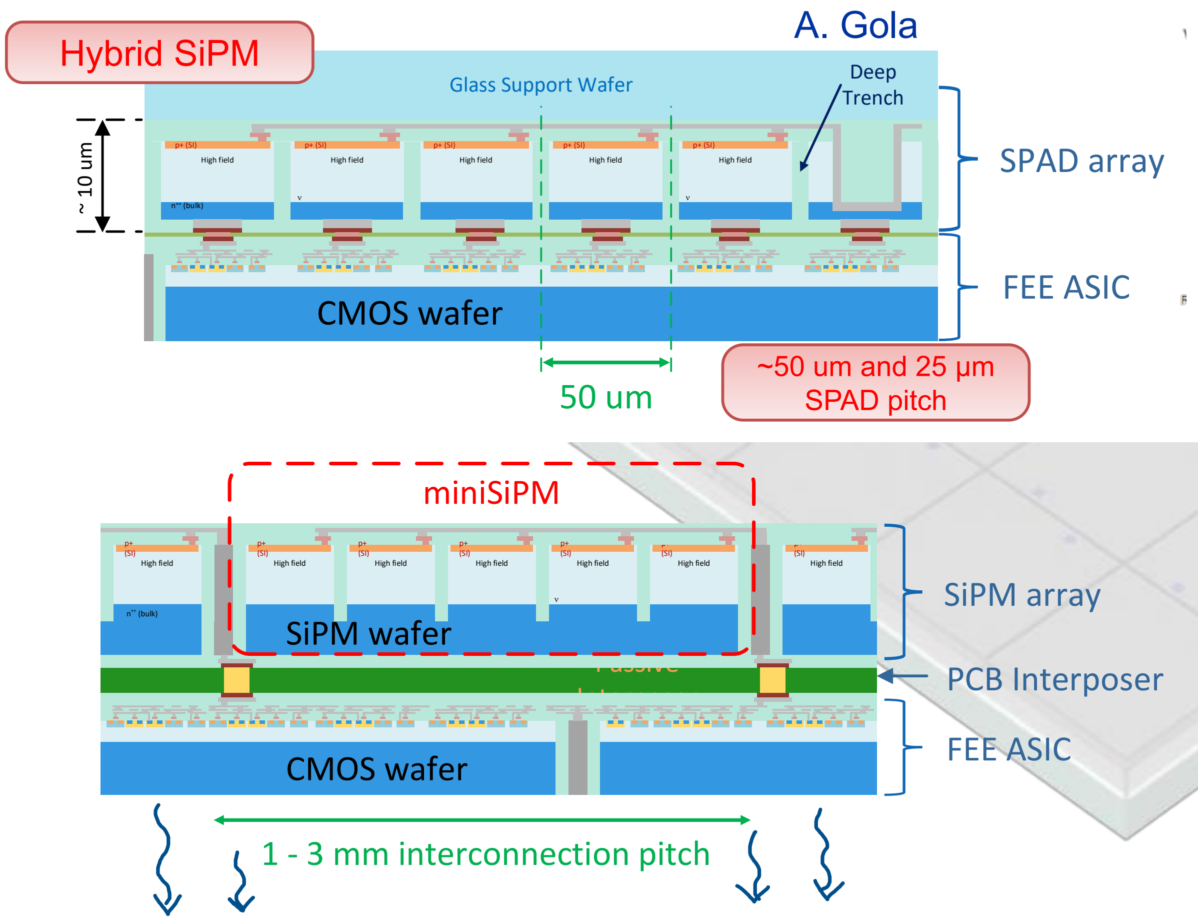
VTRX+ footprint 10mm by 20mm + fragile pigtail

Compact, close-packing and 2.5D or 3D sensors

For even **better SPAD coupling and control**, electronics can also be (partially) integrated into the silicon.

- **Digital SiPM** (Talk C. Brushini, Poster R. Dolenec) and **2.5 and 3D sensors** (Talk R. Pestotnik).
- Suitable for **compact designs** e.g. ARC.





Highly interesting for performance but also brings power consumption of FE readout close to the SiPM.

- Potential issue for **cooling of SiPMs at low temperatures**.

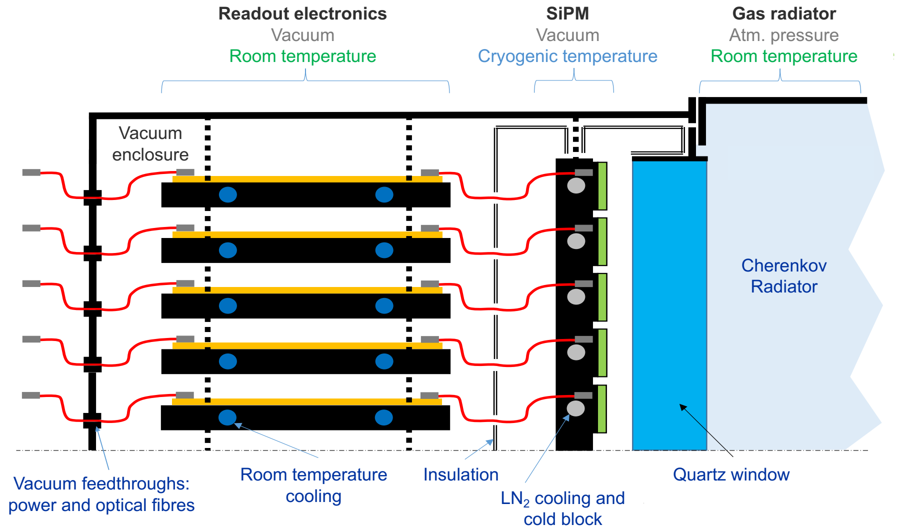
Cryogenic demonstrator for LHCb RICH

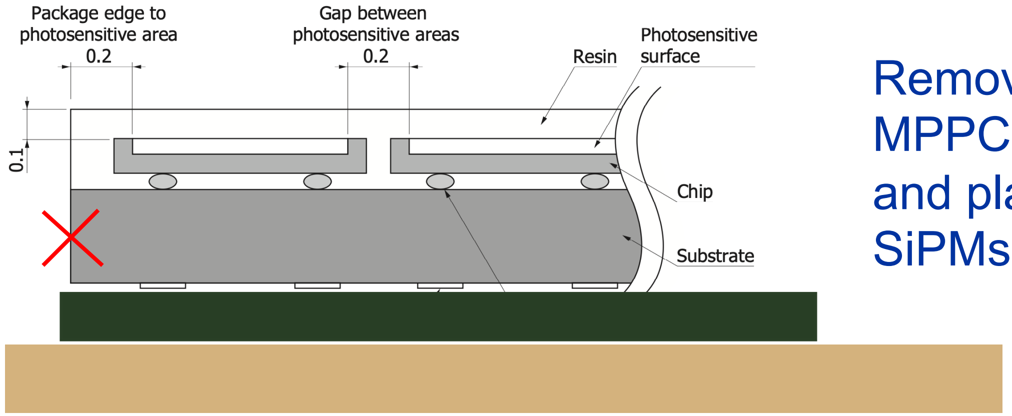
Thermal path typically from the **back-side** with flex-PCB.

Complex ASIC analogue + digital not simulated at cryo-T. Also the **optical links** would not be suitable.

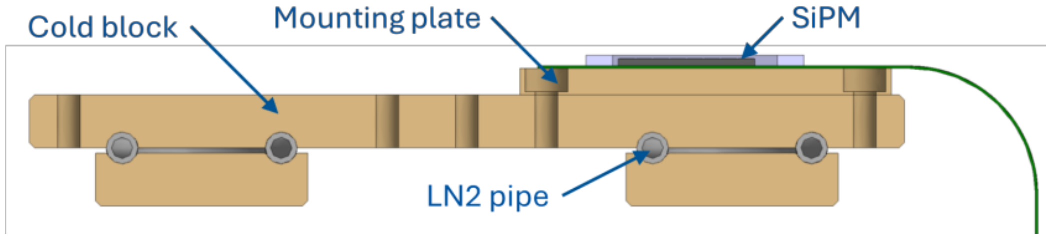
Flexible-PCB to absorb **thermal expansion mismatches** and keep **electronics at room-T**.

- **Transmission line** (order 10 cm) – inductance slows fast-timing edge (but also shunts capacitance).
- **$\sigma \sim 103 \pm 5$ ps** (59V for 3mm S13361-series) with FastIC+picoTDC (FastRICH). Poster L. Malentacca.





Remove HPK MPPC substrate and place single SiPMs directly?



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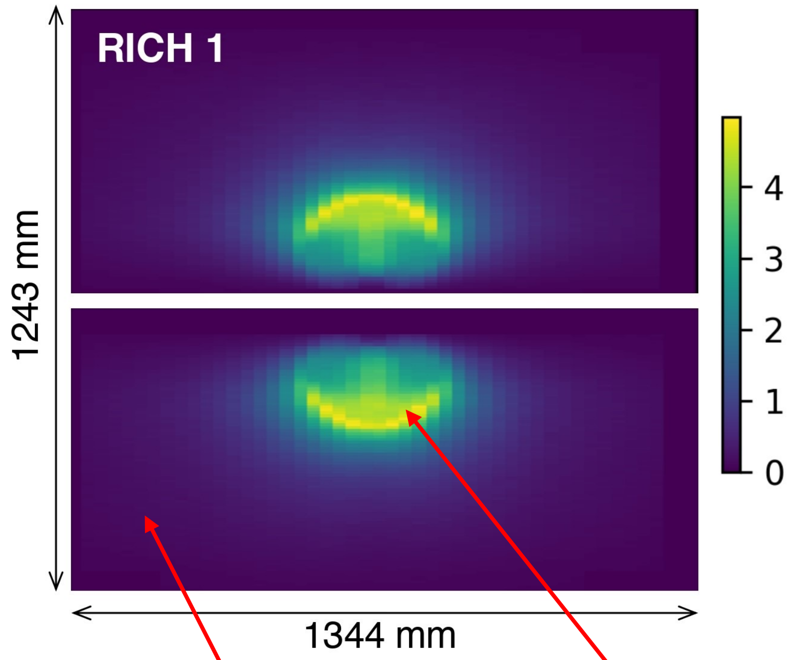
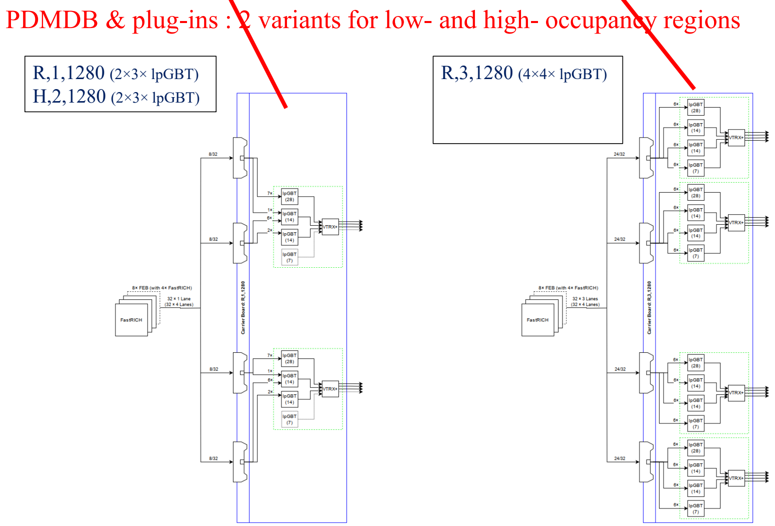
Data throughput at the front-end

Increasing **granularity** + additional picosecond **time** information = more **data**.

- Hits may be concentrated in smaller region of the detector: **allocate bandwidth non-uniformly**.
- **Configurable** number & speed of serialisers: low-occupancy regions equipped with fewer optical links.





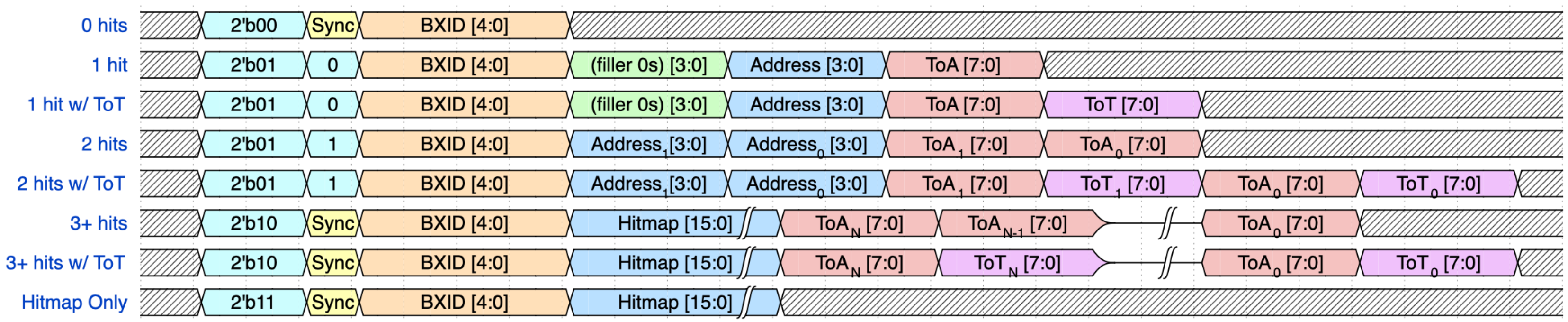
Other tools to reduce data throughput:

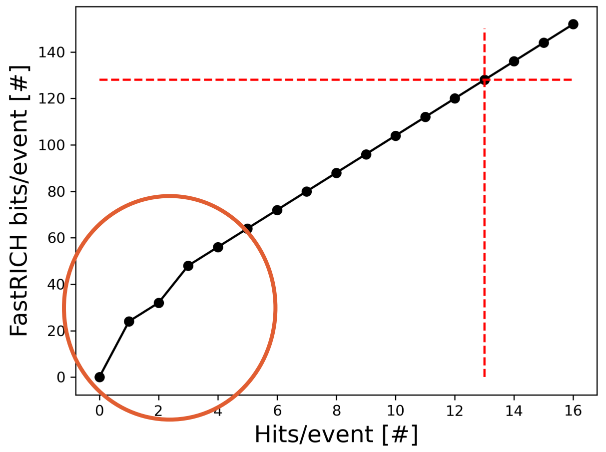
- **CFD** (constant-fraction discrimination) avoids need to submit ToT bits for time-walk correction.
- **Time gating**.
- **Zero-suppressed** dynamic output format.

Data packet scheme (FastRICH)

Shift towards more **decoding complexity** at back-end (i.e. packets & Aurora).

- **Commercial** electronics at back-end and **fewer custom FE links**.



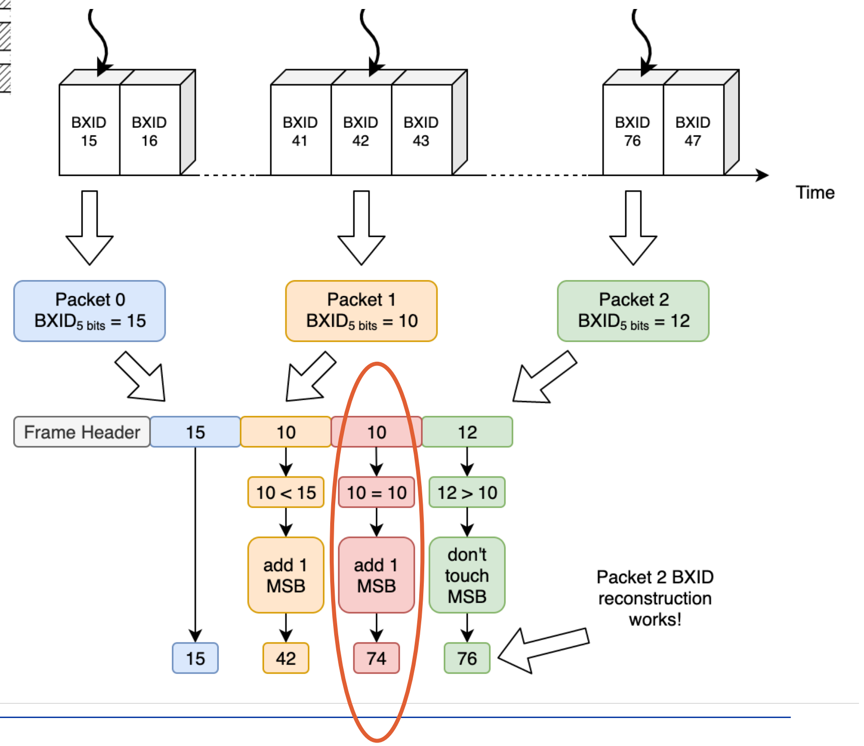


Packet scheme with reduced size for 1 and 2 hits.

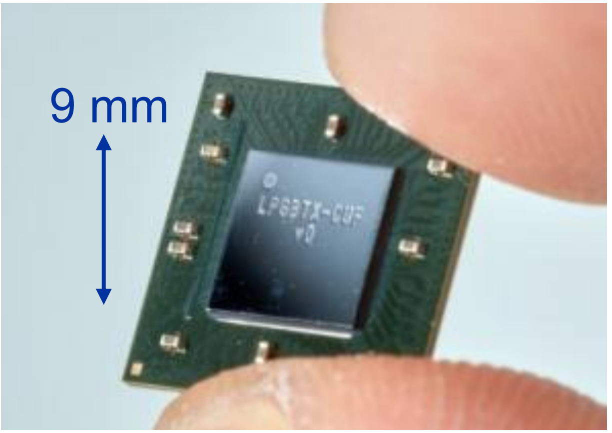
- More than 20% additional data reduction (mostly from low-occupancy regions)
- Some filler bits to align to byte-boundaries.

5-bit BXID information.

- Risk of **BXID aliasing** at the back-end.
- Automatically insert **0-hit data packets** when needed. Full BXID also sent with Aurora **64b66b** frame header.

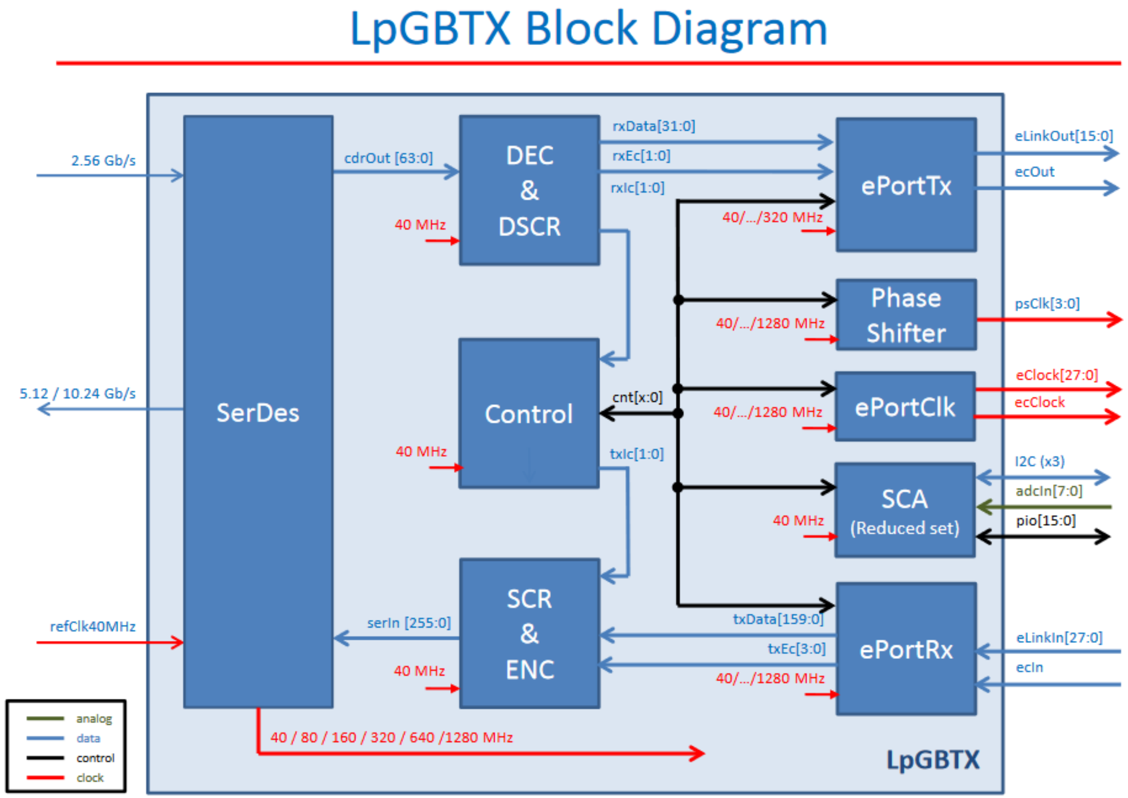


Optical link chipset and compatibilty



For ‘**all-ASIC**’ solution, no ‘glue’ layer of FPGA to optical interface.

- Need **direct compatibility by design** with e.g. lpGBT / VTRX+ chipset (CERN radiation-hard optical links for HL-LHC experiments).



lpGBT (low-power GBT)

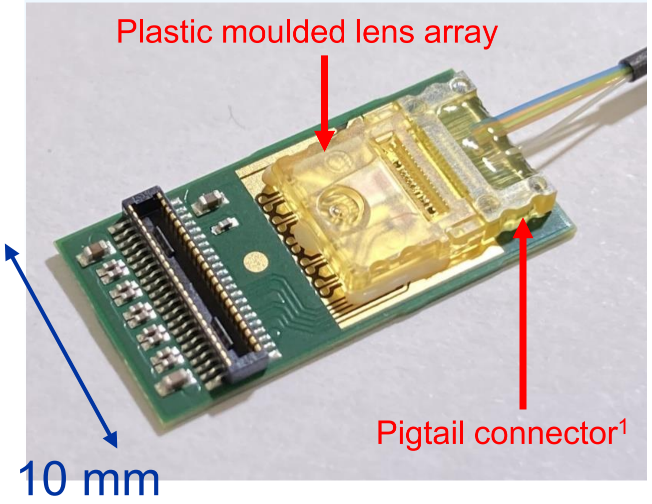
- Data acquisition with forward-error correction, up-links up to 10.24 Gbps.
- Typically bi-directional controls link (Timing Trigger Control and Slow Control) including 2.56 Gbps down link. .
- **Negiligble clock jitter** (order ps).
- Very high **radiation hardness** (>1MGy).

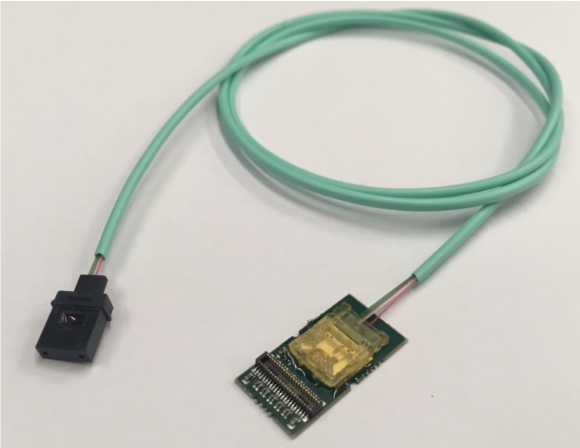
Optical link chipset: VTRX+

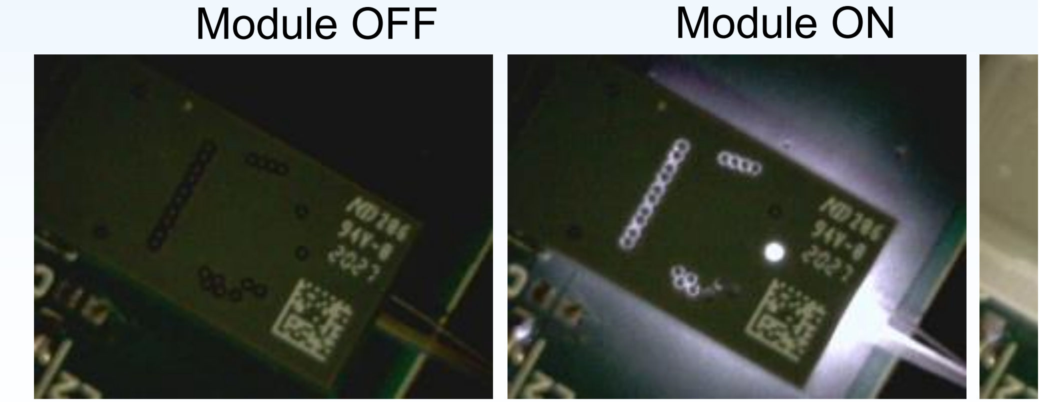
Commercial alternative e.g. SFP+.
- High material budget
- Not radiation hard.

VTRX+ is miniaturised, pluggable and radiation-hard.

- Up to 4 Tx and 1 Rx link.
- Temperature from -35°C to +60°C, dose of 1 MGy and 10^{15} n_{eq}/cm^2.
- Electrical assembly with optics is **extremely fragile**.
- Optics and pigtail **emit light around 850 nm**: **large background for single-photon SiPMs**.
- Optics include “open” mirror: cannot be painted.
- Need custom cover that is compatible with cooling (typically couple hundred mW).







Photos taken using an infrared sensitive camera

J. Troska “The VTRX+ story”

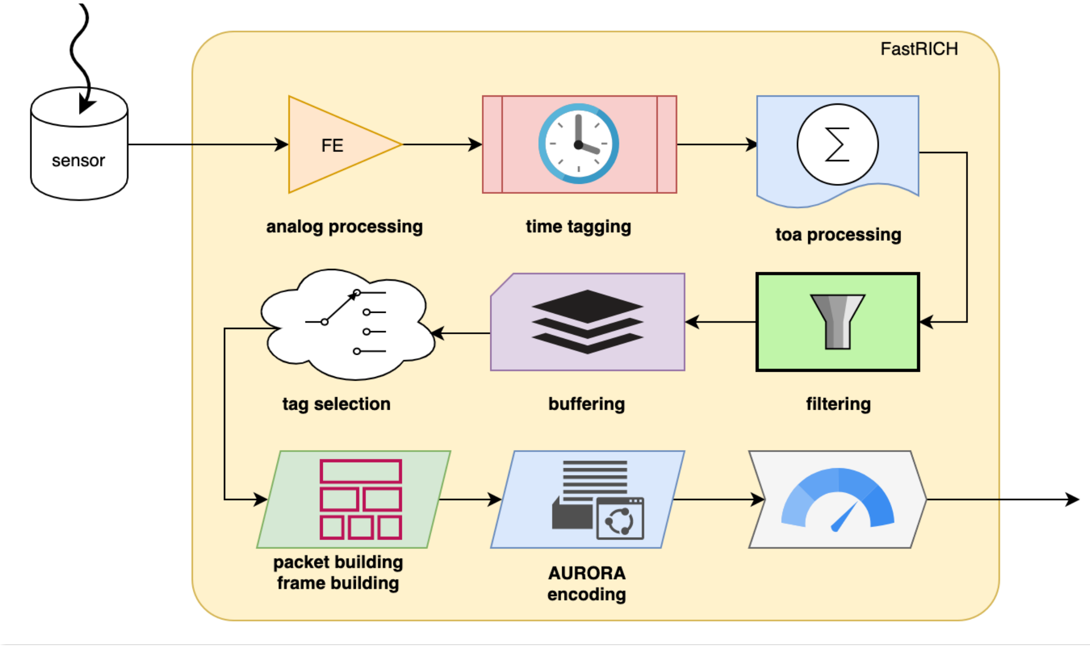
Front-end electronics

- Time resolution (MCP)
- High-rate operation (SiPM)
- Readout density and integration
- Data throughput and optical links
- **Considerations on ASICs**

‘Digital-on-top’ ASIC design

New method for design of complex ASICs: ‘digital-on-top’.

- **Complex design** means more **complex bugs**.
- **Fully scripted** automated flow to drive digital tools to design and implement digital circuitry around the analogue blocks.
- **High level simulation and verification** throughout design.
- “**First silicon success**” and strong mitigation of risk.



Upside: **Reduced cycles of prototyping**.

- Gain **time** (typically 3+ months for Multi-Project Wafer run plus additional time for packaging)
- and **cost** (increasing price of MPW runs).

Downside: need **verification engineers** with specific skillset, **significant fraction of development time**.

Many different front-ends

Specifications
Technology
Target sensor
Channel
Amplifier
TDC bin
Input bandwidth
Mode
Power [mW/ch]
Bits per hit
Encoding
Event rate [MHz/ch]
Serialiser max. rate [Gbps]
Target radiation

The wide range of requirements also leads to a large number of ASICs and readout electronics in the field.

- Often more **generic ASICs** may not pass due to one missing requirement.
- It may help to **unify experimental control systems** i.e. try to avoid different hard requirements imposed by DAQ sync commands, start-up and reset sequences, slow-control interfaces etc.
- **Compatibility with the lpGBT** (well-established for HL-LHC upgrades) may be a good step.
- **System-in-Package** may bring flexibility in number of channels/package i.e. tailor the package not the silicon die.

ASIC “families”

More abundant as **design modules can be shared** between different ‘flavours’ of ASICs.

- Perhaps easier with digital-on-top design flow.

Some examples

- Weeroc (MAROC, PETIROC) commercial series.
- Timepix4 and VeloPix.
- Fast(RI)IC(+).
- … and more!

weeroc

Product lineup

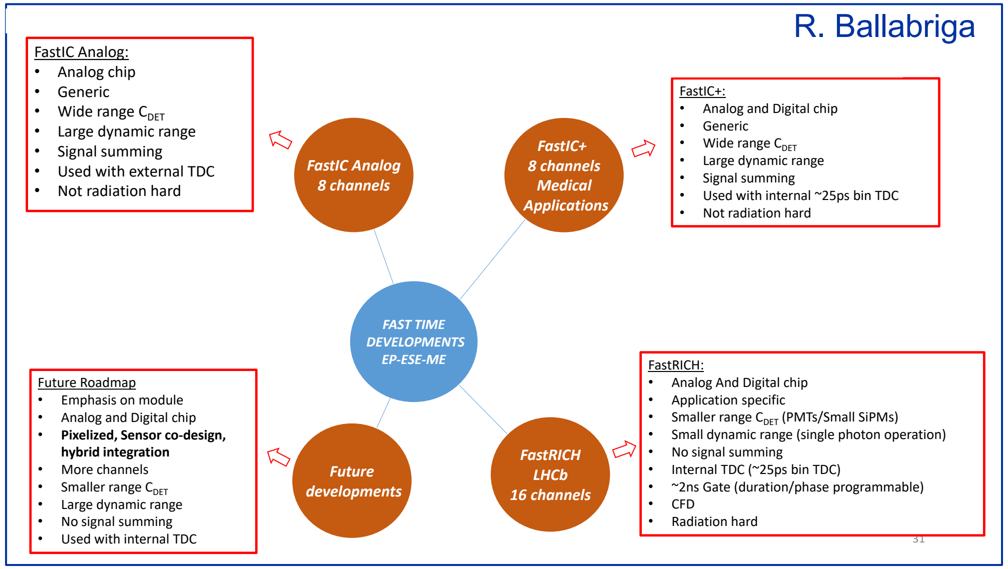
	Citiroc	Radioroc	Temporoc	Psiroc	Poproc	Liroc
Prod. Version	1A	2	2	1	1	2
TRL	9	4	4	4	4	4
Package	PQFP160 TFBGA353	BGA516	BGA516	BGA516	BGA516	BGA516
Detector Compatibility	- SiPM - SiPM array	- SiPM - SiPM array	- SiPM - SiPM array	- PIN diodes - Silicon strips - GEMs	- SiPM - SiPM array	- SiPM - SiPM array
Channel	32	64	64	64	64	64
Measurements and operations	- Free running trigger - Ext trigger - Charge (shaper) - Time (trigger)	- Free running trigger - Ext trigger - Charge (shaper, TOT) - Time & charge trigger - Photon counting	- Free running trigger - Charge (shaper) - Time (TDC)	- Free running trigger - Ext trigger - Charge (shaper, TOT) - Time (trigger)	- Free running trigger - Photon counting - Time (trigger) - Charge (TOT)	- Free running trigger - Photon counting - Time (trigger) - Charge (TOT)
Outputs	- 32 triggers - Trigger OR - 1 analog multiplexer (charge)	- Selectable per channel: • 1 LVDS trigger • 2 Single ended triggers • 2 shaper outputs - 3 triggers NOR - 2 Analog MUX	- Trigger OR - Analog MUX (charge) - Digital MUX (trigger) - ADC (10b) - TDC (50 ps)	- Selectable per channel: • 1 LVDS trigger • 2 Single ended triggers • 2 shaper outputs - 3 triggers NOR - 2 Analog MUX	- 64 LVDS trigger outputs	- 64 LVDS trigger outputs
Input Polarity	Positive	Positive	Positive	Positive (optimized) Negative	Positive (optimized) Negative	Positive, negative
Applications Main features	Energy measurement Time of flight Photon counting Calibration input SPE spectrum Input DAC SiPM HV adjust.	Energy measurement Time of flight Photon counting ~ 200 MHz SPE spectrum Dual time thresholds SiPM HV adjust.	Energy measurement Time of flight Time stamping SiPM HV adjust.	Energy measurement	Time of flight Photon counting ~ 300 MHz SPE spectrum Energy measurement SiPM HV adjust.	Time of flight Photon counting ~ 300 MHz SPE spectrum Energy measurement SiPM HV adjust.

*QFP packaging will be phased out and replaced with equivalent BGA packaging. Glossary: ADC : Analog to Digital Converter – TDC : Time to Digital Converter

Product lineup

Maroc	Catiroc	Gemroc	Skiroc	Petiroc	Triroc
3A	1	1	2A	2A	1A
9	8	9	8	6	8
PQFP240 TFBGA353	TQFP208	PQFP160	BGA400	TQFP208 TFBGA353	TFBGA353
- MA-PMT, PMT - SiPM, SiPM array	- MA-PMT, PMT	- micromegas - GEMs	- Si PIN diodes - Silicon strips	- SiPM - SiPM array	- SiPM - SiPM array
64	16	64	64	32	64
- Free running trigger - External trigger - Charge (shaper) - Photon counting - Time (trigger)	- Free running trigger - Ext trigger - Charge (shaper) - Time (trigger) - Time (TDC)	- Free running trigger - Ext trigger - Charge (shaper) - Data 3-level trigger	- Free running trigger - Ext trigger - Charge(shaper) - Time (TDC)	- Free running trigger - Charge (shaper) - Time (trigger) - Time (TDC)	- Free running trigger - Charge (shaper) - Time (TDC)
- 64 Triggers - Trigger OR - 1 analog multiplexer (charge) - ADC (8/10/12b)	- 16 Triggers - 16 Shapers - Trigger OR - ADC (10b) - TDC (10b)	- Trigger OR - 1 analog multiplexer (charge)	- Trigger OR - 1 analog multiplexer (charge) - ADC (10/12b) - TDC (10/12b)	- 32 triggers - Trigger OR - 1 analog multiplexer (charge) - 1 digital multiplexer (trigger) - ADC (10b) - TDC (10b)	- Trigger OR - analog multiplexer (charge) - 1 digital multiplexer (trigger) - ADC (10b) - TDC (10b)
Negative	Negative	Negative	Positive	Negative (optimized) Positive	Negative (optimized) Positive
Energy measurement SPE application Photon counting rate < 30MHz MA-PMT gain adj.	Energy measurement Time stamping Low dead time Zero suppress data	Energy measurement Time stamping Data readout: 3-level trigger	Energy measurement Time stamping	Energy measurement Time of flight Time stamping Photon counting Input DAC SiPM HV adjust.	Energy measurement Time of flight Time stamping Zero suppress data Input DAC SiPM HV adjust.

out and replaced with equivalent BGA packaging. Glossary: ADC : Analog to Digital Converter – TDC : Time to Digital Converter



Conclusion

Choice of RICH front-end readout is strongly application-specific.

- Looser constraints: **off-the-shelve** (FPGA, SFP+), **flexible** solutions preferred.
- Tighter constraints: **ASIC** solutions, **custom** readout.

4D resolution, **rate** capability and **readout density** are key parameters.

- But measures needed to keep control over **power** consumption and **data** throughput.

ASICs are getting more **complex** and **abundant**.

- **Digital-on-Top** designs with ASIC families.
- Enabling our community with the tools for **next-generation RICH detectors**.