STT read-out

- Detectors requirements and layout
- Read-out concept
- Developments of Analog FEE and Digital Boards
- Test results (next presentations)

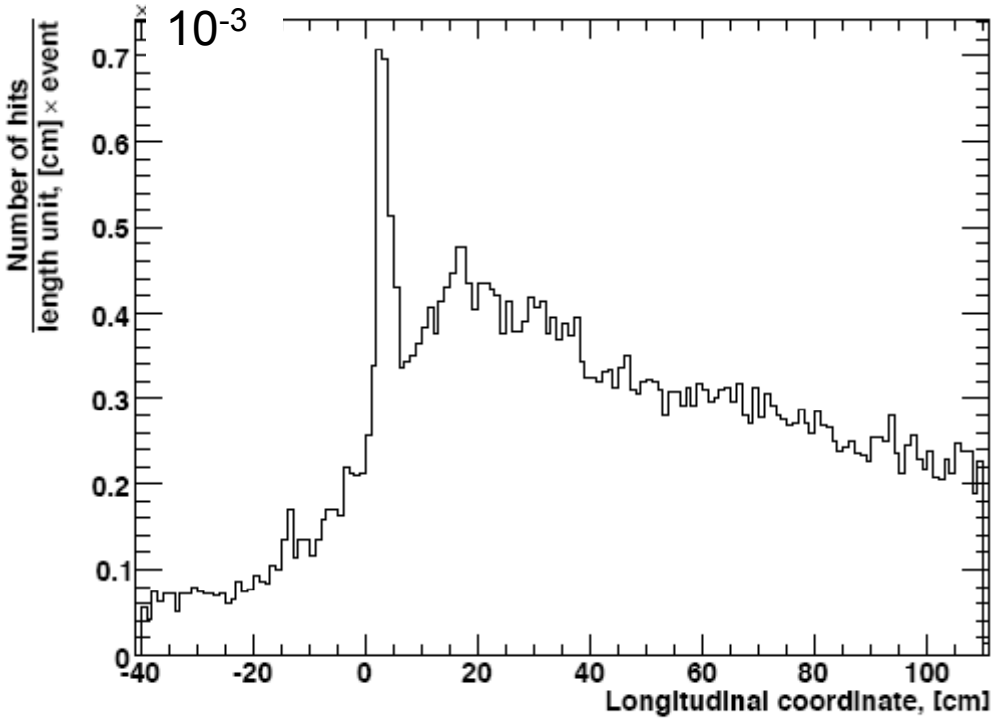
PANDA STT

- Central tracker : 4636 straws
- Forward tracker : ~13500 straws
- Drift time ~ 200 ns (B=2T)
- **Time measurement**: req. electronic resolution < 1 ns
- sensitivity (threshold) ~ 2 fC
- **dE/dx, Q for PID :** π**/p/K** separation for p<0.8 GeV/c
  PID (Central tracker): 10% resolution in 24 layers
- detector capacitance: ~ 10-15 pF (9 pF/m)
- Hit rates up to 800 kHz/channel

Expected rates

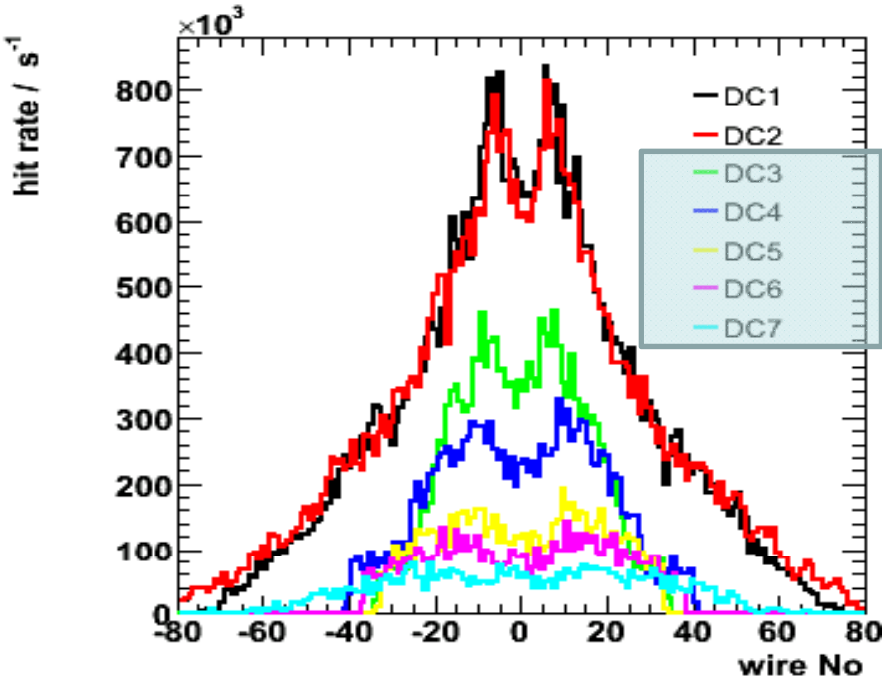
p_{beam} = 15 GeV/c, N_{Int}=2x10^{7} s^{-1}

Hit rate/cm/event in Central STS



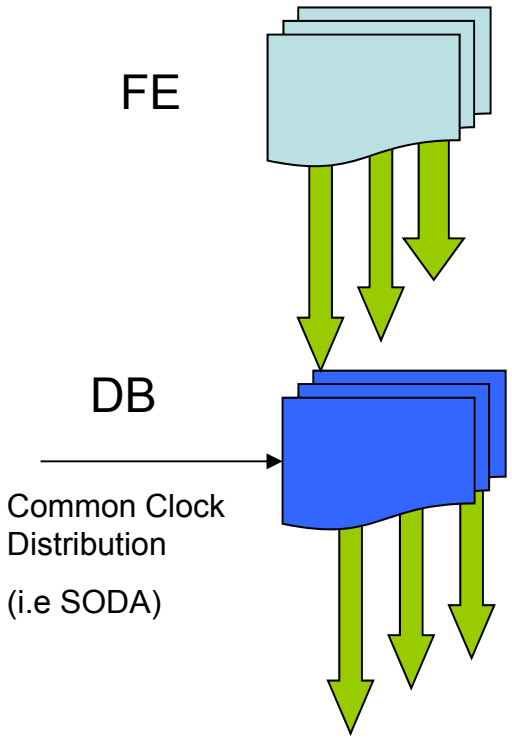
Mean rate: ~ 800 kHz for 150cm long tube (Max 14 KH/z for z~ 2 cm (±1)

Hit rate per wire in Forward STS



Max rate: ~400 kHz for STS3 (New simulation shows x 3 ! more)

Straw tubes read-out chain



Panda DAQ - network

FEE anlog : Preamp+ Shaper+ BLR + Discriminator

- Dynamic Range ~ 5fC - 1pC, noise <1 fC
- Peaking time ~10-40 ns,
- Signal duration < 250 ns (pile-up < 10% @ 800 kHz)
- Gain 2-15 mV/fC

Digital Boards

- Multihit TDC : Time measurement + TimeOverThreshold (TOT) for charge measurement OR/AND signal after shaper as input to FADC
- binning 0.5-0.8 ns
- Zero suppression & Hit detection.. Slow /Run/Data flow control

Data Concentration :

- gathering and sorting of hits marked by time stamps in epoques (i.e 500 μs bunch)
- nGbit/s Optical serial link

Developments

- Paralel concepts based on TDC Kraków (AGH, JU) , GSI and FADC (Juelich) :
- New dedicated analog ASIC (preamp+shaper+ BLR+ LE discriminator)

  D. Przyborowski/M.Idzik (AGH)
- Booster + Shaper (BLR, tail cancelation) (based on discrete elements)

  (Juelich)
- TRBv3: TDC in in FPGA - follow-up of TRB based on HPTDC

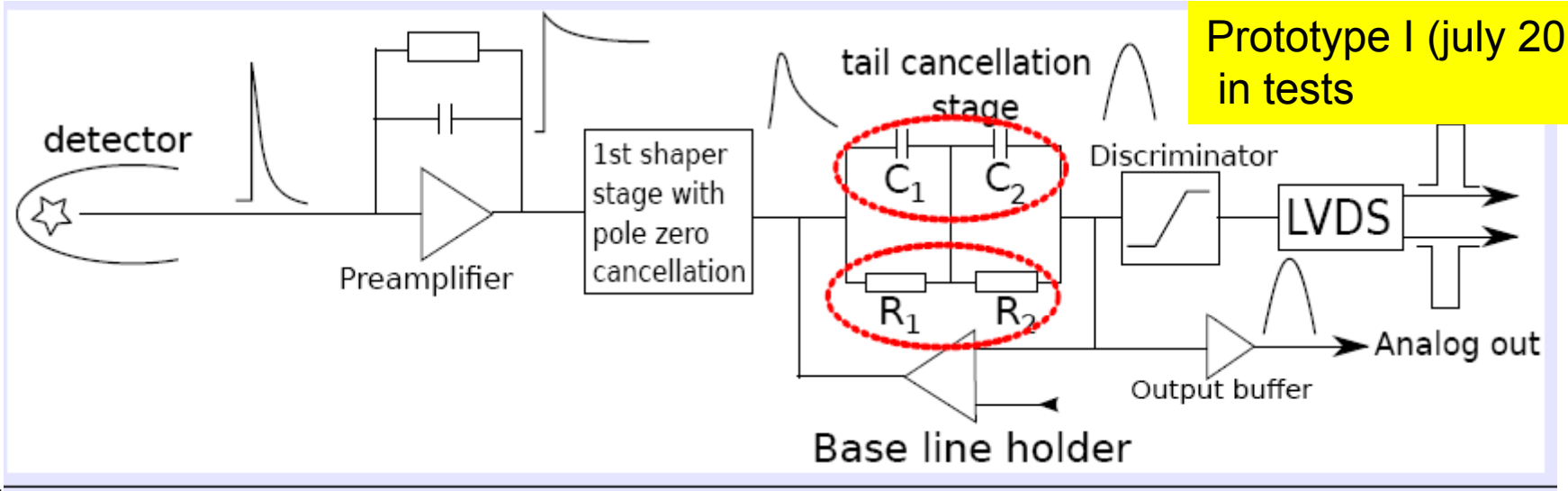
  (M.Traxler/J.Michel/M.Pałka/C. /Ugur/G. Korcyl)

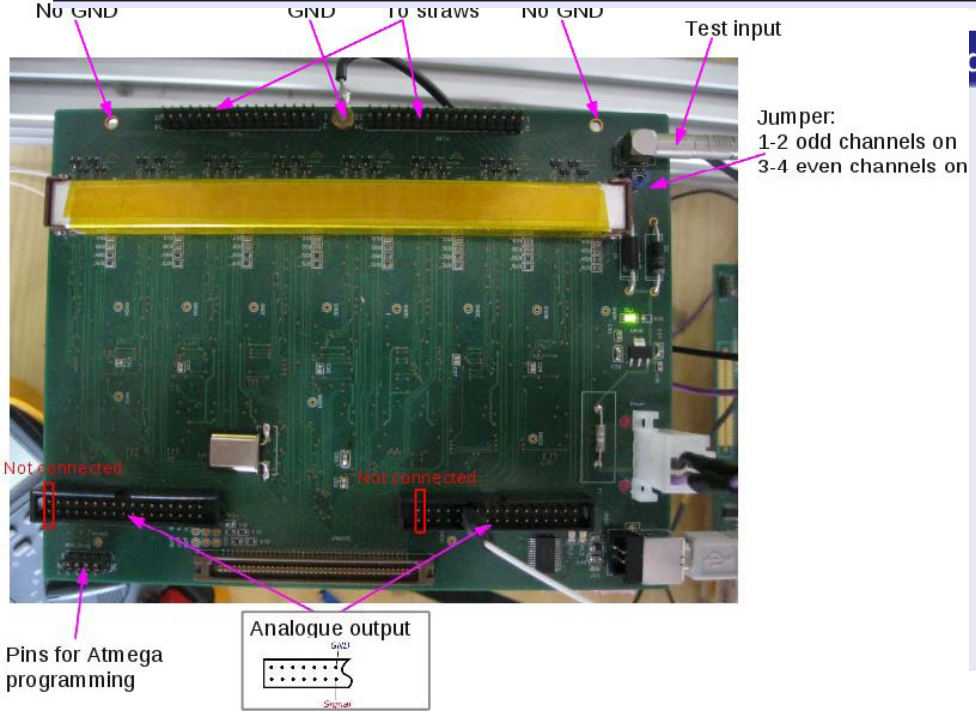
  TOT: amplitude measurement via width of signal above threshold (TDC)

  sufficient for needs of FTS but maybe not good enough for CTS
- FADC: charge measurement in FADC (~250 MHz sampling) – Juelich or via time measurement in FPGA on Addon card on TRBv3 –M. Pałka

New ASIC for Panda STS

Prototype I (july 2011)
in tests

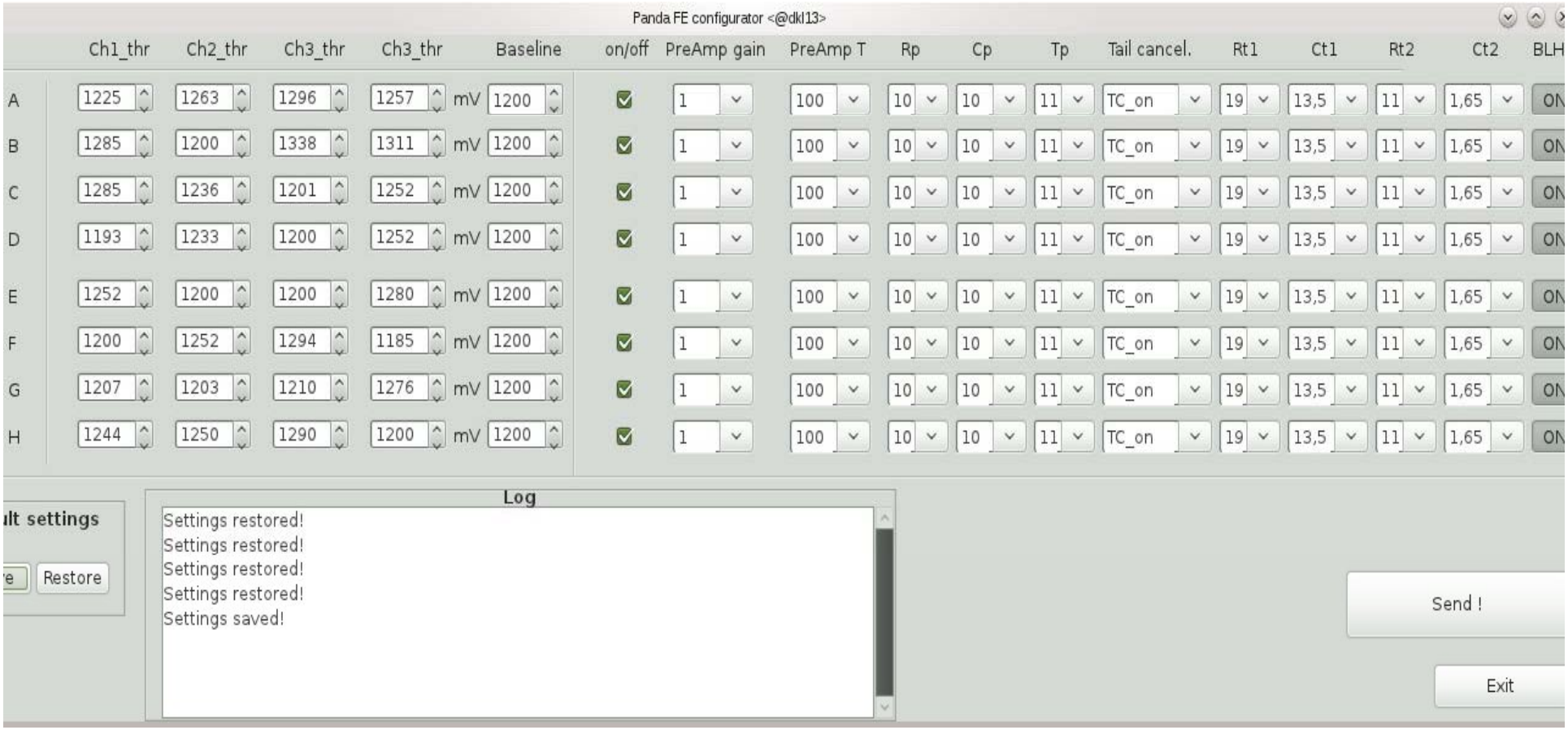




detailed specification

Parameter	Range/Value
Charge gain [mV/fC]	3 – 20
Peaking time (for delta) [ns]	15–40
Power consumption [mW]	$\approx$ 16
ENC [fC]	$<$ 0.4
1^{st} TC time constant [ns]	20 – 500
2^{nd} TC time constant [ns]	3 – 40
Input transistor parameters	
Dimensions W/L	$2000\mu/0.35\mu$
Transconductance [mS]	$\approx$ 26
Drain current [mA]	2

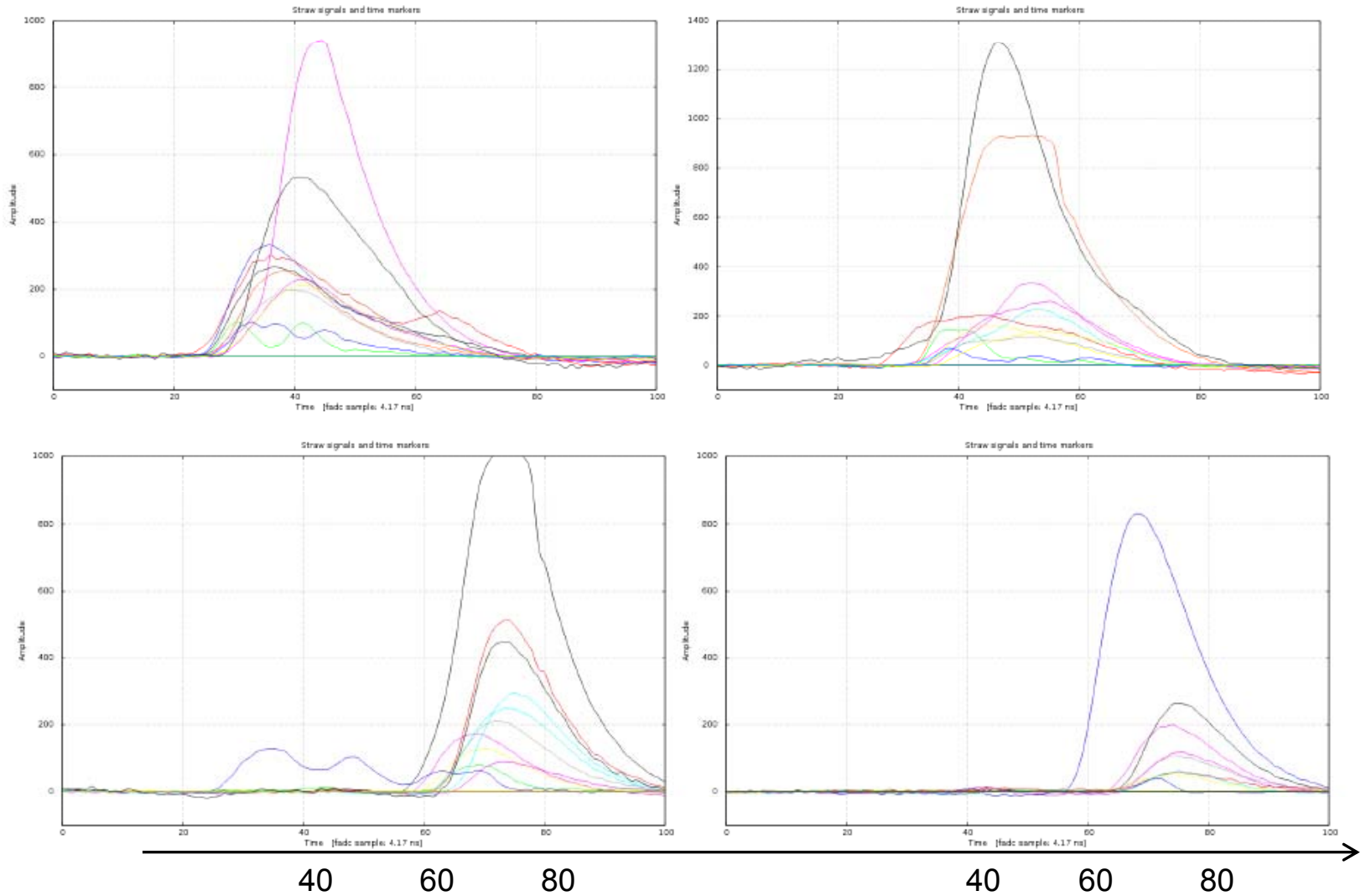
ASIC set-up



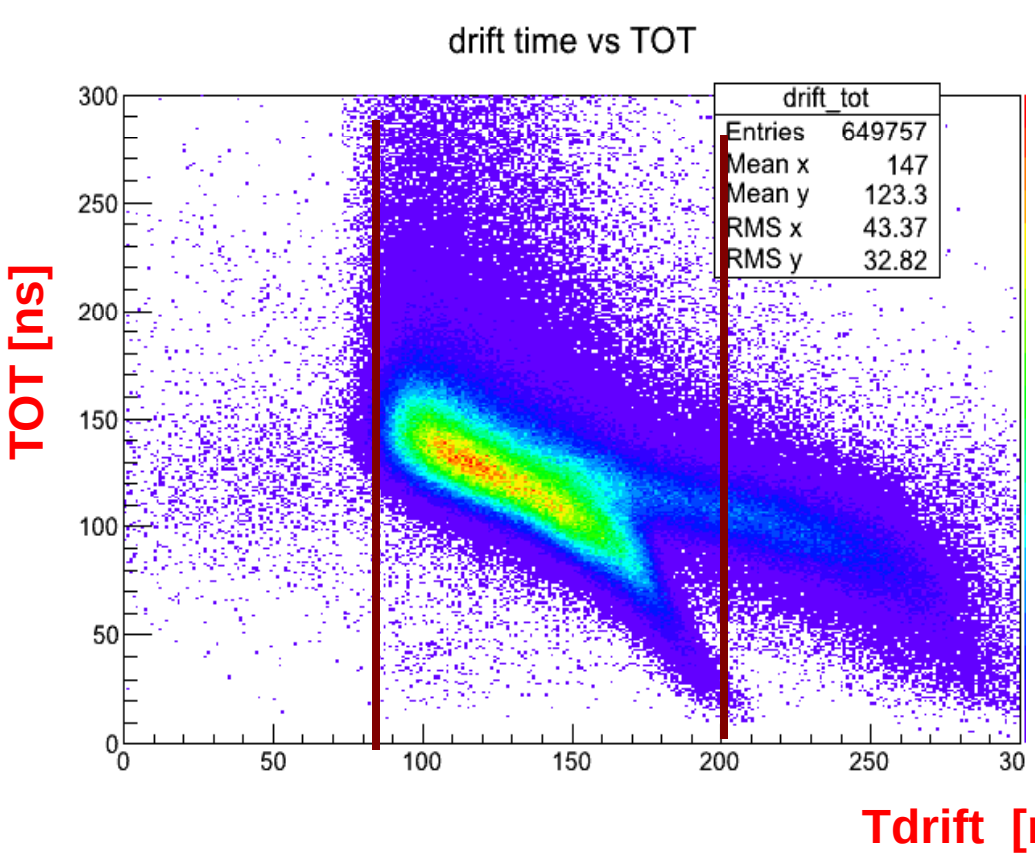
Preamp Gain 1, rising time ~40 ns,pulse duration ~ 150 ns

- stable ASIC operation (no oscilation etc), used for beam time tests in Juelich
- 3 boards (32 channel each produced)

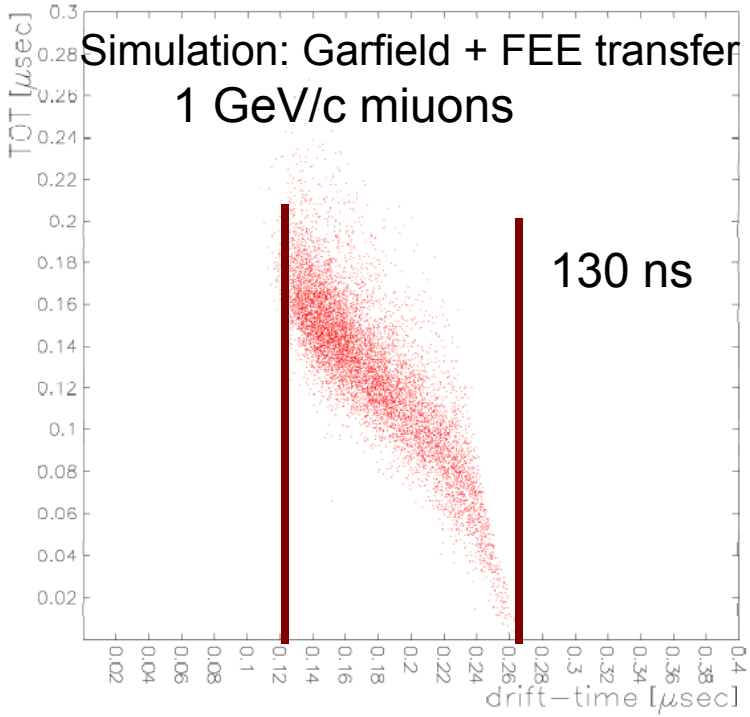
Examples of ASIC signals in FADC



TOT vs Tdrift -0.9 GeV protons



September' 12 Juelich



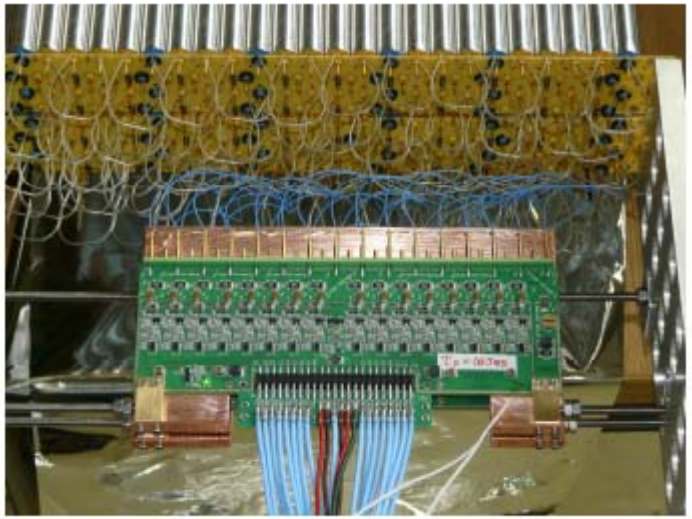
as expected besides second leg structure in TDrift>130 ns ?

: pile-up due to micro bunch structure of the beam

Juelich FEE (analog) solution (based on discrete components)

Signal booster

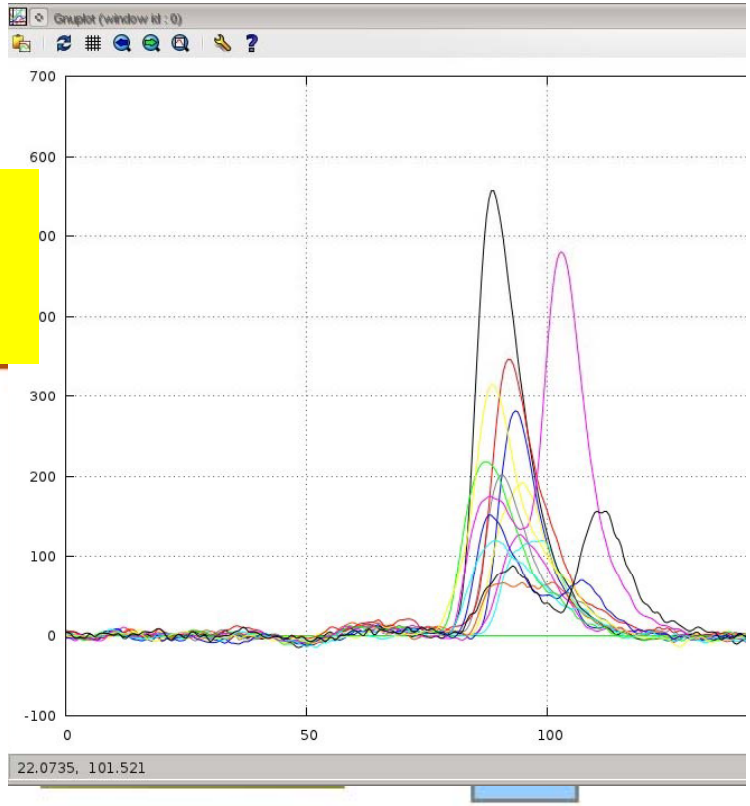
Low power charge sensitive
Preamplifier (installed at detector)



FADC:
Q, LE,
TOT

up to 5 m

Examples of signals taken
with 0.9 GeV protons



IKP FZJ & IFJ PAN Kraków

Specification of shaper

Signal booster

16-channel charge preamplifier:

- input impedance adjusted to straw impedance;
- 2 stages:
  - integration amplifier,
  - voltage amplifier (gain factor 4).

Shaper

16 channel shaping amplifier:

- differential input amplifier (gain 1.4);
- signal tail cancellation;
- three integration stages;
- baseline restoration circuit at last integration stage.

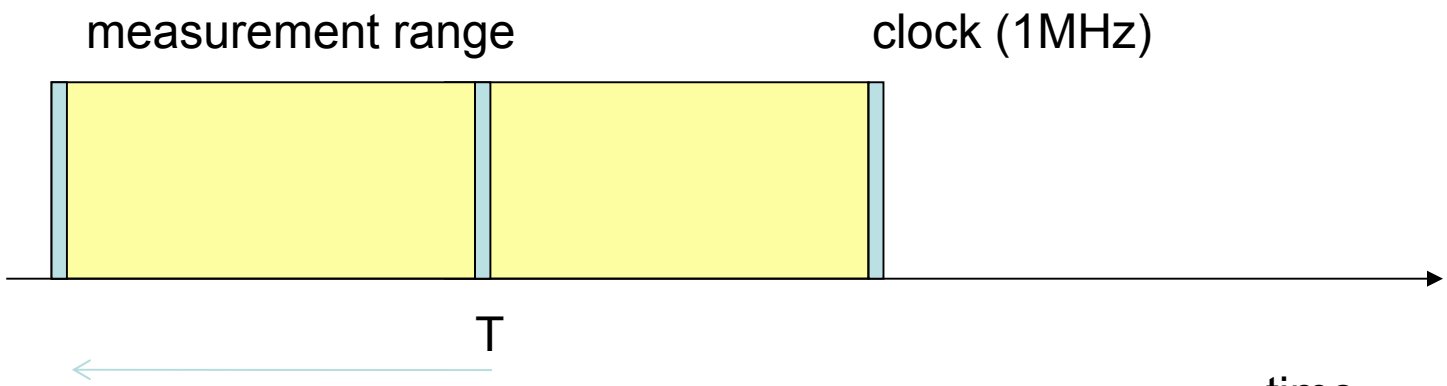
Total gain of each channel of whole system: 2.3 mV/fC
Noise level (peak-to-peak): 2fC

Intermediate signal transmission: concentric cable up to 5 m long

8 prototypes installed and tested at proton beam together with PANDA STT prototype.
Available integration constants τ : 6-, 15-, 33-, 73-, 165 ns.

Search for optimal integration time of the system allowing simultaneous precise measurement of time and energy.

TDC operation mode & data volume



- 1 MHz trigger clock (derived from SODA)
- •: TDC with 0.5 ns binning: time 1 μs range: 11 bits
  - TOT 200 ns : 8 bits
  - channel number(1-64): 6bits
  - time stamp (i.e 1-500); 8 bits
  - TDC id, +trailer/header

  } 5 Bytes/hit

- Data volume: 256 channels in 4TDC @ max 800 kHz hit rate/channel -> ~1.024 GB/s
- Data buffer : 256 channel TDC (i.e for 500 μs epoque): 500-600 kB

step I (done): Trigger and Read-out Board

- TRBv2 board developed by HADES DAQ group
- many boards TRB v2 installed and used in the HADES DAQ

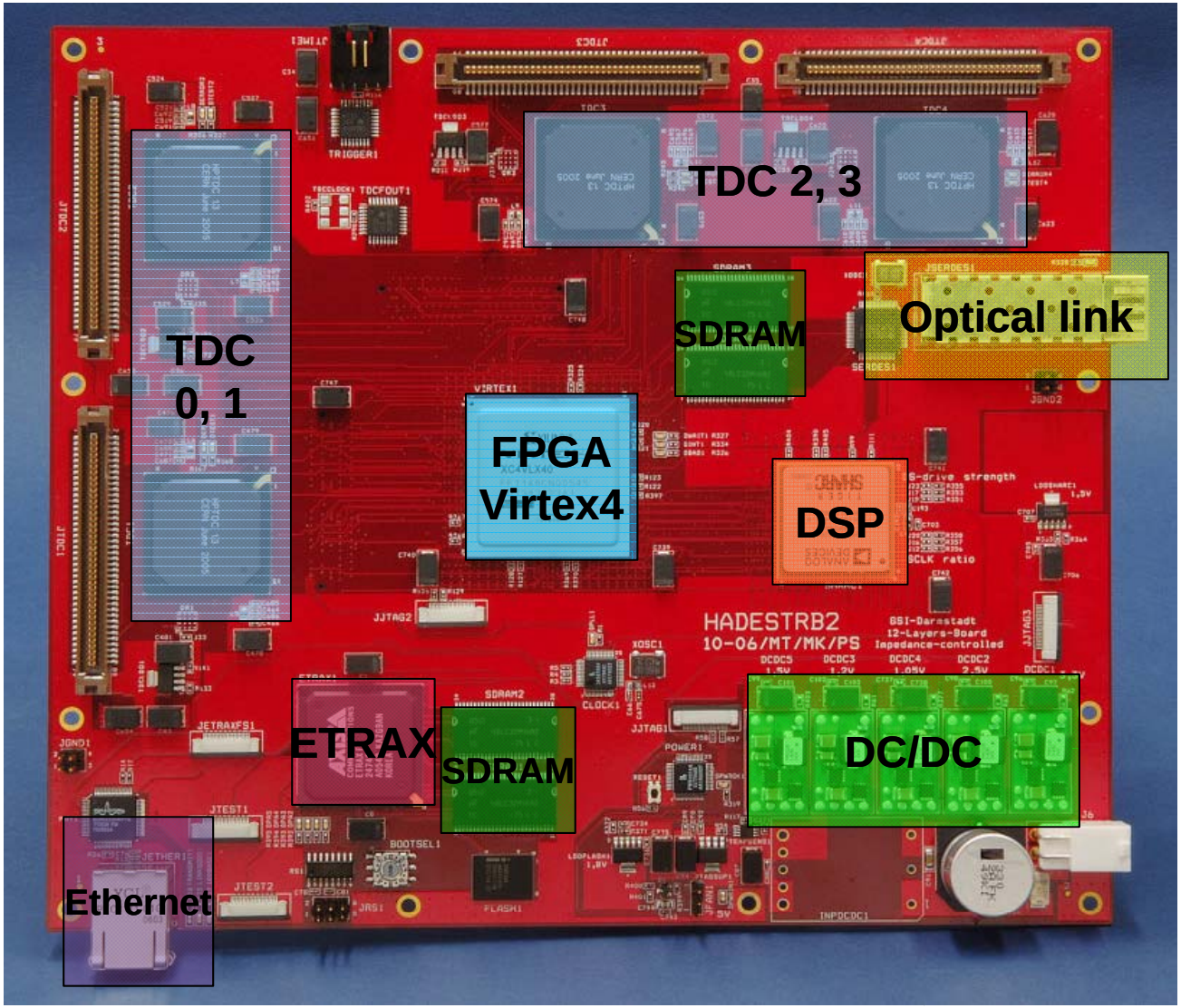
✓128 TDC channels (HPTDC: 25, 100 ,780 ps binning)

✓130 MB/s data throughput achieved via optical links with TRBnet (8/10B via 2 Gbit/s)

✓TRBnet protocol (FPGA): 3 logical channels; data transport, slow control, run control

✓ used for many test runs with FEE for straws

TRBv2



- 128 TDC channels (100ps, 192ps, 780 ps)

- 2.5 Gb/s serial 8/10b link

FPGA: TDC control + TrbNet
- Data flow control
- Slow control
- Run control

more powerfull: TRBv3

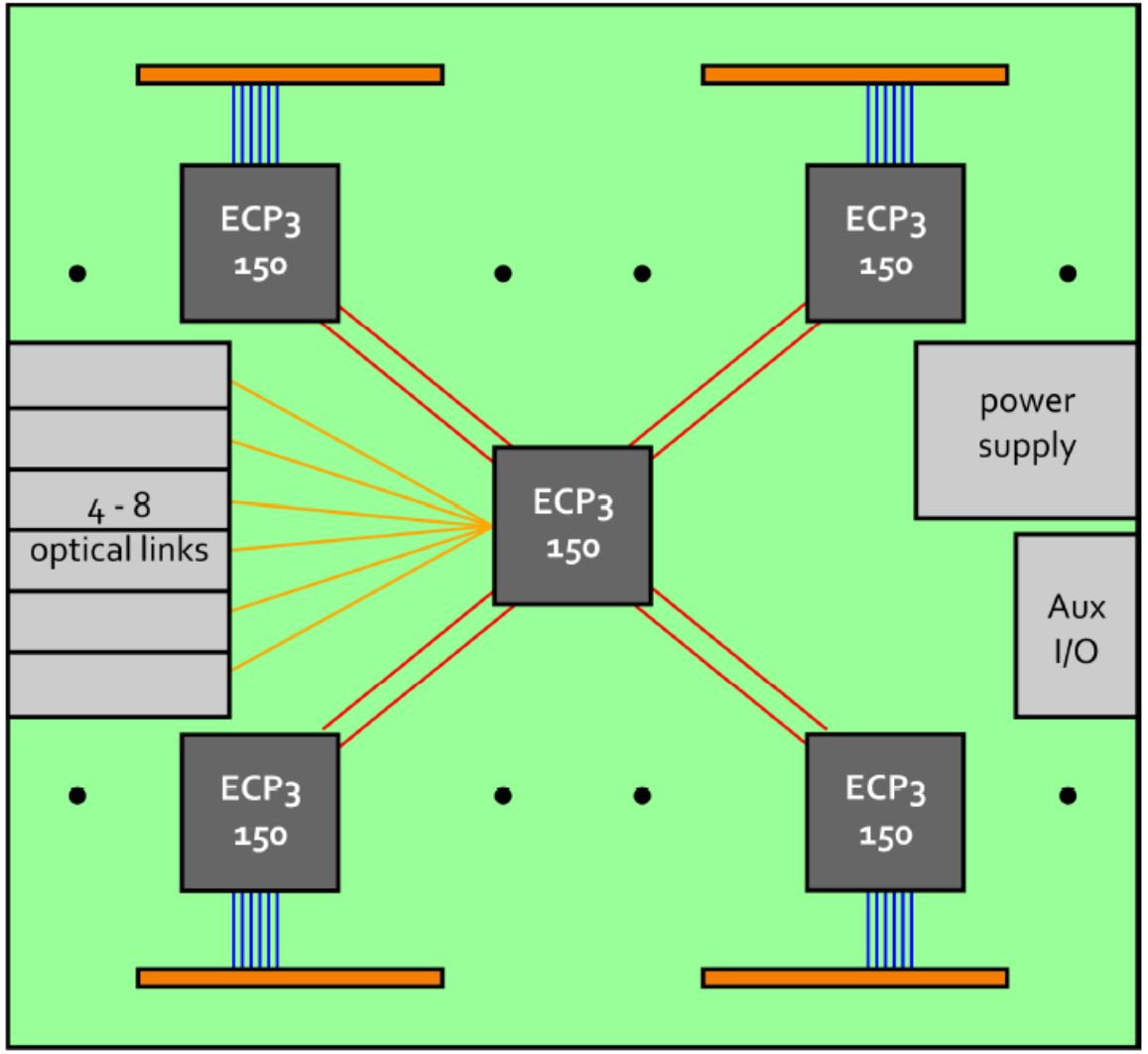
- 4 TDC in FPGA (Lattice ECP3M) up to 256 TDC channels
  4Mbit memory (enough to store one 0.5 ms bunch)

- 1 FPGA for control (Run, Data, Slow-control)

- up to 8 x 3.2Gbit/s (8/10b) serial links for data transmission
(4 links enough to send data from 256 channels with 0.8 MHz hit rate)

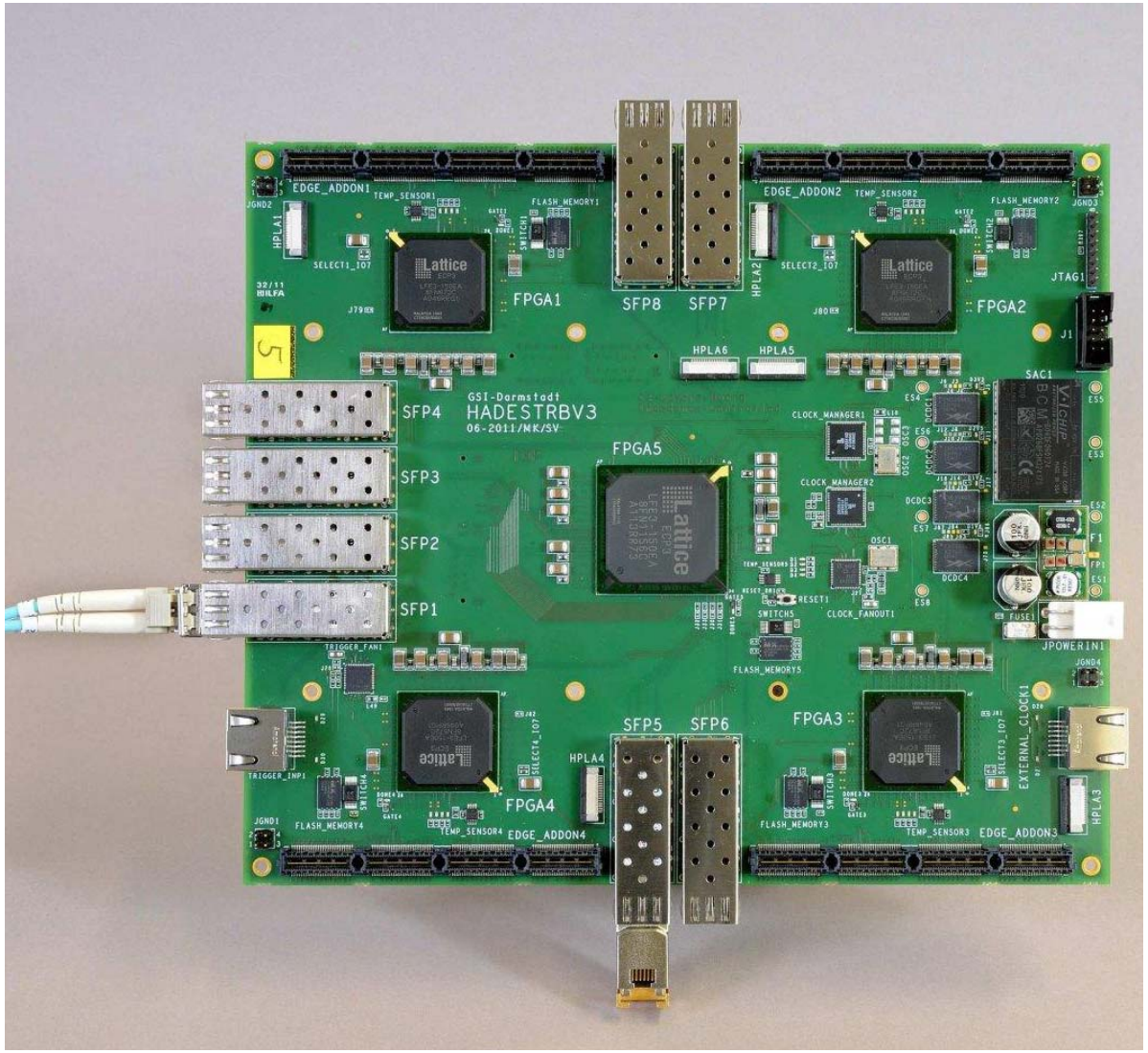
- interface for Add-on connectors : i.e ADC

- ~ 20 W power



Status TRB v3

- Board produced and has all basic functionality (FPGA programming etc.)
- configuration loaded via network (no ETRAX CPU needed), data transfer implemented (G.Korcyl)
- TDC firmware provided (C. Ugur)
- TRBnet implemented (J.Michel/U.Frankfurt)
- Ready for tests with detector !



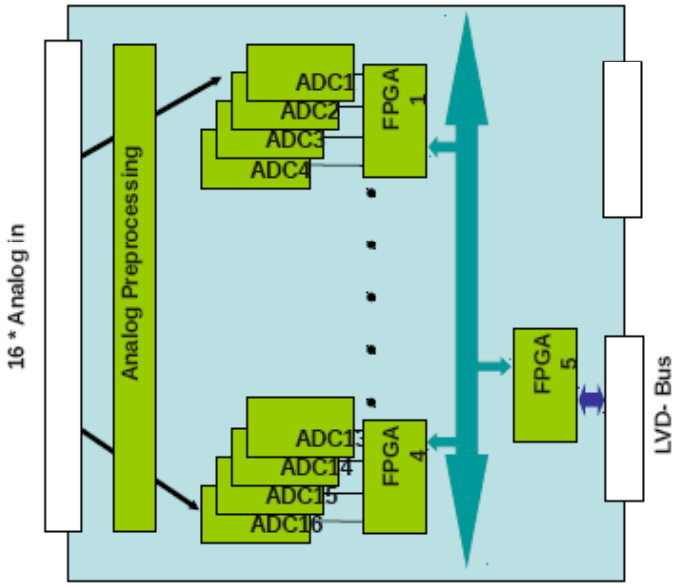
Flash ADC

12 Bit sampling ADCs (developed by ZEL FZJ + Uppsala University)

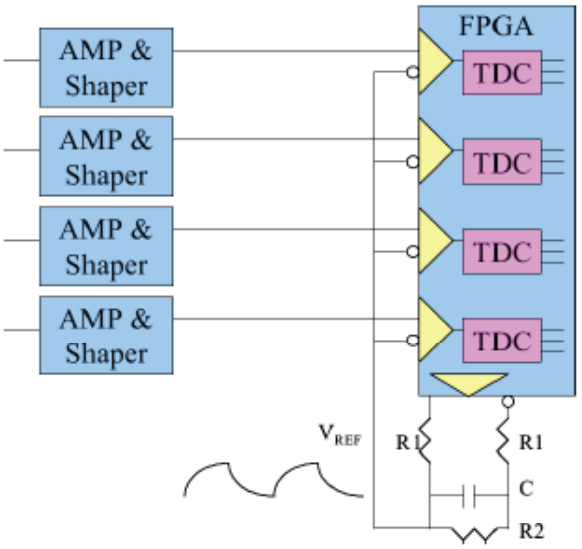
240 MHz sampling frequency

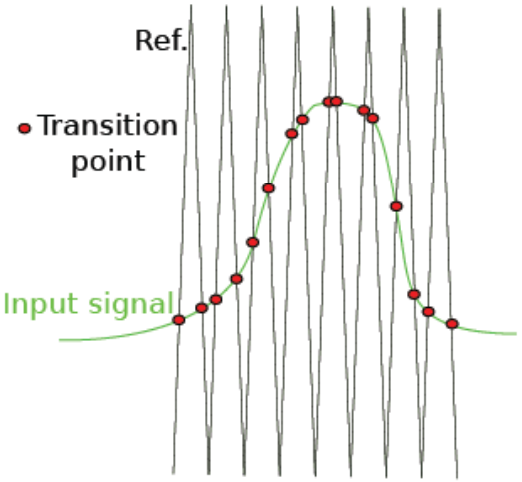
Algorithms implemented in FPGA :

- baseline restoration
- cluster detection
- pileup detection
- constant Fraction Discriminator
- time measurement (better than 1 ns)
- triggering
- ……

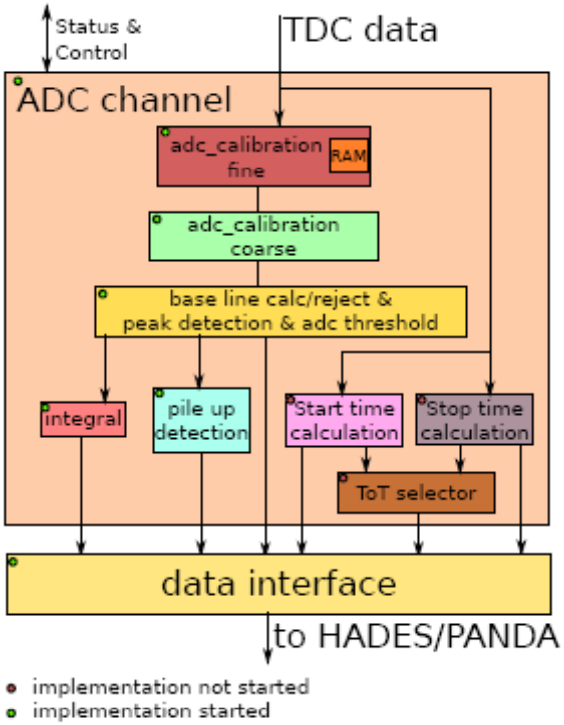


ADC based on time meaurement





VHDL code status:



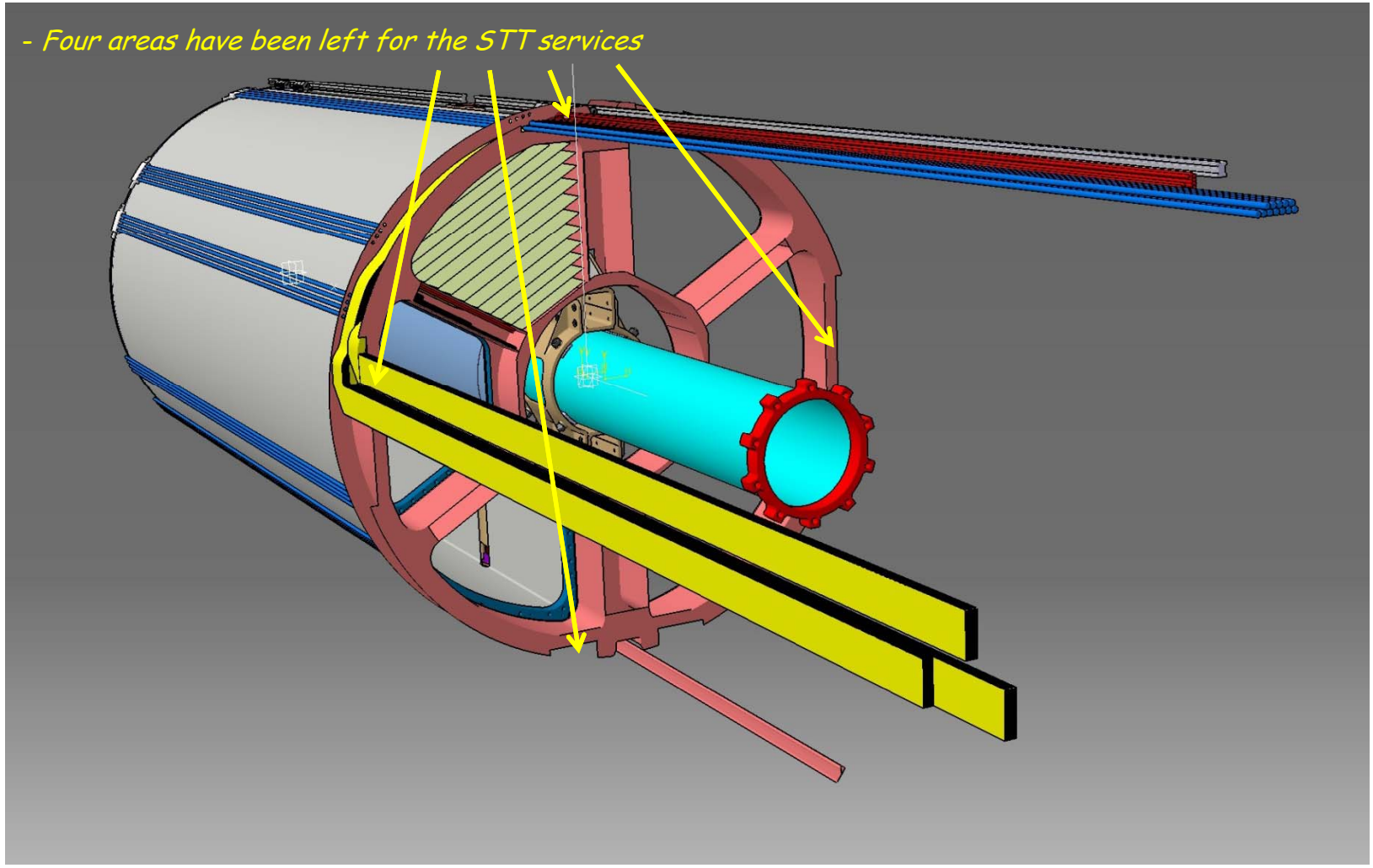
M. Pałka

Tests started : Preliminary results :
8/9 bit ADC seems to be in rich

Next steps

- ASIC: discussion about next iteration – dedicated meeting planned (February in Kraków?)
- new iteration for Juelich Shaper+Booster planned for next year
- Quantify/understand and optimize noise (grounding scheme)
- TRBv3 tests with FEE and detectors (will start in new year in Kraków)
- tests of new ADC concept based on time measurement in progress

Cabling FEE layout



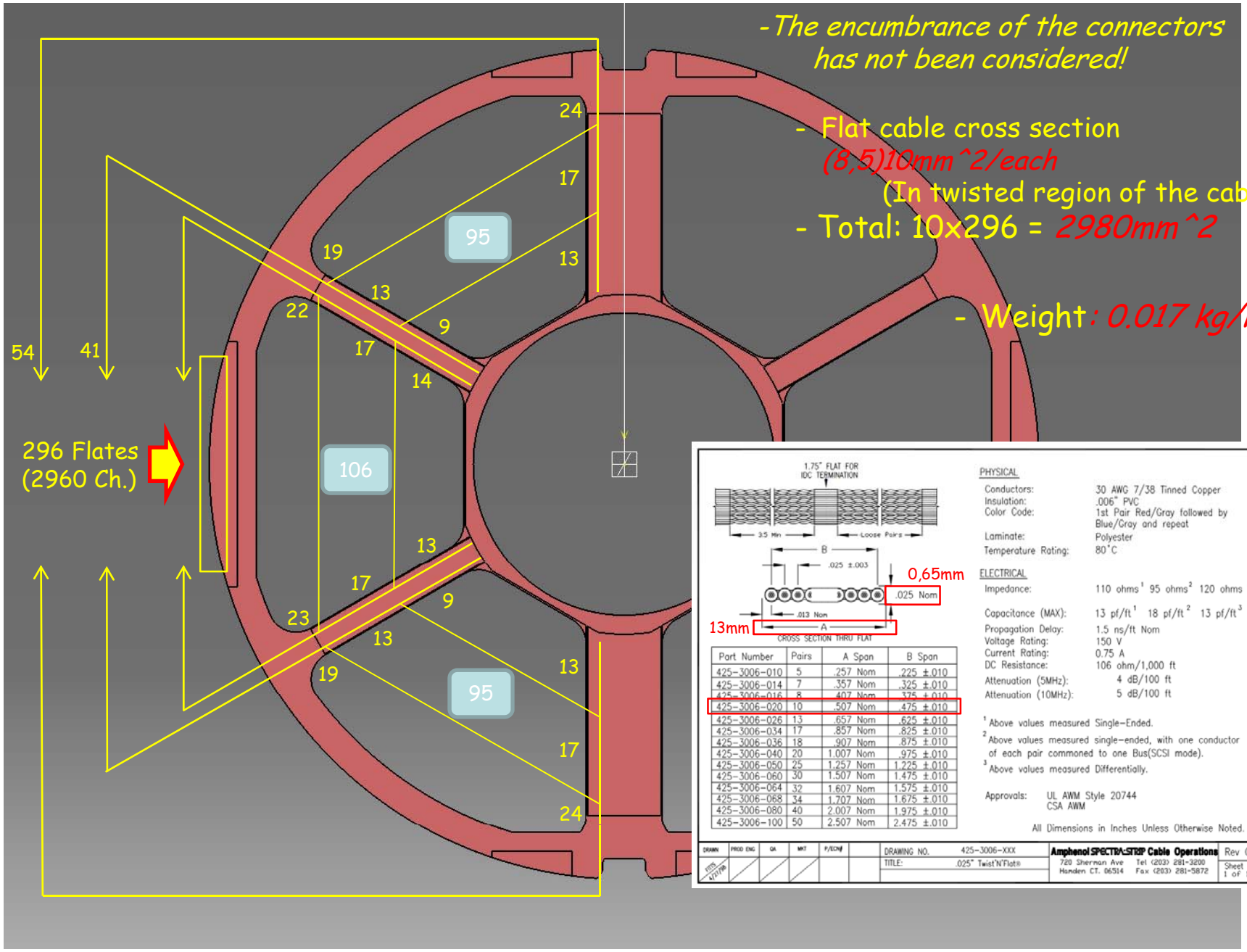
- Signals cables, HV cables, gas pipes etc.. are connected and routed in the 4 available zones.

- PATHWAYS OF FLAT CABLES BUNCHES -

-The encumbrance of the connectors has not been considered!

- Flat cable cross section *(8,5)10mm^2/each*
  (In twisted region of the cable)
- Total: 10x296 = *2980mm^2*

- Weight: *0.017 kg/m*



Part Number	Pairs	A Span	B Span
425-3006-010	5	.257 Nom	.225 ±.010
425-3006-014	7	.357 Nom	.325 ±.010
425-3006-016	8	.407 Nom	.375 ±.010
425-3006-020	10	.507 Nom	.475 ±.010
425-3006-026	13	.657 Nom	.625 ±.010
425-3006-034	17	.857 Nom	.825 ±.010
425-3006-036	18	.907 Nom	.875 ±.010
425-3006-040	20	1.007 Nom	.975 ±.010
425-3006-050	25	1.257 Nom	1.225 ±.010
425-3006-060	30	1.507 Nom	1.475 ±.010
425-3006-064	32	1.607 Nom	1.575 ±.010
425-3006-068	34	1.707 Nom	1.675 ±.010
425-3006-080	40	2.007 Nom	1.975 ±.010
425-3006-100	50	2.507 Nom	2.475 ±.010

PHYSICAL

Conductors:	30 AWG 7/38 Tinned Copper
Insulation:	.006" PVC
Color Code:	1st Pair Red/Gray followed by Blue/Gray and repeat
Laminate:	Polyester
Temperature Rating:	80°C

ELECTRICAL

Impedance:	110 ohms[1] 95 ohms[2] 120 ohms[3]
Capacitance (MAX):	13 pf/ft[1] 18 pf/ft[2] 13 pf/ft[3]
Propagation Delay:	1.5 ns/ft Nom
Voltage Rating:	150 V
Current Rating:	0.75 A
DC Resistance:	106 ohm/1,000 ft
Attenuation (5MHz):	4 dB/100 ft
Attenuation (10MHz):	5 dB/100 ft

[1] Above values measured Single-Ended.
[2] Above values measured single-ended, with one conductor of each pair commoned to one Bus(SCSI mode).
[3] Above values measured Differentially.

Approvals: UL AWM Style 20744
CSA AWM

All Dimensions in Inches Unless Otherwise Noted.

DRAWN | PROD ENG | QA | MKT | P/ENG

DRAWING NO. 425-3006-XXX
TITLE: .025" Twist'N'Flat®

Amphenol SPECTRA-STRIP Cable Operations
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Hamden CT. 06514 Fax (203) 281-5872

Rev C
Sheet 1 of 1