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NEXT GENERATION NETWORKING – GBE ON TRBV3 AND COMPUTE NODE

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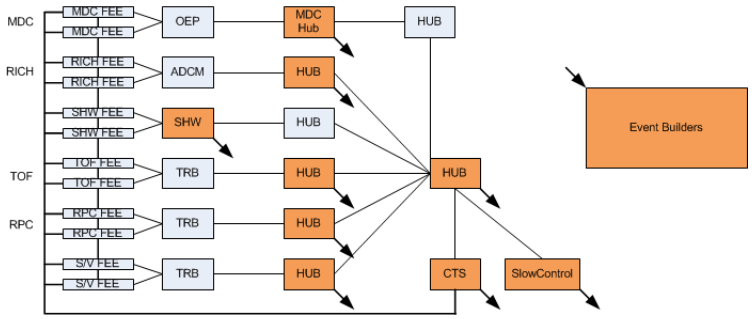
Jagiellonian University – PANDA Collaboration Meeting 12/2012

Plan

1. High level networking concept
    1. Previous implementation
    2. Current development
2. Implementations
    1. TRBv3
    2. Compute Node
3. Other ongoing projects
4. Summary

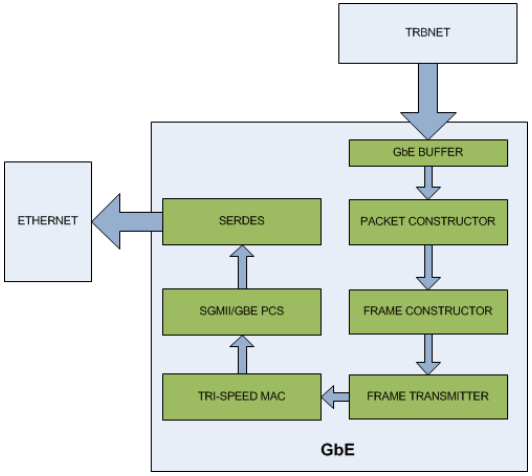
High level networking concept

- Previous implementation
  - Requirements:
    - Transport data out from electronics to Event Builders
    - Compose UDP packets and transmit them over GbE
    - Implement for main data collectors in HADES (HUB, MDC, Shower addons)



High level networking concept

- Previous implementation
  - Results
    - Few successfull beamtimes with HADES
    - Unnoticeable packet loss
    - UDP fragmentation into Eth Frames
    - Performance:
      - 50MBps – buffered mode
      - 118MBps – no-buffered mode
    - Good starting point for further development

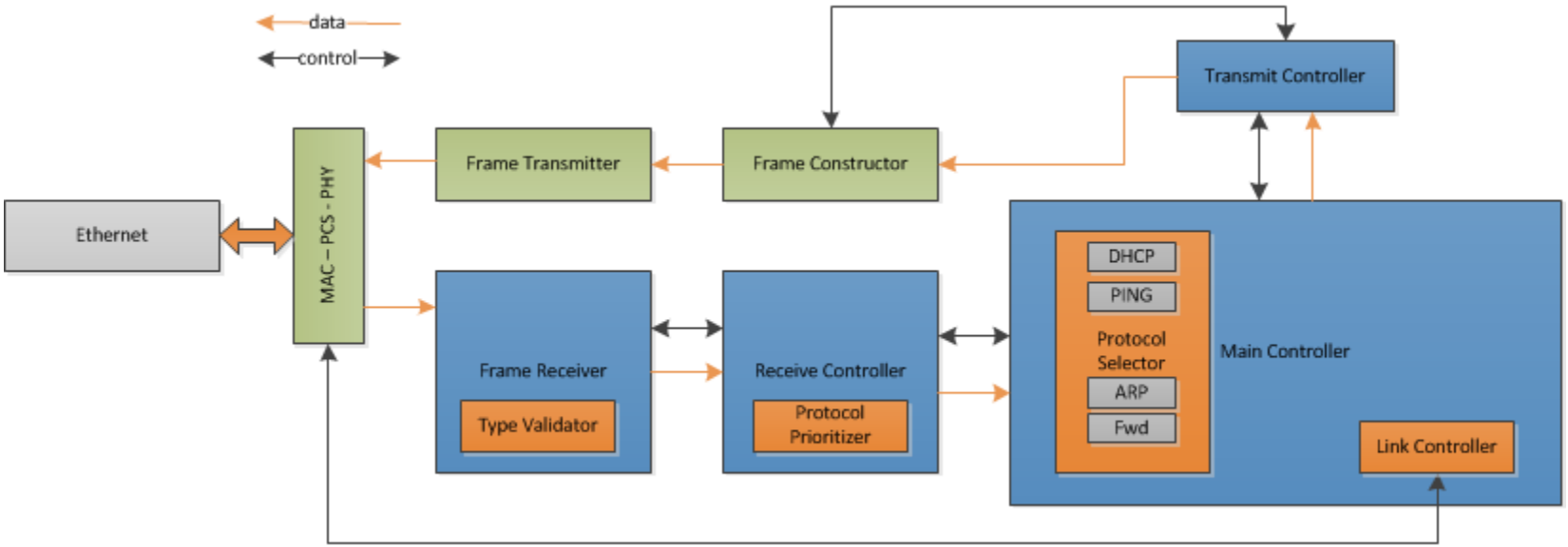


High level networking concept

- Current development
  - Requirements
    - Full-duplex transmission
      - Transmission and reception of packets
    - Variety of protocols
      - Different experiments require different data handling
      - Basic networking protocols
    - Reliable transmission
    - Maximum speed available
    - Different platforms
      - Different experiments use different electronics
      - Interface with different internal protocols and data structures

High level networking concept

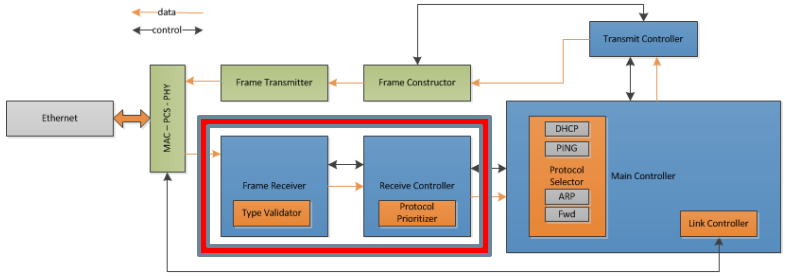
- Current development
  - Solution



- Platform independent framework for Ethernet networks on FPGA devices

High level networking concept

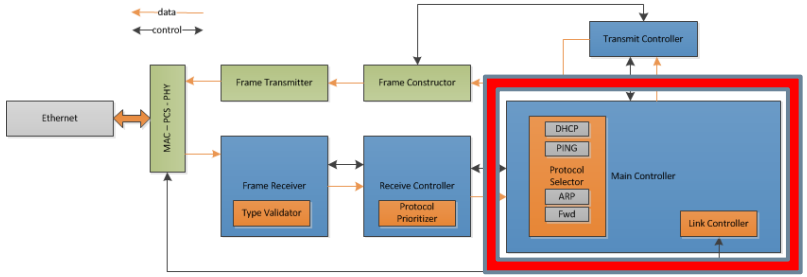
- Current development
  - Solution



    - Frame Receiver and Receive Controller
      - Full speed Ethernet frames reception
        - Real preformance dependent on specific protocol implementation
      - Frames filtering based on addresses and protocol types
      - Protocol queuing based on priority settings
      - VLAN support

High level networking concept

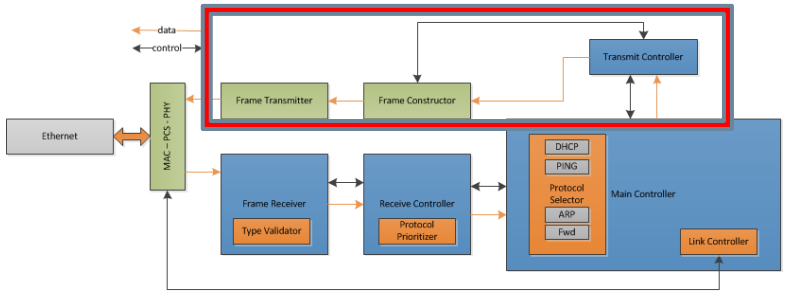
- Current development
  - Solution



    - Main Controller
      - Controls the link
      - Controls the flow of data in both directions
      - Contains Protocol Selector
        - A place to put specific protocols implementations
        - Transfers the received data to the appropriate protocol
        - Selects the protocols that has data ready to be transmitted
        - Simple to implement and add a new protocol
          - Intuitive interface
          - No deep interference with the framework needed
          - Proper design and buffering needed to keep performance at max

High level networking concept

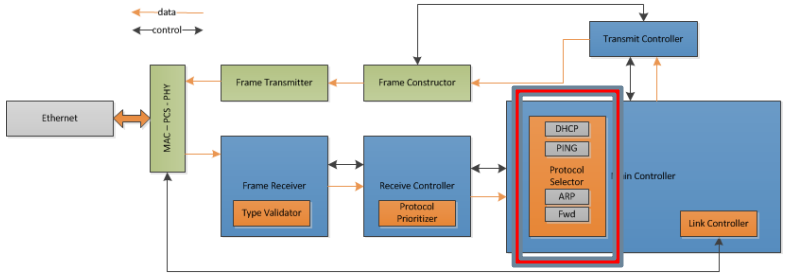
- Current development
  - Solution



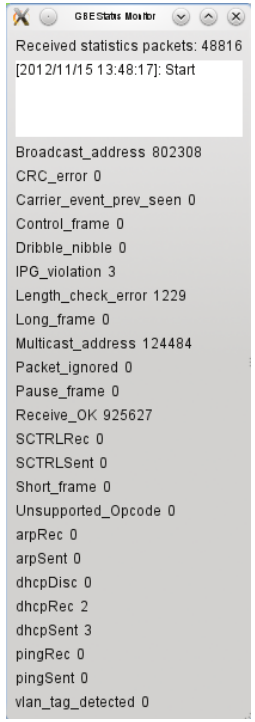
    - Transmit Controller and Frame Constructor
      - Full speed data transmission
        - Real preformance dependent on specific protocol implementation
      - Creates appropriate headers based on protocol which is selected to transmit data
      - Allows the injection of data from outside of Main Controller
      - Calculation of checksums etc…

High level networking concept

- Current development
  - Solution

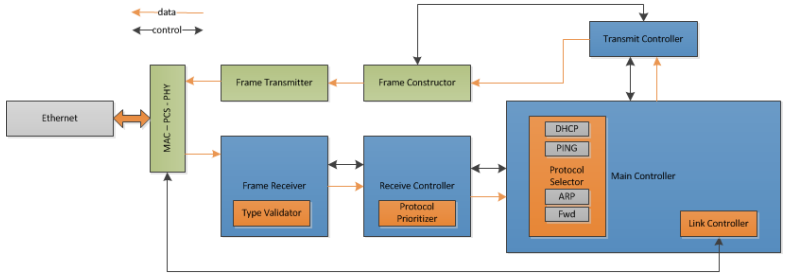


    - Protocols implementations:
      - Basic – needed for duplex communication
        - ARP (Address Resolution Protocol)
          - Network visibility
        - DHCP (Dynamic Host Configuration Protocol)
          - Network addresses acquisition
        - PING – ICMP (Internet Control Message Protocol)
          - Checking if the board is alive
      - Additional
        - Statistics
          - UDP packets with statistics gathered from every protocol implementation



High level networking concept

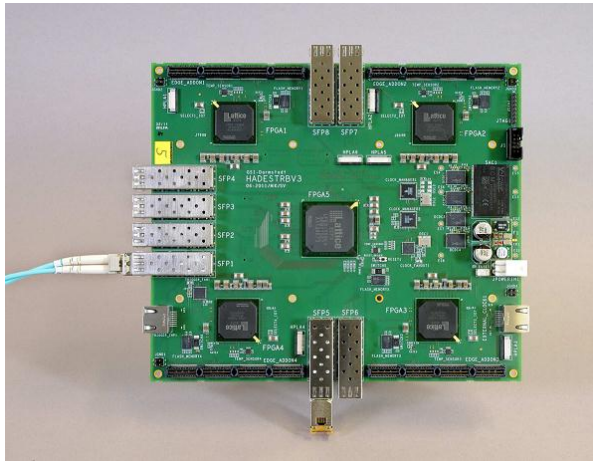
- Current development
  - Solution



    - Features summary:
      - High-performance transmission and reception of Ethernet Frames
      - Filtering of incoming data
      - Framework ready – solution easy to adjust for specific needs by replacing protocols implementations only
      - Basic protocols implemented – solution working out of the box
      - Compact – basic solution uses
        - 11% of slices on V4FX60
        - 5% of RAM on V4FX60
      - Runs so far on:
        - Lattice SC2, ECP2M, ECP3M, Xilinx Virtex4 FX, Virtex5 TX/FX
        - Over optical fibers, copper cables
        - Directly or via additional chips (Marvell)

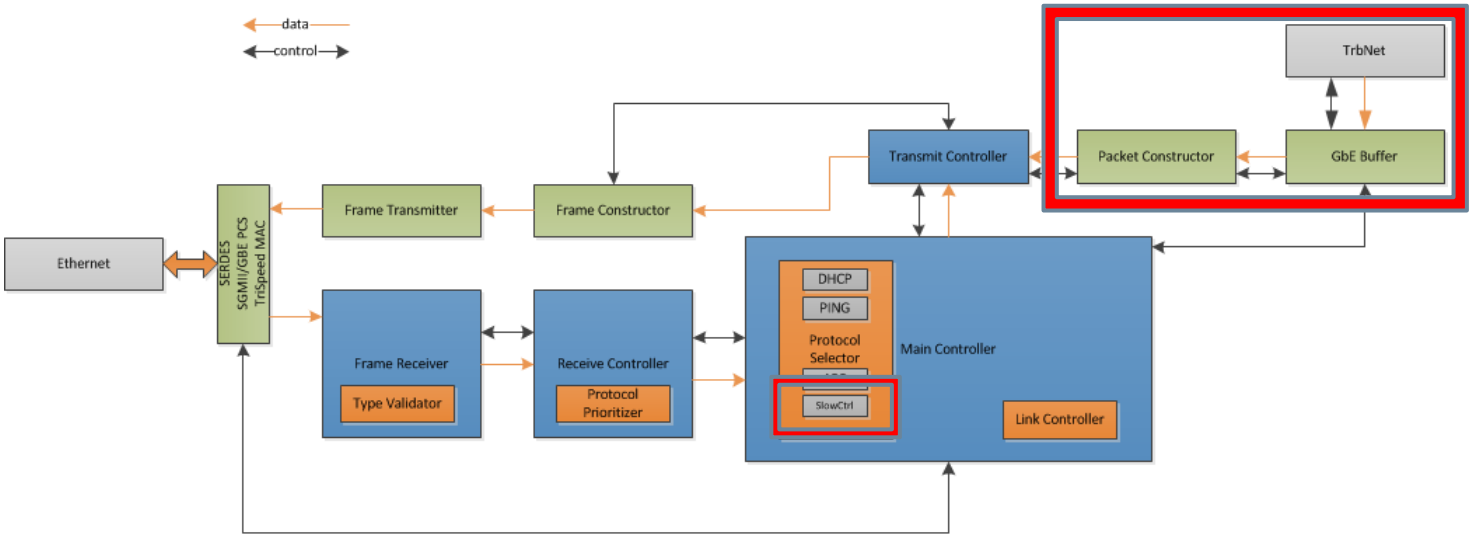
Implementations – TRBv3

- Universal measuring platform
- Part of a complex system or standalone
- 5x FPGA and no ETRAX
  - Possible communication
    - Gigabit Ethernet
    - TrbNet
  - Slow Control over Ethernet
  - Readout over Ethernet



Implementations – TRBv3

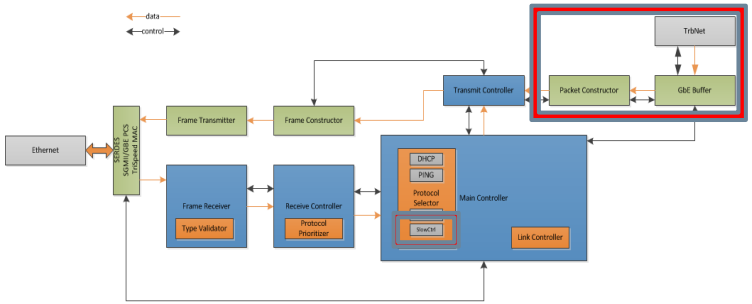
- Networking



  - Injection on readout data packets
  - TrbNet-over-GbE for Slow Control client
    - Upgrade of the Slow Control server – work of Ludwig Maier

Implementations – TRBv3

- Networking



  - Readout data can be sent out

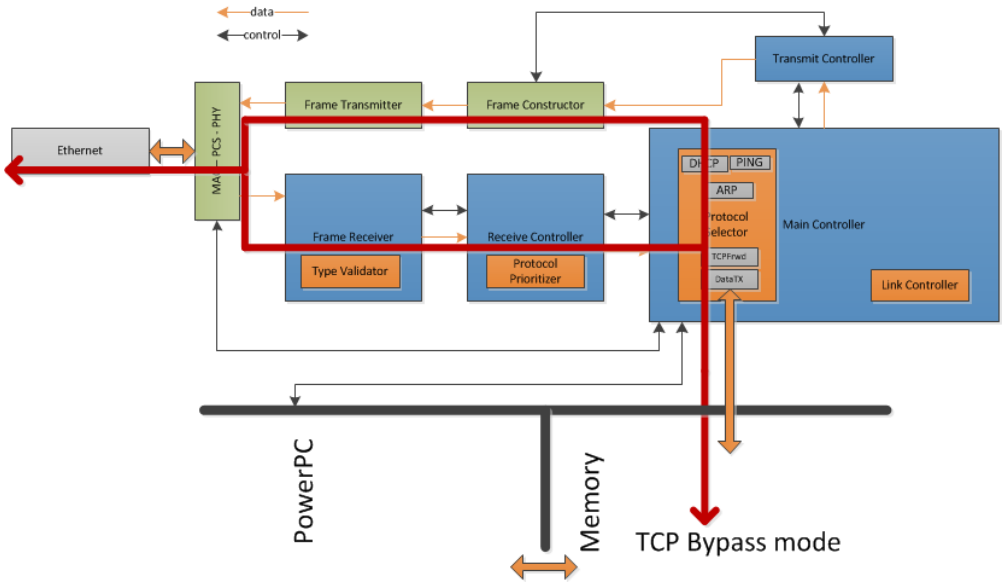
    while other protocols work simultaneously
  - Work in the same way as the „old” GbE together with the same features
  - TrbNet-over-GbE allows to control a single TRBv3 in the same way and with the same scripts as the „full” system

Implementations - CN

- Data collector and compute power for PANDA
- ATCA based system
- CNv2 – single unit „blade” with 5x V4FX60
- CNv3 – „blade” as motherboard for 4x mezzanine cards with V5FX70
- Networking – CNv2
  - 2x Optical Links per FPGA
  - 1x RJ45 per FPGA
  - DDR memory
- Networking – CNv3 (mezzanine card)
  - 2/4x Optical Links
  - 1x RJ45
  - DDR Memory

Implementations - CN

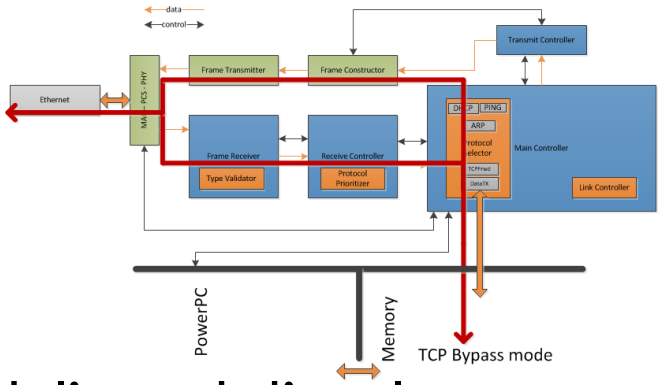
- Networking



- Transmission over UDP of data collected in memory
- Delivery in and out of Ethernet frames for linux on PPC
- Slow control over Ethernet

Implementations - CN

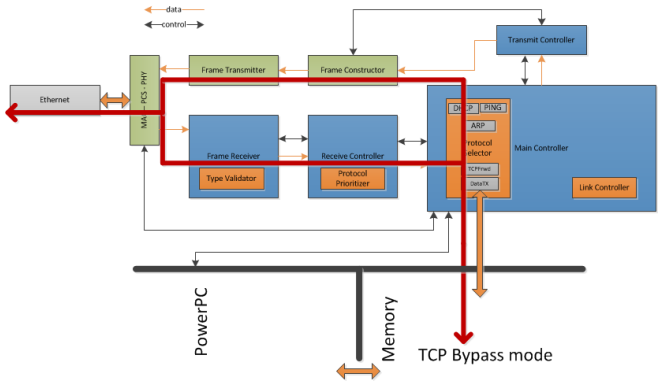
- Networking



  - Algorithms running on PPC produce data stored in memory
  - Slow Control runs via linux – packets delivered directly to memory
  - Differnet media available
    - SFP
    - RJ45 – Marvell Chip
  - Operation and addressing configurable through shared registers

Implementations - CN

- Networking



  - Problems and tasks:
    - Performance tests needed
      - Where is the bottleneck?
      - Optimize protocol implementations to reduce deadtime
    - Permil of dropped frames on PPC
      - Bit errors?
      - Dependent on the transport medium – timing issues?

Other ongoing projects

- Simplified TCP implementation
  - Data storage and buffering in DDR memories
  - Flow control logic
  - Multiple transactions
  - Progress:
    - Basic Telnet message exchange
- GbE Framework as traffic generator
  - Configurable generation of different types of packets
  - Useful in testing network infrastructures
  - As verification for modeling results
  - Progress:
    - Basic UDP flooding with timestamps and time measurement
- Used in readout prototypes for:
  - PANDA EMC
  - BELLE 2
  - FAZIA
  - CBM…

Summary

- GbE Framework as versatile solution for networking on FPGA based electronics
- Many features developed and tested
- Some parts verified during beamtimes – others still to evaluate
- Many bugs to fix…
- Many applications to discover…