PANDA FEE Electronics

Sezione di Torino

MVD readout status report

G. Mazza
on behalf of the MVD group

PANDA MVD

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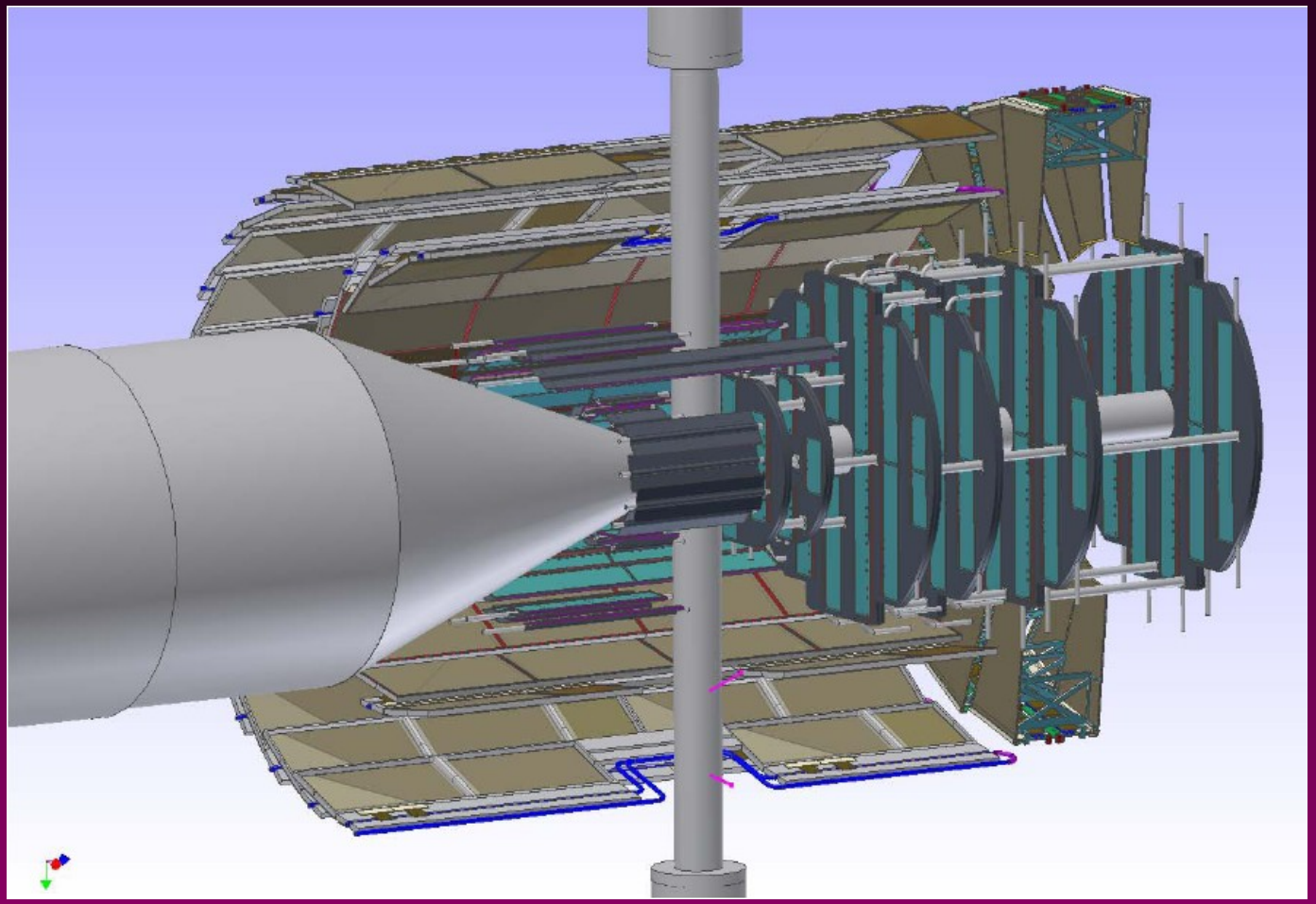

- Barrel :

Layer 1 : radius 28 mm, SPDs

Layer 2 : radius 53 mm, SPDs

Layer 3 : radius 92 mm, SSDs

Layer 4 : radius 120 mm, SSDs

- Forward :

Disks 1-2 : radius 37.5 mm, SPDs

Disks 3-4 : radius 75 mm, SPDs

Disks 5-6 : radius 130 mm, SPDs + SSDs

Pixel Detector

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Pixel size	*100 × 100 μm²*
Chip active area	*11.4 × 11.6 mm² (116 rows, 110 cols)*
dE/dx measurement	*ToT, 12 bits dynamic range*
Max input charge	*50 fC*
Noise floor	*<32 aC (200 e⁻)*
Input clock frequency	*155.52 MHz*
Time resolution	*6.43 ns (1.86 ns r.m.s.)* *12.86 ns (3.71 ns r.m.s.)*
Power consumption	*< 800 mW/cm²*
Max event rate	*6.1 · 10⁶*
Total ionizing dose	*< 100 kGy*

Module readout

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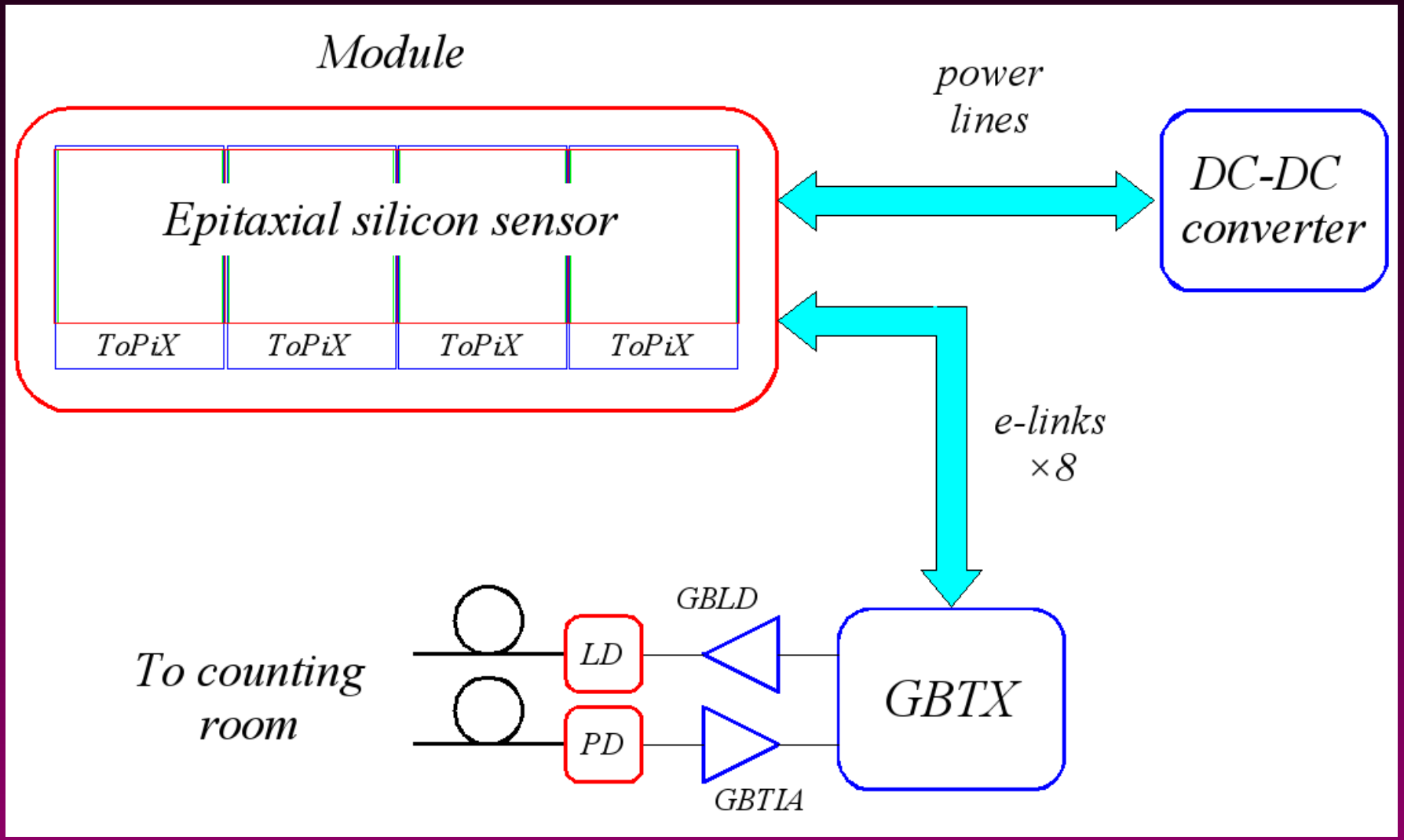

ToPiX v3

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- Layout submitted on February 7th – received May 16th 2011
- 4.5x4 mm^2 die area
- CMOS 0.13 µm DM technology
- Triple redundancy-based SEU protection
- End of column logic
- 160 Mb/s SLVS serial output
- Pads for bump bonding

ToPiX v3 layout

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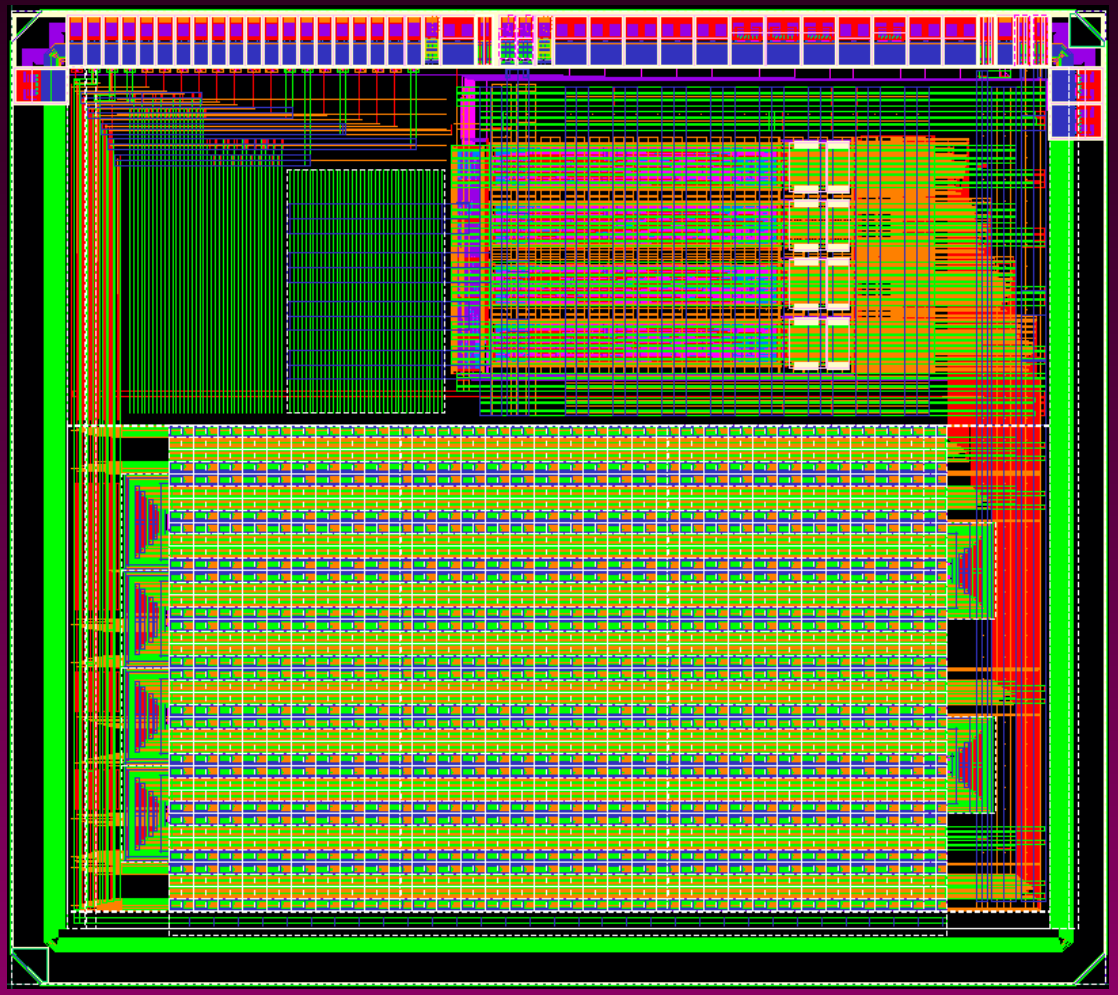

- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

ToPiX test results

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- At 160MHz can only read and program first ~32 pixels of each column
- At 50MHz (with pre-emphasis disabled) full operation
- S-curve working well (programmable internal test pulse)
- Baseline measurements ok
- On-pixel DACs characterised and correction applied
- Transfer function measurements in good agreement with simulations
- Acquisition system is working (4 boards)
- TID (@X ray-CERN) and SEU (@SIRAD-LNL) tests done

ToPiX + sensor

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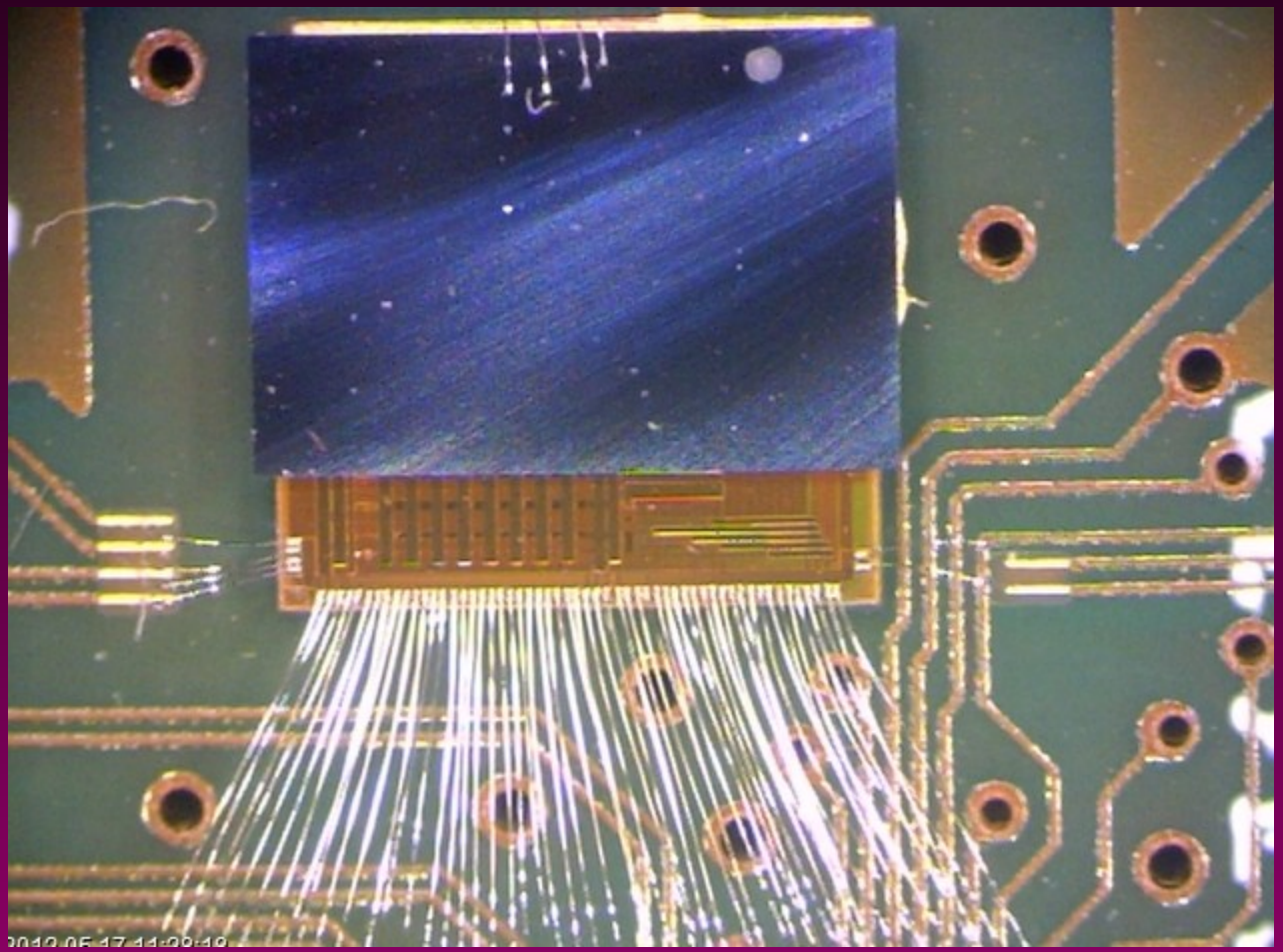

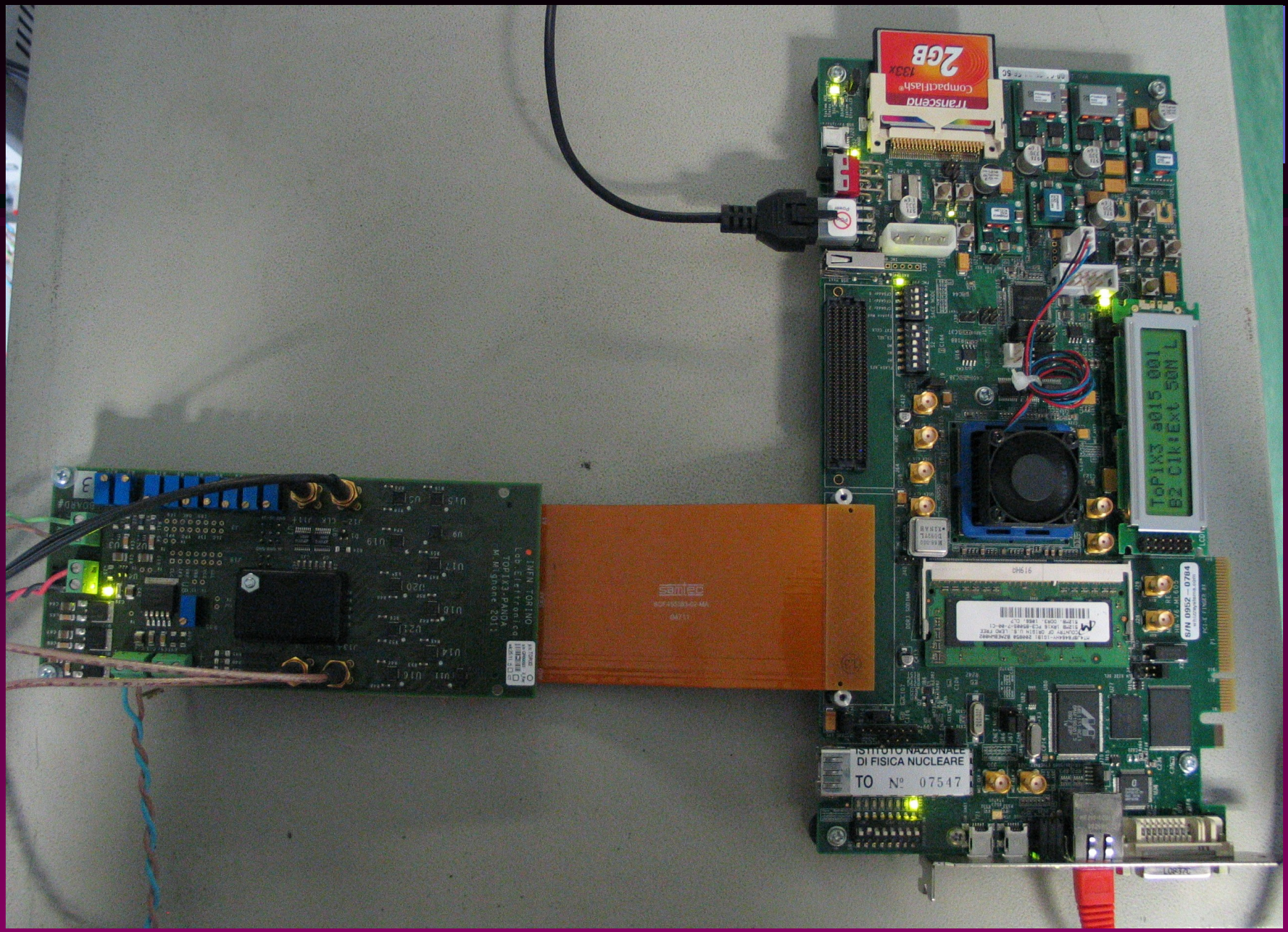
2GB
133x
Transcend
CompactFlash
INFN TORINO
Lab. Elettronico
TOF1X3-PANDA
M.Mignone 2011
ISTITUTO NAZIONALE
DI FISICA NUCLEARE
TO Nº 07547

Baseline correction

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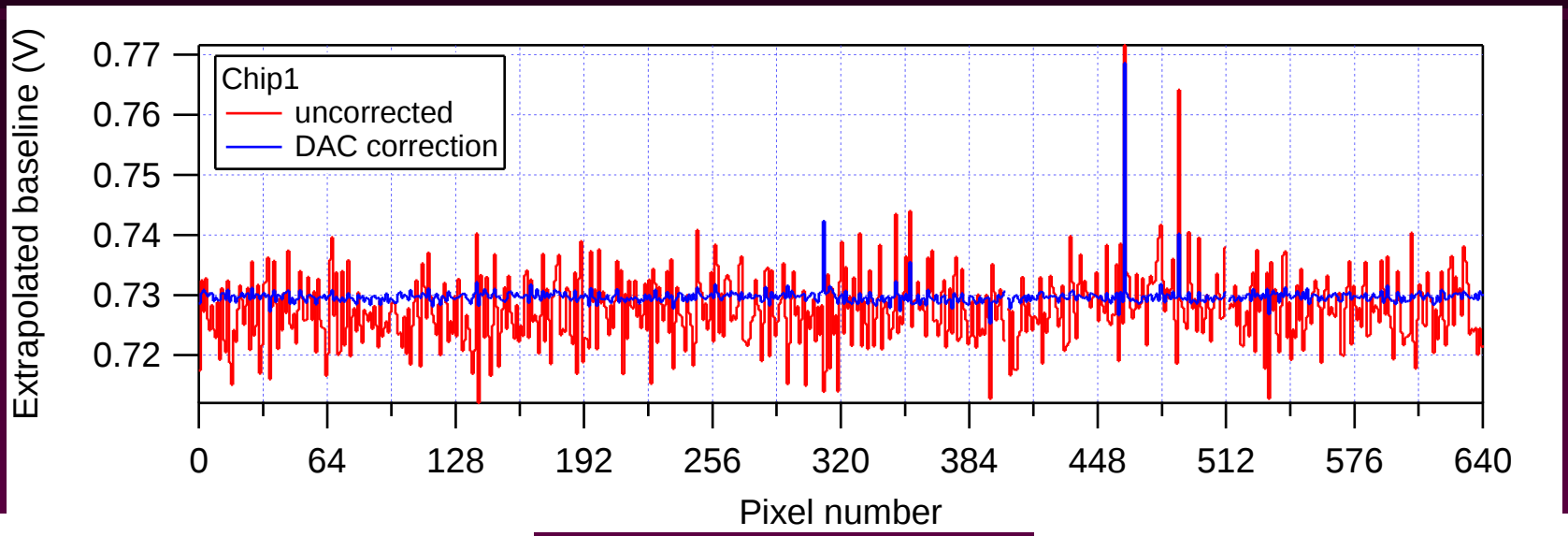
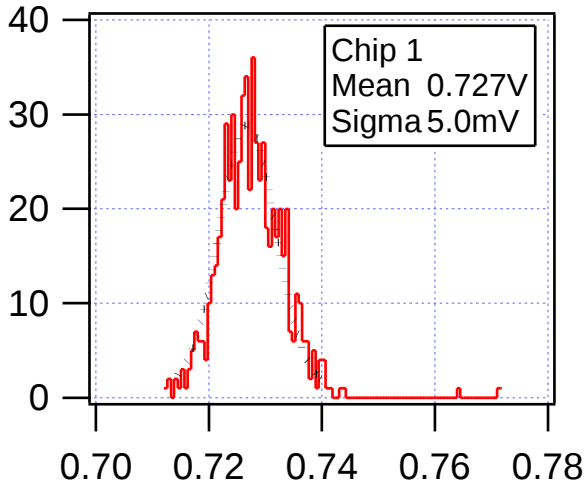
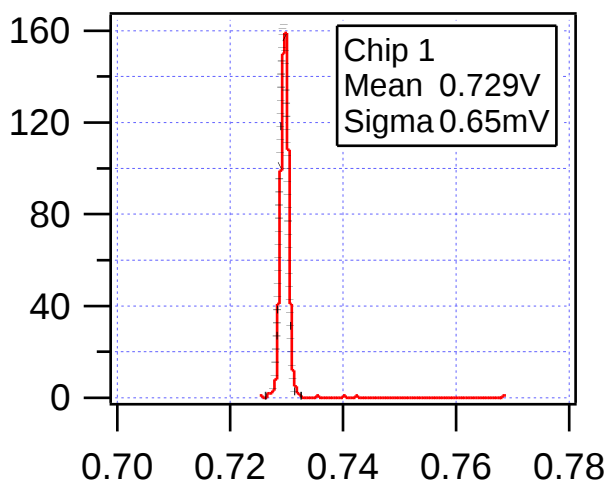
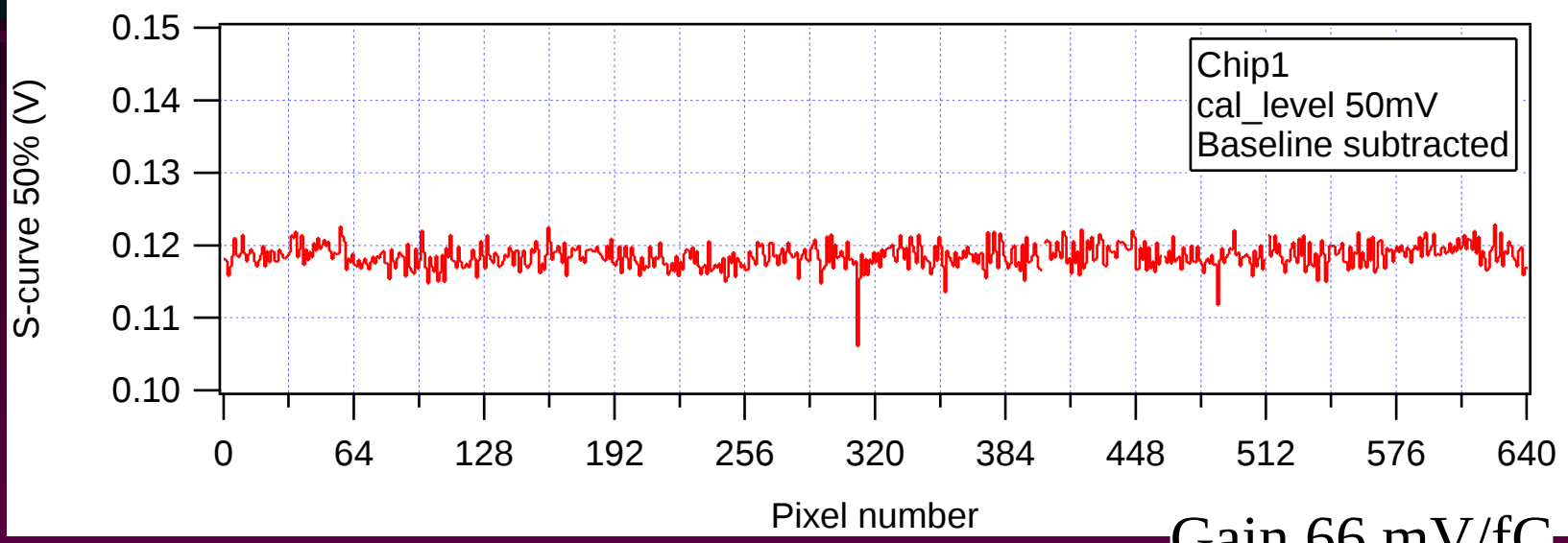




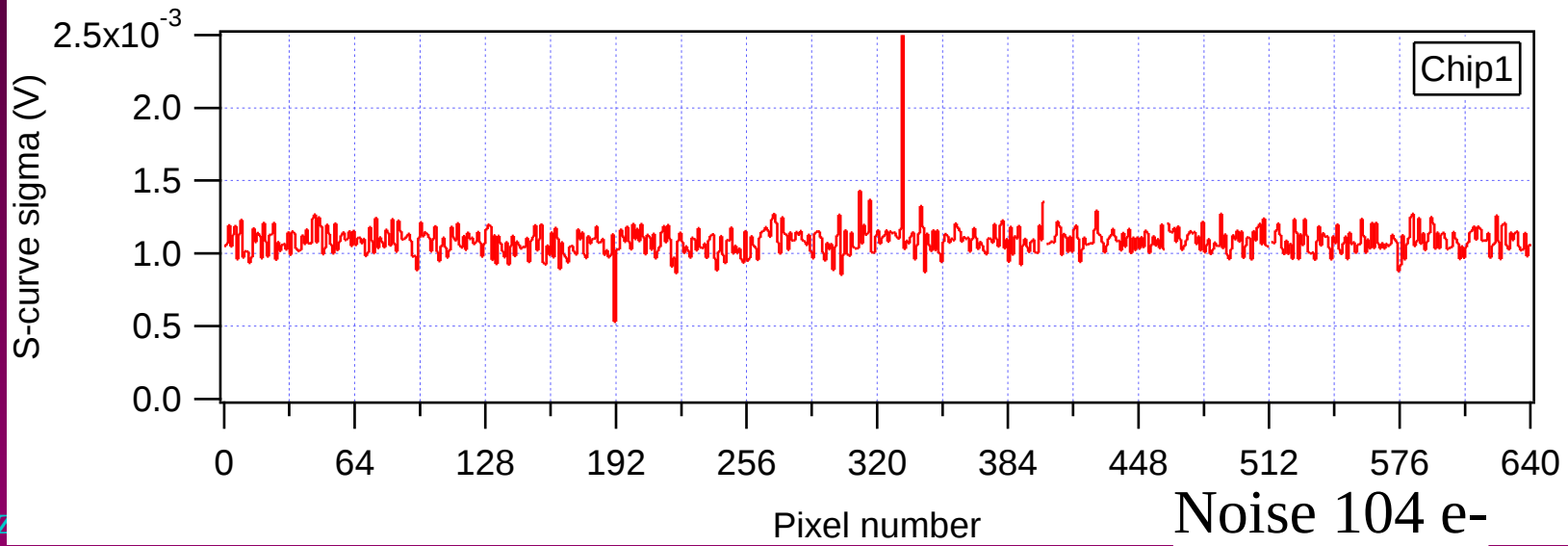
DAC correction



Gain & Noise



Gain 66 mV/fC



Noise 104 e-

ToT @ 5 nA

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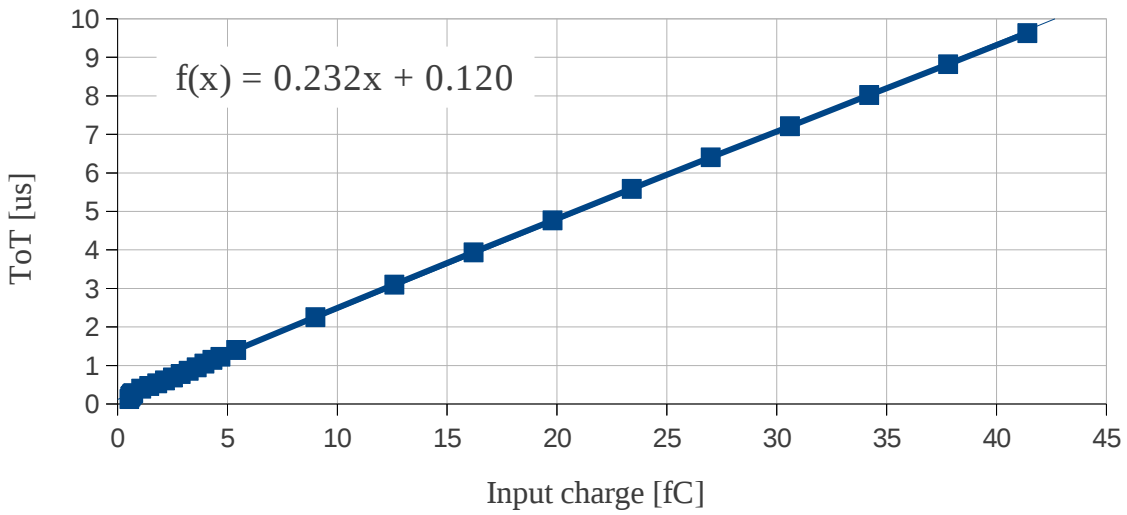

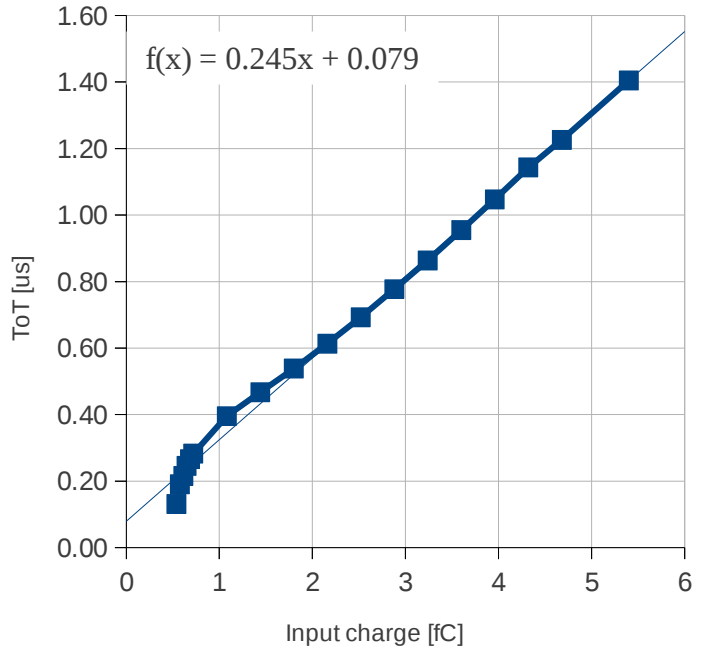

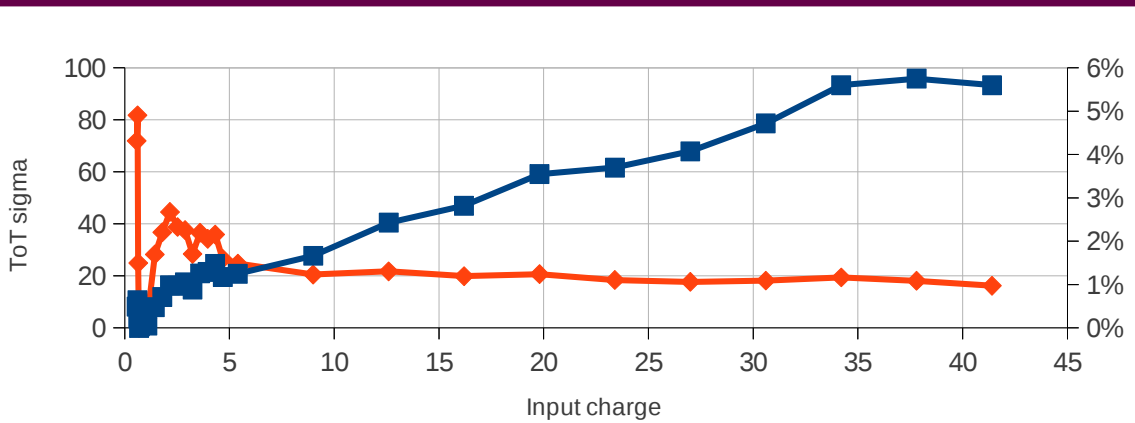

$I_{FB} = 5\ nA$

Simulated gain : 202 ns/fC

Open issues

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- Clock frequency
- Power consumption
- Radiation tolerance
  - TID effects
  - SEU effects

Clock frequency problem

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- At 160 MHz only the columns with 32 double cells work correctly
- Response improves when the frequency is decreased
- "Easy" corrections :
  - *Prototype full column has 30% longer bus and 10% more cells than the final chip*
  - *Triple redundancy latches have been connected without buffers*
  - *Buffers can serve two pixels*
  - *Change in le readout timing – see next slide*
- Bus estimated capacitance : 47.35 fF/cell (55% due to the cell, 45% due to interconnection capacitance)
- Total bus capacitance per line : 6.88 pF (now), 2.98 pF (est.)

Timing issue

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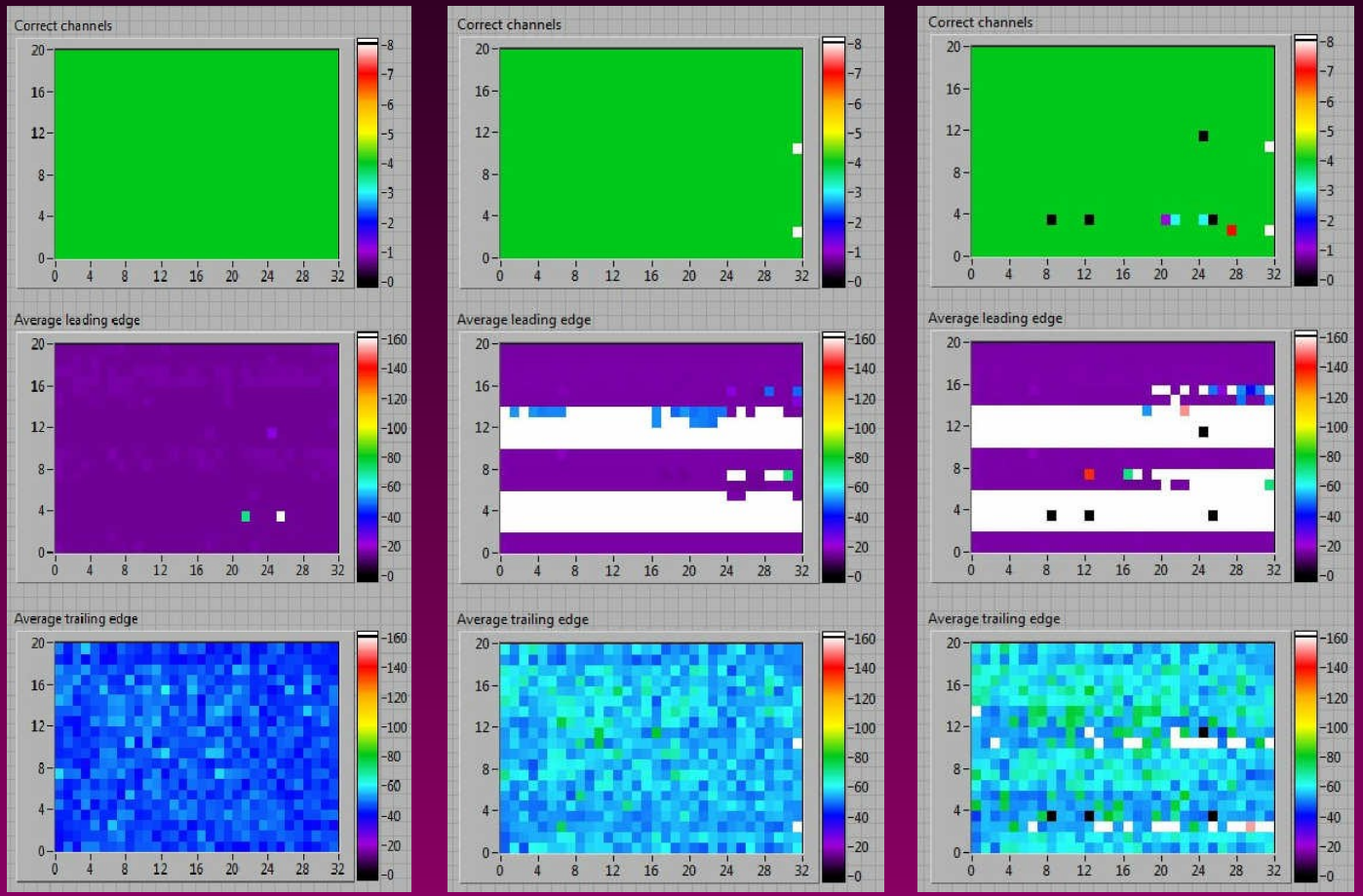
50 MHz *65 MHz* *70 MHz*



- Trailing edge still good @ 65 MHz
- Read leading edge cmd asserted at the same time as read cmd.
- Read trailing edge cmd asserted when read cmd is already high
- *Clock cycle to be inserted between read cmd and read leading edge cmd.*

New line driver

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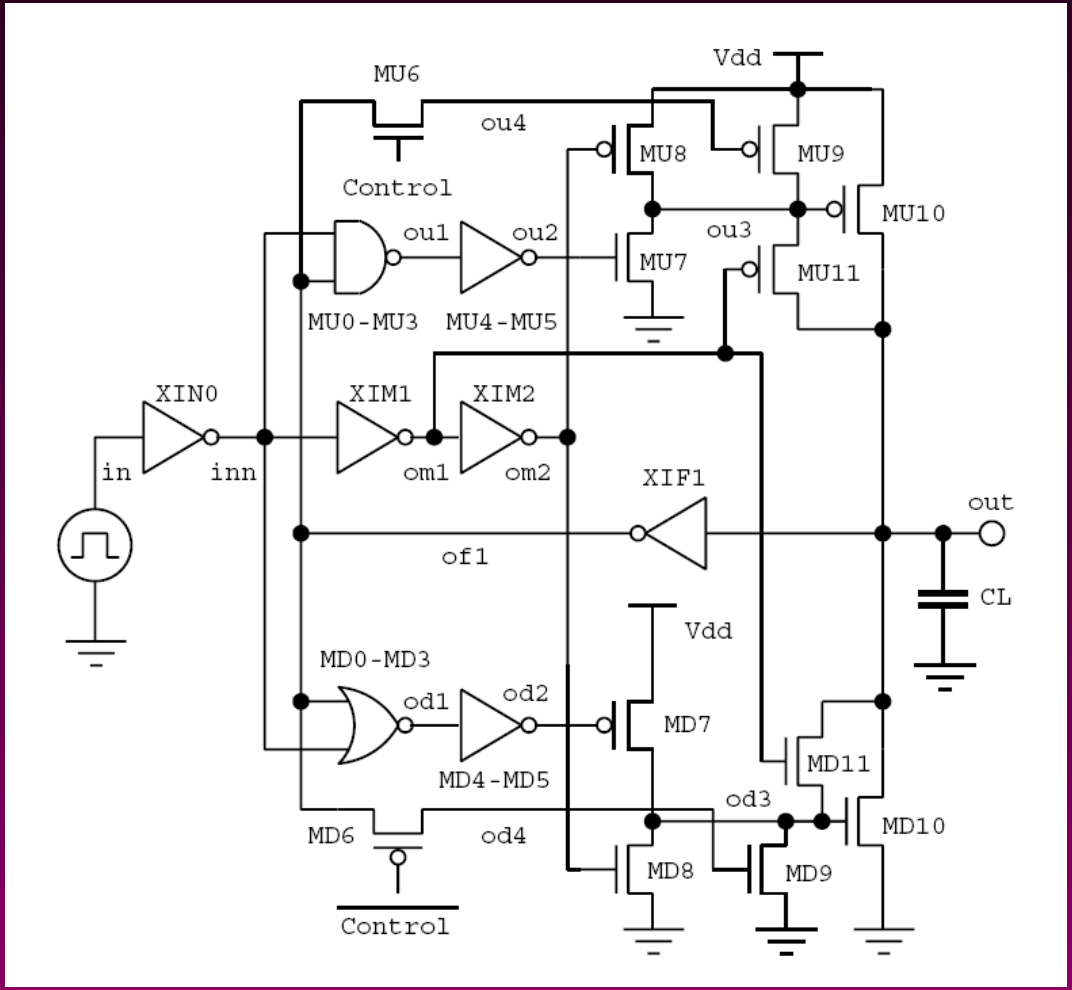

Provides both reduced voltage swing and pre-emphasis or full voltage swing

J.C.Garcia, J.A.Montiel, S.Nooshabadi
Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects
ISCAS 2007

ToPiX v3 supply

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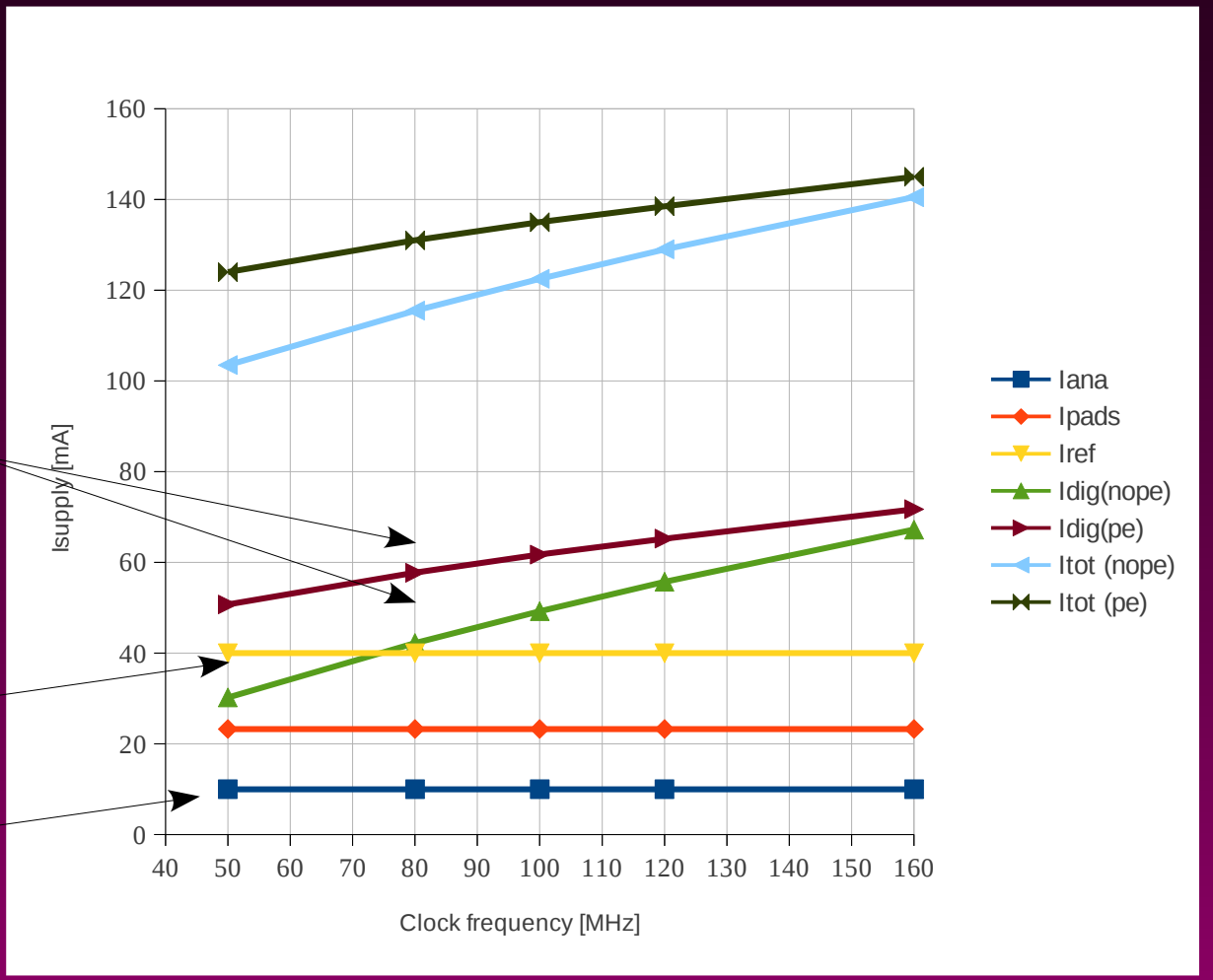
55% from the time stamp counter

Can be made almost negligible (zero in theory)

15 μA/pixel



Full chip estimate

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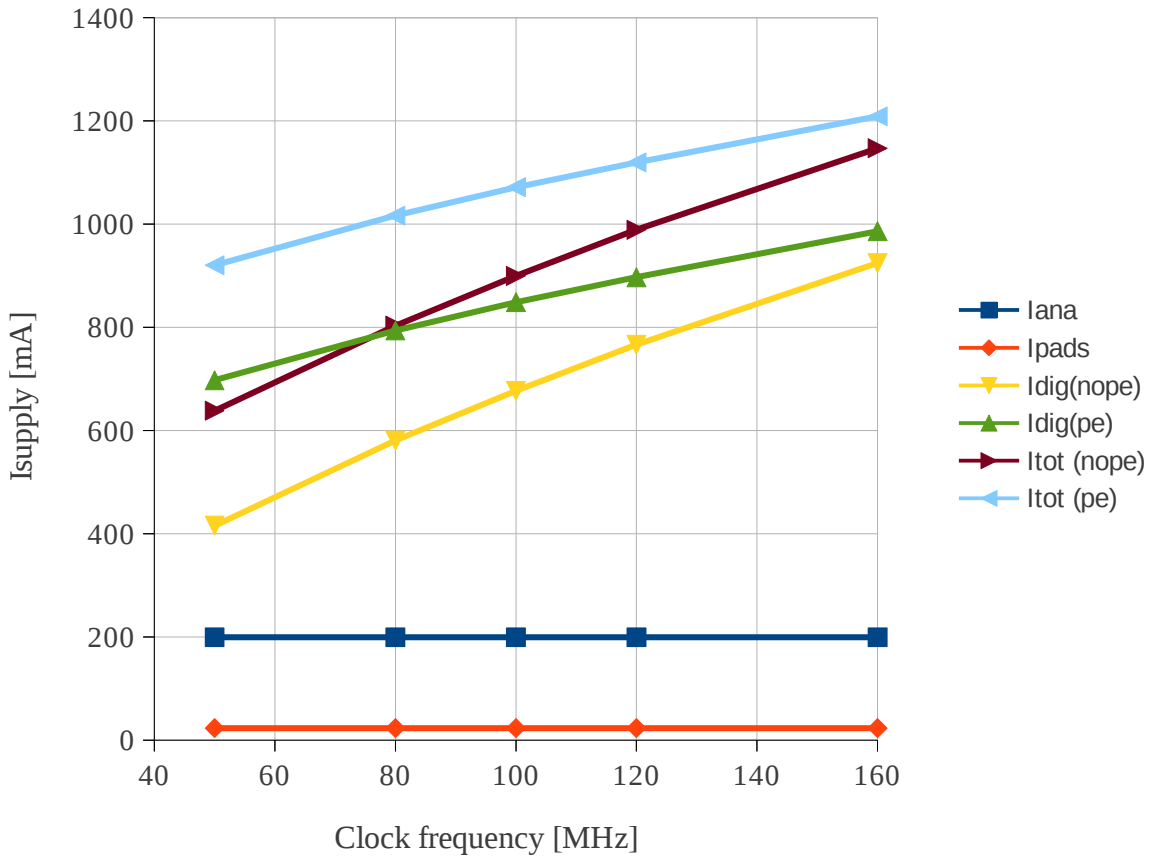

- Very rough estimate
- Still room for improvements (ToPiX v3 not really designed having low power in mind...)
- Time stamp column drivers taken from NA62 GtkTo → room for improvement
- *However, power is dominated by digital logic, therefore it is* $\propto$ *fclock*

v4 Tx-Rx simulations

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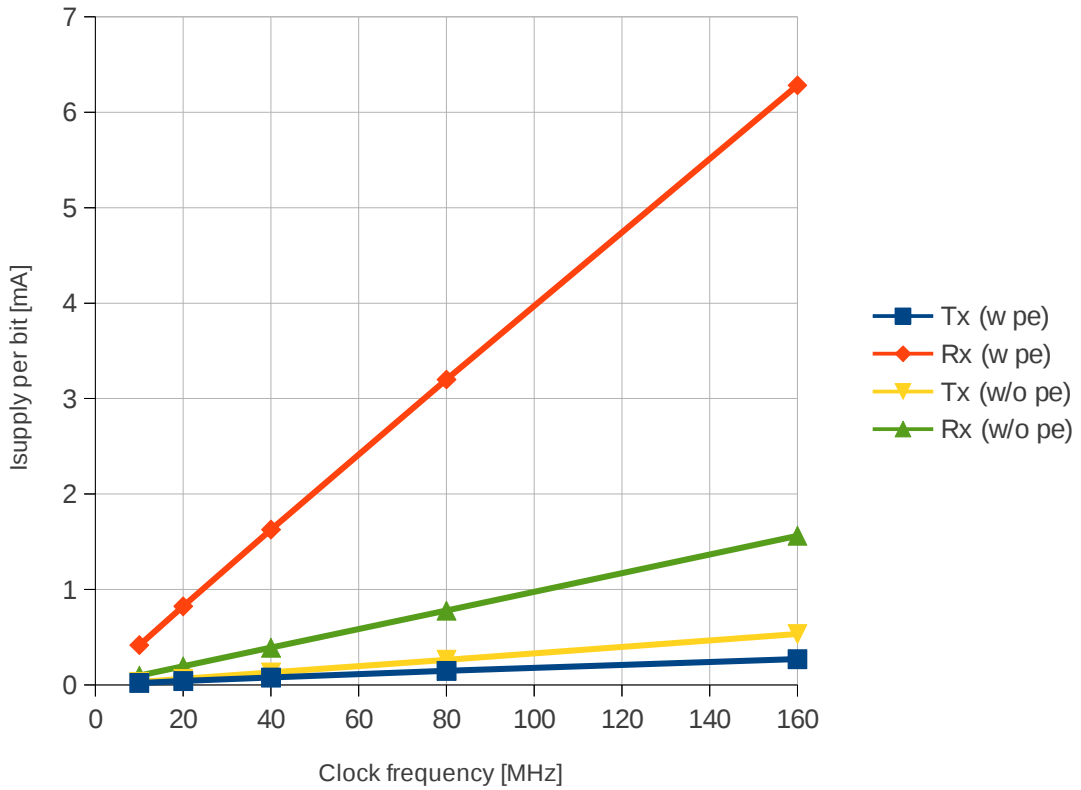

Simulations of the new driver and 128 receivers for different frequencies assuming Gray encoding.

- w pe : with reduced voltage swing and pre-emphasis
- w/o pe : with full voltage swing and without pre-emphasis

Double column drivers current supply

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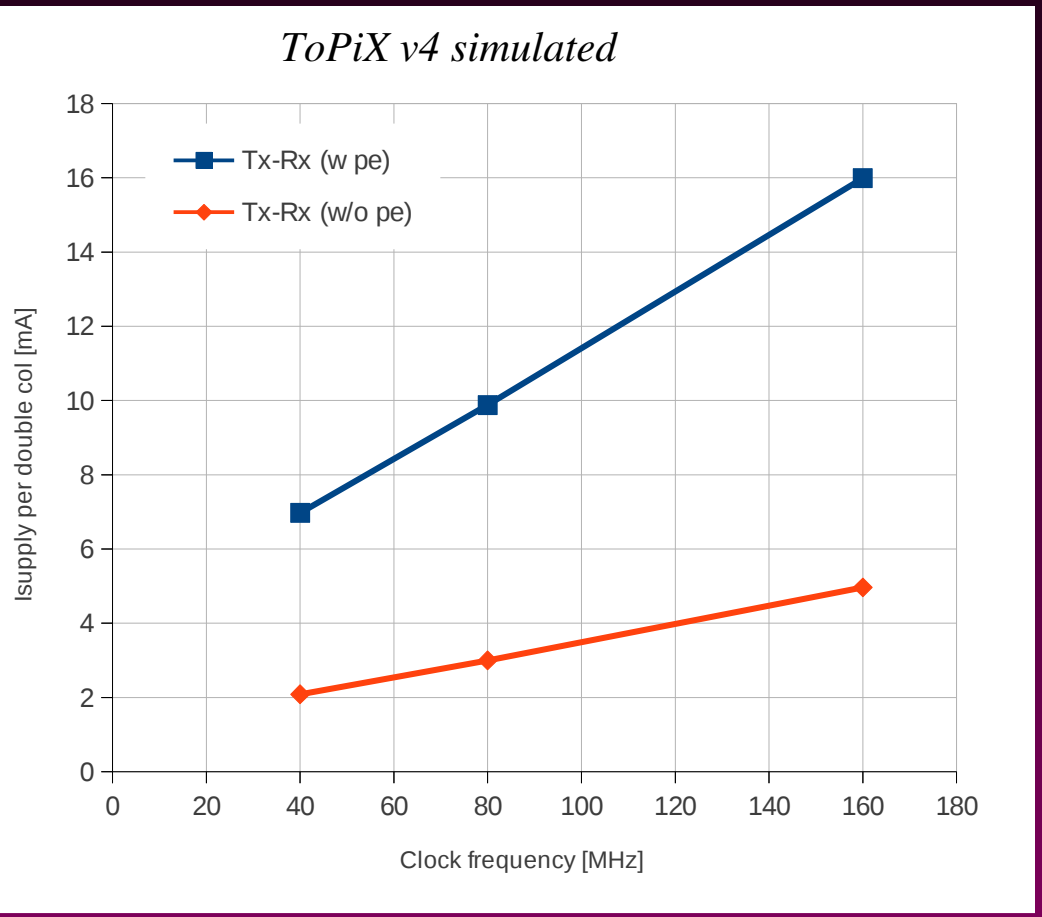
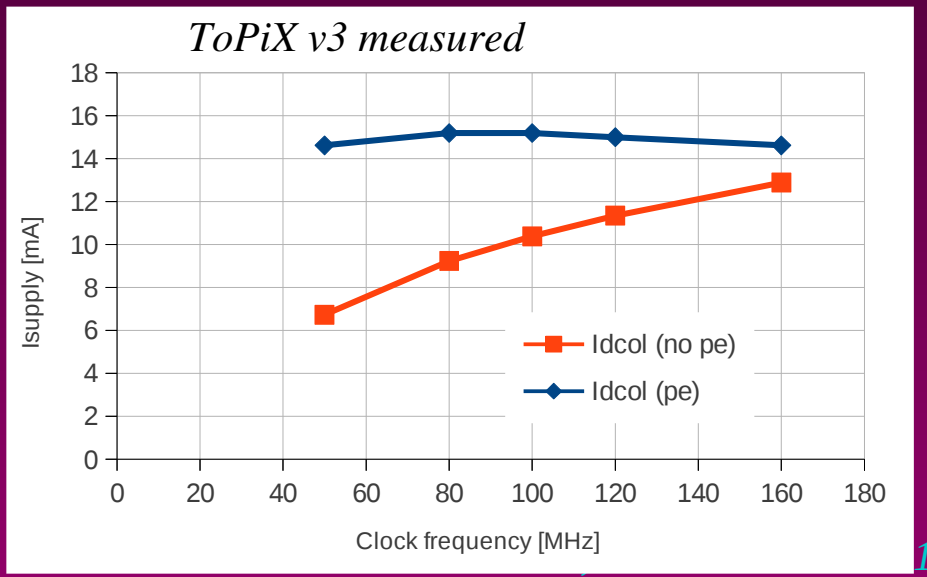


- Power goes linearly with frequency
- Reduced voltage swing reduces the driver power consumption but increases the power at the pixel receiver
- Full swing looks a better solution unless a more efficient receiver architecture can be found



TID tests - ToT

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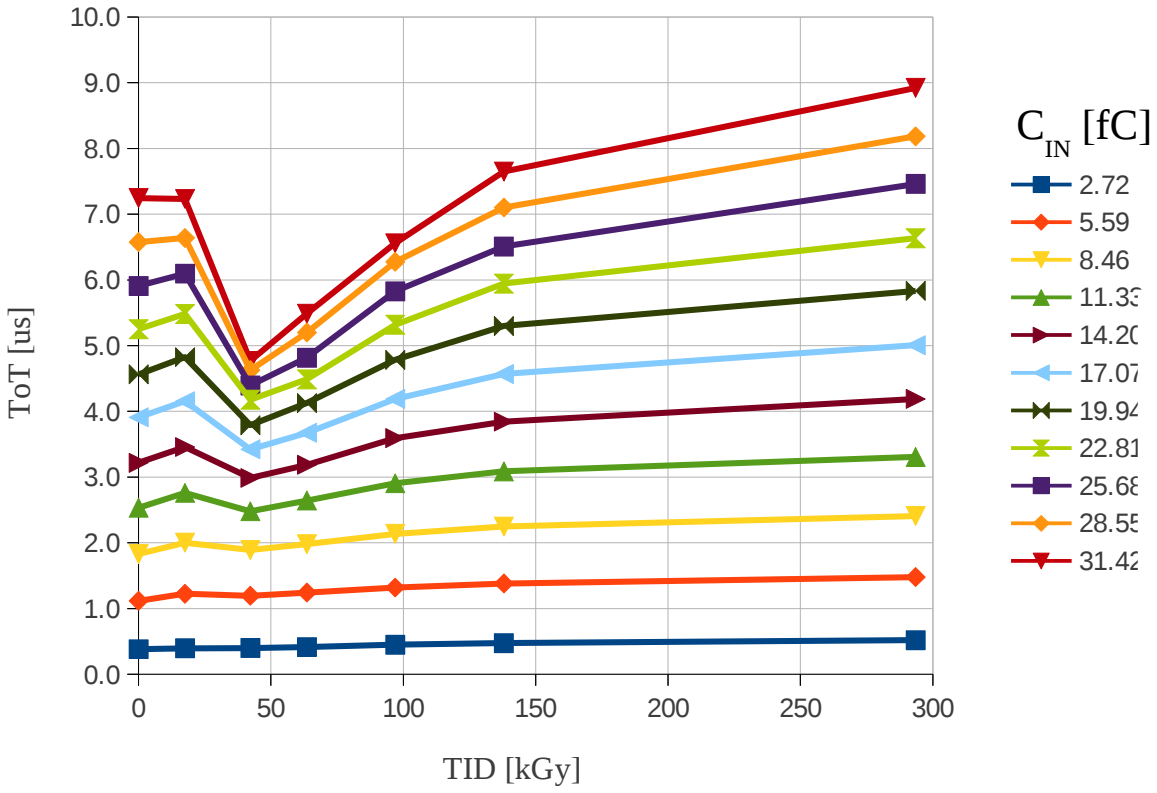
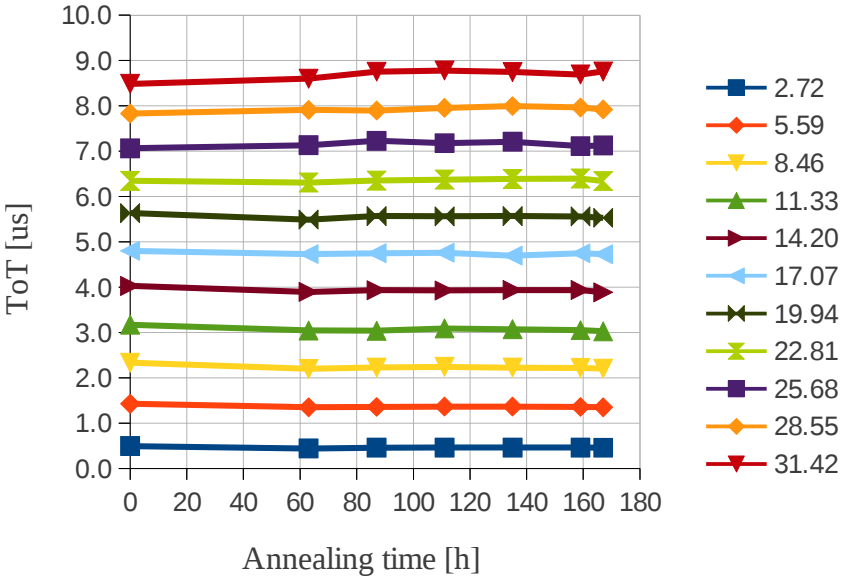
During irradiation



Annealing @ 80 °C



Probably due to effects in the clipping circuit – enclosed layout required ?

SEU tests

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- SEU data from LNL beam test under analysis
- Both ToPiX v3 and GBLD v4 have been irradiated
  - Comparison of the two SEU protection schemes
- First feeling : the SEU protection is not sufficient for the configuration register
- Space constraints in the pixel cell lead to a very compact cell which is more sensitive to SEU even with triple redundancy
- A new concept for the digital part of the pixel cell has to be found :
  - Standard cells based layout with automatic synthesis (design time, SEU tolerance)
  - Region of pixel concept (ATLAS FE-I4)

GBT

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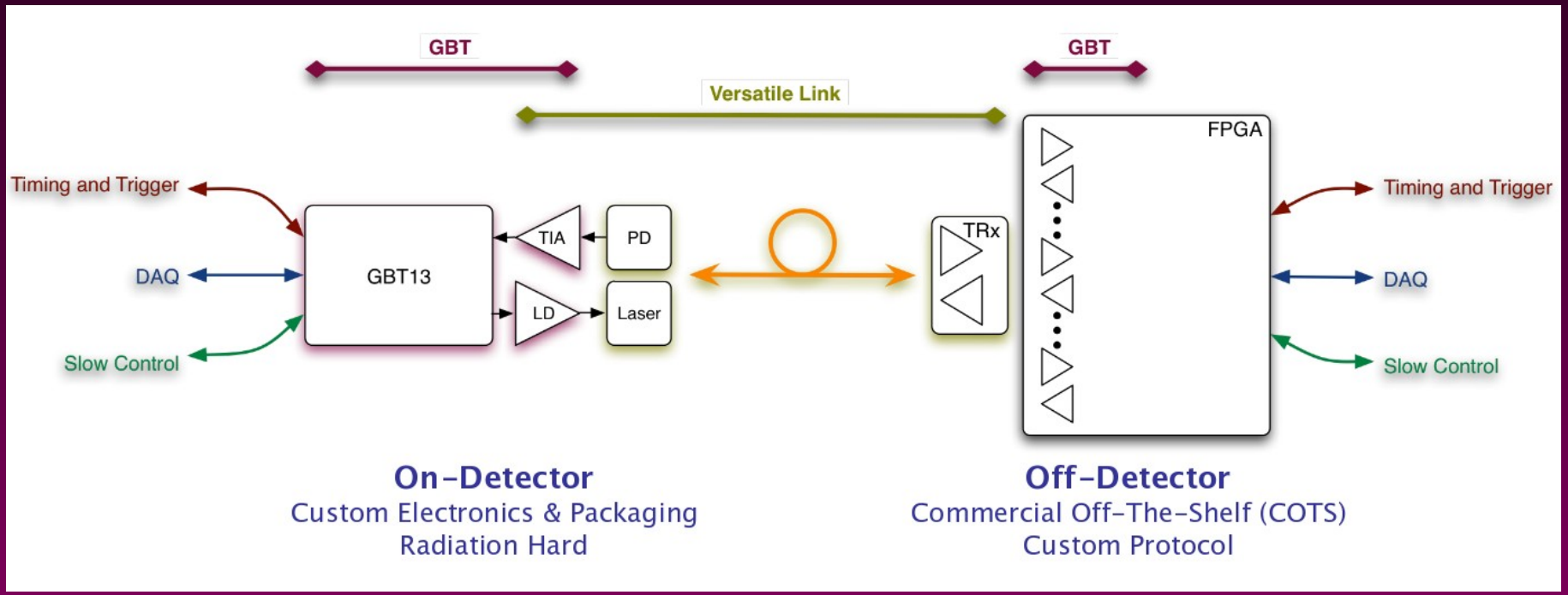
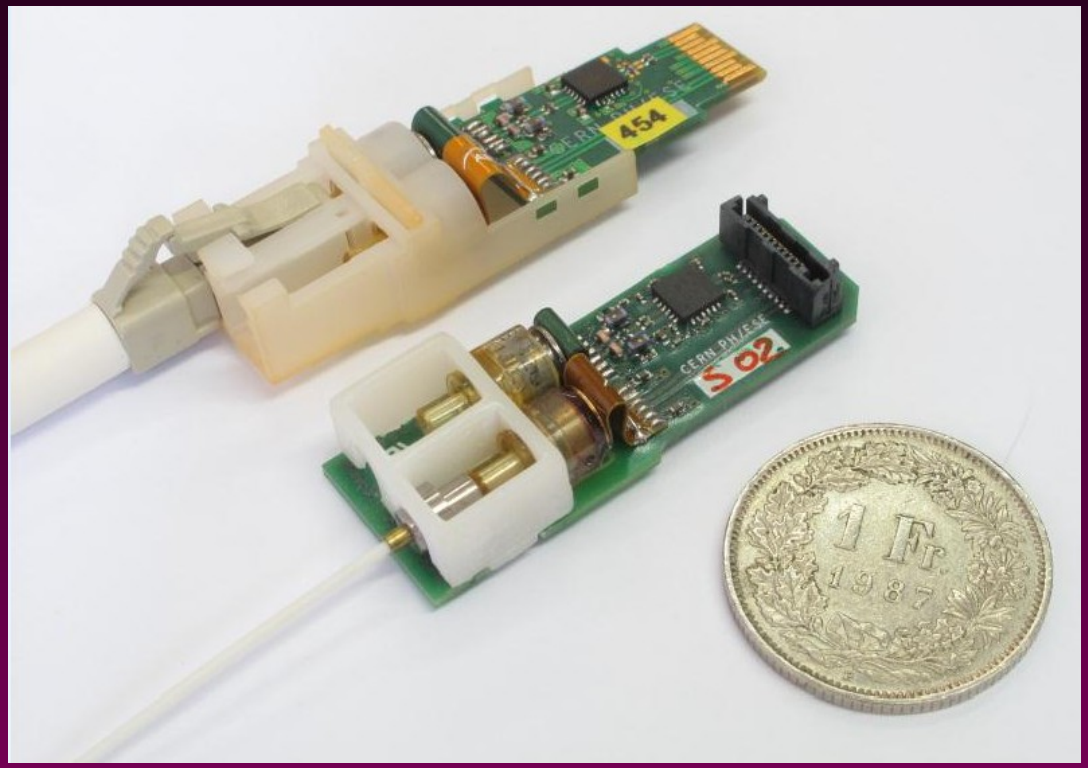


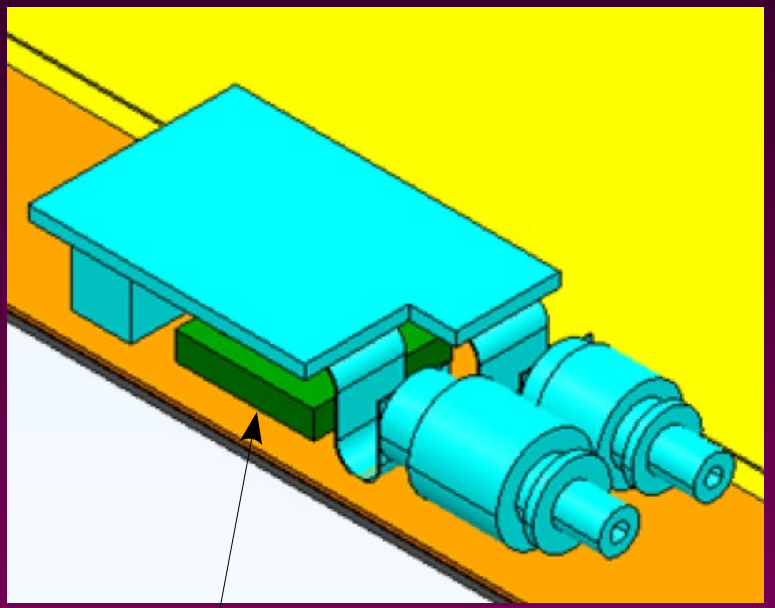
GBT components

Sezione di Torino



Versatile Transceiver
$50\times14\times10$ mm^3
$45\times15\times8$ mm^3
(F.Vasey, J.Troska, C.Soos)

Proposed arrangement for CMS tracker (C.Soos)



GBTx 10×10 mm^2
(P.Moreira et al.)

Power regulator

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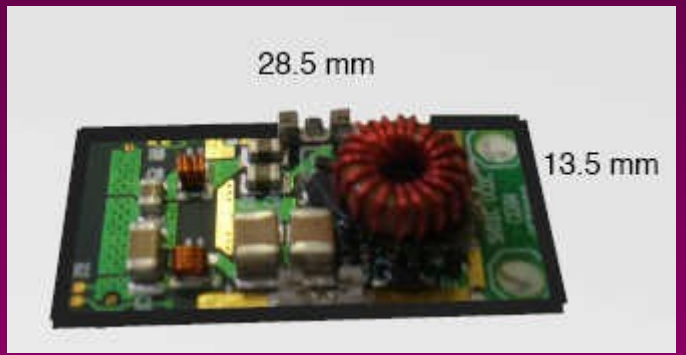
- ToPiX power supply 1.2 V – I_{DC} ~ 1 A (estimated)

  → *voltage drop on cables is not negligible*

- A DC-DC converter solution compatible with the radiation levels and the magnetic field of a silicon tracker is under development @ CERN for sLHC
- Current CERN version : V_{IN} 10÷12 V, V_{OUT}=1.2÷3.3 V, I_{OUT} < 3 A
- V_{OUT}= 1.5 V, I_{OUT} < 3-4 A now avail.
- Board position t.b.d.

  → *ToPiX internal regulator t.b.d.*



Conclusions

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- Developments on the ToPiX project show that the two critical trade-off:
  - ➔ Power consumption *vs* time resolution
  - ➔ SEU immunity *vs* pixel size
- Decisions has to be taken on the time resolution and the SEU requirements in order to finalize the design
- An on-chip voltage regulator will be probably mandatory
- Cabling could be the real show-stopper